RECEIVE CIRCUIT FOR USE IN A POWER CONVERTER

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ABSTRACT
A multi-die isolated integrated circuit controller includes a magnetically coupled communication link, a transmitter circuit coupled to the magnetically coupled communication link, and a receiver circuit coupled to the magnetically coupled communication link. The transmitter circuit is galvanically isolated from the receiver circuit. The transmitter circuit is coupled to send an input pulse to the receiver circuit by way of the magnetically coupled communication link. The receiver circuit is coupled to receive a receiver voltage by way of the magnetically coupled communication link to generate an output voltage in response to the receiver voltage and a threshold voltage.
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CROSS-REFERENCE TO RELATED APPLICATIONS


BACKGROUND INFORMATION

[0002] 1. Field of the Disclosure

[0003] The present invention relates generally to communication between circuits that require galvanic isolation. More specifically, examples of the present invention are related to communication across an isolation barrier in switch mode power converters.

[0004] 2. Background

[0005] Switch mode power converters are widely used for household or industrial appliances that require a regulated direct current (dc) source for their operation, such as for example battery chargers that are commonly used in electronic mobile devices. Off-line ac-dc converters convert a low frequency (e.g., 50 Hz or 60 Hz) high voltage ac (alternating current) input voltage to a required level of dc output voltage. Various types of switch mode power converters are popular because of their well regulated output, high efficiency, and small size along with their safety and protection features. Popular topologies of switch mode power converters include flyback, forward, boost, buck, half bridge and full bridge, among many others including resonant types.

[0006] Safety requirements for isolated switch mode power converters generally require the use of high frequency transformers to provide galvanic isolation between the inputs and outputs of the switch mode power converters in addition to the voltage level change at the output.

[0007] A major challenge in the market of switch mode power converters is reducing the size and cost of the switch mode power converter while maintaining high performance operating specifications. In known isolated switch mode power converters, the sensing of the outputs of the switch mode power converters and communication of feedback signals for regulating switch mode power converter output parameters such as current or voltage is usually accomplished using external isolation components such as, for example, opto-couplers. These known methods add unwanted additional size as well as cost to switch mode power converters. In addition, opto-couplers are slow in operation and in many cases limit the feedback bandwidth and the transient response of the switch mode power converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

[0009] FIG. 1 shows a schematic of one example of a synchronous flyback switch mode power converter with a receive circuit receiving signals from a transmitter via a magnetically coupled communication link between two dice of a controller of the power converter, in accordance with the teachings of the present invention.

[0010] FIG. 2 shows a schematic of a transmitter sending pulses to a receiver by way of a magnetically coupled communication link and the receive circuit outputting an output voltage in response to receiving the pulse from the transmitter, in accordance with the teachings of the present invention.

[0011] FIG. 3 illustrates an example timing diagram showing a current and corresponding voltage generated by a transmitter and an input pulse voltage received by a receive circuit and an output voltage generated by the receive circuit, in accordance with the teachings of the present invention.

[0012] FIG. 4 illustrates an example block diagram schematic of a receiver circuit that includes amplifiers and pre-biasing circuitry, in accordance with the teachings of the present invention.

[0013] FIG. 5 shows a schematic illustrating one example of the amplifiers and pre-biasing circuitry that can be utilized in a receive circuit, in accordance with the teachings of the present invention.

[0014] Corresponding reference characters indicate corresponding components throughout the several views of the drawings. Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of various embodiments of the present invention. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present invention.

DETAILED DESCRIPTION

[0015] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

[0016] Reference throughout this specification to “one embodiment”, “an embodiment”, “one example” or “an example” means that a particular feature, structure or characteristic described in connection with the embodiment or example is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment”, “in an embodiment”, “one example” or “an example” in various places throughout this specification are not necessarily all referring to the same embodiment or example. Furthermore, the particular features, structures or characteristics may be combined in any suitable combinations and/or sub-combinations in one or more embodiments or examples. Particular features, structures or characteristics may be included in an integrated circuit, an electronic circuit, a combinational logic circuit, or other suitable components that provide the described functionality. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

[0017] FIG. 1 shows a schematic of one example of a synchronous flyback switch mode power converter 100 with a receiver 100 receiving signals from a transmitter 162 via a magnetically coupled communication link 146 between two dice of an integrated circuit controller 140 of a synchronous
flyback switch mode power converter 100, in accordance with the teachings of the present invention.

[0018] In the example illustrated in FIG. 1, synchronous flyback switch mode power converter 100 utilizes secondary control. It is appreciated that secondary control for a flyback converter has advantages of tighter output regulation and faster response to load transients. However, conventional methods of secondary control often use external isolation devices, such as for example opto-couplers, which increase the complexity and cost of the switch mode power converter. By using an example multi-die isolated integrated circuit controller 140 having a magnetically coupled communication link 146 with galvanically isolated primary and secondary control dice, externally added isolation components such as opto-couplers may no longer be needed. Galvanic isolation prevents dc current between primary and secondary control dice. In other words, a dc voltage applied between the primary control die and the secondary control die will produce substantially no dc current between the primary control die and secondary control die of integrated circuit controller 140. A package of integrated circuit controller 140 may provide a magnetically coupled communication link 146 by using the lead frame of the package. Galvanic isolation may be maintained between the primary and secondary sides of the switch mode power converter at nearly zero additional cost, without having to add external isolation components in accordance with the teachings of the present invention.

[0019] In the example synchronous flyback switch mode power converter 100, the primary and secondary controllers are galvanically isolated from one another, but there is still reliable communication between the primary and secondary controllers in accordance with the teachings of the present invention. It is appreciated that although the example of FIG. 1 shows a synchronous flyback converter, a standard flyback converter, where a synchronous rectification circuit 126 is replaced by a diode, would also benefit from the teachings of the present invention.

[0020] In the example illustrated in FIG. 1, synchronous flyback switch mode power converter 100 includes an energy transfer element 124, which includes a primary winding 110 and a secondary winding 112, as shown. A clamp 106 is coupled across primary winding 110 of energy transfer element 124 and clamp 106 is coupled to a first line of an input V_{IN} 102 of synchronous flyback switch mode power converter 100.

[0021] In the depicted example, a switching device S1 150 is coupled to energy transfer element 124 at primary winding 110 and coupled to the input of synchronous flyback switch mode power converter 100 at the primary ground 104. In the illustrated example, switching device S1 150 may be included in a monolithic or hybrid structure in the integrated circuit package. As shown in the depicted example, integrated circuit controller 140 is coupled to control switching of switching device S1 150 (via switching signal 148) to control a transfer of energy through the energy transfer element 124 from the input V_{IN} 102 to the output V_{O} 120. Integrated circuit controller 140 includes a primary die 142 and a secondary die 144. Clamp 106 is coupled to clamp any turn-off spikes that result from leakage inductance from primary winding 110 across the switching device S1 150.

[0022] As shown in the example of FIG. 1, synchronous rectification circuit 126 is coupled to secondary winding 112 at the secondary side and serves as a synchronous rectifier of synchronous flyback switch mode power converter 100. In one example, synchronous rectification circuit 126 is controlled by a signal 128 from secondary die 144 that is coupled to the gate of a metal oxide semiconductor field effect transistor (MOSFET) switch of synchronous rectification circuit 126. When turned on by the signal 128 from secondary die 144, the MOSFET switch of synchronous rectification circuit 126 may conduct current. In the depicted example, the secondary ripple is smoothed by output filter capacitance C1 116 and the dc output V_{O} 120 is applied to load 123 with load current I_{L} 118. The output V_{O} 120 may be sensed by a sense circuit 152 via an output sense signal U_{O}. Secondary die 144 may receive a feedback signal U_{FB} 154 from sense circuit 152 at a feedback pin of secondary die 144. It is appreciated that in other examples, sense circuit 152 could be integrated within integrated circuit controller 140 while still benefiting from the teachings of the present invention.

[0023] At startup, primary die 142, which is referenced to the primary ground 104, starts the switching of switching device S1 150, which starts the transfer of energy to the secondary side of synchronous flyback switch mode power converter 100. Communication between primary die 142 and secondary die 144 may be through a magnetic coupling provided by a magnetically coupled communication link 146 formed by isolated conductors of the lead frame of the integrated circuit package. In the illustrated example, receiver 160 is disposed on primary die 142 and transmitter 162 is disposed on secondary die 144. In another example, receiver 160 can be disposed on secondary die 144 and transmitter 162 can be disposed on primary die 142. In yet another example, transmitter 162 and receiver 160 can be disposed both on primary die 142 and secondary die 144. In various examples, the magnetically coupled communication link 146 is implemented using galvanically isolated conductive loops included in the lead frame of the integrated circuit package.

[0024] FIG. 2 shows a schematic of a transmitter 262 sending an input pulse to a receiver 260 by way of a magnetically coupled communication link 246, in accordance with the teachings of the present invention. In the illustrated example, the input pulse is formed by generating a transmitter current I_{T} 264 through an inductive loop, which induces voltage V_{I} 266 across the inductive loop. When transmitter current I_{T} 264 is varying or changing over time, it produces a changing magnetic field in the proximity of the inductive loop. Due to the laws of electromagnetic induction, a voltage is generated across a conductor that is subjected to a changing magnetic field. In response to transmitter current I_{T} 264 changing, a receiver voltage V_{R} 268 may be induced across a receiver conductor in the proximity of the inductive loop of transmitter 262. Therefore, receiver 260 may receive an input pulse from transmitter 262 via magnetically coupled communication link 246. In the illustrated example, receiver 260 outputs an output voltage V_{OUT} 270 in response to receiving the input pulse.

[0025] FIG. 3 illustrates an example timing diagram showing transmitter current I_{T} 364 and corresponding voltage V_{I} 366 generated by a transmitter (e.g., transmitter 262), in accordance with the teachings of the present invention. The solid lines of transmitter current I_{T} 364 and voltage V_{I} 366 represent the ideal signals, while the dashed lines 308 and 310 represent an estimated actual signal. In practice, the actual signal may likely differ from the ideal signal because of parasitic elements such as capacitance and/or inductance or the like that may be present in magnetically coupled communication link 246. For example, these parasitic elements may...
cause losses in the transmitter and/or the receiver resulting in lower amplitudes for voltage \( V_{p} \) and/or voltage \( V_{r} \).

[0026] In the example timing diagram of FIG. 3, the positive amplitude signal for voltage \( V_{p} \) between \( t_{1} \) and \( t_{2} \) at a value \( V_{pp} \) corresponds with the upward slope of \( I_{p} \) of transmitter current \( I_{p} \) between \( t_{1} \) and \( t_{2} \) from 0 to \( t_{pp} \). This relationship indicates that transmitter current \( I_{p} \) through the inductive loop of the transmitter is increasing at a rate corresponding with the upward slope of \( V_{pp} \) and the increasing current through the inductive loop of the transmitter induces a positive voltage of the value \( V_{pp} \) across the inductive loop. In one example, the value \( V_{pp} \) is 40 mV between \( t_{1} \) and \( t_{2} \).

[0027] The zero amplitude signal for \( V_{p} \) between \( t_{1} \) and \( t_{2} \) corresponds with the flat top of \( I_{p} \) of transmitter current \( I_{p} \) between \( t_{1} \) and \( t_{2} \). This relationship indicates that transmitter current \( I_{p} \) is substantially constant between \( t_{1} \) and \( t_{2} \). Since a constant current does not induce a corresponding voltage across the inductive loop of the transmitter, \( V_{p} \) has substantially zero amplitude between \( t_{1} \) and \( t_{2} \).

[0028] The negative amplitude signal for voltage \( V_{p} \) between \( t_{1} \) and \( t_{2} \) at a value \( V_{pp} \) corresponds with the downward slope \( I_{p} \) of transmitter current \( I_{p} \) between \( t_{1} \) and \( t_{2} \) from \( t_{pp} \) to 0. This relationship indicates that transmitter current \( I_{p} \) through the inductive loop of the transmitter is decreasing at a rate corresponding with the downward slope \( V_{pp} \) and the decreasing current through the inductive loop of the transmitter induces a negative voltage of the value \( V_{pp} \) across the inductive loop of the transmitter.

[0029] In the illustrated example, it is noted that the increasing slope \( I_{p} \) for current \( I_{p} \) is steeper than the decreasing slope \( V_{pp} \), so the value \( V_{pp} \) is greater than the value \( V_{pp} \) because according to the laws of electromagnetic induction, the voltage induced across an inductive loop is proportional to the slope of the curve in the inductive loop. In addition, changing up the inductive loop of the transmitter is done in a shorter time period than discharging the inductive loop of the transmitter. Even so, those skilled in the art will realize that the area under the positive amplitude signal of voltage \( V_{p} \) between \( t_{1} \) and \( t_{2} \) should be the same as the area under the negative amplitude signal of \( V_{p} \) between \( t_{1} \) and \( t_{2} \) to retain substantially zero net energy in the magnetically coupled communication link.

[0030] FIG. 3 also illustrates example input pulse voltage \( V_{p} \) received by a receiver (e.g., receiver \( 260 \)) and an output voltage \( V_{pp} \) generated by the receiver, in accordance with the teachings of the present invention. Similar to the timing diagrams for transmitter current \( I_{p} \) and voltage \( V_{p} \), the solid line for voltage \( V_{p} \) represents the ideal signal, while the dashed line \( 312 \) represents an estimated actual signal. As discussed above, a voltage is induced on a conductor of a receiver in the proximity of an inductive loop having a changing current. Therefore, voltage \( V_{p} \) substantially tracks transmitter current \( I_{p} \) and voltage \( V_{p} \). As previously mentioned, parasitic elements in the magnetically coupled communication link may cause losses. In one example, losses in the receiver may be greater than the losses in the transmitter. As illustrated, this may leave the actual signal for voltage \( V_{p} \) with lower magnitude amplitudes than the corresponding magnitudes of the actual signal for voltage \( V_{p} \).

[0031] When the actual signal for voltage \( V_{p} \) is greater than a threshold voltage \( V_{pp} \) in the receiver, the receiver generates an output voltage \( V_{pp} \) in output voltage \( V_{pp} \). When the actual signal for voltage \( V_{p} \) is less than the threshold voltage \( V_{pp} \) in the receiver, the receiver generates an output voltage \( V_{pp} \) in output voltage \( V_{pp} \).
old voltage $V_{TH}$, output signal $U_{OUT}$ is logic high. In various examples, output circuit 460 may include a comparator, an inverter, a driver or the like to generate output signal $U_{OUT}$ in accordance with the teachings of the present invention.

In the illustrated example, first pre-bias circuit 420 is coupled to reset the first output 412 to a first value in response to output signal $U_{OUT}$ 470. In the example depicted in FIG. 4, the first value is $V_1$. First pre-bias circuit 420 may include a first switch SW 422 coupled to reset the first output 412 to the first value. Second pre-bias circuit 450 is coupled to reset the second output 440 to a second value in response to output signal $U_{OUT}$ 470, as shown. In the example depicted in FIG. 4, the second value is $V_2$. Second pre-bias circuit 450 may include a second switch SW 452 coupled to reset the second output 440 to the second value.

In operation, resetting first output 412 and second output 440 to the first and second values, respectively, in response to output signal $U_{OUT}$ 470 may prepare receive circuit 400 to receive and amplify a subsequent input pulse that may follow input pulse $U_{IN}$ 402 within a short period of time in accordance with the teachings of the present invention. In some applications, receive circuit 400 may be receiving information (via an input pulse) representing a state of a power converter and may be configured to respond to a first stream of input pulses. In one example, this will allow an output quantity of the power converter (e.g., output $V_{OUT}$ 120) to be more tightly regulated in accordance with the teachings of the present invention.

In one example, delay circuit 480 is coupled to receive output signal $U_{OUT}$ 470 and delay circuit 480 is also coupled to generate a pre-bias control signal $U_{PREB} 482$ that is responsive to output signal $U_{OUT} 470$. Delay circuit 480 may be further coupled to first pre-bias circuit 420 and coupled to second pre-bias circuit 450. Delay circuit 480 may also be coupled to generate a pulse of the pre-bias control signal $U_{PREB} 482$ that is delayed from a corresponding pulse of the output signal $U_{OUT} 470$. In one example, delay circuit 480 delays output signal $U_{OUT} 470$ by approximately 20 ms. In one example, delay circuit 480 may include a current source coupled to a capacitor to generate pre-bias control signal $U_{PREB} 482$ by delaying output signal $U_{OUT} 470$.

FIG. 6 shows a schematic illustrating one example of the amplifiers and pre-bias circuitry that may be utilized in receive circuit 400 in accordance with the teachings of the present invention. First amplifier 510 is one possible example of first amplifier 410. As shown in the depicted example, first amplifier 510 includes transistors $Q_1, Q_5, Q_6, Q_7, Q_8, Q_9, Q_{11}, Q_{13}, Q_{15}, Q_{17}, Q_{514}$ and $Q_{526}$. In the illustrated example of FIG. 5, transistors $Q_5, Q_6$ and $Q_7$ are bipolar junction transistors (BJTs), transistors $Q_8, Q_{11}, Q_{13}, Q_{15}$ and $Q_{17}$ are n-channel metal oxide semiconductor field effect transistors (MOSFETs), and transistors $Q_{514}$ and $Q_{526}$ are n-channel MOSFETs.

In the illustrated example, first amplifier 510 includes a differential amplifier with a single ended output. The differential amplifier includes transistors $Q_5, Q_6$ and $Q_7$ coupled together at their bases. Transistor $Q_5$ is coupled to receive an input pulse $U_{IN} 502$ at the emitter of transistor $Q_5 505$. The emitters of transistors $Q_5, Q_6$ and $Q_7$ may be considered the inputs terminals of the differential amplifier. The emitter of transistor $Q_5 503$ is coupled to a ground 504, while the emitter of transistor $Q_5 505$ is coupled to an input node that may be coupled to a conductor comprising a portion of an inductive loop of a receiver (e.g., receiver 260). In the illustrated example, ground 504 represents a reference voltage or potential against which all other voltages or potentials of the amplifiers and the pre-bias circuitry are defined or measured. In one example, one end of the inductive loop may be coupled to ground 504 whereas the other end of the inductive loop may be coupled to the input node through the conductor. Accordingly, input pulse $U_{IN} 502$ may be substantially determined by the voltage across the inductive loop plus ground 504. A voltage may be induced across the inductive loop by a changing magnetic field in the proximity of the inductive loop. If there is no changing magnetic field in the proximity of the inductive loop, input pulse $U_{IN} 502$ is substantially ground 504 (i.e., the emitter of transistor $Q_5 505$ receives no input pulse). Transistor $Q_5 505$ may represent any number of transistors that are identical to transistor $Q_6 503$ and coupled together in parallel (i.e., bases are coupled together, emitters are coupled together and collectors are coupled together). As a result, for the same base to emitter voltage, a collector current of transistor $Q_5 505$ is substantially equal to the collector current of transistor $Q_6 503$ multiplied by the number of identical transistors that transistor $Q_5 505$ represents. In the illustrated example of first amplifier 510, transistor $Q_5 505$ represents two identical transistors (e.g., identical to $Q_6 503$) coupled together in parallel and hence, for the same base to emitter voltage, demands a collector current that is twice the collector current of transistor $Q_6 503$.

A first branch of first amplifier 510 includes transistors $Q_{515}, Q_{511}, Q_{507}$, and $Q_5 503$. A second branch of first amplifier 510 includes transistors $Q_{517}, Q_{513}, Q_{509}$, and $Q_5 505$. Transistors $Q_{515}$ and $Q_{517}$ act as a current source to supply current to the first and second branch of first amplifier 510. In one example, these transistors are sized in a way such that a ratio of an aspect ratio (i.e., the ratio of the width of a transistor to the length of the transistor) of transistor $Q_{517}$ to the aspect ratio of transistor $Q_{515}$ is less than the number of identical transistors that transistor $Q_5 505$ represents. In the illustrated example of first amplifier 510, the aspect ratio of transistor $Q_{517}$ is less than twice the aspect ratio of transistor $Q_{515}$. As a result, the current that transistor $Q_{517}$ can provide in the second branch of first amplifier 510 is less than twice the current that transistor $Q_{515}$ can provide to the first branch of first amplifier 510.

This has two implications for the operation of first amplifier 510. First, when the emitter of transistor $Q_{505}$ receives no input pulse at the input node (i.e., when the base to emitter voltage of transistor $Q_{505}$ becomes equal to the base to emitter voltage of transistor $Q_{503}$), the second branch of first amplifier 510 cannot meet the current demand of transistor $Q_{505}$ forcing first output 512 to drop. Additional current is needed to meet the current demand of transistor $Q_{505}$ to stabilize first amplifier 510. This current may come from transistor $Q_{535}$ of second amplifier 530 to settle first amplifier 510 such that first output 512 is at a level not sufficient to turn transistor $Q_{539}$ ON (i.e., conducting the full current available on the second branch of second amplifier 530).

The second implication is that there needs to be a difference in the base to emitter voltages of transistors $Q_5 503$ and $Q_5 505$ to lower the current demand of transistor $Q_{505}$ to be able to raise first output 512. Specifically, the base to emitter voltage of transistor $Q_{505}$ has to be less than the base
to emitter voltage of transistor Qo. 503 by a certain amount in order for first output 512 to rise to a level that is sufficient to turn transistor Qo. 539 ON (and thereby, transition output signal U_{OUT.570} from logic low to logic high). The difference between the base to emitter voltages of transistors Qo. 503 and Qo. 505 may be considered an offset of first amplifier 510 or a detection threshold of receive circuit 400. In other words, input signal U_{IN.502} needs to rise above ground 504 by this offset (detection threshold) to raise first output 512 to the required level.

In practice, the signal level at the output of first amplifier 510 does not react immediately to the changes in input pulse U_{IN.502}. Therefore, the signal level at first output 512 depends not only on the magnitude of input pulse U_{IN.502}, but also on the duration of an input pulse U_{IN.502}. For example, if there is an input pulse needs to have a larger magnitude to produce the same first output 512 that a longer input pulse with less magnitude does. In one example, the input pulse needs to be at least 22 mV for 15 ns to be able to raise first output 512 to the level required to turn transistor Qo. 539 ON.

In the illustrated example, transistors Qo. 507 and Qo. 509 have identical width and length (and hence, identical aspect ratios), and are coupled together at their gates to form a current mirror. Similarly, transistors Qo. 511 and Qo. 513 are also coupled at their gates to form a current mirror. In the illustrated example, these current mirrors increase the gain of first amplifier 510.

In FIG. 5, transistor Qo. 526 is coupled to a supply voltage VA to provide the base current for transistors Qo. 505 and Qo. 503. In one example, transistor Qo. 526 may supply more current than transistors Qo. 503 and Qo. 505 need to ensure that transistors Qo. 503 and Qo. 505 are always able to conduct current. Transistor Qo. 514 is coupled to sink the excess current to ground 504.

In the illustrated example, a bias voltage V_{BIAS} is received at a bias node that is coupled to the gates of transistors Qo. 514, Qo. 528, and Qo. 524. In one example the bias voltage V_{BIAS} is a temperature insensitive voltage generated by a separate circuit and provided to the bias node. The bias voltage V_{BIAS} may be used for generating reference currents that are substantially constant with respect to temperature for first amplifier 510 and second amplifier 530. In addition, the bias voltage V_{BIAS} may be used to set the amount of current that transistors Qo. 514 and Qo. 524 can conduct. In the illustrated example, the bias voltage V_{BIAS} is applied to the gate of Qo. 528 to generate a reference current I_{BIAS}, which is then reflected through current mirror combinations Qo. 515, Qo. 517, Qo. 515, Qo. 527-Qo. 528, Qo. 527-Qo. 528, and Qo. 527-Qo. 528 to generate the desired currents for the first and second branches of first amplifier 510 and second amplifier 530. In this manner, transistors Qo. 515, Qo. 517, Qo. 515, Qo. 527-Qo. 528, and Qo. 527-Qo. 528 can operate as a current source coupled to the supply voltage VA to provide the desired currents to the first and second branches of first amplifier 510 and second amplifier 530. Depending on the aspect ratios of transistors Qo. 503 and Qo. 505, currents in the first and second branches of first amplifier 510 and second amplifier 530 can be the same as or different from the reference current I_{BIAS}. As an example, transistor Qo. 509 may have the same aspect ratio as the aspect ratio of transistor of Qo. 503, making the current in the first branch of first amplifier 530 substantially the same as the reference current I_{BIAS}.

As discussed previously, the first branch for first amplifier is the leg corresponding to transistors Qo. 503, Qo. 507, Qo. 511 and Qo. 515 and the second branch is the other leg corresponding to transistors Qo. 505, Qo. 509, Qo. 513 and Qo. 517. The first branch for second amplifier 530 is the leg corresponding to transistors Qo. 532, Qo. 533, Qo. 534, Qo. 537 and Qo. 538 and the second branch is the other leg corresponding to transistors Qo. 531, Qo. 539, Qo. 536 and Qo. 539. The aspect ratios of transistors Qo. 515 and Qo. 517 may be different from the aspect ratios of transistors Qo. 538 and Qo. 539. In this case, currents in the first and second branches of first amplifier 510 are different from the currents in the first and second branches of second amplifier 530.

In the illustrated example, the first and second branches of second amplifier 530 may have the same current, which can be important for setting the bias voltage (i.e., the gate to source voltage) of transistor Qo. 539 on first output 512.

Referring to second amplifier 530, the bias voltage of transistor Qo. 539 is set to a value such that transistor Qo. 539 is not ON (i.e., not conducting full current available on the second branch of second amplifier 530), but still conducts some current when there is no input pulse at the input node. As such, transistor Qo. 539 can be thought of as operating in a sub-threshold region, which is achieved by setting the gate to source voltage of transistor Qo. 539 to a value slightly lower than the threshold voltage (V_T) of transistor Qo. 539. One reason for doing this is to keep second output 540 of second amplifier 530 above a threshold voltage of output circuit 560. Otherwise, if transistor Qo. 539 conducts the full current available on the second branch of second amplifier 530 when there is no input pulse, then second output 540 can drop below the threshold voltage of output circuit 560 and erroneously cause output signal U_{OUT.570} to transition from logic low to logic high. In practice, output circuit 560 should only generate an output logic high in response to receiving an input pulse U_{IN.502}.

As shown in the illustrated example, multiple transistors (transistors Qo. 531, Qo. 532, Qo. 533, Qo. 534, and Qo. 535 in particular) are used to set the bias voltage of transistor Qo. 539. In the illustrated example, transistors Qo. 531, Qo. 532, Qo. 534, and Qo. 535 all have the same aspect ratio, meaning that for the same collector current, their base to emitter voltages (V_{BE}) are substantially equal to each other. The collector current of transistor Qo. 535 may be different from the collector currents of transistors Qo. 532, Qo. 534, and Qo. 531, which may have the same current courtesy of transistors Qo. 538 and Qo. 539 having the same aspect ratio, as previously mentioned. However, the base to emitter voltage of transistor Qo. 535 may still be very close to the V_{BE} of transistors Qo. 532, Qo. 534, and Qo. 531 since a small change in the V_{BE} can correlate to a large change in collector current. Assuming that the currents in first and second branches of first amplifier 510 and second amplifier 530 are small (to reduce power dissipation), the gate to source voltage of transistor Qo. 535 is forced to be equal (or very near) to the threshold voltage of transistor Qo. 535. In one example, transistors Qo. 531 and Qo. 532 have equal threshold voltages. With this in mind, the base voltage of transistor Qo. 535 may equate to the sum of the V_{BE} of transistor Qo. 532 plus the gate to source voltage of Qo. 531 (i.e., the V_{TH} of transistor Qo. 531) plus the V_{BE} of transistor Qo. 534.

It is also known that transistor Qo. 535 is coupled to conduct current (when there is no input pulse at the input node) that goes from the supply voltage VA to ground 504 through transistors Qo. 505 and Qo. 509 of first amplifier 510. Therefore, the gate voltage of transistor Qo. 539 equates to...
the base voltage of transistor Q₂₃ 535 (2VBE + V_B) minus the VBE of transistor Q₂₃ 535. That is, the gate voltage of transistor Q₂₀ 539 is VBE + V_T. As previously mentioned, the VBE of transistor Q₁₉ 531 is substantially the same as the VBE of transistors Q₄ 532, Q₆ 534, and Q₂₃ 535. Since there is a resistive divider between the collector, the base, and the emitter of transistor Q₁₉ 531 (formed by resistors R₈ 584 and R₉ 586), the collector voltage of transistor Q₁₉ 531 becomes (1 + R₈ / R₉) VBE which is also the source voltage of transistor Q₄ 532. In the illustrated example, resistor R₈ 584 is 500 kΩ and resistor R₉ 586 is 3 MΩ, hence the collector voltage of transistor Q₁₉ 531 is VBE + VBE/6. As such, the gate to source voltage of transistor Q₂₀ 539 is approximately V_T - VBE/6. In the illustrated example, the VBE of transistors Q₄ 532, Q₆ 534, Q₂₃ 535 and Q₂₃ 535 is around 0.65V so the gate to source voltage of transistor Q₂₀ 539 is about 100 mV lower than the threshold voltage of transistor Q₂₀ 539. Until the gate voltage of transistor Q₂₀ 539 rises higher than the source voltage of transistor Q₂₀ 539 by an amount that is equal to or greater than the threshold voltage of transistor Q₂₀ 539 which happens with a proper input pulse at the input node), second output 540 remains greater than the threshold of the output circuit 560, and as a consequence, output signal U_OUT 570 remains logic low.

When an input pulse is received at the input node (i.e., at the emitter of transistor Q₁ 505), the base to emitter voltage of transistor Q₁ 505 decreases resulting in lower collector current for transistor Q₁ 505. In response, first output 512 starts to rise. When first output 512 reaches a level such that the gate to source voltage of transistor Q₂₀ 539 becomes higher than the threshold voltage of transistor Q₂₀ 539, transistor Q₂₀ 539 turns ON conducting all of the available current on the second branch of second amplifier 530. Subsequently, second output 540 starts to drop and may go below the threshold of output circuit 560, which transitions output signal U_OUT 570 from logic low to logic high.

Even after input pulse Uᵢᵣ 502 has disappeared, first output 512 may stay high long enough to keep transistor Q₂₀ 539 ON. Similarly, second output 540 may stay low long enough to keep output signal U_OUT 570 logic high for longer than desired. Therefore, if a subsequent input pulse arrives too quickly after the initial input pulse, first amplifier 510 and second amplifier 530 may not be ready to properly react to the subsequent pulse.

To address this possible problem, first pre-bias circuit 520 may operate to return or reset first output 512 to a first initial value by drawing current from the first output 512, thereby pulling first output 512 down towards the initial value. In the illustrated example, delay circuit 580 delays first pre-bias circuit 520 from resetting first output 512 to the first initial value. Specifically, delay circuit 580 generates a pre-bias control signal Uₜᵢᵣ 582 by delaying output signal U_OUT 570 and provides pre-bias control signal Uₜᵢᵣ 582 to first pre-bias circuit 520 to turn ON transistor Q₅ 522. The first initial value may be the gate voltage of transistor Q₂₀ 539 when there is no input pulse at the input node. In other words, the first initial value may be VBE + V_T, as discussed above. Delay circuit 580 may also provide pre-bias control signal Uₜᵢᵣ 582 to second pre-bias circuit 550 to turn ON transistor Q₅ 552, which then raises second output 540 to a second initial value as shown.

In discussing FIG. 4, a positive feedback signal 432 provided first amplifier 410 with positive feedback signal Uₚᵢᵣ 432 from the second output 440 of second amplifier 430. FIG. 5 shows one example of circuitry that could be implemented to provide the positive feedback signal Uₚᵢᵣ 432. Specifically, parasitic capacitance C₂₉ 541 between the gate and drain of transistor Q₂₉ 536 couples second output 540 to the gate of transistor Q₅ 513. As the gate to source voltage of transistor Q₅ 539 increases and transistor Q₂₉ 539 conducts more current in response to increasing first output 512, second output 540 decreases. Since second output 540 is coupled (via parasitic capacitance C₂₉ 541) to the gate of transistor Q₅ 513, the gate voltage of transistor Q₅ 513 becomes more negative with respect to the source voltage of transistor Q₅ 513, which for a p-channel MOSFET means that the transistor conducts more current. Therefore, transistor Q₅ 513 will conduct more current driving first output 512 to increase at a faster rate. In this manner, positive feedback signal Uₚᵢᵣ 432 of FIG. 4 is provided from second output 540 through parasitic capacitance C₂₉ 541 to first amplifier 510 in accordance with the teachings of the present invention. Therefore, first amplifier 510 may have a faster response time for raising first output 512 to the necessary level to turn transistor Q₂₀ 539 ON, upon receiving an input pulse Uᵢᵣ 502 as well as the positive feedback signal from second output 540 in accordance with the teachings of the present invention.

The above description of illustrated examples of the present invention, including what is described in the Abstract, are not intended to be exhaustive or to limitation to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible without departing from the broader spirit and scope of the present invention. Indeed, it is appreciated that the specific example voltages, currents, frequencies, power ranges values, times, etc., are provided for explanation purposes and that other values may also be employed in other embodiments and examples in accordance with the teachings of the present invention.

What is claimed is:
1. A multi-die isolated integrated circuit controller, comprising:
   a) a magnetically coupled communication link;
   b) a transmitter circuit coupled to the magnetically coupled communication link; and
   c) a receiver circuit coupled to the magnetically coupled communication link, wherein the transmitter circuit is galvanically isolated from the receiver circuit, wherein the transmitter circuit is coupled to send an input pulse to the receiver circuit by way of the magnetically coupled communication link, wherein the receiver circuit is coupled to receive a receiver voltage by way of the magnetically coupled communication link to generate an output voltage in response to the receiver voltage and a threshold voltage.
2. The multi-die isolated integrated circuit controller of claim 1, further comprising a secondary die, wherein the transmitter circuit is included in the secondary die.
3. The multi-die isolated integrated circuit controller of claim 1, further comprising a primary die, wherein the receiver circuit is included in the primary die.
4. The multi-die isolated integrated circuit controller of claim 1, wherein the input pulse comprises a transmitter current that varies over time.
5. The multi-die isolated integrated circuit controller of claim 1, wherein the magnetically coupled communication link comprises a conductive loop.
6. The multi-die isolated integrated circuit controller of claim 5, wherein the transmitter current induces a transmitter voltage across the conductive loop.

7. The multi-die isolated integrated circuit controller of claim 7, wherein the time period has a length determined by a switching period of a switch mode power converter.

8. The multi-die isolated integrated circuit controller of claim 1, wherein the receiver circuit is coupled to generate a logic low output voltage in response to the receiver voltage being less than the threshold voltage.

9. The multi-die isolated integrated circuit controller of claim 1, wherein the receiver circuit is coupled to generate a logic high output voltage in response to the receiver voltage being greater than the threshold voltage.

10. The multi-die isolated integrated circuit controller of claim 1, wherein the multi-die isolated integrated circuit controller is included in a monolithic package.

11. The multi-die isolated integrated circuit controller of claim 12, further comprising receiving an input pulse representative of a state of a power converter;

12. A method of controlling a receiver circuit for a power converter controller, comprising:

   amplifying the input pulse and generating a first output;
   amplifying the first output and generating a second output;
   generating an output signal in response to comparing the second output to a threshold voltage; and
   resetting the first output and the second output to prepare the receiver circuit to receive and amplify subsequent input pulses.

13. The method of claim 12, further comprising receiving the output signal and generating a pre-bias control signal in response to the output signal to reset the first output and the second output.

14. A receiver circuit for use in a power converter controller, comprising:

   a first amplifier comprising a differential amplifier having a first transistor and a second transistor coupled together at their bases, wherein the first transistor is coupled to receive an input pulse at an emitter of the first transistor and generate a first output;
   a second amplifier coupled to receive the first output to compare a gate-source voltage of a second transistor to a threshold voltage, wherein the second transistor is coupled to be turned ON in response to the gate-source voltage and the threshold voltage; and
   an output circuit coupled to the second amplifier to generate an output signal.

15. The receiver circuit of claim 14, further comprising:

   a delay circuit coupled to receive the output signal, wherein the delay circuit is coupled to generate a pre-bias control signal responsive to the output signal;
   a first pre-bias circuit coupled to an output of the first amplifier, and coupled to receive the pre-bias control signal from the delay circuit; and
   a second pre-bias circuit coupled to an output of the second amplifier, and coupled to receive the pre-bias control signal from the delay circuit.

16. The receiver circuit of claim 15, wherein the delay circuit is coupled to generate a pulse of the pre-bias control signal that is delayed from a corresponding pulse of the output signal by at least a pulse width of the input pulse.

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