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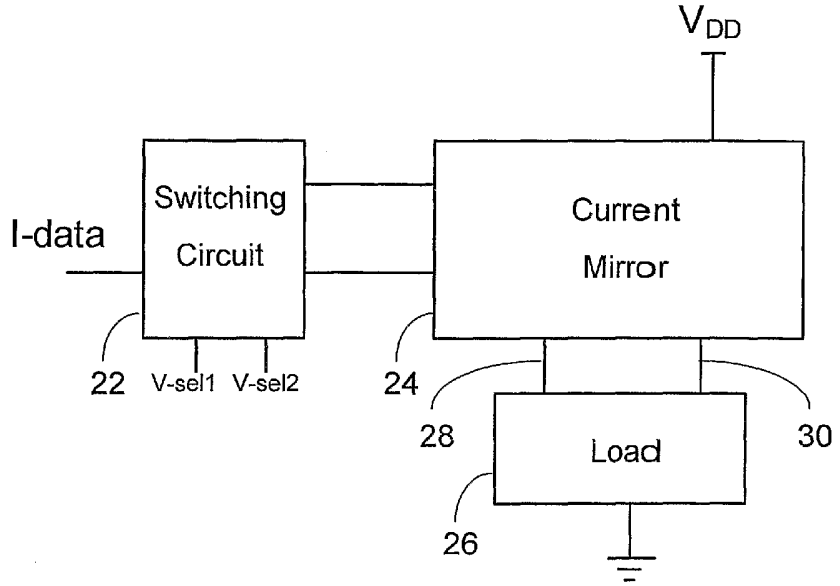
(54) Title: PIXEL DRIVER CIRCUIT



(57) Abstract: A pixel circuit for use in a display comprising a plurality of pixels is provided. The load-balanced current mirror pixel circuit can compensate for device degradation and/or mismatch, and changing environmental factors like temperature and mechanical strain. The pixel circuit comprises a pixel drive circuit comprising, switching circuitry, a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor; and a capacitor connected between the gate of the reference transistor and a ground potential, and a load connected between the current mirror and a ground potential, the load having a first load element and a second load element, the first load element being connected to the first node of the reference transistor and the second load element being connected to the first node of the drive transistor.

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Pixel Driver Circuit

FIELD OF INVENTION

[0001] The present invention relates to circuitry for use in an active matrix display, and more particularly to a current drive circuitry used to drive the electro-luminescent elements.

BACKGROUND OF THE INVENTION

[0002] OLED based displays have gained significant interest recently for many display applications because of their faster response times, larger viewing angles, higher contrast, lighter weight, lower power, and amenability to flexible substrates, as compared to liquid crystal displays (LCDs).

[0003] The simplest way of addressing an OLED display is to use a passive matrix format. Although passive matrix addressed OLED displays are already in the marketplace, they do not support the resolution needed for next generation displays, which use high information content (HIC) formats. HIC formats are only possible with an active matrix addressing scheme.

[0004] Active matrix addressing involves a layer of backplane electronics, based on thin-film transistors (TFTs). These thin film transistors provide the bias voltage and drive current needed in each OLED pixel and may be fabricated using amorphous silicon (a-Si:H), polycrystalline silicon (poly-Si), organic, polymer, or other transistor technologies. When compared to passive matrix addressing, active matrix addressing uses a lower voltage on each pixel and the current throughout the entire frame period is a low constant value. Thus, active matrix addressing avoids the excessive peak driving and leakage currents associated with passive matrix addressing. This increases the lifetime of the OLED.

[0005] LCDs are electric field driven devices. OLEDs, on the other hand, are current driven devices. Thus, the brightness and stability of the light emitted by a given

OLED used in a display is dependent on the operation of the TFTs in the current drive circuit. Thus AMOLED displays are far more sensitive to TFT instabilities including, spatial and temporal variations in transistor threshold voltage, mobility instability, and mismatch issues. These instabilities need to be addressed for widespread use of OLED based displays.

[0006] Figure 1 presents a graph of threshold voltage shift vs. stress voltage for various times for amorphous silicon based TFTs. It is readily apparent from Figure1 that the threshold voltage of the transistors varies over time. If these transistors were used in a display, the variation in threshold voltage would likely result in variation in the brightness of the OLED across the array and/or a decrease in brightness over time, both of which are unacceptable.

[0007] A simple pixel driver circuit is shown in Figure 2. This "2T" circuit is a voltage programmed circuit. Such a circuit is not practical for OLED displays as such a circuit can not compensate for variations in transistor threshold voltage. One solution to this variation in threshold voltage is to use a current programmed circuit to drive the OLED of the pixels. Current programming is a good method for driving AMOLED displays since the OLED is a current driven device, and its brightness is approximately linearly dependent upon the current flowing through it.

[0008] One such current programmed circuit is presented in Figure 3. This circuit incorporates a current-mirror which compensates for any shift or mismatch in the threshold voltage of the drive transistor 12 which ensures that the brightness of the OLED 14 does not decrease over time. This feature of the circuit allows its drive characteristics to be much improved as compared to the 2T circuit of Fig. 2.

[0009] When programming the circuit of Figure 3, $V_{ADDRESS}$ is high and a current I_{DATA} is applied. This current initially flows through transistor T1 and charges capacitor C_S. As the capacitor voltage rises, T3 begins to turn on and I_{DATA} starts to flow through T2 and T3 to ground. The capacitor voltage stabilizes at the point when all of I_{DATA} flows through T2 and T3, and none through T1. This process is independent of the threshold voltage V_T of transistors T3 and T4.

[0010] The gates of T3 and T4 are connected, so the current flowing through T3 is mirrored in T4. This topology allows us to have on-pixel current gain or attenuation depending on the sizing of T3 and T4, so that the respective data current can be

proportionately smaller or larger than the OLED current. In an active matrix array, pixels are scanned and programmed in a row-by-row fashion. The time taken to scan all rows (one frame) is called the frame time. During array operation, the switching TFTs (T1 and T2) are ON only once in the frame time.

[0011] However, existing current programmed circuits do not adequately address long-term stability in the OLED drive current due to differential Vt-shift and other bias, temperature, or mechanical stress related degradations and mismatches in the current mirror.

SUMMARY OF THE INVENTION

[0012] The present invention relates to a circuit for driving light emitting elements in a display and more particularly relates to a current drive circuit that implements a current mirror wherein each transistor of the current mirror is connected to a load.

[0013] It is an object of the invention to provide improvedAMOLED Display Backplanes and Pixel Driver Circuits.

[0014] Accordingly, it is an object of the present invention to provide pixel current driver circuits for active matrix organic light emitting displays (AMOLED), capable of providing stable and predictable drive currents, in the presence of device degradation and/or mismatch, and changing environmental factors like temperature and mechanical strain. The latter is particularly important for mechanically flexible AMOLED displays.

[0015] According to an aspect of the invention a pixel circuit for use in a display comprising a plurality of pixels is provided. The pixel circuit comprises a pixel drive circuit comprising, switching circuitry, a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor; and a capacitor connected between the gate of the reference transistor and a ground potential, and a load connected between the current mirror and a ground potential, the load having a first load element and a second load element, the first load element being connected to the

first node of the reference transistor and the second load element being connected to the first node of the drive transistor.

[0016] According to another aspect of the invention a pixel circuit for use in a display comprising a plurality of pixels is provided. The pixel circuit comprises a pixel drive circuit comprising, switching circuitry, a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor, the second node of the reference and drive transistors connected to a ground potential, and a capacitor connected between the gate of the reference transistor and a ground potential, and a load connected between the current mirror and a potential.

[0017] This summary of the invention does not necessarily describe all features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

[0019] FIGURE 1 shows a graph of threshold voltage shift v. gate stress voltage for various times for thin film transistors made from amorphous silicon;

[0020] FIGURE 2 shows a schematic diagram of a 2T voltage-programmed pixel driver circuit;

[0021] FIGURE 3 shows a schematic diagram of a 4T current-programmed driver circuit;

[0022] FIGURE 4 shows a block diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0023] FIGURE 5A shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0024] FIGURE 5B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0025] FIGURE 5C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0026] FIGURE 6A shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0027] FIGURE 6B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0028] FIGURE 6C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0029] FIGURE 7A shows a block diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0030] FIGURE 7B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0031] FIGURE 7C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

[0032] FIGURE 7D shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention; and

[0033] FIGURE 7E shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention.

[0034] The above objects and features of the present invention will become more apparent by the following description of the preferred embodiments with reference to the attached drawings.

DETAILED DESCRIPTION

[0035] It has been found that the long-term stability of the OLED drive current can be addressed by providing a load to each transistor of the current mirror of a current based drive circuit.

[0036] A block diagram of a pixel driver circuit according to one aspect of the invention is shown in FIGURE 4. The driver circuit can generally be considered to include a switching circuit 22, a current mirror 24 and a load 26. Of particular note is that the load 26 is configured, with respect to the current mirror 24, such that the two transistors of the current mirror 24 have a load connected to them. In the configuration shown in FIGURE 4 the load 26 is connected between the current mirror 24 and ground with connections 28 and 30. Where the connections 28 and 30 are each connected to a node of a transistor of the current mirror and the load 26. This architecture provides for a balancing of the load between the transistors of the current mirror. Embodiments of the invention that implement this architecture will now be presented.

[0037] In the embodiment presented in Figure 4 the switching circuit 22 is connected to two select lines, namely V-sel1 and V-sel2. The embodiments presented in Figures 5A-5C, 6A-6C and 7A-7E likewise have two select lines. The switching circuit 22 is further connected to a single data line, I-data.

[0038] The circuits presented in Figures 5A to 5C have the same basic architecture as the circuit presented in Figure 4, i.e. both transistors of the current mirror are connected to the load 26. The circuits of Figures 5A to 5C present type and configuration variations for the load 26.

[0039] In Figure 5A the current mirror 24 includes a reference transistor 31, a drive transistor 33. The transistors 31 and 33 are thin film transistors which have an amorphous silicon channel. A storage capacitor 25 is included in the current mirror 24. The gates of the transistor 31 and the transistor 33 are tied together and both connected to a plate of the storage capacitor 25. The other plate of the storage capacitor Cs is connected to ground. The source of the reference transistor 31 is connected to potential Vc and the drain is connected to the switching circuit 22. Connecting the source to the potential Vc allows the two sides of the current mirror to

be balanced with proper biasing. The source of the drive transistor 33 is connected to a light emitting diode 32 and the drain is connected to V_{DD}. In this embodiment the light emitting diode 32 is an organic light emitting diode (OLED).

[0040] Figure 5B is a schematic diagram of a pixel driver circuit according to another embodiment of the invention. In this embodiment the source of the reference transistor 31 and the drive transistor 33 are connected to light emitting diodes 36 and 32, respectively.

[0041] Figure 5C presents the currently preferred configuration for the load 26. The transistors 31 and 33 are tied together using a connection 37. In Figure 5C the connection 37 is pictorially located within the load 26. The current embodiment is not limited by this representation. A single OLED 37 is connected to the common connection 37.

[0042] Figures 6A to 6C present embodiments of the invention wherein the current mirror 24 and the load 26 are the same as the embodiment presented in Figure 5C while various configurations of the switching circuitry are provided. The switching circuits presented in Figures 6A to 6C each have a feedback transistor 44 and a switch transistor 46.

[0043] In the circuit presented in Figure 6A one terminal of the feedback transistor 44 and one terminal of the switch transistor 46 are connected to data line I-data. The second terminal of the feedback transistor 44 is connected to the drain of reference transistor 31 while the second terminal of the switch transistor 46 is connected to the gate of the reference and drive transistors 31 and 33, respectively. Finally, the gate of the feedback transistor 44 and switch transistor 46 is connected to the select line V-sel1 and select line V-sel2, respectively.

[0044] In the embodiment presented in Figure 6B the first terminal of the switch transistor 46 is connected to the data line I-data while the first terminal of the feedback transistor 44 is connected to the second terminal of the switch transistor 46 which is connected to the gate of the reference and drive transistors 31 and 33, respectively. The second terminal of the feedback transistor 44 is connected to the drain of the reference transistor 31. Finally, the gate of the feedback transistor 44 and switch transistor 46 is connected to the select line V-sel2 and select line V-sel1, respectively.

[0045] In the embodiment presented in Figure 6C the first terminal of the switch transistor 46 is connected to the data line I-data while the first terminal of the feedback transistor 44 is connected to the second terminal of the switch transistor 46 which is connected to the drain of the reference transistor 31. The second terminal of the feedback transistor 44 is connected to the gate of the reference and drive transistors 31 and 33, respectively. Finally, the gate of the switch transistor 46 and feedback transistor 44 is connected to the select line V-sel1 and select line V-sel2, respectively.

[0046] The circuits that have been considered are embodiments of the circuit presented as a block diagram in Figure 4. An alternative embodiment of the circuit architecture of Figure 4 is presented in Figure 7A. The organization of the switching circuit 22 and the current mirror 24 is the same as the embodiment presented in Figure 4. In this embodiment the load 26 is arranged such that it is between the potential V_{DD} and the current mirror 24. Figure 7B-7E present embodiments of the invention based on the block diagram of Figure 7A. These embodiments implement the same circuit for the current mirror 24 while the configuration of the load 26 varies.

[0047] In the embodiment presented in Figure 7B the load 26 includes light emitting diodes 40 and 42. The diodes 40 and 42 are connected between the potential V_{DD} and the drain of reference transistor 31 and drive transistor 33, respectively. The sources of the reference transistor 31 and the drive transistor 33 are connected to ground. The gates of the reference transistor 31 and the drive transistor 33 are tied together and connected to both the switching circuit 22 and a plate of the storage capacitor 25. In the embodiment presented in Figure 7C the light emitting diode 40 is connected to a potential V_C and the diode 42 is connected to the potential V_{DD}. The embodiments presented in Figures 7D and 7E differ from the embodiments of Figures 7B and 7C, respectively, in that the light emitting diode 40 is replaced with a transistor 47. The gate of transistor 47 is connected to a third select line V-sel3, a first terminal is connected to a potential and a second terminal is connect to the source terminal of reference transistor 32.

[0048] In the schematic diagram of Figures 5B, 7B, and 7C there are two OLEDs in each pixel. Such a double OLED structure is formed by partitioning the bottom electrode of the OLED of each pixel into two electrodes. Partitioning of the electrode provide for the formation of two OLEDs in each pixel. One of the OLEDs is

connected to the drive transistor and the other is connected to the reference transistor. Therefore the load of reference and drive transistors is the same, resulting in a minimization of mismatches between these two transistors. It is noted that the ratio between the areas of the two OLEDs and the gain of the current mirror can be engineered to achieve desired circuit performance.

[0049] According to an alternative embodiment of the invention the transistors can be any appropriate material for the fabrication of thin film transistors including polycrystalline silicon, polymer and organic materials. In particular this embodiment considers appropriate changes for including p-type TFTs that are relevant to persons skilled in the art.

[0050] According to another alternative embodiment of the invention the pixel drive circuits do not include the capacitor Cs.

[0051] According to another alternative embodiment of the invention the switching circuit 22 is appropriate for the use with a single select line.

[0052] According to another alternative embodiment of the invention the transistors of the pixel driver circuits may have more than one gate. In particular the transistors may be dual gate transistors.

[0053] According to another alternative embodiment of the invention there is more than one driver circuit for a given pixel. In particular there may be three pixel driver circuits as would be appropriate for pixels in an RGB or colour display.

[0054] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A pixel circuit for use in a display comprising a plurality of pixels, the pixel circuit comprising:

a pixel drive circuit comprising:

switching circuitry;

a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor; and

a capacitor connected between the gate of the reference transistor and a ground potential; and

a load connected between the current mirror and a ground potential, the load having a first load element and a second load element, the first load element being connected to the first node of the reference transistor and the second load element being connected to the first node of the drive transistor.

2. The pixel circuit according to claim 1, wherein the first node of the reference transistor is connected to a first potential and a light emitting diode is connected between the first node of the drive transistor and the ground potential.

3. The pixel circuit according to claim 1, wherein a first light emitting diode is connected between the node of the drive transistor and a ground potential and a second light emitting transistor is connected between the node of the reference transistor and a ground potential.

4. The pixel circuit according to claim 3, wherein the node of the drive transistor and the node of the reference transistor are connected.

5. The pixel circuit according to claim 1, wherein the node of the drive transistor and the node of the reference transistor are connected and a light emitting diode is connected between the node of the drive transistor and a ground potential.

6. The pixel circuit according to claim 1, wherein the switching circuitry comprises:

a feedback transistor having a gate connected to a first select line, a first node connected to a data line and a second node connected to the second node of the reference transistor; and

a switch transistor having a gate connected to a second select line, a first node connected to the data line and a second node connected to the gate of the reference transistor.

7. The pixel circuit according to claim 1, wherein the switching circuitry comprises:

a switch transistor having a gate connected to a first select line, a first node connected to the data line and a second node connected to the gate of the reference transistor; and

a feedback transistor having a gate connected to a second select line, a first node connected to the gate of the reference transistor and a second node connected to the second node of the reference transistor.

8. The pixel circuit according to claim 1, wherein the switching circuitry comprises:

a switch transistor having a gate connected to a first select line, a first node connected to a data line and a second node connected to the second node of the reference transistor;

a feedback transistor having a gate connected to a second select line, a first node connected to the second node of the reference transistor and a second node connected to the gate of the reference transistor.

9. The pixel circuit according to claim 1 wherein the transistors are thin film transistors.

10. The pixel circuit according to claim 9 wherein the thin film transistors are amorphous silicon.

11. The pixel circuit according to claim 9 wherein the thin film transistors are polycrystalline silicon.

12. The pixel circuit according to claim 11 wherein the polycrystalline silicon is p-type.

13. The pixel circuit according to claim 9 wherein the thin film transistors are organic.

14. The pixel circuit according to claim 13 wherein the organic is p-type.

15. A pixel circuit for use in a display comprising a plurality of pixels, the pixel circuit comprising:

a pixel drive circuit comprising:

switching circuitry;

a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor, the second node of the reference and drive transistors connected to a ground potential; and

a capacitor connected between the gate of the reference transistor and a ground potential; and

a load connected between the current mirror and a potential.

16. The pixel circuit according to claim 15 wherein, the load comprises a first and second load element connected between the current mirror and the potential.

17. The pixel circuit according to claim 16 wherein the first and second load elements are light emitting diodes.

18. The pixel circuit according to claim 17 wherein the potential is V_{DD}.

19. The pixel circuit according to claim 16 wherein the first load element is connected to a first potential and the second load element is connected to V_{DD}.

20. The pixel circuit according to claim 15 wherein the first load element is a transistor having a gate, a first node and a second node, the gate being connected to a third select line, the first node being connected to the second node of the reference

transistor and the second node connected to V_{DD}, the second load element being a light emitting diode connected between the second node of the drive transistor and V_{DD}.

21. The pixel circuit according to claim 15 wherein the first load element is a transistor having a gate, a first node and a second node, the gate being connected to a third select line, the first node being connected to the second node of the reference transistor and the second node connected to a second potential, the second load element being a light emitting diode connected between the second node of the drive transistor and V_{DD}.

22. The pixel circuit according to claim 15 wherein the transistors are thin film transistors.

23. The pixel circuit according to claim 22 wherein the thin film transistors are amorphous silicon.

24. The pixel circuit according to claim 22 wherein the thin film transistors are polycrystalline silicon.

25. The pixel circuit according to claim 24 wherein the polycrystalline silicon is p-type.

26. The pixel circuit according to claim 22 wherein the thin film transistors are organic.

27. The pixel circuit according to claim 26 wherein the organic is p-type.

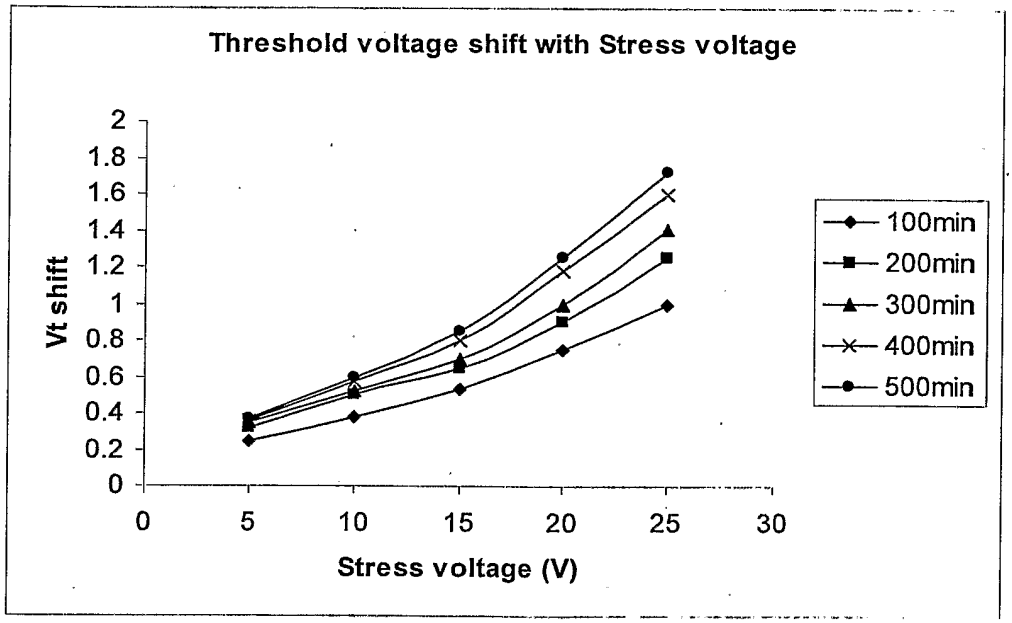

Figure 1 (PRIOR ART)

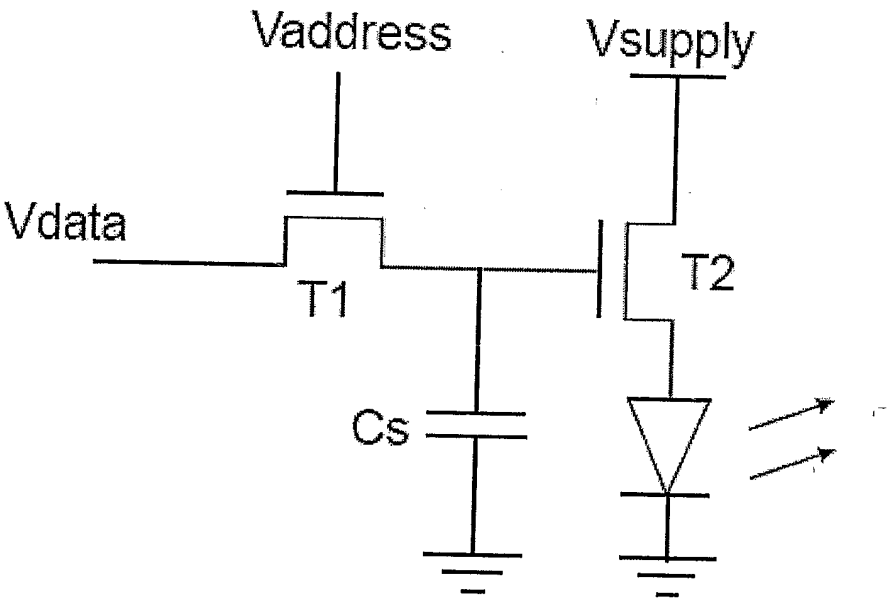

Figure 2 (PRIOR ART)

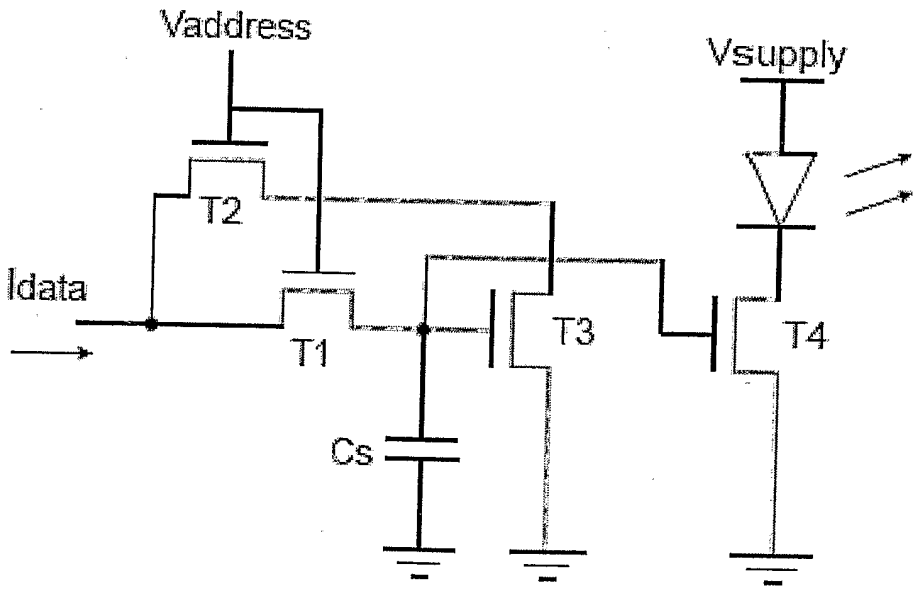

Figure 3 (PRIOR ART)

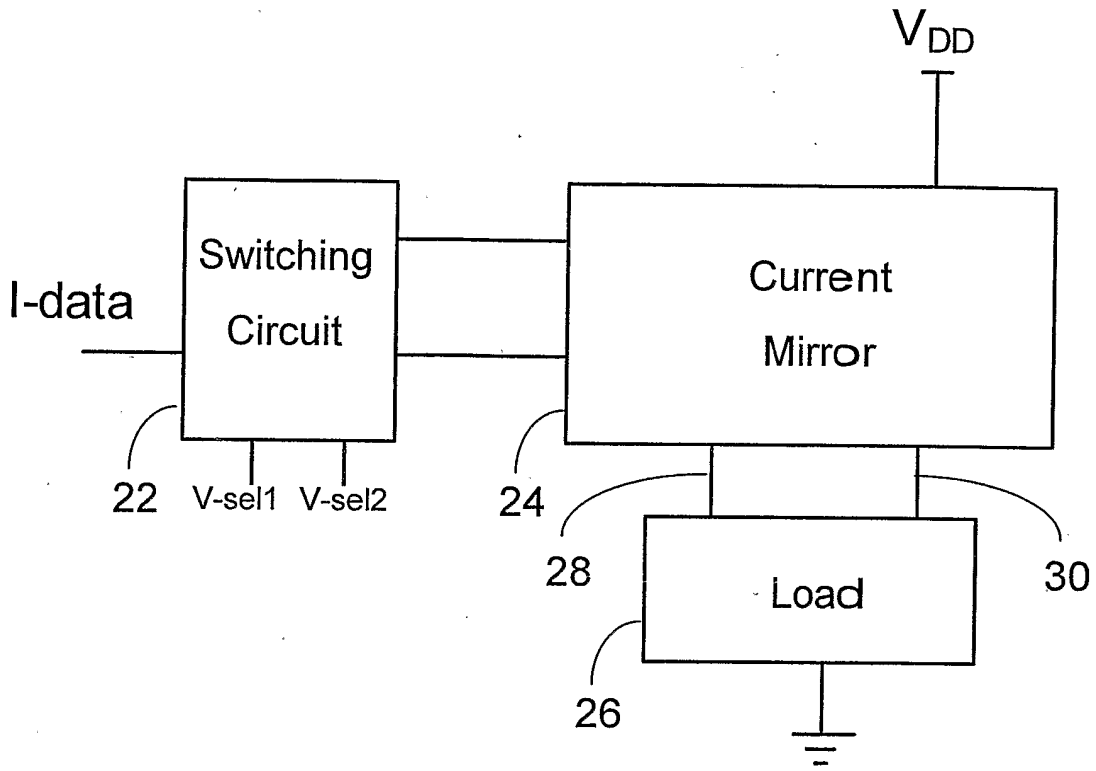
V_{DD}
Switching
Circuit
I-data
Current
Mirror
22
V-sel1
V-sel2
24
28
Load
30
26

Figure 4

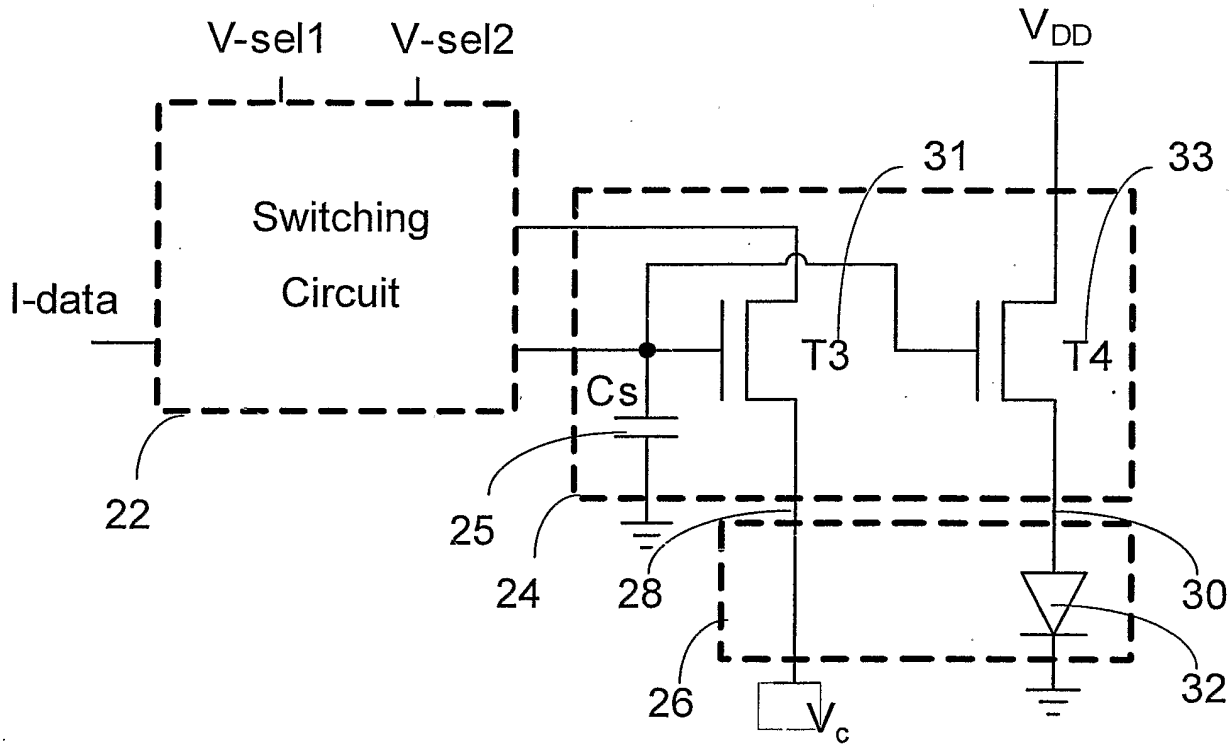
V-sel1
V-sel2
V_{DD}
31
33
Switching
Circuit
I-data
T3
T4
Cs
22
25
24
28
30
26
32
V_c

Figure 5A

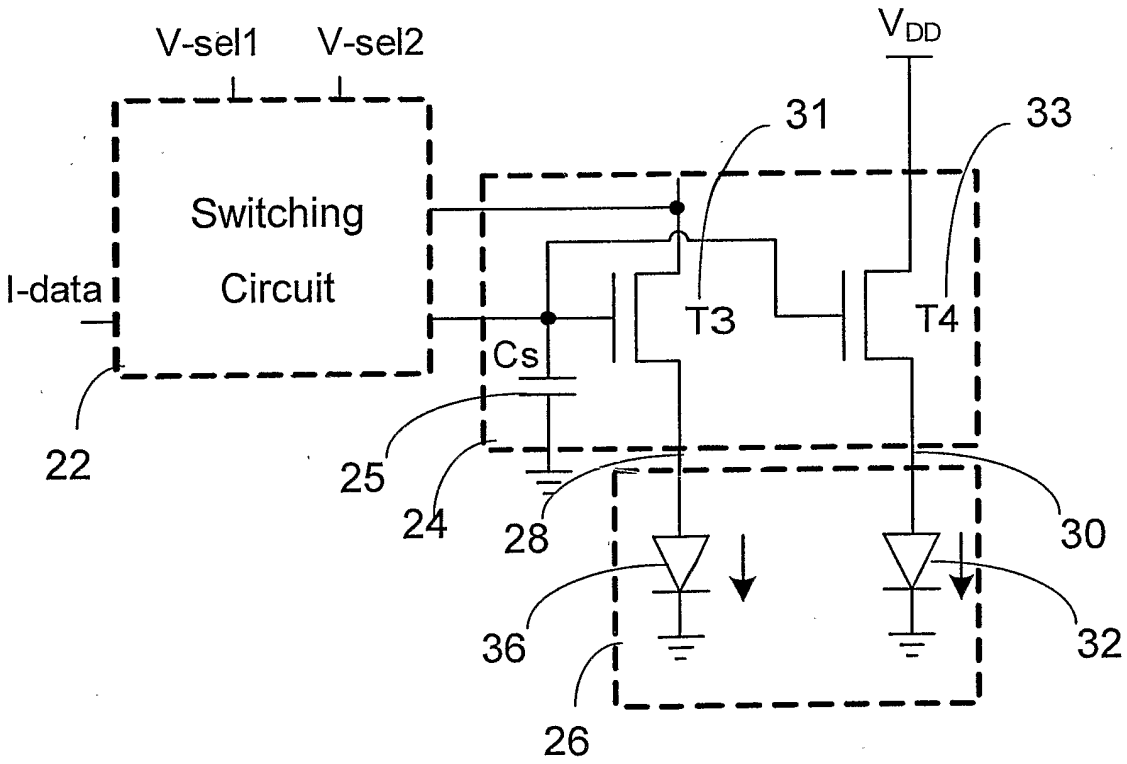
V-sel1
V-sel2
V_{DD}
31
33
Switching
Circuit
I-data
T3
T4
Cs
22
25
24
28
30
36
32
26

Figure 5B

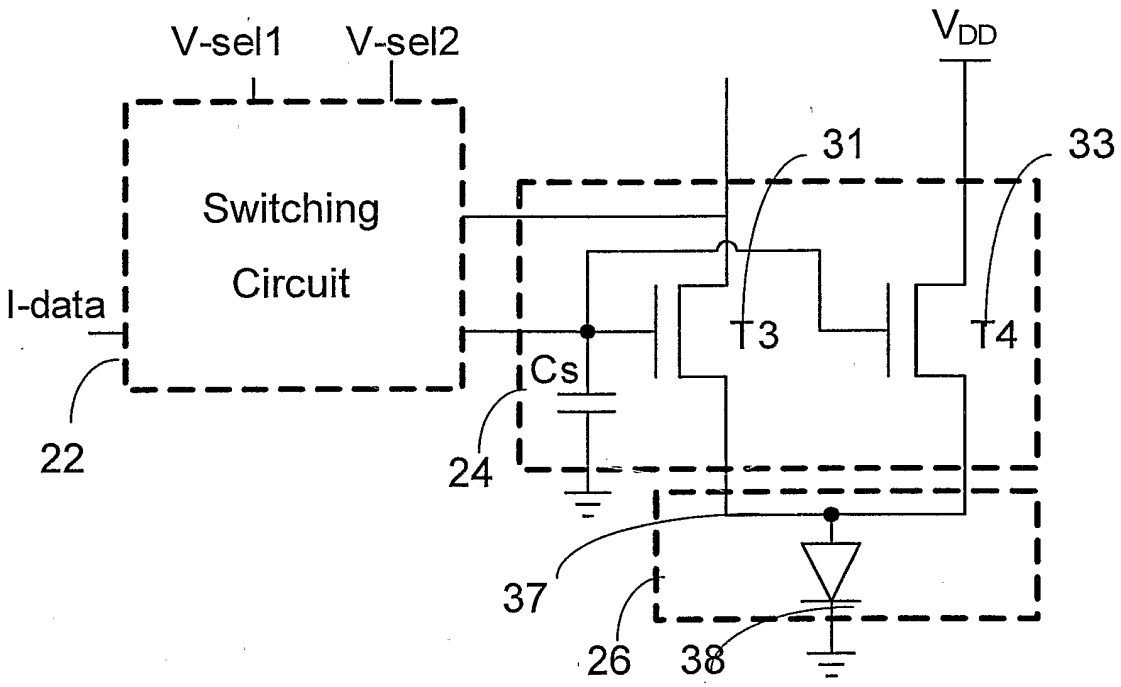
V-sel1
V-sel2
V_{DD}
31
33
Switching
Circuit
I-data
T3
T4
Cs
22
24
37
26
38

Figure 5C

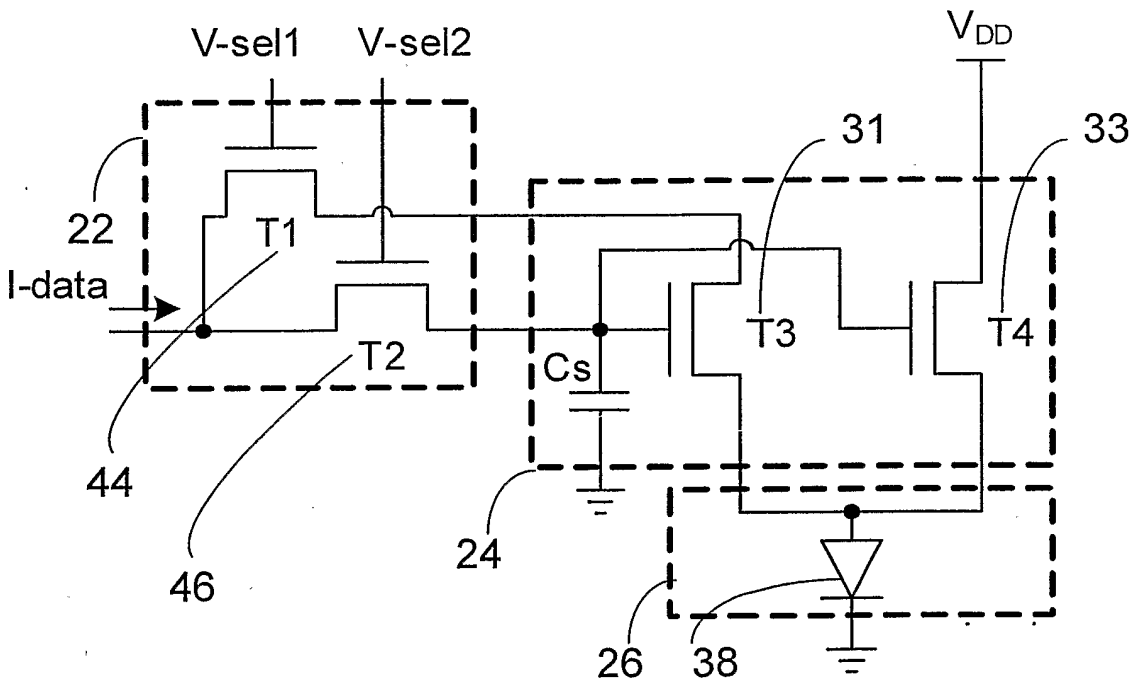

Figure 6A

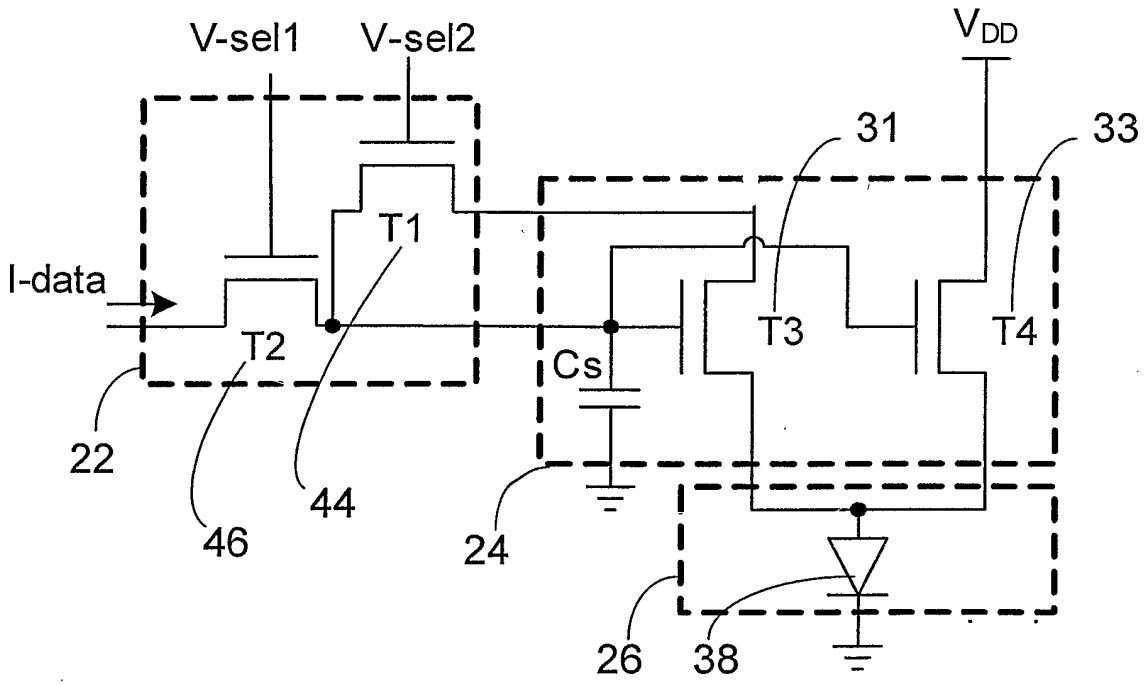

Figure 6B

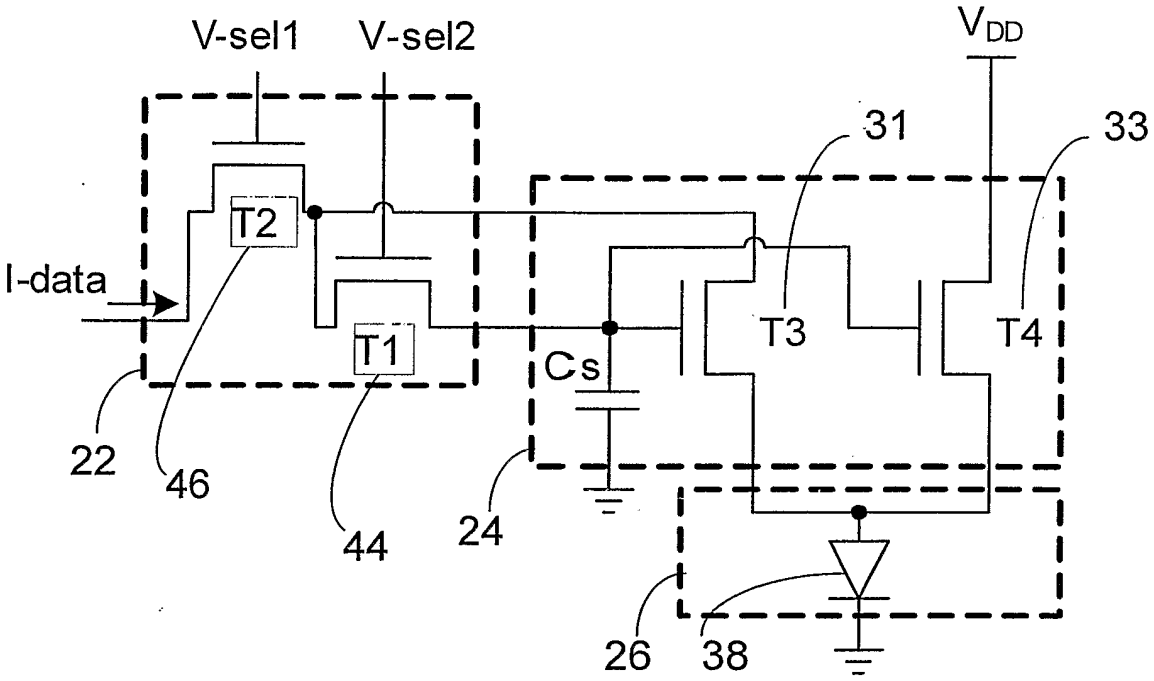

Figure 6C

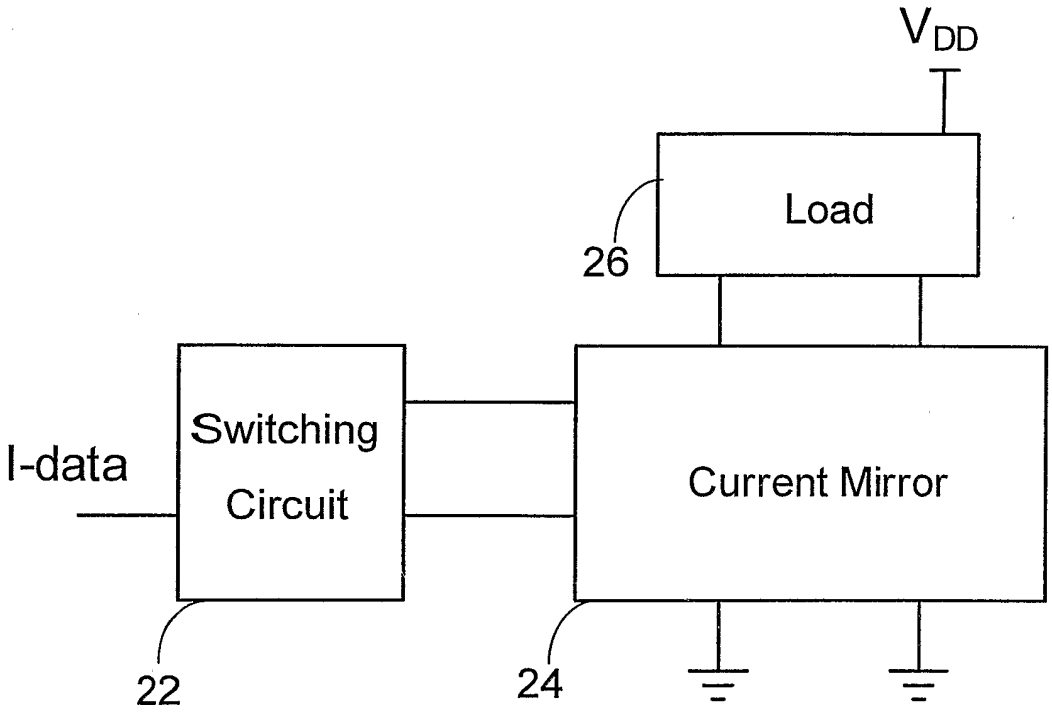

Figure 7A

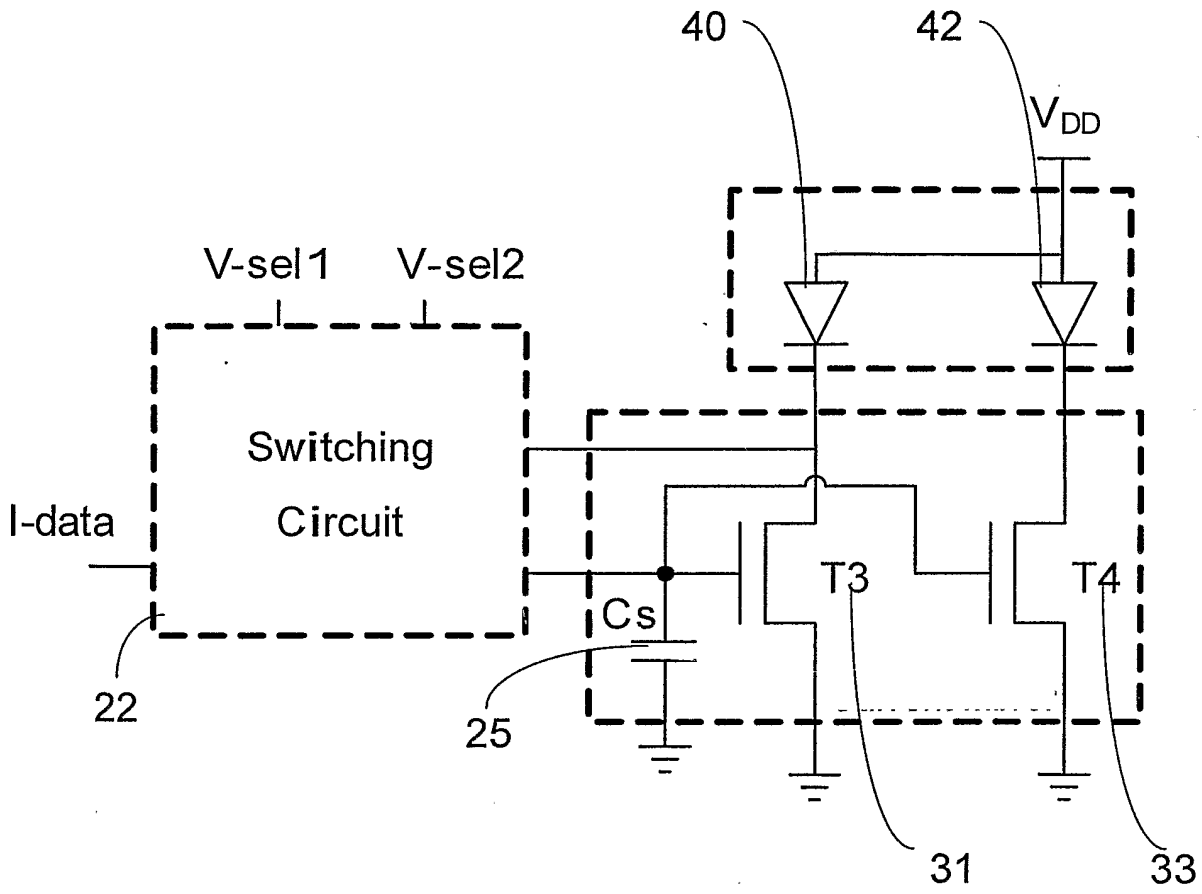
40
42
V_{DD}
V-sel1
V-sel2
Switching
Circuit
I-data
Cs
T3
T4
22
25
31
33

Figure 7B

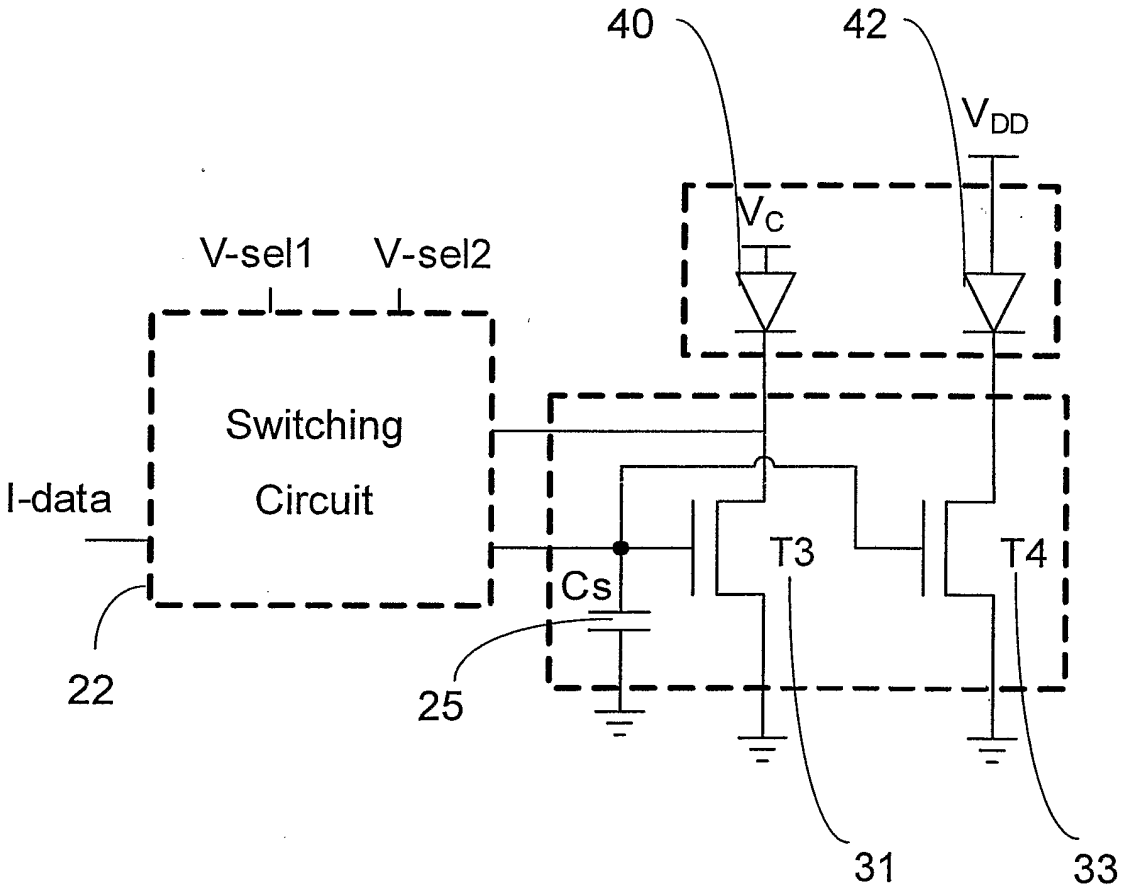
40
42
V_{DD}
V_C
V-sel1
V-sel2
Switching
Circuit
I-data
Cs
T3
T4
22
25
31
33

Figure 7C

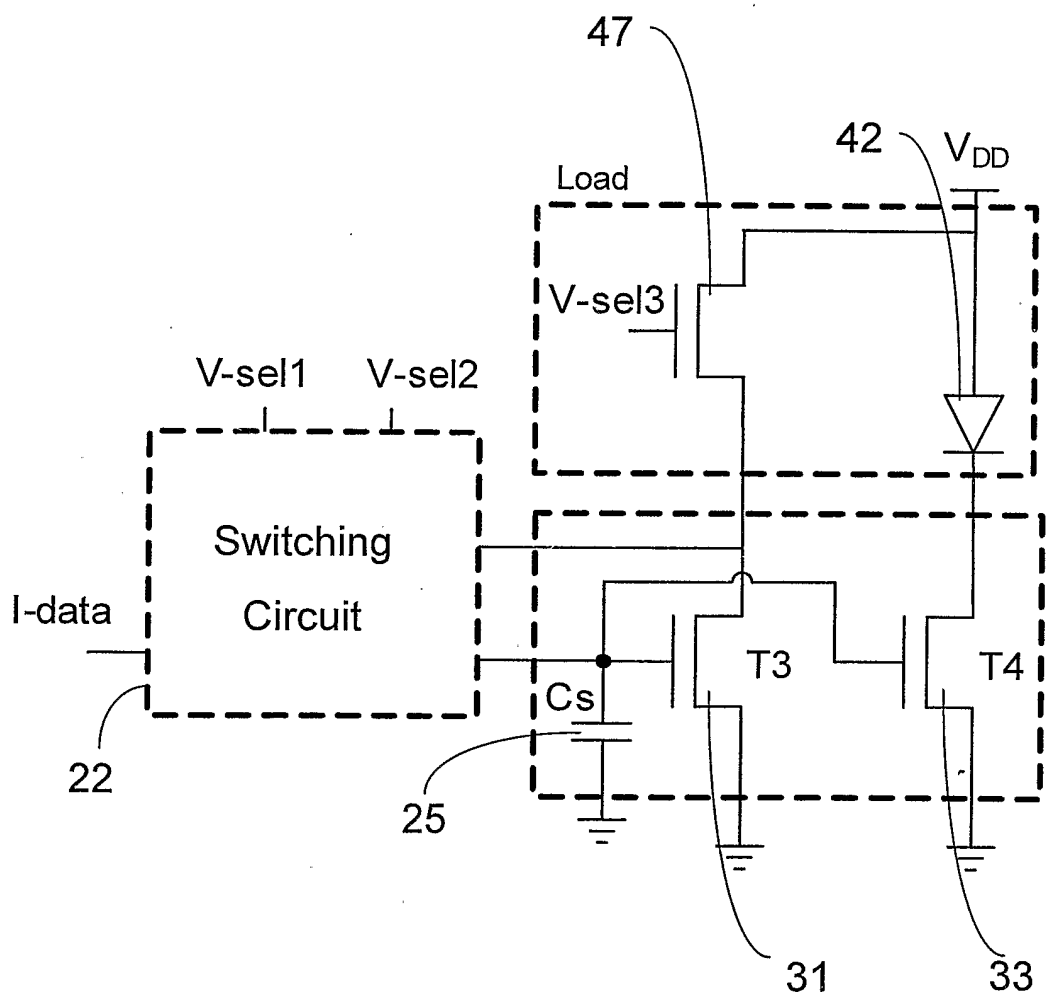
47
42
V_{DD}
Load
V-sel3
V-sel1
V-sel2
Switching
Circuit
I-data
T3
T4
Cs
22
25
31
33

Figure 7D

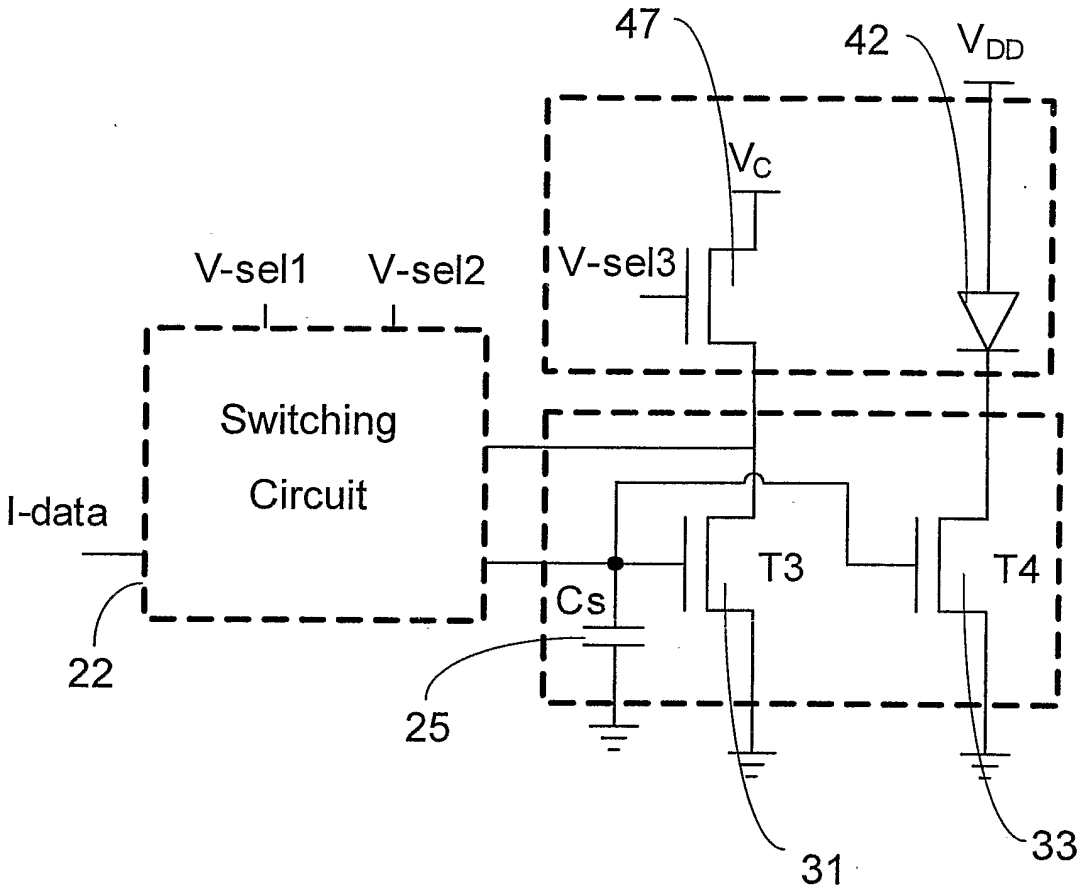
47
42
V_{DD}
V_C
V-sel1
V-sel2
V-sel3
Switching
Circuit
I-data
T3
T4
Cs
22
25
31
33

Figure 7E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2004/001741

A. CLASSIFICATION OF SUBJECT MATTER

G09G-3/32; G09F-9/33

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC[7] G09G-3/32, G09F-9/33; CA 40/43, 40/53, 375; US 323/315

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base, and, where practicable, search terms used) :
Delphion, USPTO, Espacenet, Canadian Patent Database;
Keywords : light emitting diode; current mirror; stable current; transistor gate; reference transistor, thin film, polycrystalline, amorphous, organic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CA 2436451 (TAKENAKA et al.) 15 August 2002 (15.08 2002), abstract; page 20 (lines 10-20)	15, 22-23
Y	CA 2354018 (VU et al.) 22 June 2000 (22.06.2000), abstract, page 1 (lines 10-15) and page 2 (lines 21-24)	15, 22, 24-25
Y	CA 2249592 (SHIOYA et al) 30 July 1998 (30 07.1998), abstract, page 1 (line 20) to page 2 (line 14)	15, 22, 26-27
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A	CA 2 368 386 (HOLLOMAN) 23 September 1999 (23 09.99), abstract	1, 15

Further documents are listed in the continuation of Box C.

Patent family members are listed in annex.

* Special categories of cited documents :
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international-type search	Date of mailing of the international-type search report
21 December 2004 (21-12-2004)	21 February 2005 (21-02-2005)
Name and mailing address of the ISA/CA *Commissioner of Patents* *Canadian Patent Office - PCT* *Ottawa/Gatineau K1A 0C9* Facsimile No 1-819-953-9358	Authorized officer Terry Cartile (819) 997-2951

Form PCT/ISA/210 (second sheet) (January 2004)

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