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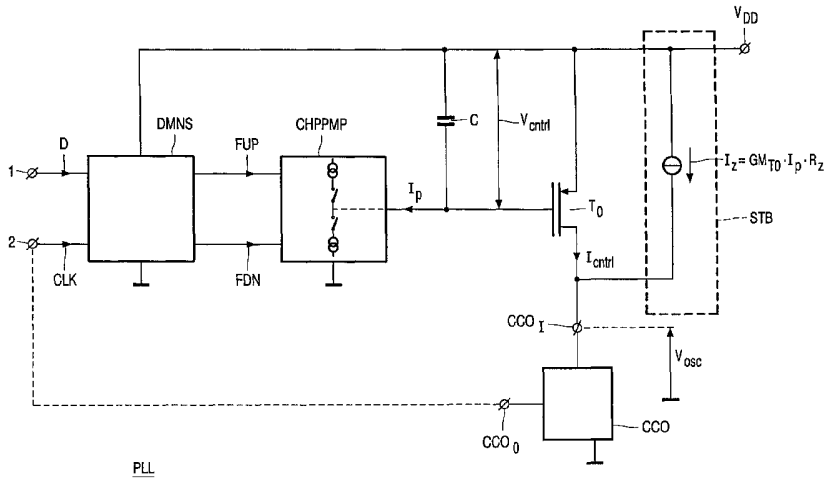
(54) Title: A FREQUENCY OR PHASE-LOCKED LOOP PROVIDED WITH IMPROVED STABILITY TECHNIQUE




(57) Abstract: An electronic circuit comprising a frequency or phase-locked loop (PLL) comprising a first input terminal (1) coupled to receive a first input signal (D); a second input terminal (2) coupled to receive a second input signal (CLK); detection means (DMNS) for comparing the frequency or phase of the first input signal (D) with the frequency or phase of the second input signal (CLK), respectively, and for supplying directly or via a charge pump (CHPPMP) a control voltage (Vcntrl) as a result of the comparison of the first (D) and second (CLK) input signals; a control transistor (T0) having a first main terminal and a control terminal which are coupled to receive the control voltage (Vcntrl) and having a second main terminal for supplying a control current (Icntrl) responsive to the control voltage (Vcntrl); a capacitor (C) coupled in between the first main terminal and the control terminal; a current controlled oscillator (CCO) having an input terminal (CCOI) coupled to receive the control current (Icntrl) and having an output terminal (CCOO) for supplying directly or via frequency dividers the second input signal (CLK) having a frequency or phase which is synchronized with the frequency or phase, respectively, of the first input signal (D); and a stabilizing circuit (STB) for stabilizing the frequency or phase-locked loop (PLL) by adding a zero to the loop transfer function of the frequency or phase-locked loop (PLL). The stabilizing circuit (STB) further comprises a further charge pump (CHPPMPF) for delivering a compensation current (Iz) to the input terminal (CCOI) of the current controlled oscillator (CCO), while the compensation current (Iz) may have an approximately zero value, a negative value, or a possitive value dependent on control signals (FUP, FDN) delivered by the detection means (DMNS), and the absolute value of said positive or negative value roughly linearly depends on the control voltage (Vcntrl).

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# A frequency or phase-locked loop provided with improved stability technique

The invention relates to an electronic circuit comprising a frequency or phase-locked loop comprising a first input terminal coupled to receive a first input signal; a second input terminal coupled to receive a second input signal; detection means for comparing the frequency or phase of the first input signal with the frequency or phase of the second input signal, respectively, and for supplying directly or via a charge pump a control voltage as a result of the comparison of the first and second input signals; a control transistor having a first main terminal and a control terminal which are coupled to receive the control voltage and having a second main terminal for supplying a control current responsive to the control voltage; a capacitor coupled in between the first main terminal and the control terminal; a current controlled oscillator having an input terminal coupled to receive the control current and having an output terminal for supplying directly or via frequency dividers the second input signal having a frequency or phase which is synchronized with the frequency or phase, respectively, of the first input signal; and a stabilizing circuit for stabilizing the frequency or phase-locked loop by adding a zero to the loop transfer function of the frequency or phase-locked loop.

Such an electronic circuit is generally known from the state of the art, as for example shown in Figure 1. In Figure 1 a phase-locked loop, further denoted as PLL, is shown. Instead of a PLL also a frequency-locked loop circuit can be used if the detection means DMNS comprises a frequency-comparator instead of a phase-comparator. In many applications the detection means DMNS is a combined frequency/phase-comparator. For clarity reasons the invention will only be described as a PLL.

PLLs are widely used in applications requiring controlled loop gains to ensure optimum time response. If a PLL is used in an integrated circuit, the loop gain of the PLL may vary with temperature, supply voltage, and process dependent parameters such as oxide thickness, sheet resistances, implant concentrations, etcetera. The PLL includes a phase comparator DMNS which receives a (self-clocking) signal D from an asynchronous data source. The phase comparator DMNS supplies a frequency incrementing control signal FUP and a frequency decrementing control signal FDN to a charge pump CHPPMP. The charge pump CHPPMP generates a pump output current $I_p$, which flows in either a positive or

negative direction depending on whether one or the other of the respective frequency incrementing/decrementing signals FUP or FDN, is supplied. The pump output current $I_p$ is generated with modulated fixed-magnitude pulses.

The $I_p$ current pulses will either add charge to or withdraw charge from a charge accumulating capacitor C. Charge accumulation in the capacitor C generates an integrated voltage $V_{CNTRL}$ which is applied to the input of the current controlled oscillator CCO via the control transistor $T_0$. The CCO produces a (periodic) signal CLK having a variable frequency $f_{osc}$ which is a function of its input voltage. The signal CLK is fed back to input 2 of the phase comparator DMNS while the signal D which is generally aperiodic and is therefore of unknown phase and frequency is supplied to input 1 of the phase comparator DMNS.

Although the signal D is generally aperiodic, it is self-clocking in the sense that is has a fundamental clock frequency which can be derived by averaging over time. The PLL is designed to derive this fundamental clock frequency and to lock on to the phase of the incoming signal D as well. The operation of the PLL will be explained for the case where the signals CLK lags behind the signal D and then for the case where the signal CLK leads the signal D. In situations where incoming edges of the signal arrive before the corresponding edges of the signal CLK (the signal CLK lags), the phase comparator DMNS outputs the frequency incrementing signal FUP to the charge pump CHPPMP and thereby causes the charge pump CHPPMP to supply a positive value of the pump current $I_p$ (see the direction of the arrow with regard to $I_p$ in Figure 1). Thus the integrating capacitor C accumulates charge. The input voltage $V_{osc}$ of the CCO, or in fact the current into the input terminal $CCO_I$, is incremented by the accumulated charge and in response the CCO increases the speed of the signal CLK. The frequency $f_{osc}$ of the signal CLK is incremented to a higher value than the fundamental clock frequency of the signal D. The edges of the faster signal CLK then begin to catch up with the edges of the slower signal D. The output frequency $f_{osc}$ drops back to the value of the fundamental clock frequency as the edges of the signal CLK close in on the edges of the signal D. Once the signal CLK is substantially in phase with the signal D, the phase comparator DMNS ceases to output the frequency incrementing signal FUP and the output frequency $f_{osc}$ is held at a steady-state value which is for practical purposes equal to the fundamental clock frequency of the signal D.

For cases where the signal D edges lag behind the signal CLK edges, the phase comparator DMNS outputs the frequency decrementing signal FDN to the charge pump CHPPMP thereby causing the charge pump CHPPMP to supply a negative value of the pump

current $I_p$. Thus the capacitor C discharges, thereby reducing $V_{cntrl}$ and $V_{osc}$ and causing the frequency $f_{osc}$ of the CCO to decrease. This delays the signal CLK edges until the edges of the signal D catch up and align with the signal CLK. The FDN control signal is shut off once phase alignment has been obtained.

Typically, the charge pump is designed to deliver the pump current $I_p$ in the form of positive or negative rectangular current pulses. The magnitude of the CCO input voltage $V_{osc}$, or in fact the current into the input terminal $CCO_I$, is changed by modulating the pulse width of the pump current pulses. A generally linearly combined transfer function results from the counterbalancing effect of the characteristic gain function belonging to the control transistor $T_0$, the current controlled oscillator CCO, and the chargepump CHPPMP. By the way, in many PLL schematic diagrams a voltage controlled oscillator VCO is shown instead of the current controlled oscillator CCO. This is, however, not a real difference; the control transistor $T_0$ in combination with the CCO of Figure 1 forms in fact a VCO.

For stability reasons, a so-called zero is implemented in the loop transfer function of the PLL. In the general state of the art the zero is usually implemented by the addition of a resistor in series with the capacitor C, as is indicated in Figure 1 by compensation resistor $R_z$. This has, however, the disadvantage that the control voltage $V_{cntrl}$ can easily be disturbed since the control voltage $V_{cntrl}$ is less effectively decoupled by the capacitor C as a result of the addition of the compensation resistor $R_z$.

It is an object of the invention to provide an electronic circuit comprising a frequency or phase-locked loop which does away with above disadvantage.

To this end, according to the invention, the stabilizing circuit comprises a further charge pump for delivering a compensation current to the input terminal of the current controlled oscillator, while the compensation current may have an approximately zero value, a negative value, or a possitive value depending on control signals delivered by the detection means, and the absolute value of said positive or negative value roughly linearly depends on the control voltage.

By these measures the desired zero for stability reasons is implemented without using a resistor in series with the capacitor. Therefore, the control voltage cannot easily be disturbed, since the capacitor also functions very effectively as a decoupling means.

US-patent 5,942,947 shows an alternative solution which needs a digital damping circuit for implementing the zero. The solution according to the invention does not need such digital circuitry.

The stabilizing circuit can be used in several ways. It is for instance possible to apply a transistor in which the drain or collector supplies a reference current for the further charge pump, because a resistor is connected in series with the source or emitter, and the gate or base, and a node of the resistor, which node is not connected to said source or emitter, receives the control voltage across the capacitor. The value of the resistor must be high in comparison with $1/g_M$ of said transistor, or, alternatively, the $g_M$ of the transistor must be enhanced by the addition of an amplifier. The enhancement of the $g_M$ of a transistor by an amplifier is well known in the prior art.

In an embodiment of the invention a field effect transistor is used as the control transistor, the former having a source, a drain, and a gate which respectively form the first main terminal, the second main terminal, and the control terminal of the control transistor, and the stabilizing circuit further comprises a first field effect transistor; a second field effect transistor; a third field effect transistor; a fourth field effect transistor; a current mirror having an input coupled to the drain of the first transistor and an output coupled to the drain of the fourth transistor; and means for supplying a DC-voltage between the drain and the gate of the fourth transistor, the sources of the third and fourth transistors being coupled to the source of the control transistor, the gate of the third transistor being coupled to the gate of the fourth transistor, the source of the first transistor being coupled to the drain of the third transistor, the source of the second transistor being coupled to the drain of the fourth transistor, the gates of the first and second transistors being coupled to the gate of the control transistor, and a reference input of the further charge pump being coupled to the current mirror in a manner that said absolute value is approximately linearly dependent on the current through the input of the current mirror.

This embodiment has the advantage that no resistor is needed at all.

Further advantageous embodiments are specified in further dependent claims.

The invention will be described in more detail with reference to the accompanying drawing, in which:

Figure 1 is a circuit diagram of an electronic circuit comprising a known PLL;

Figure 2 shows circuit diagrams of current or voltage controlled oscillators which can be used in PLLs;

Figure 3 shows a diagram of a current controlled oscillator and a control transistor for delivering a control current to the current controlled oscillator in response to a control voltage, and figures for indicating the relation of the frequency of the current

controlled oscillator to the control voltage, the current through the current controlled oscillator, and the voltage across the current controlled oscillator;

Figure 4 is a circuit diagram of an electronic circuit comprising a PLL according to the invention;

Figure 5 is a detailed circuit diagram of an inventive stabilizing circuit which can be applied in the inventive PLL according to Figure 4;

Figure 6 is a circuit diagram of a charge pump which can be used in PLLs; and

Figure 7 is a more detailed circuit diagram of the inventive stabilizing circuit according to Figure 5 in which a use of the further charge pump is shown.

In these figures parts or elements having like functions or purposes bear like reference symbols.

Figure 4 shows a PLL according to the invention. The differences with respect to the PLL according to Figure 1 are the removal of the compensation resistor $R_z$ and the addition of the stabilizing circuit STB. A field effect transistor $T_O$ is used as the control transistor $T_0$ by way of example. In this situation the current controlled oscillator CCO, further denoted as CCO, is preferably used by one of the circuits shown in Fig. 2A, Fig. 2B, or Fig. 2C. By doing so the frequency $f_{osc}$ of the CCO is approximately linearly dependent on the control voltage $V_{cntrl}$ or the voltage $V_{osc}$ across the CCO, as is schematically indicated in Figure 3.

The stabilizing circuit STB is demonstrated as a current source (in Figure 4) which can either push ($I_p$ is positive) or pull ($I_p$ is negative) a current into the input terminal $CCO_I$ of the CCO, or do not deliver current at all ($I_p$=0), which is determined by the control signals FUP and FDN. To obtain a good stability, the compensation current $I_z$ is determined by formula:

$$I_z = GM_{T0} \cdot I_p \cdot R_z \qquad [1]$$

in which: $GM_{T0}$ is the transconductance of the control transistor $T_0$; $I_p$ is the pump output current from the charge pump CHPPMP; and $R_z$ is the value of the compensation resistor $R_z$ which would have been necessary in well-known prior art PLLs.

With the aid of formula [1] the inventive PLL of Figure 4 is dimensioned as follows for stability purposes: determine the value of the resistor $R_z$ in the prior art PLL of

Figure 1, determine the value of the compensation current $I_z$ by filling in the value of said resistor $R_z$ in formula [1]. So if for example the optimal value of resistor $R_z$ in the prior art would have been 100 Ohm, then the value of the compensation current $I_z$ is determined by:

$I_z = 100 \bullet GM_{TO} \cdot I_p$

Figure 5 shows a detailed circuit diagram of a preferred embodiment of the stabilizing circuit STB. The stabilizing circuit STB comprises a first field effect transistor $T_1$; a second field effect transistor $T_2$; a third field effect transistor $T_3$; a fourth field effect transistor $T_4$; a current mirror CM having an input connected to the drain of the first transistor $T_1$ and an output connected to the drain of the fourth transistor $T_4$; and means for supplying a DC-voltage $V_{TUNE}$ between the drain and the gate of the fourth transistor $T_4$, the sources of the third and fourth transistors are $T_3$ and $T_4$ being connected to the source of the control transistor $T_0$, the gate of the third transistor $T_3$ being connected to the gate of the fourth transistor $T_4$, the source of the first transistor $T_1$ being connected to the drain of the third transistor $T_3$, the source of the second transistor $T_2$ being connected to the drain of the fourth transistor $T_4$ and the gates of the first and the second transistors $T_1$ and $T_2$ being connected to the gate of the control transistor $T_0$. The stabilizing circuit STB further comprises a further charge pump $CHPPMP_F$ for delivering a compensation current $I_z$ to the input terminal $CCO_I$ of the current controlled oscillator CCO.

The current mirror CM comprises a first current mirror transistor $cm_1$ having a first main terminal, a second main terminal, and a control terminal, the second main terminal and the control terminal being connected to each other and thereby forming the input of the current mirror CM; and a second current mirror transistor $cm_2$ having a first main terminal connected to the first main terminal of the first current mirror transistor $cm_1$, a second main terminal which forms the output of the current mirror CM, and a control terminal which is connected to the control terminal of the first current mirror transistor $cm_1$.

The first main terminals of the first current mirror transistor $cm_1$ and of the second current mirror transistor $cm_2$ are connected to the first power supply terminal $V_{SS}$. The sources of the third and fourth transistors $T_3$ and $T_4$ are connected to the second power supply terminal $V_{DD}$. Field effect transistors or bi-polar transistors may be used as the first and second current mirror transistors $cm_1$ and $cm_2$.

A reference input $Iz_{RF}$ of the further charge pump $CHPPMP_F$ is connected to the input of the current mirror CM.

A transistor $T_5$ which is arranged as a diode configuration and which is biased by a current $I_{TUNE}$ is used as the means for supplying the DC-voltage $V_{TUNE}$ by way of example.

The stabilizing circuit STB is dimensioned in a manner that the first and second transistors $T_1$ and $T_2$ are in their saturation region, the third and fourth transistors $T_3$ and $T_4$ are in their linear region, and in a manner that the drain-source voltage of the third transistor $T_3$ is approximately two times as high as the drain-source voltage of the fourth transistor $T_4$. In this way the stabilizing circuit STB delivers a reference current $I_{mr}$ which is approximately linearly dependent on the control voltage $V_{CNTRL}$. It in fact "matches" with formula [1] in that $R_z$ is now determined by $V_{TUNE}$ (or $I_{TUNE}$). By the connection of the reference input $Iz_{RF}$ of the further charge pump $CHPPMP_F$ to the input (gate and drain connection of first current mirror transistor $cm_1$) of the current mirror CM the reference current $I_{mr}$ is copied (see Figure 7) into the further charge pump $CHPPMP_F$ to serve as the reference current for the further charge pump $CHPPMP_F$.

Figure 6 shows a use for the charge pump CHPPMP which comprises N-type field effect transistors $T_6$, $T_8$, $T_9$ and $T_{12}$, P-type field effect transistors $T_7$, $T_{10}$, and $T_{11}$, and a reference current source $I_{ref}$. The gates of transistor $T_8$ and $T_{10}$ are coupled to receive the control signals FUP and FDN, respectively. The sources of transistors $T_6$, $T_8$, and $T_{12}$ are connected to the first power supply terminal $V_{SS}$. The sources of transistors $T_7$ and $T_{10}$ are connected to the second power supply terminal $V_{DD}$. The gates of transistors $T_7$ and $T_{11}$ and the drains of transistors and the drains of transistors $T_6$ and $T_7$ are connected to each other. The gates of transistors $T_6$, $T_9$, and $T_{12}$, and the drain of transistor $T_{12}$ are connected to each other. The drain of transistor $T_8$ is connected to the source of transistor $T_9$. The drain of transistor $T_{10}$ is connected to the source of transistor $T_{11}$. The drains of transistors $T_9$ and $T_{11}$ are connected to each other to form an output for supplying the pump output current $I_p$. The reference current source $I_{ref}$ is coupled to supply a reference current $I_{ref}$ through the transistor $T_{12}$.

The charge pump CHPPMP according to Figure 6 operates as follows. Transistors $T_{12}$ and $T_6$ form a current mirror which in this example has a mirror ratio of approximately one. Therefore, a reference current $I_{ref}$ is supplied through the transistor $T_7$.

If the control signal FUP has a logic low level and the control signal FDN has a logic high level, both transistors $T_8$ and $T_{10}$ are non-conducting. Therefore, also transistors

$T_9$ and $T_{11}$ are non-conducting. As a consequence, the value of the pump output current $I_p$ is zero.

A substantially zero pump output current $I_p$ can alternatively also be obtained if the control signal FUP has a logic high level and the control signal FDN has a logic low level. All 4 transistors $T_8$ - $T_{10}$ are conducting in that situation. A higher switching frequency can then be reached compared to the former situation. (By mismatch the pump output current $I_p$ may slightly differ from zero, however.)

If the control signal FUP has a logic high level and the control signal FDN has a logic high level, both transistors $T_{10}$ and $T_{11}$ are again non-conducting. Transistor $T_8$ is conducting, thereby in fact connecting the source of transistor $T_9$ to the first power supply terminal $V_{SS}$. In this situation transistors $T_{12}$ and $T_9$ also form a current mirror which in this example has a mirror ratio of approximately one. Therefore, a reference current $I_{ref}$ is supplied through the transistor $T_9$. As a consequence, the value of the pump output current $I_p$ is approximately equal to the value $+I_{ref}$.

If the control signal FUP has a logic low level and the control signal FDN has a logic low level, both transistors $T_8$ and $T_9$ are non-conducting. Transistor $T_{10}$ is conducting, thereby in fact connecting the source of transistor $T_{11}$ to the second power supply terminal $V_{DD}$. In this situation transistors $T_7$ and $T_{11}$ also form a current mirror which in this example has a mirror ratio of approximately one. Therefore, a reference current $I_{ref}$ is supplied through the transistor $T_{11}$. As a consequence, the value of the pump output current $I_p$ is approximately equal to the value $-I_{ref}$.

Figure 7 shows a more detailed circuit diagram of the inventive stabilizing circuit STB according to Figure 5 in which a use for the further charge pump $CHPPMP_F$ is shown. The further charge pump $CHPPMP_F$ is basically used in the same way as the charge pump CHPPMP as shown in Figure 6. Transistors $T_{6F}$ - $T_{11F}$ in Figure 7 correspond to transistors $T_6$ - $T_{11}$ in Figure 6. The reference current $I_{ref}$ and the transistor $T_{12}$ are not indicated in Figure 7. This is because the gate of transistor $T_{6F}$, which forms the reference input $Iz_{RF}$ of the further charge pump $CHPPMP_F$, is connected to the gate of the transistor $cm_1$. Therefore, the transistor $cm_1$ performs in figure 7 also the function of transistor $T_{12}$, whereby the reference current $I_{mr}$ replaces the reference current $I_{ref}$. An important difference between the CHPPMP and the further charge pump $CHPPMP_F$ is that the reference current $I_{mr}$ is approximately linearly dependent on the control voltage $V_{CNTRL}$. Another difference is that the gates of transistors $T_{8F}$ and $T_{10F}$ are coupled to receive the control signals FDN and FUP, respectively. This is because the compensation current $I_z$ and the control current $I_{cntrl}$

must be in phase, while the control transistor $T_0$ has an inverting property from its gate to its drain. (See also Figure 4).

The field effect transistors in the charge pump CHPPMP and the further charge pump $CHPPMP_F$ may be fully or partly replaced by bi-polar transistors. However, transistors which form a current mirror cannot be different types of transistors. So if, for example, a bi-polar transistor is used as the transistor $cm_1$, also transistor $cm_2$ and transistor $T_{6F}$ must be bi-polar transistors.

Current mirror ratios in the charge pump CHPPMP and the further charge pump $CHPPMP_F$ need not necessarily be equal to one.

The inventive PLL (or frequency locked-loop) can be used in an integrated circuit or can be built up by discrete components.

CLAIMS:

1. An electronic circuit comprising a frequency or phase-locked loop comprising a first input terminal coupled to receive a first input signal; a second input terminal coupled to receive a second input signal; detection means for comparing the frequency or phase of the first input signal with the frequency or phase of the second input signal, respectively, and for supplying directly or via a charge pump a control voltage as a result of the comparison of the first and second input signals; a control transistor having a first main terminal and a control terminal which are coupled to receive the control voltage and having a second main terminal for supplying a control current responsive to the control voltage; a capacitor coupled in between the first main terminal and the control terminal; a current controlled oscillator having an input terminal coupled to receive the control current and having an output terminal for supplying directly or via frequency dividers the second input signal having a frequency or phase which is synchronized with the frequency or phase, respectively, of the first input signal; and a stabilizing circuit for stabilizing the frequency or phase-locked loop by adding a zero to the loop transfer function of the frequency or phase-locked loop, the stabilizing circuit comprising a further charge pump for delivering a compensation current to the input terminal of the current controlled oscillator, while the compensation current may have an approximately zero value, a negative value, or a possitive value depending on control signals delivered by the detection means, and the absolute value of said positive or negative value roughly linearly depends on the control voltage.

2. An electronic circuit as claimed in claim 1, wherein a field effect transistor is used as the control transistor, the former having a source, a drain, and a gate which respectively form the first main terminal, the second main terminal, and the control terminal of the control transistor, and the stabilizing circuit further comprises a first field effect transistor; a second field effect transistor; a third field effect transistor; a fourth field effect transistor; a current mirror having an input coupled to the drain of the first transistor and an output coupled to the drain of the fourth transistor; and means for supplying a DC-voltage between the drain and the gate of the fourth transistor, the sources of the third and fourth transistors being coupled to the source of the control transistor, the gate of the third transistor

being coupled to the gate of the fourth transistor, the source of the first transistor being coupled to the drain of the third transistor, the source of the second transistor being coupled to the drain of the fourth transistor, the gates of the first and second transistors being coupled to the gate of the control transistor, and a reference input of the further charge pump being coupled to the current mirror in a manner that said absolute value is approximately linearly dependent on the current through the input of the current mirror.

3. An electronic circuit as claimed in claim 2, wherein the current mirror comprises a first current mirror transistor having a first main terminal, a second main terminal, and a control terminal, the second main terminal and the control terminal being coupled to each other and thereby forming the input of the current mirror; and a second current mirror transistor having a first main terminal coupled to the first main terminal of the first current mirror transistor, a second main terminal forming the output of the current mirror, and a control terminal being coupled to the control terminal of the first current mirror transistor, and the reference input of the further charge pump being coupled to the input of the current mirror.

4. An electronic circuit as claimed in claim 2, wherein the stabilizing circuit is dimensioned in a manner that the first and second transistors are in their saturation region, the third and fourth transistors are in their linear region, and in a manner that the drain-source voltage of the third transistor is approximately two times as high as the drain-source voltage of the fourth transistor.

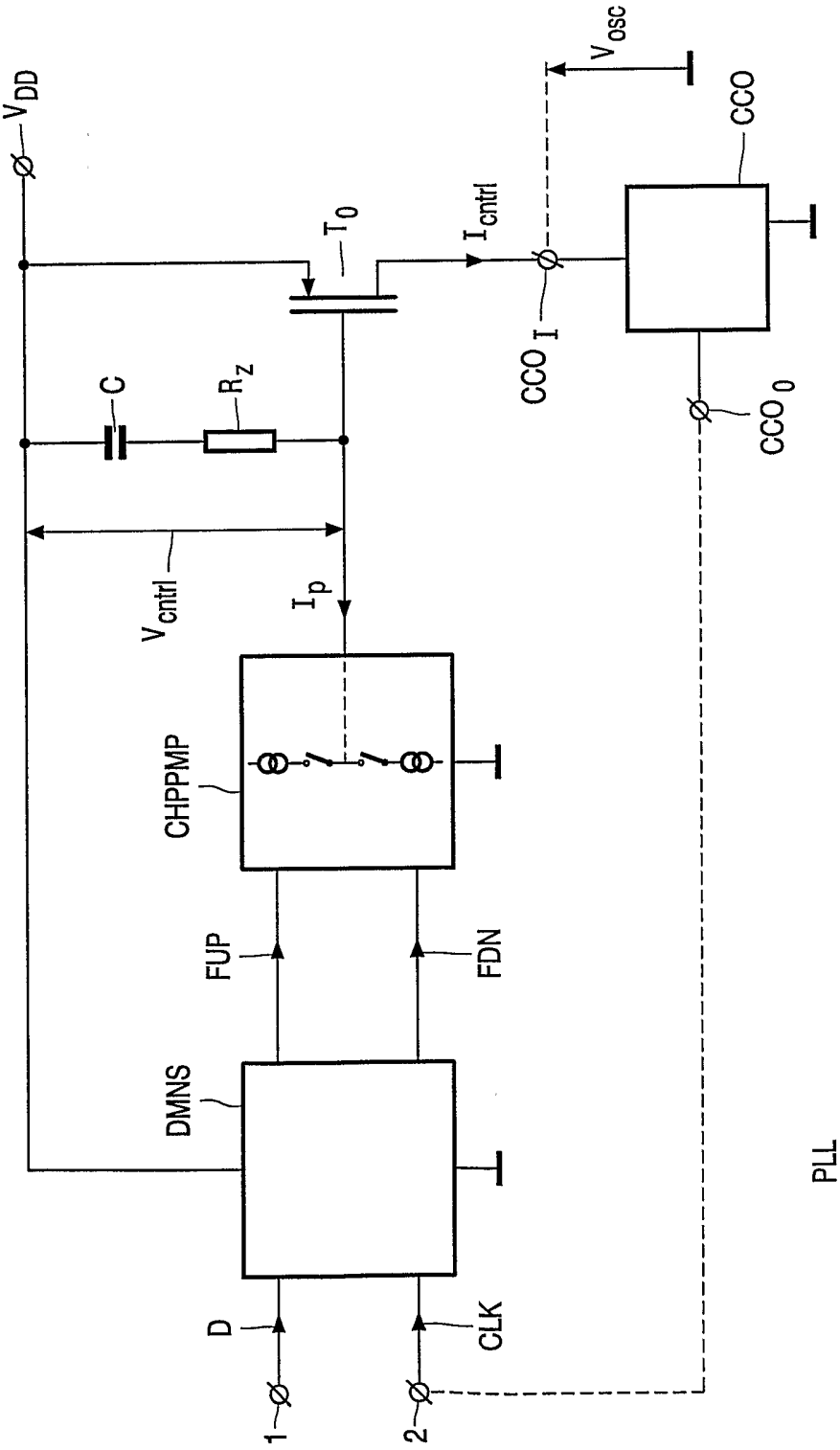

V_DD
T_0
I_cntrl
V_osc
CCO
CCO_I
CCO_0
C
R_Z
V_cntrl
I_p
CHPPMP
FUP
FDN
DMNS
D
CLK
1
2
PLL

FIG. 1

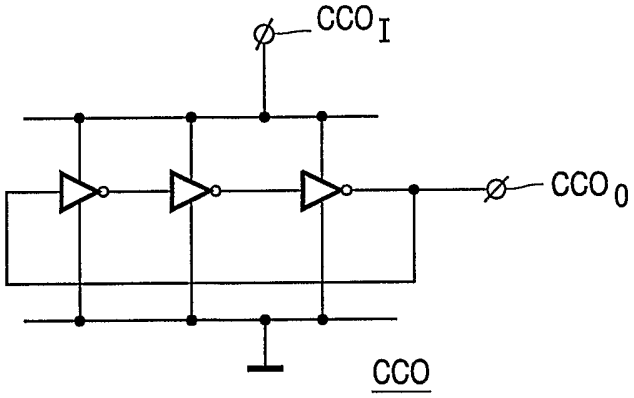



FIG. 2A

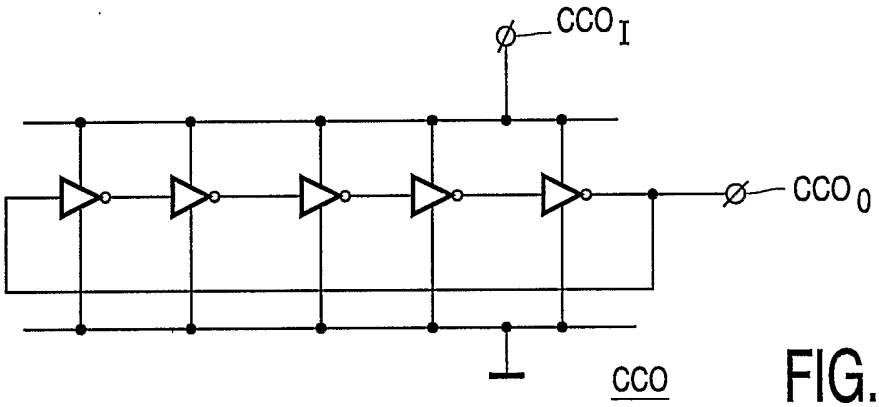



FIG. 2B

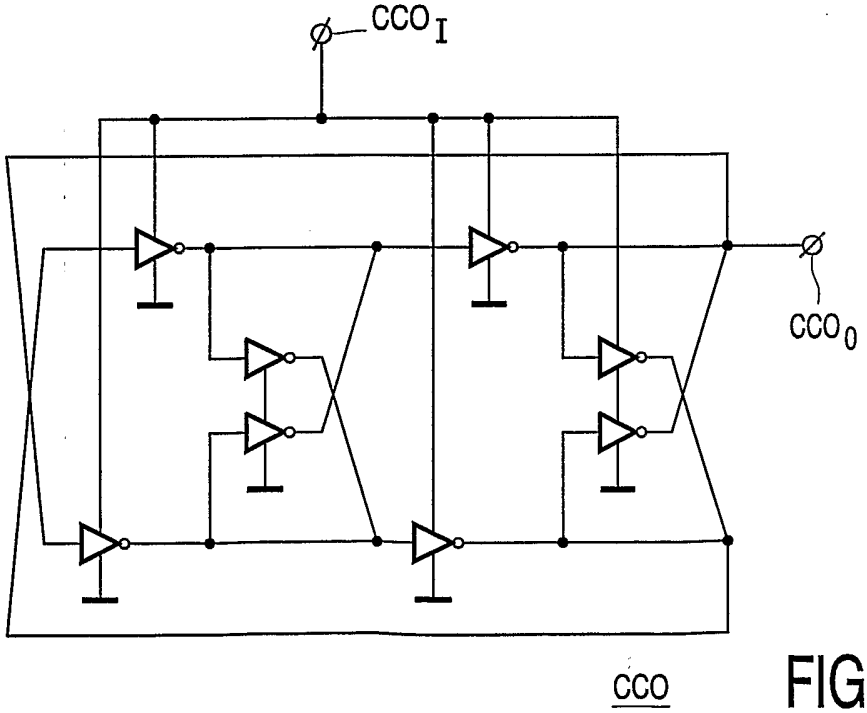



FIG. 2C

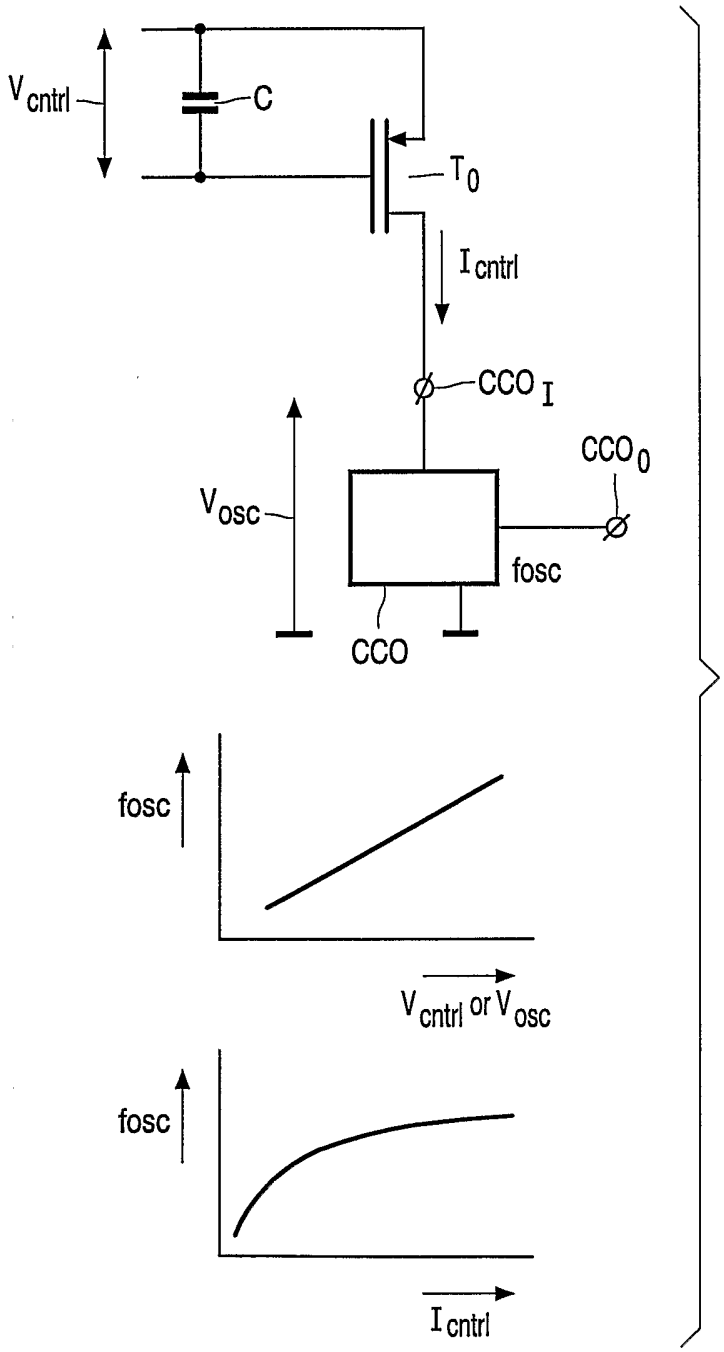

V cntrl
C
T0
I cntrl
CCO I
CCO 0
V osc
fosc
CCO
fosc
V cntrl or V osc
fosc
I cntrl

FIG. 3

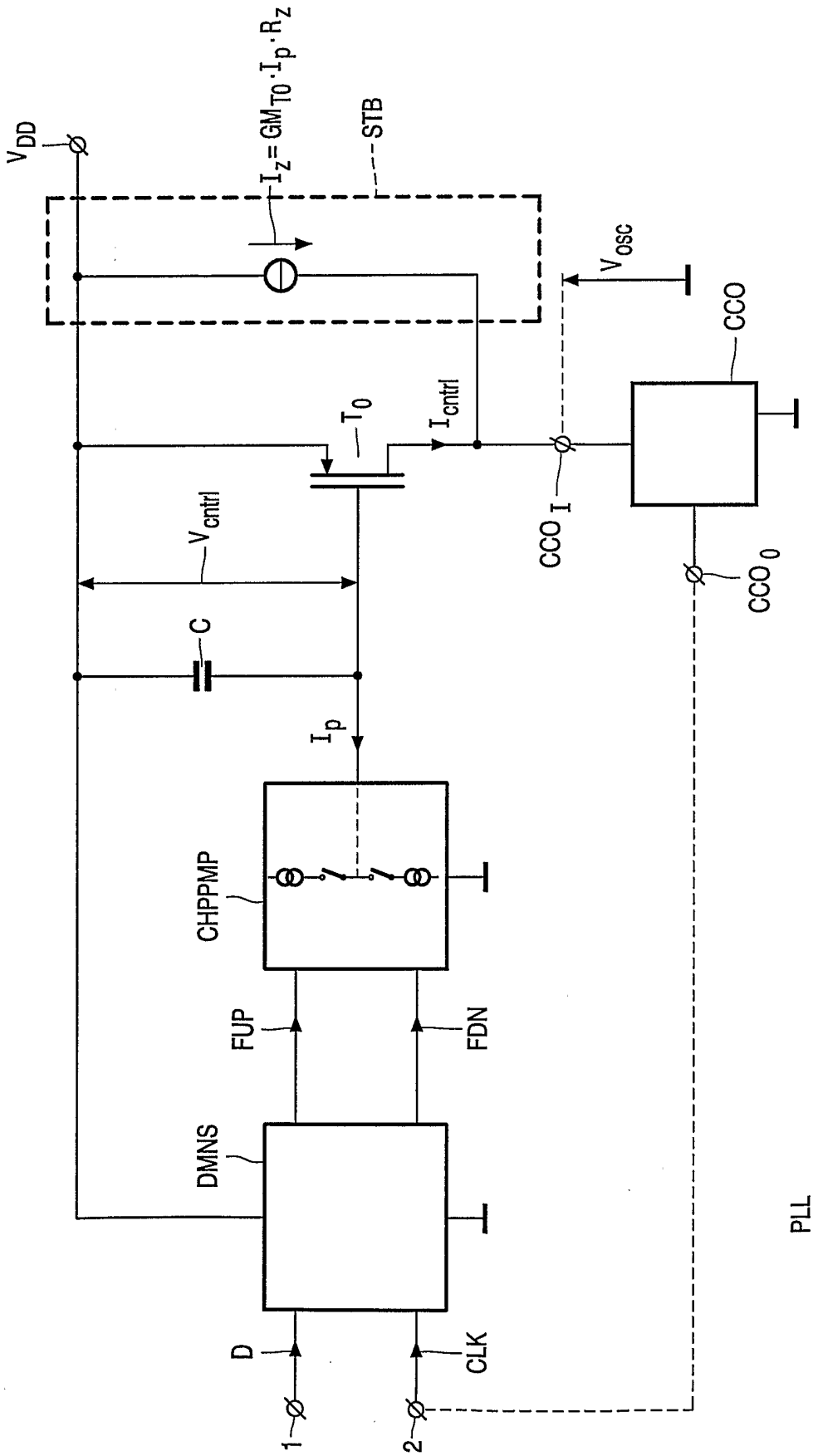
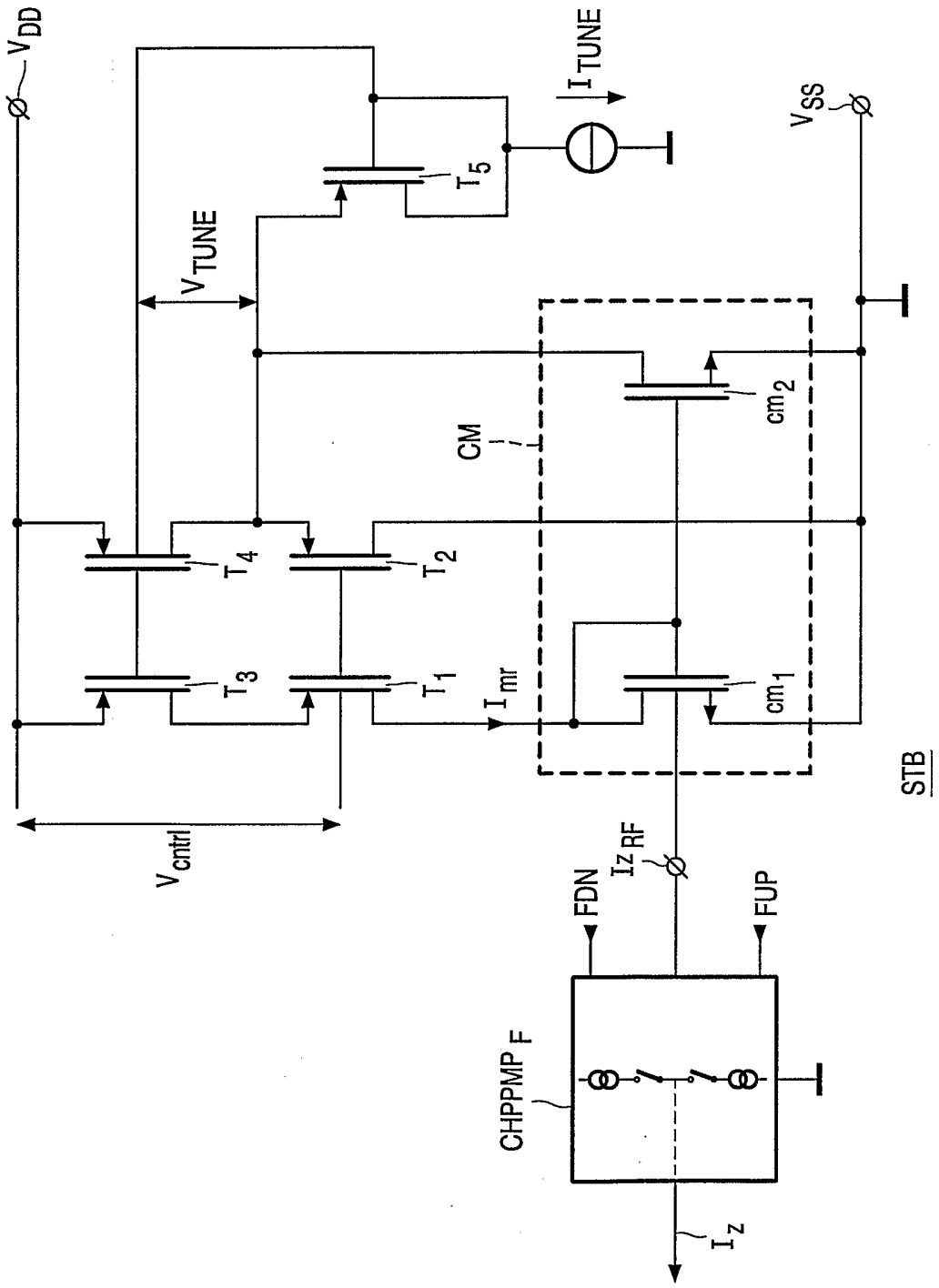

$V_{DD}$
$I_Z = GM_{T0} \cdot I_p \cdot R_Z$
STB
$V_{osc}$
CCO
$T_0$
$I_{cntrl}$
$V_{cntrl}$
$CCO_I$
$CCO_0$
C
$I_p$
CHPPMP
FUP
FDN
DMNS
D
CLK
1
2
PLL

FIG. 4

FIG. 5


$V_{DD}$
$I_{TUNE}$
$V_{SS}$
$T_5$
$V_{TUNE}$
CM
$cm_2$
$T_4$
$T_2$
$T_3$
$T_1$
$I_{mr}$
$cm_1$
STB
$V_{cntrl}$
$I_{Z\,RF}$
FDN
FUP
CHPPMP F
$I_Z$

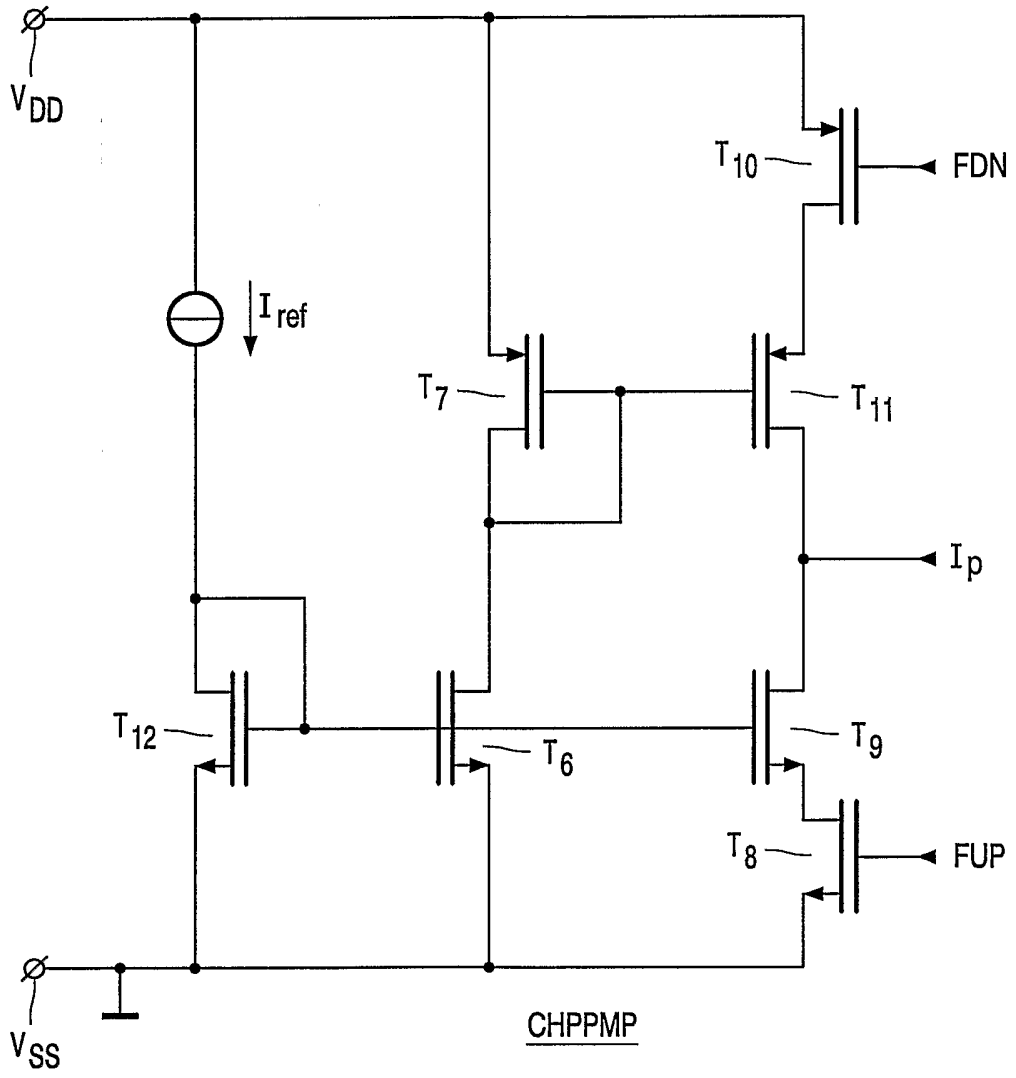



FIG. 6

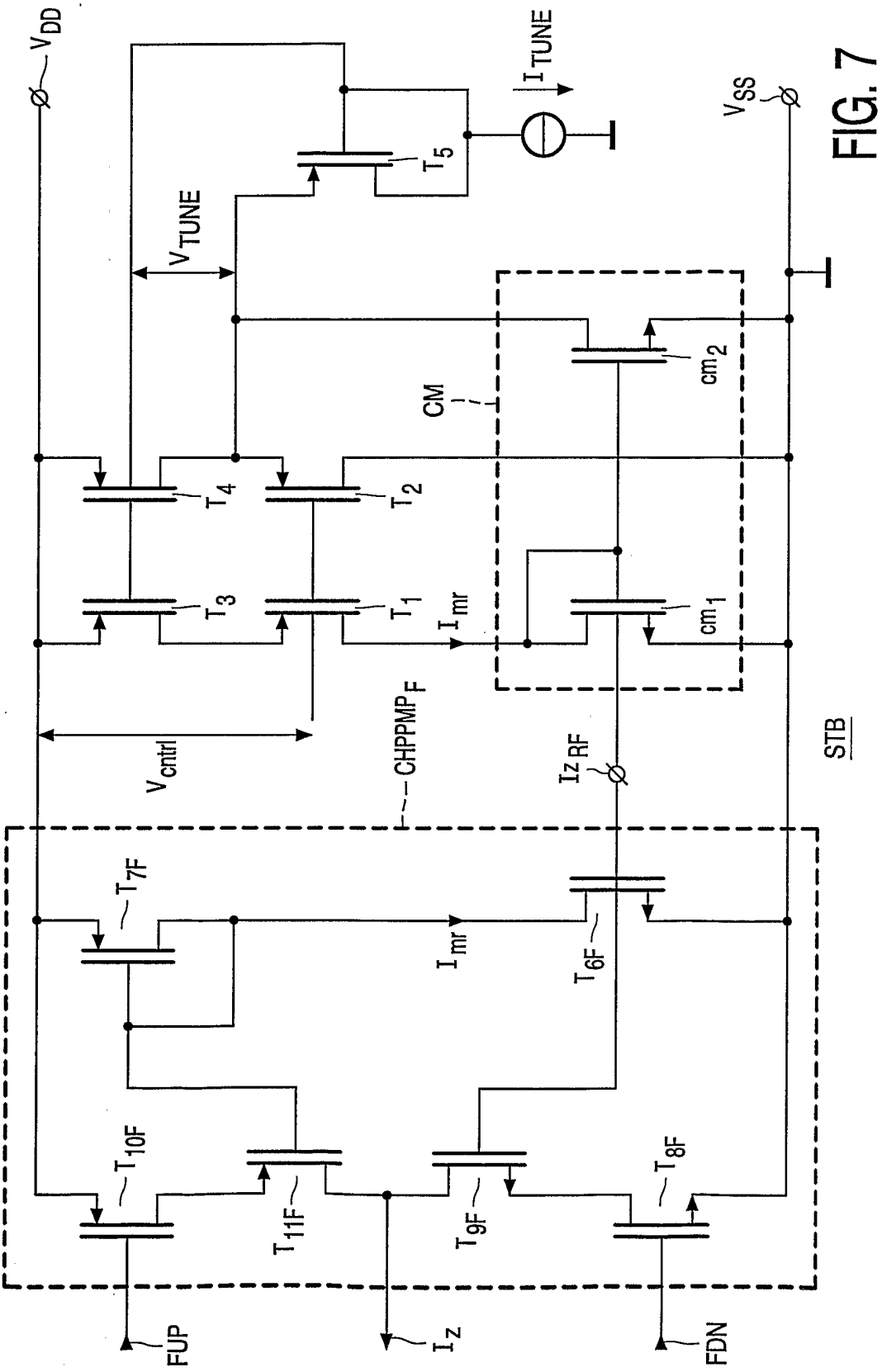

VDD
ITUNE
VSS
T5
VTUNE
CM
cm2
T4
T2
T3
T1
Imr
cm1
Vcntrl
CHPPMPF
IzRF
STB
T7F
Imr
T6F
T10F
T11F
T9F
T8F
FUP
Iz
FDN

FIG. 7