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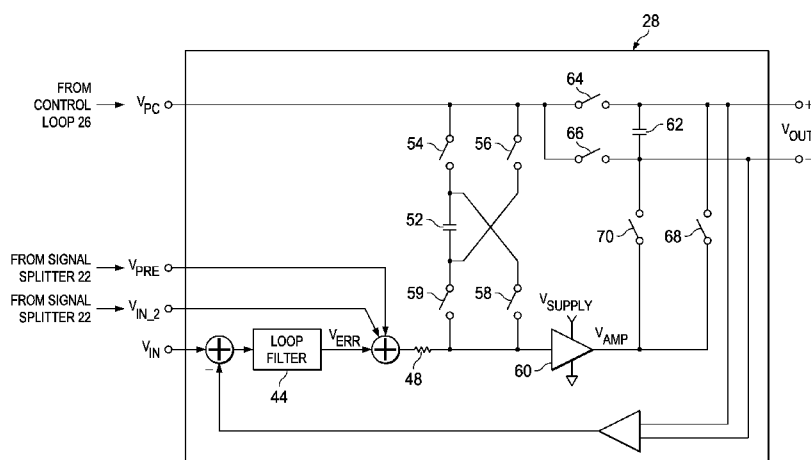
(54) **Title:** PREVENTION OF SWITCHING DISCONTINUITY IN A HYBRID SWITCHED MODE AMPLIFIER

FIG. 5

(57) **Abstract:** A method may include controlling switches of a switching full-bridge of a signal processing system to commutate polarity of a capacitor with respect to the first processing path output and a second processing path output of the signal processing system in response to a condition for commutating connectivity of the switching full-bridge and inserting a feedforward compensation that bypasses a loop filter of the second processing path in order to prevent discontinuities caused by commutating polarity of the capacitor from being compensated by the loop filter.

PREVENTION OF SWITCHING DISCONTINUITY IN A HYBRID SWITCHED MODE AMPLIFIER

FIELD OF DISCLOSURE

5 The present disclosure relates in general to circuits for audio devices, including without limitation personal audio devices such as wireless telephones and media players, and more specifically, to a switched mode amplifier including a switched mode converter for driving an audio transducer of an audio device.

BACKGROUND

10 Personal audio devices, including wireless telephones, such as mobile/cellular telephones, cordless telephones, mp3 players, and other consumer audio devices, are in widespread use. Such personal audio devices may include circuitry for driving a pair of headphones or one or more speakers. Such circuitry often includes a speaker driver
15 including a power amplifier for driving an audio output signal to headphones or speakers.

SUMMARY

 In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to driving an audio
20 output signal to an audio transducer may be reduced or eliminated.

 In accordance with embodiments of the present disclosure, a signal processing system for producing a load voltage at a load output of the signal processing system, wherein the load output comprises a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a
25 difference between the first load voltage and the second load voltage, may be provided. The signal processing system may include a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output, a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing
30 path output, wherein the second processing path comprises a feedback control loop having a loop filter, wherein the feedback control loop is configured to generate the

second load voltage based on the input signal and the load voltage, a capacitor having a first capacitor terminal and a second capacitor terminal, a switching full-bridge, and a controller. The switching full-bridge may include a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first
5 capacitor terminal and a second switch coupled between the first processing path output and the second capacitor terminal, and a second plurality of switches, comprising at least a third switch coupled between the second processing path output and the first capacitor terminal and a fourth switch coupled between the second processing path output and the second capacitor terminal. The controller may be configured to control switches of the
10 switching full-bridge to commutate polarity of the capacitor with respect to the first processing path output and the second processing path output in response to a condition for commutating connectivity of the switching full-bridge and insert a feedforward compensation that bypasses the loop filter in order to prevent discontinuities caused by commutating polarity of the capacitor from being compensated by the loop filter.

15 In accordance with these and other embodiments of the present disclosure, a method for producing a load voltage at a load output of a signal processing system, wherein the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, may be provided.
20 The signal processing system may include a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output, a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output, wherein the second processing path comprises a feedback control loop
25 having a loop filter, wherein the feedback control loop is configured to generate the second load voltage based on the input signal and the load voltage, a capacitor having a first capacitor terminal and a second capacitor terminal, and a switching full-bridge. The switching full-bridge may include a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first capacitor terminal
30 and a second switch coupled between the first processing path output and the second capacitor terminal, and a second plurality of switches, comprising at least a third switch

coupled between the second processing path output and the first capacitor terminal and a fourth switch coupled between the second processing path output and the second capacitor terminal. The method may include controlling switches of the switching full-bridge to commute polarity of the capacitor with respect to the first processing path output and the second processing path output in response to a condition for commutating connectivity of the switching full-bridge and inserting a feedforward compensation that bypasses the loop filter in order to prevent discontinuities caused by commutating polarity of the capacitor from being compensated by the loop filter.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features,
5 and wherein:

FIGURE 1 illustrates an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components of an example audio integrated circuit of a personal audio device, in accordance with embodiments of
10 the present disclosure;

FIGURE 3 illustrates a block and circuit diagram of selected components of an example switched mode amplifier, in accordance with embodiments of the present disclosure;

FIGURE 4 illustrates a circuit diagram of selected components of an example
15 control loop that may be used to implement the first control loop depicted in FIGURE 3, in accordance with embodiments of the present disclosure;

FIGURE 5 illustrates a circuit diagram of selected components of an example control loop that may be used to implement the second control loop depicted in FIGURE 3, in accordance with embodiments of the present disclosure;

FIGURE 6 illustrates a graph depicting the relationship of a voltage driven by the
20 first control loop depicted in FIGURE 3 and a voltage driven by a linear amplifier of the output stage depicted in FIGURE 3 as a function of a desired output voltage, in accordance with embodiments of the present disclosure; and

FIGURE 7 illustrates a graph depicting the relationship of a voltage driven by the
25 first control loop depicted in FIGURE 3 and a voltage driven by a linear amplifier of the output stage depicted in FIGURE 3 as a function of time, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 illustrates an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may provide for connection of headset 3 to an electrical terminal of personal audio device 1. Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. As also shown in FIGURE 1, personal audio device 1 may include an audio integrated circuit (IC) 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 illustrates a block diagram of selected components of an example audio IC 9 of a personal audio device, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, a microcontroller core 18 may supply a digital audio input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital audio input signal to an analog signal V_{IN} . DAC 14 may supply analog signal V_{IN} to an amplifier 16 which may amplify or attenuate audio input signal V_{IN} to provide a differential audio output signal V_{OUT} , which may operate a speaker, a headphone transducer, a line level signal output, and/or other suitable output. In some embodiments, DAC 14 may be an integral component of amplifier 16. A power supply 10 may provide the power supply rail inputs of amplifier 16. In some embodiments, power supply 10 may comprise a battery. Although FIGURES 1 and 2 contemplate that audio IC 9 resides in a personal audio device, systems and methods described herein may also be applied to electrical and electronic systems and devices other than a personal audio device, including audio systems for use in a computing device larger than a personal audio device, an automobile, a building, or other structure.

FIGURE 3 illustrates a block and circuit diagram of selected components of an example switched mode amplifier 20, in accordance with embodiments of the present

disclosure. In some embodiments, switched mode amplifier 20 may implement all or a portion of amplifier 16 described with respect to FIGURE 2. As shown in FIGURE 3, switched mode amplifier 20 may comprise a signal splitter 22, a first control loop 26, and a second control loop 28.

5 Signal splitter 22 may comprise any system, device, or apparatus configured to receive audio input signal V_{IN} (or a derivative thereof) and generate a first signal V_{IN_1} derived from audio input signal V_{IN} and generate a second signal V_{IN_2} derived from audio input signal V_{IN} , wherein second signal V_{IN_2} comprises information of the input signal absent from first signal V_{IN_1} (e.g., $V_{IN\_2} = V_{IN} - V_{IN\_1}$). For example, in some
10 embodiments, first signal V_{IN_1} and second signal V_{IN_2} may be governed by the following set of equations:

$$\begin{aligned} V_{IN\_1} &= V_{IN}; \text{ for } |V_{IN}| > V_{SAT\_IN} \\ V_{IN\_1} &= V_{SAT\_IN}; \text{ for } |V_{IN}| \leq V_{SAT\_IN} \\ V_{IN\_2} &= 0; \text{ for } |V_{IN}| > V_{SAT\_IN} \\ V_{IN\_2} &= V_{SAT\_IN} - V_{IN}; \text{ for } |V_{IN}| \leq V_{SAT\_IN} \end{aligned}$$

15 where V_{SAT_IN} represents a lower saturation voltage of audio input signal V_{IN} which may be related to a lower saturation voltage of a power converter implemented by first control loop 26, as described in greater detail below.

In addition to the foregoing, signal splitter 22 may also generate a precompensation voltage signal V_{PRE} , which may be communicated to control loop 28.
20 The value of precompensation voltage signal V_{PRE} is discussed in greater detail below with respect to FIGURE 5.

First control loop 26 may receive first signal V_{IN_1} at its input and may generate at its output a voltage V_{PC} as a function of first signal V_{IN_1} . Turning briefly to FIGURE 4, FIGURE 4 illustrates a circuit diagram of selected components of an example control
25 loop 26 that may be used to implement first control loop 26 depicted in FIGURE 3, in accordance with embodiments of the present disclosure. As shown in FIGURE 4, first control loop 26 may comprise a loop filter 32 and a power converter 40.

Loop filter 32 may comprise any system, device, or apparatus configured to receive an input signal (e.g., first signal V_{IN_1} or a derivative thereof) and a feedback

signal (e.g., voltage V_{PC} , a derivative thereof, or other signal indicative of signal V_{PC}) and based on such input signal and feedback signal, generate a controller input signal to be communicated to converter controller 34. In some embodiments, such controller input signal may comprise a signal indicative of an integrated error between the input signal and the feedback signal. In other embodiments, such controller input signal may comprise a signal indicative of a target voltage signal to be driven as voltage V_{PC} or a target current signal to be driven by power converter 40.

Converter controller 34 may comprise any system, device, or apparatus configured to, based on an input signal (e.g., output signal of loop filter 32), voltage V_{PC} , and/or other characteristics of first control loop 26, control switching of switches integral to power converter 40, in order to cause first control loop 26 to generate voltage V_{PC} as a function of first signal V_{IN_1} .

As shown in FIGURE 4, power converter 40 may include a power inductor 42, and switches 44, 46, 47, and 49 arranged as shown. In some embodiments, a voltage V_{SUPPLY} (e.g., provided by power supply 10 depicted in FIGURE 2) may be received via input terminals including a positive input terminal and a negative input terminal which may be coupled to a ground voltage. Accordingly, in operation, converter controller 34 may be configured to control switches 44, 46, 47, and 49 in order to convert voltage V_{SUPPLY} to voltage V_{PC} , such that voltage V_{PC} is a function of first signal V_{IN_1} to loop filter 32.

Turning again to FIGURE 3, second control loop 28 may receive at its inputs voltage V_{PC} generated by first control loop 26, second signal V_{IN_2} , and audio input signal V_{IN} , and based thereon may generate at its output audio output signal V_{OUT} . As described in greater detail in this disclosure (including, without limitation, in reference to FIGURE 5, below), second control loop 28 may comprise at least one linear amplifier and, in some embodiments, a plurality of switches, wherein the at least one linear amplifier and the plurality of switches, if present, are controlled by a loop filter in order generate audio output signal V_{OUT} based on voltage V_{PC} , second signal V_{IN_2} , and audio input signal V_{IN} , such that audio output signal V_{OUT} is a function of audio input signal V_{IN} .

FIGURE 5 illustrates a circuit diagram of selected components of an example control loop 28 that may be used to implement second control loop 28 depicted in

FIGURE 3, in accordance with embodiments of the present disclosure. As shown in FIGURE 5, second control loop 28 may comprise a loop filter 44, a linear amplifier 60, an output capacitor 62, a first full-switching bridge comprising switches 64, 66, 68, and 70, a switched capacitor 52, and a second full-switching bridge comprising switches 54, 56, 58, and 59.

Loop filter 44 may comprise any system, device, or apparatus configured to receive an input signal (e.g., audio input signal V_{IN} or a derivative thereof) and a feedback signal (e.g., audio output signal V_{OUT} , a derivative thereof, or other signal indicative of audio output signal V_{OUT}) and based on such input signal and feedback signal, generate a filtered error signal V_{ERR} to be combined with second signal V_{IN_2} and communicated to linear amplifier 60. In some embodiments, such filtered error signal V_{ERR} may comprise a signal indicative of an integrated error between the input signal and the feedback signal. In other embodiments, such filtered error signal V_{ERR} may comprise a signal that when combined with second signal V_{IN_2} is indicative of a target voltage signal to be driven as linear output voltage V_{AMP} . In these and other embodiments, loop filter 44 may include control circuitry and may drive control circuitry for controlling switches 54, 56, 58, 59, 64, 66, 68, and 70, in order to cause second control loop 28 to generate audio output signal V_{OUT} as a function of voltage V_{PC} and second signal V_{IN_2} (and thus a function of audio input signal V_{IN}).

As shown in FIGURE 5, first control loop 26 may drive voltage V_{PC} which is received by second control loop 28. Accordingly, first control loop 26 may be considered a first processing path configured to process a first signal (e.g., first signal V_{IN_1}) derived from an input signal (e.g., audio input signal V_{IN}) to generate a first path voltage (V_{PC}) at a first processing path output (e.g., output of first control loop 26).

Switch 64 may be coupled between the output of first control loop 26 and a first load terminal of second control loop 28, and switch 66 may be coupled between the output of first control loop 26 and a second load terminal of second control loop 28. Linear amplifier 60 may be configured to drive a linear amplifier output voltage V_{AMP} which is a function of the filtered error signal V_{ERR} generated by loop filter 44. Switch 68 may be coupled between the output of linear amplifier 60 and the first load terminal of second control loop 28, and switch 70 may be coupled between the output of linear

amplifier 60 and the second load terminal of second control loop 28. Output capacitor 62 may be coupled between a first load terminal (e.g., positive terminal of audio output signal V_{OUT}) and a second load terminal (e.g., negative terminal of audio output signal V_{OUT}). Accordingly, linear amplifier 60 may be considered a second processing path
5 configured to process a second signal (e.g. second signal V_{IN_2}) derived from an input signal (e.g., audio input signal V_{IN}) to generate a second path voltage (V_{AMP}) at a second processing path output (e.g., output of linear amplifier 60). In addition, the first full-switching bridge may accordingly include a first plurality of switches (e.g., 64 and 66) comprising at least a first switch (e.g., 64) coupled between the first processing path
10 output and a first load terminal, and a second switch (e.g., 66) coupled between the first processing path output and a second load terminal and a second plurality of switches (e.g., 68 and 70) comprising at least a third switch (e.g., 68) coupled between the second processing path output and the first load terminal and a fourth switch (e.g., 70) coupled between the second processing path output and the second load terminal.

15 In operation of second control loop 28, loop filter 44 or another controller may activate switches 64 and 70 and deactivate switches 66 and 68 for positive values of audio output signal V_{OUT} and activate switches 66 and 68 and deactivate switches 64 and 70 for negative values of audio output signal V_{OUT} . Loop filter 44 or such other controller may, as power converter output voltage V_{PC} approaches its lower saturation limit, cause linear
20 amplifier 60 to drive a non-zero linear amplifier output voltage V_{AMP} in order to increase a common mode voltage between the first output terminal and the second output terminal, allowing audio output signal V_{OUT} to approach and cross zero. Above the lower saturation limit of power converter output voltage V_{PC} , converter controller 34 may cause linear amplifier 60 to drive an approximately zero linear amplifier output voltage V_{AMP}
25 such that a magnitude of audio output signal V_{OUT} is equal to power converter output voltage V_{PC} .

In other words, first control loop 26 and linear amplifier 60 may be controlled to generate voltages in accordance with the following functions, which are graphically depicted in FIGURE 6, and wherein voltage V_{TGT} represents a target or desired voltage to
30 be output as audio output signal V_{OUT} :

$$\begin{aligned}
 V_{PC} &= V_{TGT}; \text{ for } |V_{TGT}| > V_{SAT} \\
 V_{PC} &= V_{SAT}; \text{ for } |V_{TGT}| \leq V_{SAT} \\
 V_{AMP} &= 0; \text{ for } |V_{TGT}| > V_{SAT} \\
 V_{AMP} &= V_{SAT} - V_{TGT}; \text{ for } |V_{TGT}| \leq V_{SAT}
 \end{aligned}$$

In some embodiments, an offset voltage may be added to each of the output of first control loop 26 and the output of linear amplifier 60, to ensure that the voltage V_{AMP}
 5 > 0 at all times.

Accordingly, presence of linear amplifier 60 and its ability to increase the common mode voltage of the output terminals in response to low magnitudes of the output signal V_{OUT} may minimize non-linearities of audio output signal V_{OUT} as a function of audio input signal V_{IN} , and permit crossing a magnitude of zero by audio
 10 output signal V_{OUT} .

With respect to the second full-switching bridge, switch 54 may be coupled between the output of first control loop 26 and a first terminal of switching capacitor 52, and switch 56 may be coupled between the output of first control loop 26 and a second load of switching capacitor 52. Switch 58 may be coupled between the input of linear
 15 amplifier 60 and the first terminal of switching capacitor 52, and switch 59 may be coupled between the input of linear amplifier 60 and the second terminal of switching capacitor 52. Accordingly, the second full-switching bridge may include a third plurality of switches (e.g., 54 and 56) comprising at least a fifth switch (e.g., 54) coupled between the first processing path output (e.g., output of first control loop 26) and a first capacitor
 20 terminal and a sixth switch (e.g., 56) coupled between the first processing path output and the second capacitor terminal and a fourth plurality of switches (e.g., 58 and 59) comprising at least a seventh switch (e.g., 58) coupled between a second processing path input (e.g., input of linear amplifier 60) and the first capacitor terminal and an eighth switch (e.g., 59) coupled between the second processing path input and the second
 25 capacitor terminal.

In operation of second control loop 28, loop filter 44 or another controller may control switches 54, 56, 58, and 59 of the second switching full-bridge such that when switches 64, 66, 68, and 70 of the first switching full-bridge are switched to reverse connectivity of the output of first control loop 26 and the output of linear amplifier 60 to

the first load terminal and the second load terminal as described above, switches 54, 56, 58, and 59 of the second switching full-bridge may be switched substantially contemporaneously with switching of switches 64, 66, 68, and 70 of the first switching full-bridge to reverse connectivity of the output of first control loop 26 and the input of linear amplifier 60 to the terminals of switching capacitor 52 in order to minimize voltage discontinuities caused by the switching of switches 64, 66, 68, and 70 of the first switching full-bridge.

To further illustrate the effect of such switching, FIGURE 7 illustrates a graph depicting the relationship of voltage V_{PC} driven by first control loop 26 and voltage driven by a linear amplifier 60 as a function of time, in accordance with embodiments of the present disclosure. FIGURE 7 depicts such signal voltages during a time when a magnitude of audio output signal V_{OUT} is less than the lower saturation value of voltage V_{PC} . Accordingly, during such time, first control loop 26 may output voltage V_{PC} having a direct-current value of lower saturation voltage V_{SAT} with a high-frequency ripple component superimposed as shown in FIGURE 7. As audio output signal V_{OUT} increases from a negative polarity to cross zero and increase to positive values, the voltage V_{OUT} at the negative terminal of the output of second control loop 28 generated by linear amplifier 60 (e.g., voltage V_{AMP} which is passed through switches 68 and 70 depending on states of such switches) may have a waveform as depicted in FIGURE 7. As seen in FIGURE 7, so that voltage V_{AMP} may maintain a positive value above zero, commutation of the first full-switching bridge of switches 64, 66, 68, and 70 may occur when audio output signal V_{OUT} is non-zero, as shown at time t_0 in FIGURE 7. When such output polarity transition occurs at non-zero audio output signal V_{OUT} , linear amplifier 60 must immediately transition from supplying a voltage that is ΔV_1 greater than output voltage V_{PC} to a voltage that is ΔV_2 lesser than output voltage V_{PC} . In order to minimize discontinuity in audio output signal V_{OUT} , ΔV_1 must be maintained approximately equal to ΔV_2 .

Referring again to FIGURE 5, a low-pass filter comprising resistance 48 and capacitor 52 may create a significant delay path in second control loop 28, such that if the transition of the first full-switching bridge of switches 64, 66, 68, and 70 is driven solely by second control loop 28, the delays imposed by the low-pass filter may now allow for fast resolution of the discontinuity. However, by commutating the second full-switching

bridge of switches 54, 56, 58, and 59 substantially contemporaneously with the first full-switching bridge of switches 64, 66, 68, and 70, such delay may be alleviated.

In addition, while switching capacitor 52 and resistance 48 may effectively form a low-pass filter as seen from the output of loop filter 44, switching capacitor 52 and
5 resistance 48 may effectively form a high-pass filter as seen from the output of control loop 26. Accordingly, high-frequency components of voltage V_{PC} , such as the high-frequency ripple depicted in FIGURE 7, may be capacitively coupled into the input of linear amplifier 60, such that the high-frequency components are coupled (e.g., in a feed-forward manner) into the input of linear amplifier 60 and passed to linear amplifier output
10 voltage V_{AMP} , such that the high-frequency components of voltage V_{PC} are effectively cancelled out by voltage V_{AMP} , and such that the high-frequency components of voltage V_{PC} are substantially absent from the load voltage. Accordingly, the feedback control loop of second control loop 28 may operate predominantly on low-frequency components of voltage V_{PC} and voltage V_{AMP} below a corner frequency of the high-pass filter.

15 In an ideal case, the polarity of audio output signal V_{OUT} could be flipped at an exact zero-crossing point. However, monitoring and determining an exact zero-crossing is difficult, and to avoid oscillation, delay and hysteresis may need to be inserted, making monitoring and determining an exact zero-crossing even more difficult. In order to cause no effect on an output load coupled to the output of second control loop 28, at least one of
20 voltage V_{PC} and voltage V_{AMP} must have a sudden voltage step in order to maintain a proper voltage balance for audio output signal V_{OUT} . Without accounting for such sudden step, discontinuities caused by commutating polarity of capacitor 52 near a zero-crossing of audio output signal V_{OUT} may be undesirably compensated by loop filter 44, which may lead to decreased total harmonic distortion. Accordingly, when a condition for
25 commutating connectivity of the switching full-bridge comprising switches 54, 56, 58, and 59 occurs (e.g., a zero-crossing of audio output signal V_{OUT}), switches of the switching full-bridge comprising switches 54, 56, 58, and 59 may be controlled to commute polarity of capacitor 52 with respect to voltage V_{PC} and the input to linear amplifier 60. However, in addition, further in response to such condition for
30 commutating connectivity of the switching full-bridge comprising switches 54, 56, 58, and 59, precompensation voltage signal V_{PRE} may be added between the output of loop

filter 44 and the low-pass filter created by resistance 48 and capacitor 52. Insertion of precompensation voltage signal V_{PRE} is thus insertion of a feedforward compensation that bypasses loop filter 44 in order to prevent discontinuities caused by commutation of the polarity of capacitor 52 from being compensated by loop filter 44. Thus, in response to a condition for commutating connectivity of the switching full-bridge comprising switches 54, 56, 58, and 59, signal splitter 22 may set precompensation voltage signal V_{PRE} for a period of time (e.g., such period of time related to the bandwidth of loop filter 44) such that the equation $V_{AMP}(t) = (V_{ERR}(t) + V_{PRE\_BW}(t))A(t)B(t)$, where V_{PRE_BW} is precompensation voltage signal V_{PRE} at a bandwidth of interest (e.g., audio band of 20 kilohertz), $A(t)$ is a transfer function of the low-pass filter created by resistance 48 and capacitor 52, and $B(t)$ is a transfer function of linear amplifier 60. In the absence of the condition for commutating connectivity of the switching full-bridge, or after a period of time after the occurrence of condition for commutating connectivity of the switching full-bridge, signal splitter 22 may set the value of voltage signal V_{PRE} to zero, as such compensation may not be needed during such periods.

As used herein, a “switch” may comprise any suitable device, system, or apparatus for making a connection in an electric circuit when the switch is enabled (e.g., activated, closed, or on) and breaking the connection when the switch is disabled (e.g., deactivated, open, or off) in response to a control signal received by the switch. For purposes of clarity and exposition, control signals for switches described herein are not depicted although such control signals would be present to selectively enable and disable such switches. In some embodiments, a switch may comprise a metal-oxide-semiconductor field-effect transistor (e.g., an n-type metal-oxide-semiconductor field-effect transistor).

As used herein, when two or more elements are referred to as “coupled” to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass

all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled
5 to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical
10 objects to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present inventions have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and
15 scope of the disclosure.

WHAT IS CLAIMED IS:

1. A signal processing system for producing a load voltage at a load output of the signal processing system, the load output comprising a first load terminal having a
5 first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage, the signal processing system comprising:
 - a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output;
 - 10 a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output, wherein the second processing path comprises a feedback control loop having a loop filter, wherein the feedback control loop is configured to generate the second load voltage based on the input signal and the load voltage;
 - 15 a capacitor having a first capacitor terminal and a second capacitor terminal;
a switching full-bridge comprising:
 - a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first capacitor terminal and a second switch coupled between the first processing path output and the second
20 capacitor terminal; and
 - a second plurality of switches, comprising at least a third switch coupled between the second processing path output and the first capacitor terminal and a fourth switch coupled between the second processing path output and the second capacitor terminal; and
 - 25 a controller configured to:
 - control switches of the switching full-bridge to commutate polarity of the capacitor with respect to the first processing path output and the second processing path output in response to a condition for commutating connectivity of the switching full-bridge; and

insert a feedforward compensation that bypasses the loop filter in order to prevent discontinuities caused by commutating polarity of the capacitor from being compensated by the loop filter.

5 2. The signal processing system of Claim 1, wherein the second processing path comprises a low-pass filter coupled to the output of the loop filter, and wherein the feedforward compensation is inserted between the output of the loop filter and the low-pass filter.

10 3. The signal processing system of Claim 2, wherein the low-pass filter comprises the capacitor.

 4. The signal processing system of Claim 1, wherein the condition for commutating connectivity of the switching full-bridge is when the load voltage is a
15 substantially non-zero voltage.

 5. The signal processing system of Claim 1, wherein the second processing path comprises a feedback control loop configured to generate the second load voltage based on the input signal and the load voltage.

20

6. A method for producing a load voltage at a load output of a signal processing system, the load output comprising a first load terminal having a first load voltage and a second load terminal having a second load voltage such that the load voltage comprises a difference between the first load voltage and the second load voltage,
5 the signal processing system comprising:

a first processing path configured to process a first signal derived from an input signal to generate a first path voltage at a first processing path output;

a second processing path configured to process a second signal derived from the input signal to generate a second path voltage at a second processing path output, wherein
10 the second processing path comprises a feedback control loop having a loop filter, wherein the feedback control loop is configured to generate the second load voltage based on the input signal and the load voltage;

a capacitor having a first capacitor terminal and a second capacitor terminal; and

a switching full-bridge comprising:

15 a first plurality of switches, comprising at least a first switch coupled between the first processing path output and the first capacitor terminal and a second switch coupled between the first processing path output and the second capacitor terminal; and

a second plurality of switches, comprising at least a third switch coupled
20 between the second processing path output and the first capacitor terminal and a fourth switch coupled between the second processing path output and the second capacitor terminal;

wherein the method comprises:

25 controlling switches of the switching full-bridge to commutate polarity of the capacitor with respect to the first processing path output and the second processing path output in response to a condition for commutating connectivity of the switching full-bridge; and

inserting a feedforward compensation that bypasses the loop filter in order to prevent discontinuities caused by commutating polarity of the capacitor from
30 being compensated by the loop filter.

7. The method of Claim 6, wherein the second processing path comprises a low-pass filter coupled to the output of the loop filter, and wherein inserting the feedforward compensation comprises inserting the feedforward compensation between the output of the loop filter and the low-pass filter.

5

8. The method of Claim 7, wherein the low-pass filter comprises the capacitor.

9. The method of Claim 6, wherein the condition for commutating connectivity of the switching full-bridge is when the load voltage is a substantially non-zero voltage.

10. The method of Claim 6, wherein the second processing path comprises a feedback control loop configured to generate the second load voltage based on the input signal and the load voltage.

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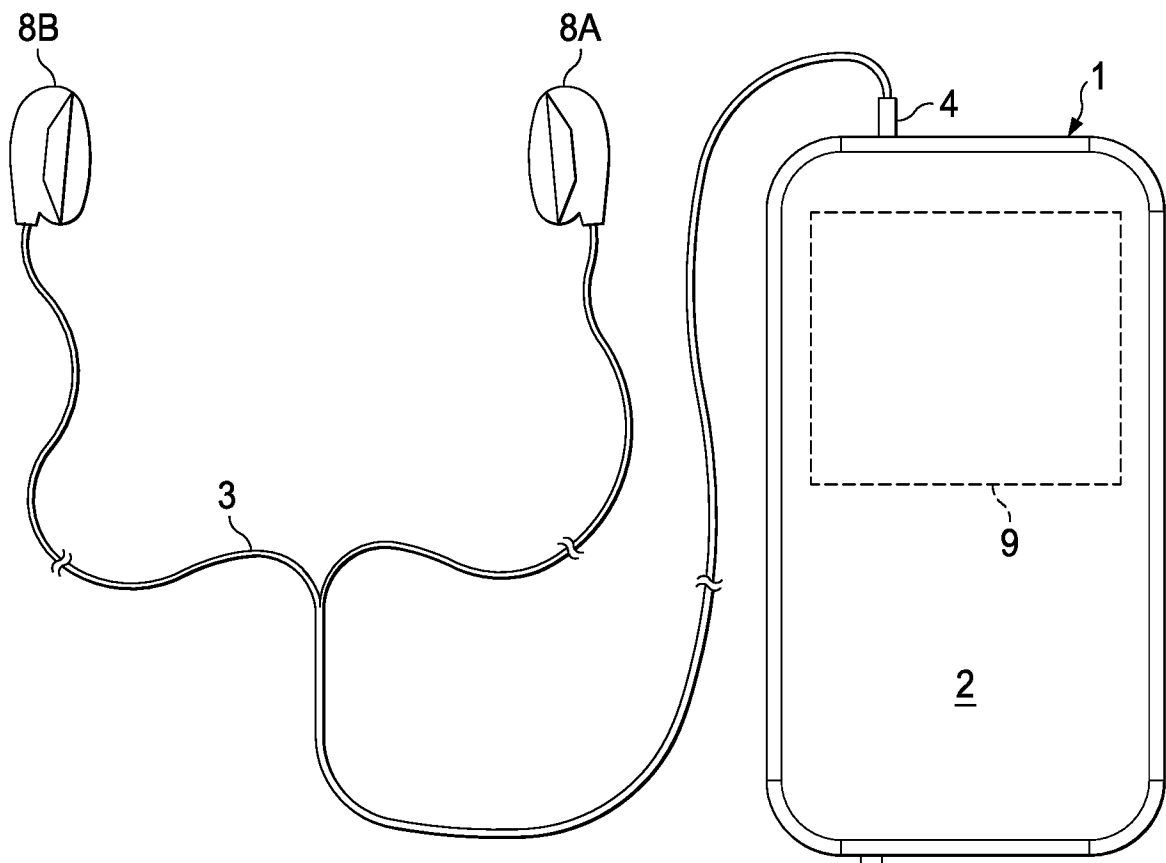


FIG. 1

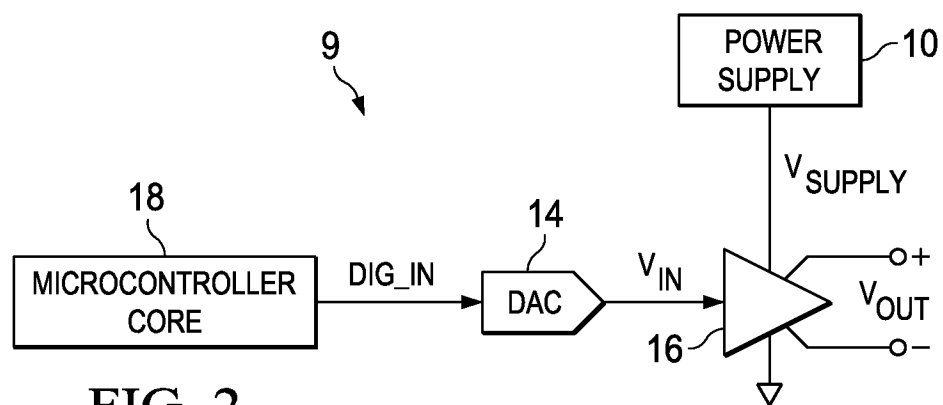


FIG. 2

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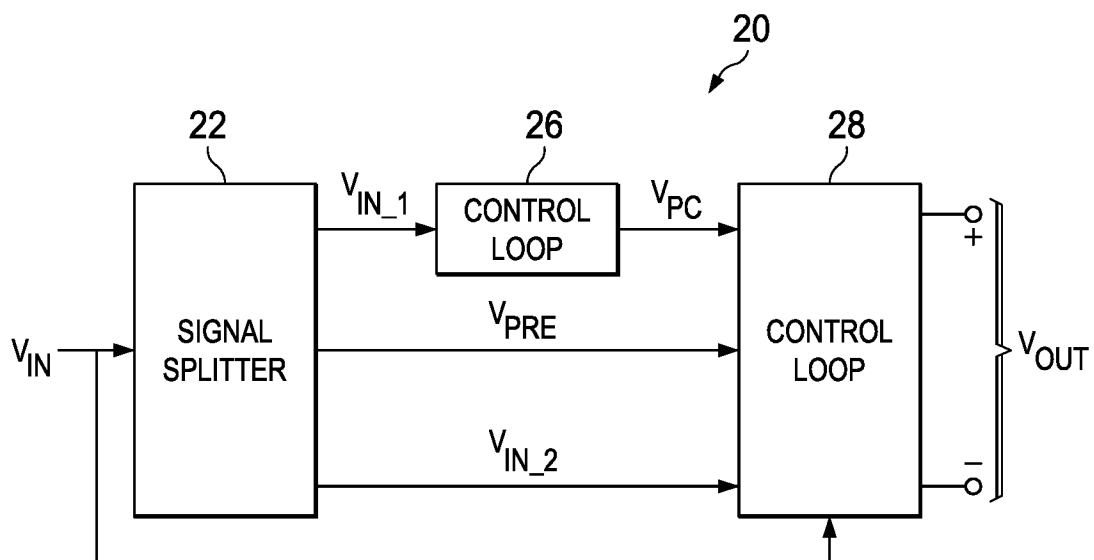


FIG. 3

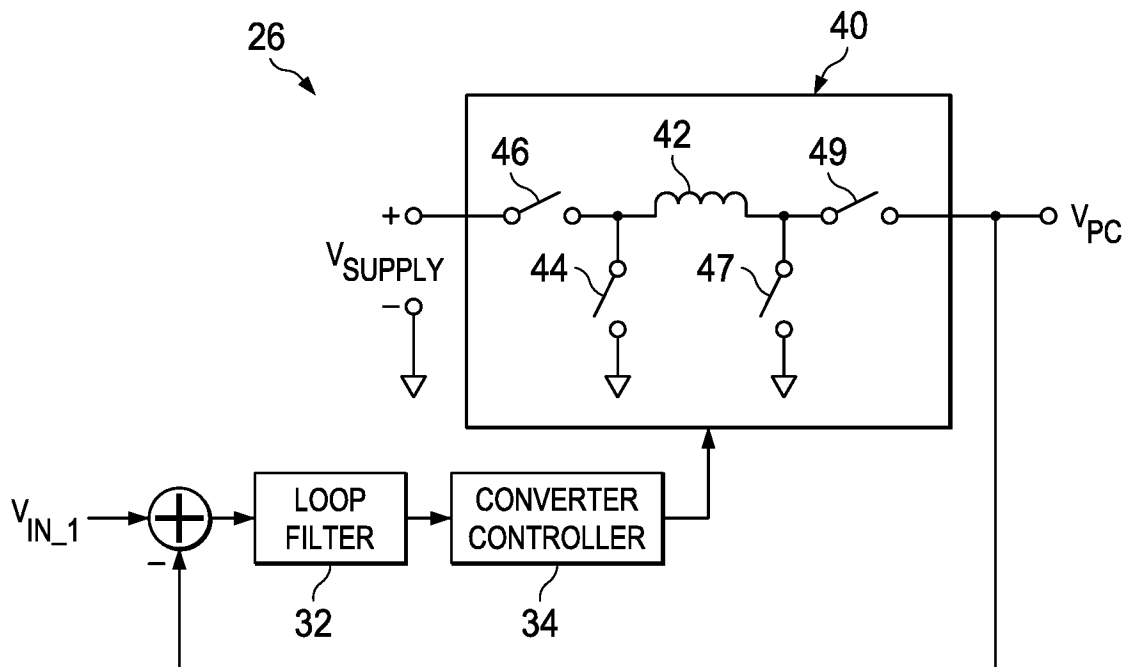


FIG. 4

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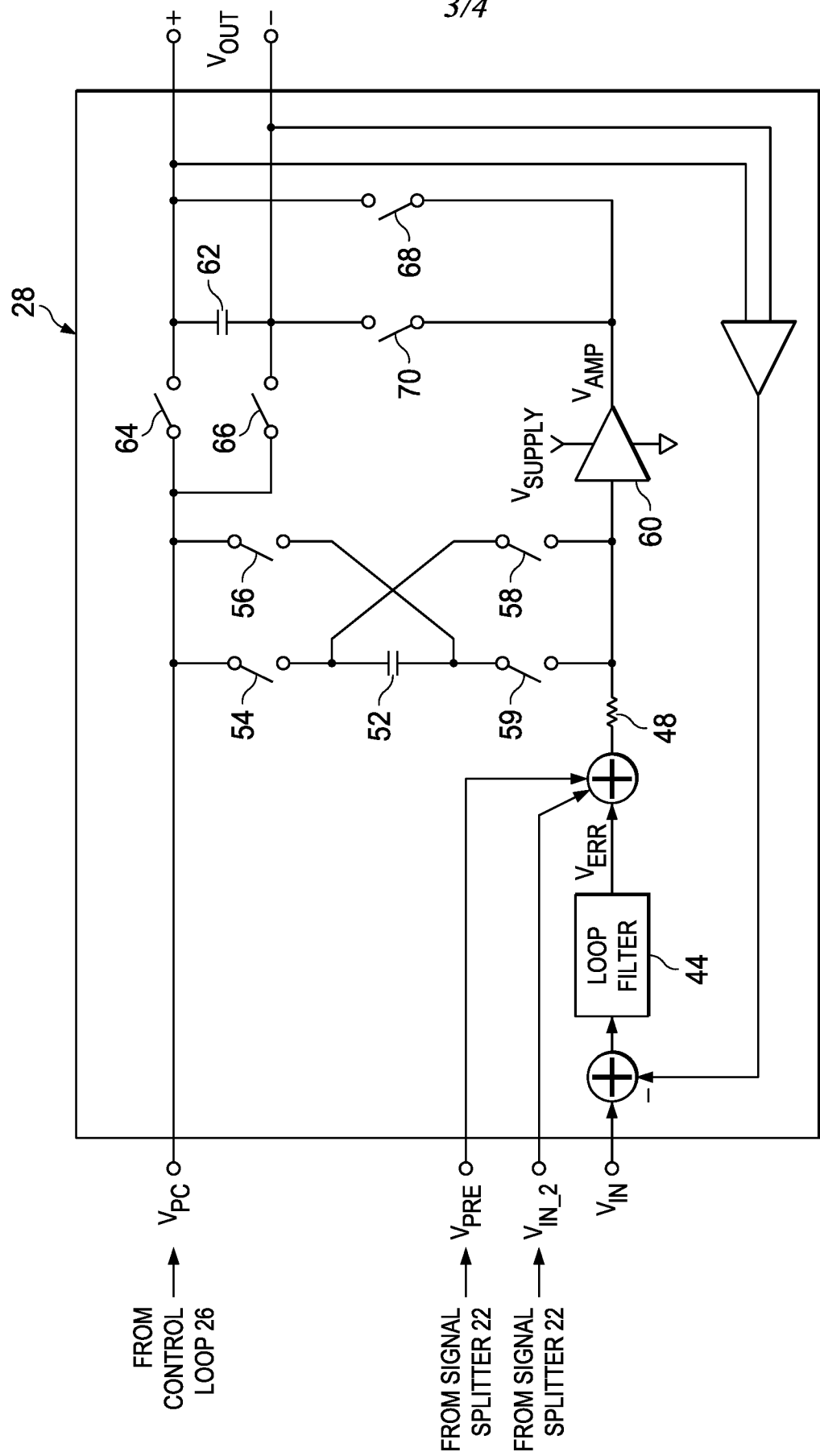


FIG. 5

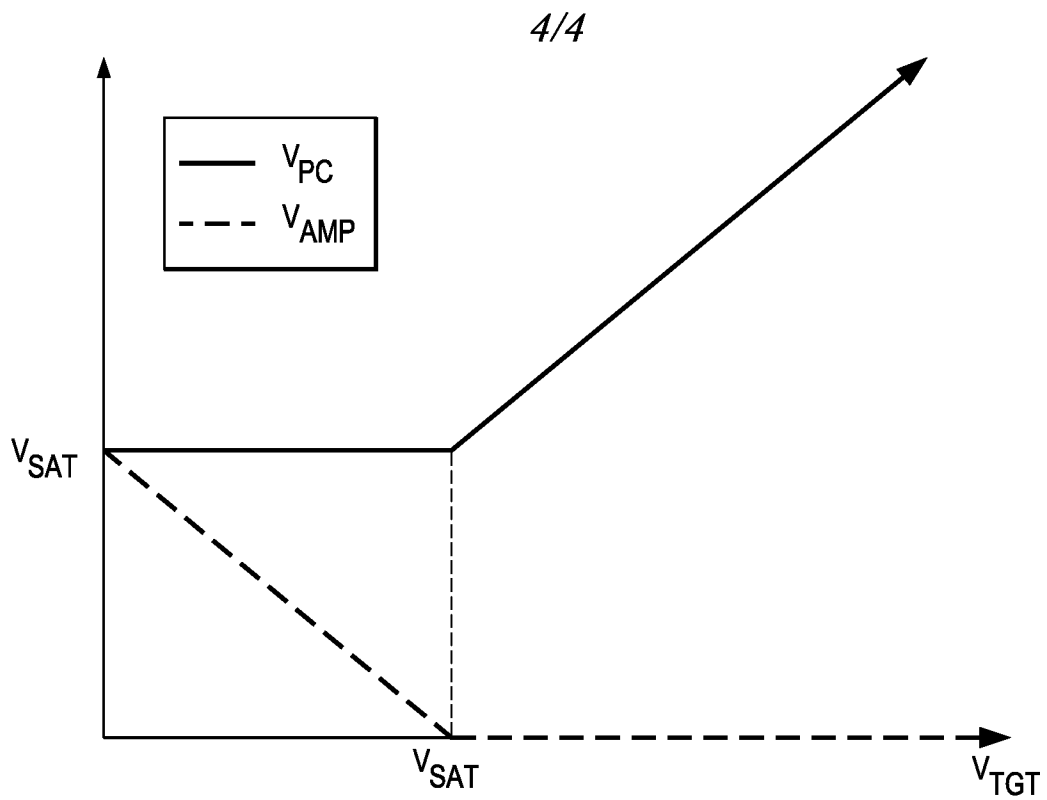


FIG. 6

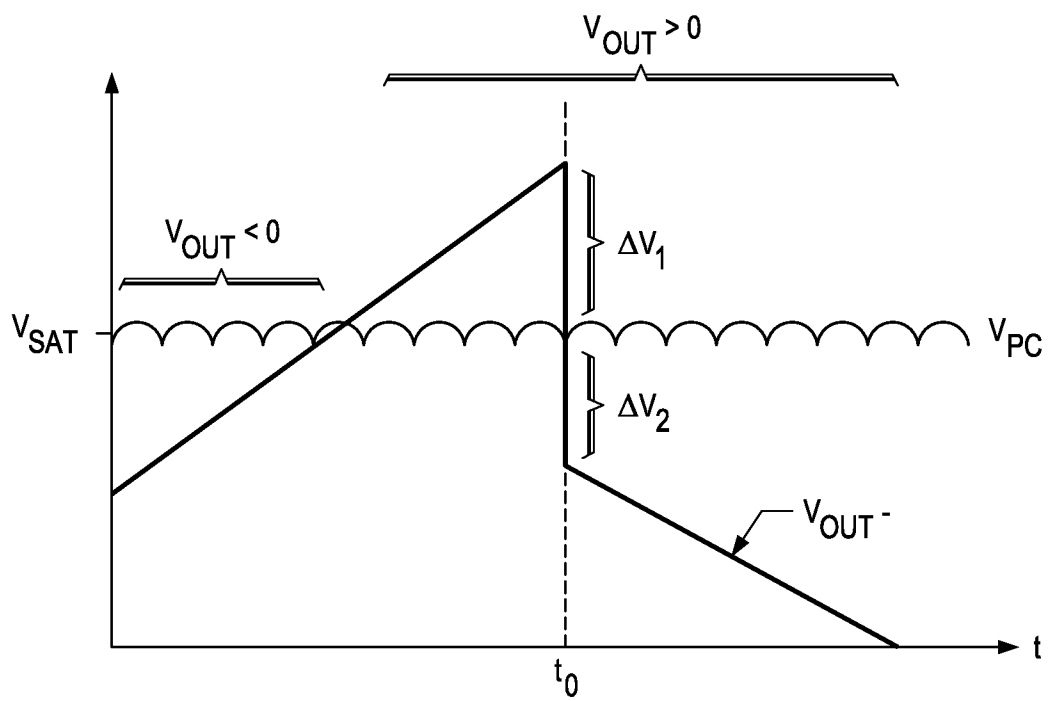


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/020927

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/217 H03F1/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/027247 A1 (KUMAMOTO TOSHIO [JP] ET AL) 29 January 2009 (2009-01-29) paragraph [0023] - paragraph [0026] paragraph [0047] paragraph [0066] - paragraph [0071] figures 1,8	1-10
A	----- US 2014/028395 A1 (CHAN CHI HONG [HK] ET AL) 30 January 2014 (2014-01-30) paragraph [0051] figure 10	1,6
A	----- US 2012/306575 A1 (SHAH PETER J [US] ET AL) 6 December 2012 (2012-12-06) paragraph [0046] figure 5 ----- -/--	1,6



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

15 May 2017

Date of mailing of the international search report

26/05/2017

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Breccia, Luca

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/020927

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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