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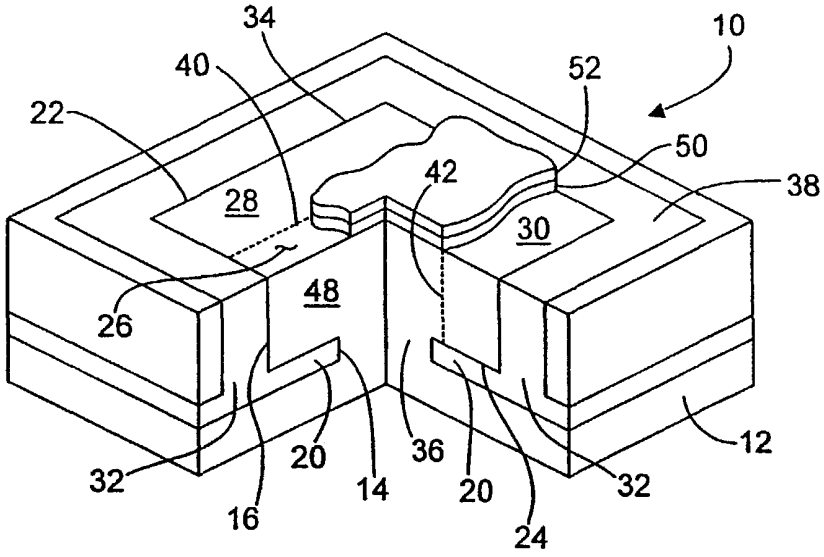
(54) Title: FIELD EFFECT TRANSISTOR WITH NON-FLOATING BODY AND METHOD FOR FORMING SAME ON A BULK SILICON WAFER



(57) Abstract: A silicon on insulator (SOI) field effect transistor (FET) structure is formed on a conventional bulk silicon wafer. The structure includes an electrical coupling between the channel region of the FET with the bulk silicon substrate to eliminate the floating body effect caused by charge accumulation in the channel regions due to historical operation of the FET. The method of forming the structure includes isolating the FET active region from other structures in the silicon substrate by forming an insulating trench about the perimeter of the FET and forming an undercut beneath the active region to reduce or eliminate junction capacitance between the source and drain regions and the silicon substrate.

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FIELD EFFECT TRANSISTOR WITH NON-FLOATING BODY AND METHOD FOR FORMING SAME ON A BULK SILICON WAFER

Technical Field

The present invention relates generally to silicon on insulator (SOI) field effect transistor structures, and more specifically to such structures formed on a conventional silicon bulk wafer.

Background Art

Conventional or bulk semiconductor devices are formed in semiconductive material by implanting a well of either P-type or N-type conductivity silicon in a silicon substrate wafer of the opposite conductivity. Gates and source/drain diffusions are then manufactured using commonly known processes. These form devices known as metal-oxide-semiconductor (MOS) field effect transistors (FETs). When a given chip uses both P-type and N-type, it is known as a complimentary metal oxide semiconductor (CMOS). Each of these transistors must be electrically isolated from the others in order to avoid shorting the circuits. A relatively large amount of surface area is needed for the electrical isolation of the various transistors. This is undesirable for the current industry goals for size reduction. Additionally, junction capacitance between the source/drain and the bulk substrate and "off" state leakage from the drain to the source both increase power consumption. Junction capacitance also slows the speed at which a device using such transistors can operate. These problems result in difficulties in reducing the size, power consumption, and voltage of CMOS technology devices.

In order to deal with the junction capacitance problem, silicon on insulator technology (SOI) has been gaining popularity. However, SOI field effect transistors suffer from floating body effects. The floating body effect occurs because the channel, or body, of the transistor is not connected to a fixed potential and, therefore the body takes on charge based on recent operation of the transistor. The floating body effect causes the current-to-voltage curve for the transistor to distort or kink, which in turn causes the threshold voltage for operating the transistor to fluctuate. This problem is particular apparent for passgate devices such as those used in dynamic random access memory (DRAM) wherein it is critical that the threshold voltage remain fixed such that the transistor remains in the "0ff" position to prevent charge leakage from the storage capacitor.

Accordingly, there is a strong need in the art for a semiconductor field effect transistor structure, and a method for forming such structure, that includes the low junction capacitance and low "off" state leakage characteristics of the SOI FET but does not suffer the disadvantages of a floating body potential.

Disclosure of the Invention

A first object of this invention is to provide a method of forming a field effect transistor on a semiconductor substrate which includes etching an insulating trench around the perimeter of an active region of said transistor to isolate the active region from other structures on said substrate and etching

an insulating undercut in the bottom of the insulating trench to isolate at least a portion of the bottom surface of the active region from the substrate. Portions of the active region may be doped to form each of a source region and a drain region on opposing sides of a central channel region. The insulating undercut may isolate at least a portion of both the source region and the drain region from the silicon substrate. Furthermore, the insulating undercut may isolate at least a portion of the central channel region from the silicon substrate.

Etching the undercut includes: a) forming a protective layer on the side walls and bottom of the trench; b) performing a vertical anisotropic etch of said layer to remove such layer to expose silicon substrate at the bottom of the trench; and c) performing an isotropic etch of the silicon substrate to form said undercut. The isotropic etch may be performed using a KOH wet etch. The protective layer may be silicon dioxide and filling the undercut may include performing a chemical vapor deposition using at least one of SiH4 and TEOS.

A second object of this invention is to provide a field effect transistor formed on a semiconductor substrate which includes an active region, including a central channel region and a source region and a drain region disposed on opposite sides of said central channel region, a bridge region, with a cross section area smaller than a cross section of the active region, consecutively coupling the central channel region with said semiconductor substrate; and an insulator isolating said active region and said bridge region from other structures formed on said semiconductor substrate. The central channel region, the bridge region, and the semiconductor substrate may all be the same conductivity and the source region and drain region may be of an opposite conductivity. The insulator may extend under a bottom surface of the active region to at least partially isolate the source region and the drain region from the silicon substrate such that the semiconductor junctions between the source region and the silicon substrate and the drain region and the silicon substrate are at least one of reduced in size or eliminated. The insulator may be silicon dioxide.

A third object of this invention is to provide a semiconductor device including a plurality of field effect transistors formed on a semiconductor substrate, each transistor including: a) an active region, including a central channel region and a source region and a drain region each on opposing sides of the central channel region; b) a bridge region, with a cross section area smaller than a cross section of the active body region, conductively coupling the central channel region with said semiconductor substrate; and c) an insulator isolating said active body region and said bridge region from at least one other of said plurality of transistors. The central channel region, the bridge region, and the semiconductor substrate all may be the same conductivity and the source region and drain region may be of an opposite conductivity. The insulator may extend under a bottom surface of the active region to at least partially isolate the source region and the drain region from the silicon substrate such that the semiconductor junctions between the source region and the silicon substrate and the drain

region and the silicon substrate are at least one of reduced in size or eliminated. The insulator isolating at least two of the plurality of transistors may be silicon dioxide.

Brief Description of the Drawings

Fig. 1 is a perspective view, partially cut away, of a field effect transistor (FET) formed on silicon substrate in accordance with this invention.

Fig. 2 is a cross sectional view of a first step in the fabrication of the FET of this invention.

Fig. 3 is a cross sectional view of a second step in the fabrication of the FET of this invention.

Fig. 4 is a cross sectional view of a third step in the fabrication of the FET of this invention.

Fig. 5 is a cross sectional view of a fourth step in the fabrication of the FET of this invention.

Fig. 6 is a cross sectional view of a fifth step in the fabrication of the FET of this invention.

Fig. 7 is a cross sectional view of a sixth step in the fabrication of the FET of this invention.

Fig. 8 is a cross sectional view of a seventh step in the fabrication of the FET of this invention.

Fig. 9 is a cross sectional view of a eighth step in the fabrication of the FET of this invention.

Fig. 10 is a cross sectional view of the FET of this invention.

Modes for Carrying Out the Invention

The present invention will now be described in detail with reference to the drawings. In the drawings, like reference numerals are used to refer to like elements throughout.

Referring to Figure 1, it can be seen that an active region 48 of a field effect transistor 10 of this invention includes a channel region 26, a source region 28, and a drain region 30. In the exemplary embodiment of this invention, the channel region 26 is preferably P-conductivity silicon while the source region 28 and the drain region 30 are each N-conductivity silicon to form two semiconductor junctions 40 and 42. However, in accordance with known silicon technology, the channel region 26 may be N-conductivity silicon while each of the source region 28 and the drain region 30 are P-conductivity silicon. The active region is isolated by an insulating trench 32 which has side walls 16 forming the perimeter 22 of the active region 48 of the FET 10. The insulating trench 32 insulates the active region 48 from other structures formed in the silicon substrate 12. The insulating trench 32 includes under cut regions 20 which form the bottom surface 24 of the active region 48 and form the sidewalls 14 of a bridge region 36 which electrically couples the channel region 26 of the active region 48 to the bulk silicon substrate 12. The active region 38 and the bridge region 36 together form the body 34 of the FET 10 of this invention.

It should be appreciated that because the bridge region 36 electrically couples the channel region 26 to the bulk silicon substrate 12, the channel region 26 potential will always remain at the potential of the silicon substrate 12 and can not accumulate a charge, or float, based on historical operation of the FET 10. It should also be appreciated that because the insulating trench 32 includes undercut regions 20, the cross sectional area of the bridge region 36 is significantly smaller than the

cross sectional area of the active region 48 and therefore there is no semiconductor junction, or minimal sized semiconductor junction, between either the source region 28 or the drain region 30 and the silicon substrate 12 thereby reducing junction capacitance.

The first step in fabricating the FET of this invention a silicon nitride layer 18 approximately 1,500 – 2,000 Angstroms thick is formed on top of a thin layer of oxide (not shown) approximately 150 – 200 on the top surface of the bulk silicon substrate 12 as shown in Figure 2.

In a second step, the silicon nitride 18 is patterned and etched to form a silicon nitride mask over the active region 48 while exposing the silicon substrate in the areas where insulating trench 32 is to be formed as shown in Figure 3. Patterning and etching the silicon nitride 18 to form the silicon nitride mask is performed using conventional photolithography techniques wherein 1) a layer of a UV sensitive photoresist layer is applied to the surface of the silicon nitride 18; 2) a UV illumination source and reticle provide collimated light to expose and pattern the photoresist; 3) A developer solution hardens the unexposed areas of the photoresist while the UV light dissolves and the developer washes away the exposed portions thereby leaving the exposed portions as a mask on the surface of the silicon nitride 18; And 4) a dry etch with an etching compound that etches silicon nitride while not etching the photoresist removes the silicon nitride layer 18 in the areas that are not masked with the photoresist thereby creating the silicon nitride mask.

In a third step in the fabrication of the FET of this invention the unmasked portions of the silicon substrate 12 (e.g. the portions where the silicon nitride mask has been etched away in the second step) are etched away to a depth of approximately 2,000 – 4,000 Angstroms to form an open trench 38 as shown in Figure 4. The open trench 38 will later be filled with silicon dioxide to become the insulating trench 32 described in the discussion of Figure 1. The etching process for the silicon substrate is typically an anisotropic dry etch using hydrogen bromide (HBr) which has selectivity characteristics such that it etches the silicon substrate 12 but not the silicon nitride 18.

A fourth step in the fabrication of the FET 10 of this invention includes depositing a layer of silicon dioxide 44, approximately 500 – 1,000 Angstroms in depth, across all exposed surfaces of the wafer including the across the top of the silicon nitride layer 18 and on the sidewalls and bottom of open trench 38 as shown in Figure 5. Depositing the layer of silicon dioxide 44 is typically performed using a conventional chemical vapor deposition (CVD) process with a gas such as SiH4.

Following the deposit of the silicon dioxide 44, a vertical anisotropic etch of the silicon dioxide layer 44 removes such silicon dioxide from all horizontal surfaces, including the top surface of the silicon nitride 18 and the bottom of open trench 38. An example of a vertical anisotropic etch includes a plasma etch using CHF3. It should be appreciated that such an etching technique removes an even thickness of the silicon dioxide layer in a vertical dimension such that the net result of the vertical etch is that a layer of silicon dioxide remains on the side walls 16 of the open trench 38 while the bottom of

trench 38 is exposed silicon substrate 12.

In the sixth step in the fabrication of the FET 10 of this invention an isotropic etch of the bulk silicon at the bottom of the open trench 38 is performed to remove approximately 1,000 – 2,000 Angstroms of material in both the horizontal and vertical dimensions to form an open undercut 46 which in a subsequent step will be filled with silicon dioxide to form the undercut region 20 of the insulating trench 32 as shown in Figure 7. This isototropic etching step is preferably a known KOH wet etch. It should be appreciated that such an etching compound must be chosen with selectivity characteristics such that it will rapidly etch the exposed silicon substrate 12 but will not materially etch the silicon dioxide coating 44 on the sidewalls of the open trench 38. Note that undercut regions 20 define the bottom surface 24 of the active region 48 and the side walls 14 of the bridge region 36.

Following the creation of the undercut regions 20, the open trench 38 is filled with silicon dioxide to form insulating trench 32. Filling the open trench 38 preferably uses a known CVD process using a gas such as SiH4 or TEOS. After filling the open trench 38, the surface of the wafer is polished using a chemical mechanical polish (CMP) to remove any excess silicon dioxide layer and the remaining silicon nitride mask as shown in Figure 8.

In a seventh step, a layer of silicon dioxide 50, serving as the gate oxide layer, and a polysilicon gate 52 are formed on the top surface of the substrate. The silicon dioxide 50 is typically grown on the surface of the active region 48 using a thermal oxidation process and the polysilicon layer is deposited on top of the silicon dioxide layer 50 using a low pressure chemical vapor deposition (LPCVD) process. The polysilicon layer is then patterned and etched using the photolithography method discussed earlier to define and mask the channel region of the FET 10 in a known self alligning gate, source and drain process as shown in Figure 9.

In the eighth step, the portions of the silicon substrate on opposing sides of the P-type silicon in the channel region of the FET 10 that are not masked by the gate applied in the 7^{th} step are doped into N-type silicon. Doping is typically performed using Ion implantation techniques. Ions of dopant such as arsenic 54 are accelerated to a high velocity in an electric field and impinge on the target wafer. Because the ions cannot penetrate the poly-silicon gate, the poly-silicon gate effectively operates as a mask which results in doping only the exposed source region 28, the drain region 30, and the polysilicon gate 52 as shown in Figure 10.

Although the invention has been shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the specification. For example, in the exemplary embodiment, two masking steps are used to mask and etch the open trench regions 38. A photoresist mask is used to create a silicon nitride mask which in turn effects the etching of the open trenches 38. Those skilled in the art will appreciate that if a compound is selective between the photoresist and the silicon substrate

(e.g. etches the silicon substrate while not materially effecting a photoresist mask.) the photoresist mask may be used to directly etch the open trenches in the silicon substrate. The present invention includes all such equivalents and modifications, and is limited only by the scope of the following claims.

CLAIMS

What is claimed is:

1. A method of forming a field effect transistor on a semiconductor substrate, comprising the steps of:

a) etching an insulating trench around the perimeter of an active region of said transistor to isolate the active region from other structures on said substrate;

c) etching an insulating undercut in the bottom of the insulating trench to isolate at least a portion of the bottom surface of the active region from the substrate.

2. The method of claim 1 further including the step of doping portions of the active region to form each of a source region and a drain region on opposing sides of a central channel region and wherein the insulating undercut isolates at least a portion of both the source region and the drain region from the silicon substrate.

3. The method of claim 2 wherein the undercut isolates at least a portion of the central channel region from the silicon substrate.

4. The method of claim 3 wherein the step of etching the undercut includes the steps of:

a) forming a protective layer on the side walls and bottom of trench;

b) performing a vertical anisotropic etch of said layer to remove such layer to expose the silicon substrate at the bottom of the trench; and

c) performing an isotropic etch of the silicon substrate to form said undercut.

5. The method of claim 4 wherein the protective layer is silicon dioxide.

6. The method of claim 4 wherein the isotropic etch is performed using a KOH wet etch. 7. The method of claim 4 wherein the step of forming the insulator includes filling at least a portion of said undercut and said trench using a chemical vapor deposition process using at least one of TEOS or SiH4.

8. A field effect transistor formed on a semiconductor substrate comprising:

a) an active region, including a central channel region and a source region and a drain region disposed on opposite sides of said central channel region;

b) a bridge region, with a cross section area smaller than a cross section of the active region, consecutively coupling the central channel region with said semiconductor substrate; and

c) an insulator isolating said active region and said bridge region from other structures formed on said semiconductor substrate.

9. The field effect transistor of claim 8 wherein the central channel region, the bridge region, and the semiconductor substrate are all the same conductivity and the source region and drain region are of an opposite conductivity.

10. The field effect transistor of claim 9 wherein the insulator extends under a bottom surface of

the active region to at least partially isolate the source region and the drain region from the silicon substrate such that the semiconductor junctions between the source region and the silicon substrate and the drain region and the silicon substrate are at least one of reduced in size or eliminated.

11. The field effect transistor of claim 10 wherein the insulator is silicon dioxide.

12. A semiconductor device including a plurality of field effect transistors formed on a semiconductor substrate, each transistor comprising:

a) an active region, including a central channel region and a source region and a drain region each on opposing sides of the central channel region;

b) a bridge region, with a cross section area smaller than a cross section of the active body region, conductively coupling the central channel region with said semiconductor substrate; and

c) an insulator isolating said active body region and said bridge region from at least one other of said plurality of transistors.

13. The semiconductor device of claim 12 wherein the central channel region, the bridge region, and the semiconductor substrate are all the same conductivity and the source region and drain region are of an opposite conductivity.

14. The semiconductor device of claim 13 wherein the insulator extends under a bottom surface of the active region to at least partially isolate the source region and the drain region from the silicon substrate such that the semiconductor junctions between the source region and the silicon substrate and the drain region and the silicon substrate are at least one of reduced in size or eliminated.

15. The semiconductor device of claim 14 wherein the insulator isolating at least two of the plurality of transistors is silicon dioxide.

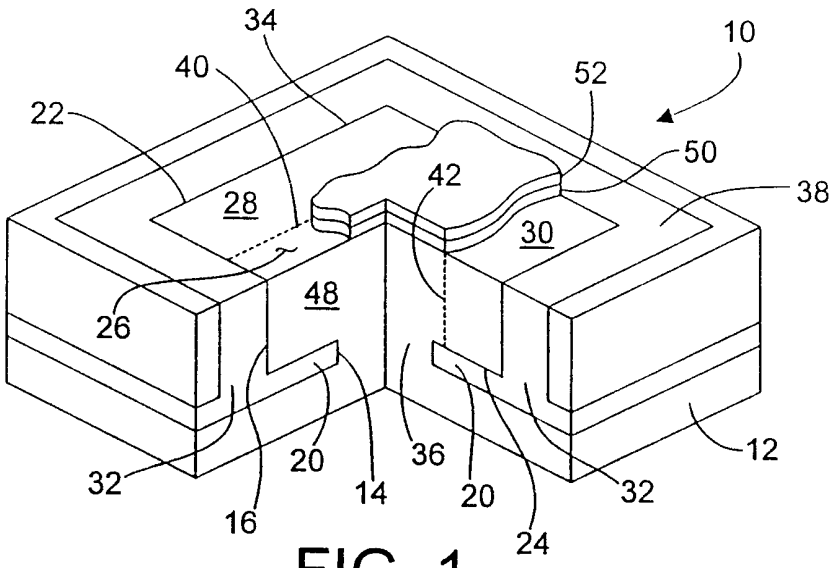

FIG. 1

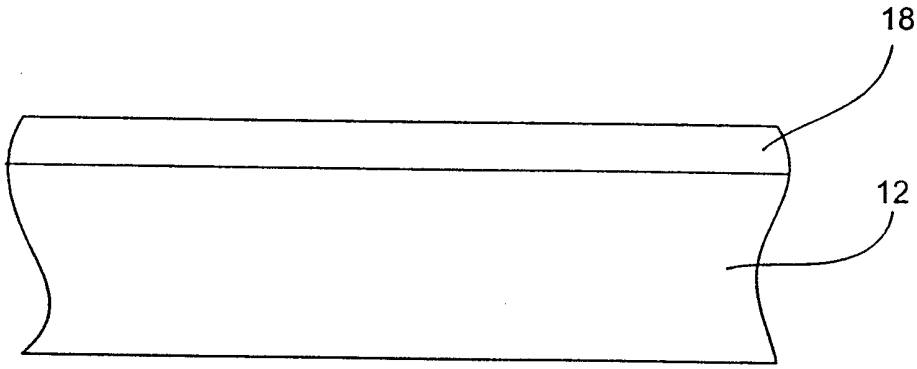

FIG. 2

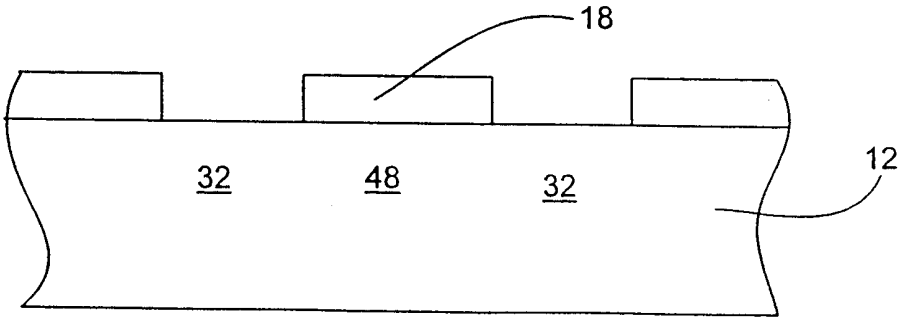

FIG. 3

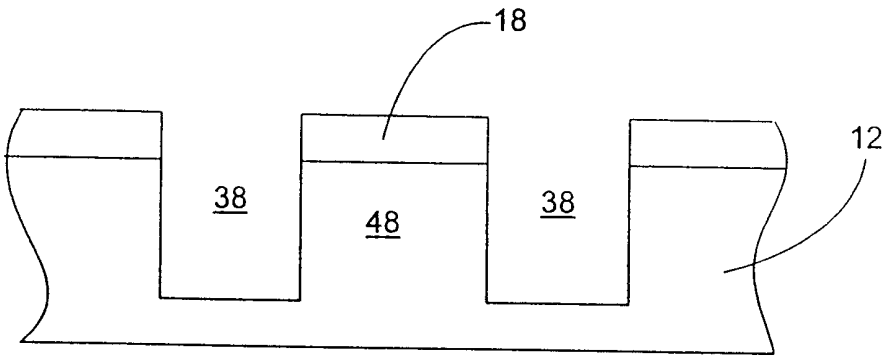

FIG. 4

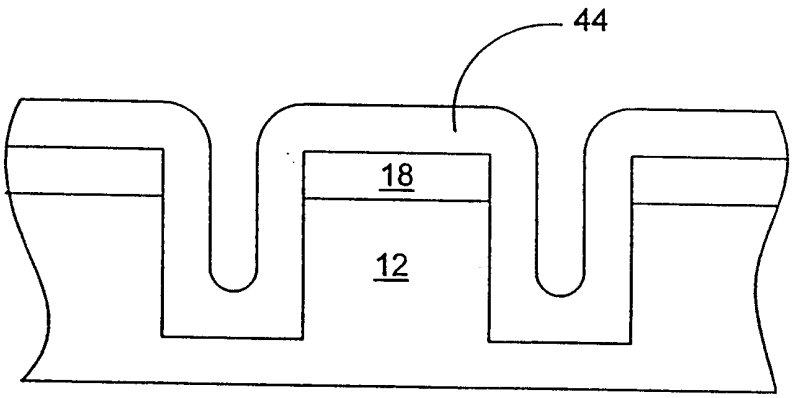

FIG. 5

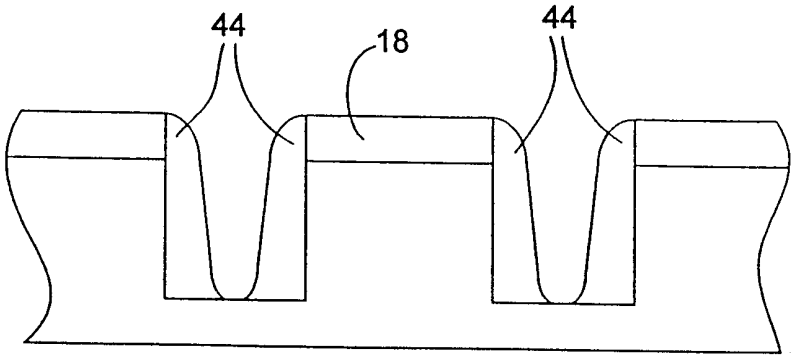

FIG. 6

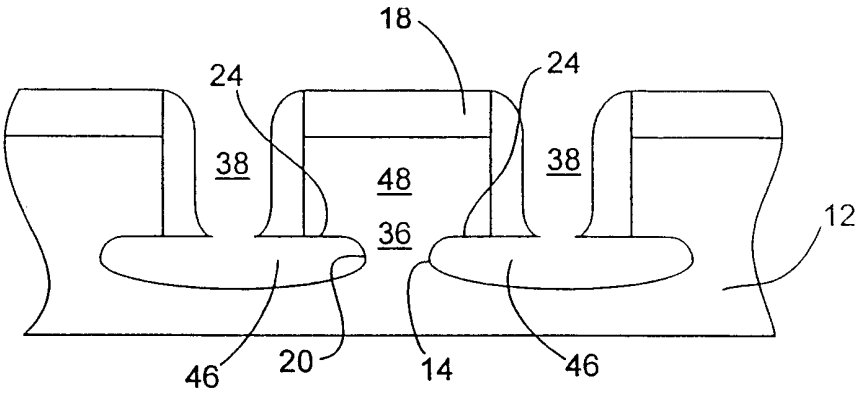

FIG. 7

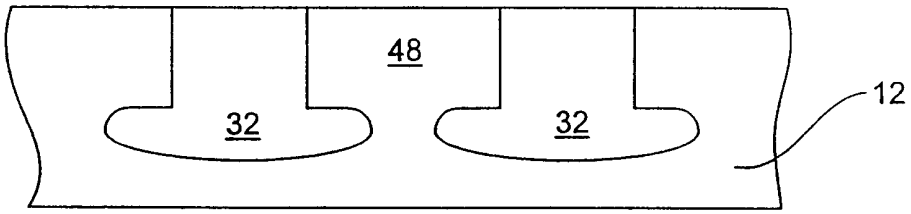

FIG. 8

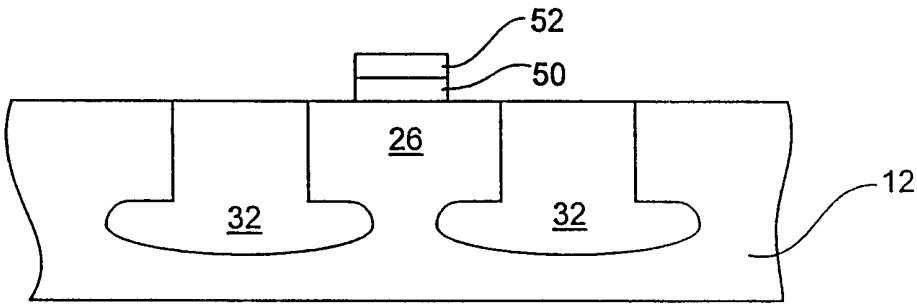

FIG. 9

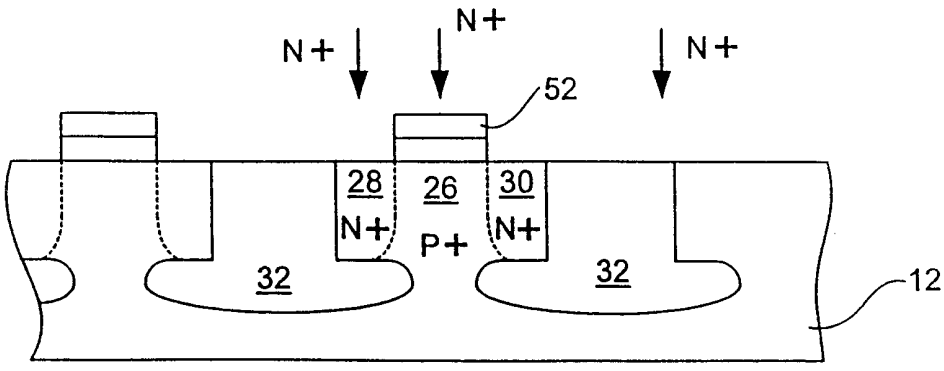

FIG. 10

INTERNATIONAL SEARCH REPORT

Inter ɔnal Application No
PCT/US 00/26165

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/762 H01L27/12 H01L21/84

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX, IBM-TDB, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	EP 0 480 373 A (SEIKO EPSON CORP) 15 April 1992 (1992-04-15) figure 4	8-15
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☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
8 November 2000	16/11/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte onal Application No
PCT/US 00/26165

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