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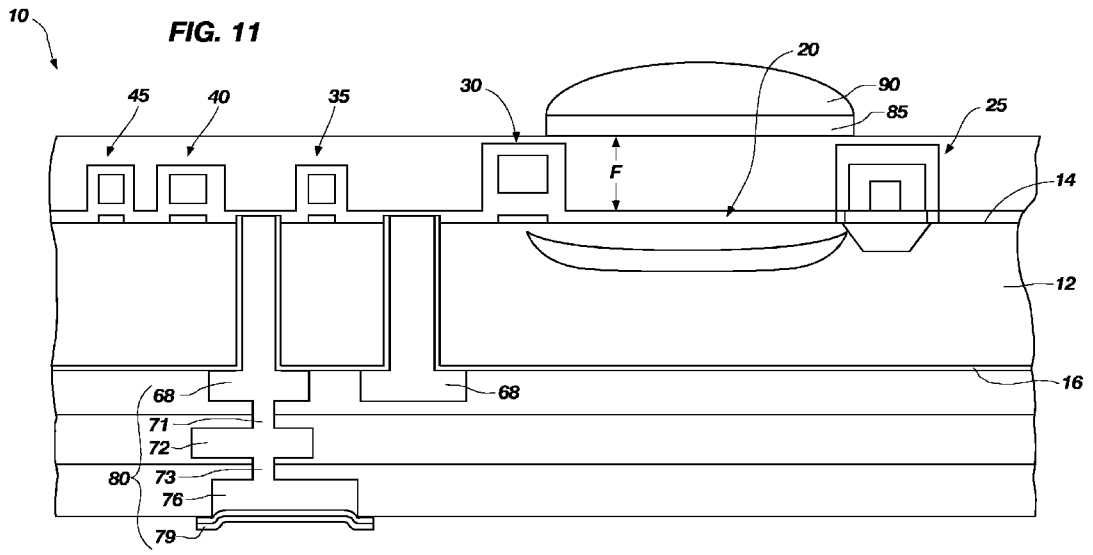
(54) **Title:** IMAGERS WITH CONTACT PLUGS EXTENDING THROUGH THE SUBSTRATES THEREOF AND IMAGER FABRICATION METHODS



(57) **Abstract:** Methods for fabricating photoimagers, such as complementary metal-oxide-semiconductor (CMOS) imagers, include fabricating image sensing elements, transistors, and other low-elevation features on an active surface of a fabrication substrate, and fabricating contact plugs, conductive lines, external contacts, and other higher-elevation features on the back side of the fabrication substrate. Imagers with image sensing elements and transistors on the active surface and contact plugs that extend through the substrate are also disclosed, as are electronic devices including such imagers.

WO 2008/157152 A1

IMAGERS WITH CONTACT PLUGS EXTENDING THROUGH THE SUBSTRATES THEREOF AND IMAGER FABRICATION METHODS

PRIORITY CLAIM

This application claims the benefit of the filing date of United States patent application Serial Number 11/761,904, filed June 12, 2007.

TECHNICAL FIELD

The present invention, in various embodiments, relates generally to methods for fabricating photoimagers, such as complementary metal-oxide-semiconductor (CMOS) imagers, which are also referred to herein more simply as "imagers." More specific embodiments of the present invention include imager fabrication methods in which transistors are fabricated on an active surface of a substrate, then contact openings, contact plugs, metallization, and contact pads are formed on and from a back side of the substrate. In addition, embodiments of the present invention comprise imagers with integrated circuitry on the back sides thereof.

BACKGROUND

Conventionally, imagers have been fabricated with image sensing regions, integrated circuitry, and contacts on the active surface of a silicon wafer. State-of-the-art semiconductor devices, including imagers, typically have dimensions that are as small as possible. Nonetheless, a significant portion of the area, or real estate, on the active surface of an imager is typically occupied by image sensing elements. Accordingly, various other elements, including conductive lines, or traces, must be densely packed into the remaining, typically peripheral, areas of the semiconductor device. When conductive lines, or traces, are densely arranged, cross-talk, capacitance, and other undesirable electrical issues must be resolved. The difficulty in resolving these issues increases the more densely the conductive lines are arranged.

Another factor that sometimes undesirably adds to the area consumed by an imager is the so-called "snowplow" effect that occurs when color filter array (CFA) materials are applied (*e.g.*, by spin coating) over imagers in which the dielectric material (*e.g.*, glass) that overlies the image sensing elements has been thinned relative

to the surrounding areas of the imager. Specifically, a peripheral "dead" zone is provided around an array of image sensing elements to accommodate thicker regions of color filter array material so as to avoid the presence of these thicker, or snowplowed, regions over the image sensing elements. The requirement of additional area prevents further decreases in the total area consumed by the imager, or introduces the additional complexities involved in increasing the density of the peripherally confined elements of the imager.

Furthermore, the presence of bond pads on the active surfaces of imagers necessitates that bond wires or other laterally extending intermediate conductive elements be used to electrically connect such imagers to carriers (*e.g.*, circuit boards) and to other electronic components. As bond wires and other laterally extending intermediate conductive elements extend beyond the periphery of an imager to contacts (*e.g.*, terminals) located outside of the periphery of the imager, they and the contacts occupy even more of the real estate upon the carrier, the value of which increases with decreases in acceptable electronic device dimensions.

DISCLOSURE OF INVENTION

Several approaches have been taken to address this undesirable occupation of real estate upon carriers for imagers. One approach has been to form through wafer interconnects (TWIs), or conductive vias, through the substrate of an imager. This approach requires that holes be formed through areas of the imager substrate that are not occupied by image sensing elements or integrated circuitry. The requirement of such "dead" area on a substrate, however, contradicts the trend toward maximized density and, thus, prevents optimal minimization of the dimensions of an imager. The other approach has been to form conductive elements that extend around the outer periphery of the imager substrate, which enables optimal circuit density, but effectively adds to the outer dimensions of the finished semiconductor device. Further, any redistribution layers (RDLs), or redistribution circuitry, required by both of these approaches undesirably adds to the overall thickness and cost of the imager.

Accordingly, there are needs for processes in which undesirable electrical effects of imagers may be reduced and contacts may be fabricated on the back sides of imagers while facilitating minimization of the peripheral dimensions of the imagers.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, in which various features of embodiments of the present invention are depicted:

FIGs. 1 through 10 are partial cross-sectional representations of imagers under fabrication in accordance with embodiments of the present invention;

FIG. 11 is a partial cross-sectional representation of an embodiment of an imager including contact holes extending through the substrate thereof, as well as circuitry carried by a back side of the substrate; and

FIG. 12 is a schematic representation depicting an embodiment of an electronic device that includes an imager according to various embodiments of the present invention.

DETAILED DESCRIPTION

The present invention includes various embodiments of methods for fabricating imagers. Such methods include the fabrication of image sensing elements and transistors on the active surface of a substrate and the fabrication of contact openings, contact plugs, conductive lines, and contacts on and from the back side of the substrate.

With reference to FIG. 1, an embodiment of a portion of a partially fabricated, or intermediate, imager 10 is illustrated. Imager 10 includes a substrate 12, comprising a fabrication substrate, such as a full or partial wafer of semiconductor material (*e.g.*, silicon, gallium arsenide, indium phosphide, etc), a full or partial silicon-on-insulator (SOI) type substrate, such as a silicon-on-glass (SOG), silicon-on-ceramic (SOC), or silicon-on-sapphire (SOS) substrate, or any other known, suitable fabrication substrate. Substrate 12 has an active surface 14 and a back side 16.

In addition, imager 10 includes a variety of elements that have been fabricated by known processes. In the illustrated embodiment, in which features corresponding to only one pixel of imager 10 are shown, imager 10 includes at least one image sensing element 20 in active surface 14 of substrate, as well as a photocell capacitor 25 and its underlying shallow trench isolation (STI) structure 27, and a transfer gate 30, a reset gate 35, a source follower gate 40, a row select gate 45, and appropriate source and drain regions (not shown) that correspond to sensing element 20. Transfer gate 30, reset gate 35, source follower gate 40, row select gate 45, and their respective source and drain regions are collectively referred to hereinafter as "imager transistors 30-45."

Like image sensing element 20, photocell capacitor 25, STI structure 27, and imager transistors 30-45 may also be located at active surface 14.

Optionally, as shown in FIG. 1A, imager 10 may include contact holes 60′ that extend into substrate 12 through active surface 14. In the depicted embodiment, contact holes 60′ are blind vias. The distance (*e.g.*, diameter, etc.) across a contact hole 60′ may be about 200 nm or less. In some embodiments, the distance across a contact hole 60′ may be as small as about 100 nm, about 50 nm, or less. Each contact hole 60′ may contain a dielectric liners 62′ and a conductive plug 64′. When present, these features may be fabricated in any suitable manner known in the art, or in a manner similar to that described in reference to FIGs. 3 through 7 below.

Imager 10 also includes a dielectric film 50 (*e.g.*, doped silicon dioxide, such as borophosphosilicate glass (BPSG), phosphosilicate glass (BSG), phosphosilicate glass (PSG) or the like, etc.) over image sensing element 20, photocell capacitor 25, and imager transistors 30-45. Dielectric film 50 may be applied in a thickness of about one-half micron (0.5 μm) or less. Following its application, an exposed surface of dielectric film 50 may, in some embodiments, be planarized. Known planarization techniques, such as chemical-mechanical polishing (CMP), may be used to planarize the exposed surface of dielectric film 50.

In some embodiments, as illustrated in FIG. 1B, a color filter array (CFA) 85 may be located over imager 10, or over at least image sensing element 20 thereof. Likewise, as is also illustrated in FIG. 1B, a microlens 90 may be present over each image sensing element 20.

After the foregoing features have been fabricated (*e.g.*, by employing known techniques or processes described herein) substrate 12 may, in some embodiments of the present invention, be thinned. Known processes (*e.g.*, grinding, wet etching, etc.) may be used to remove material from back side 16 of substrate and, thus, to thin substrate 12. Substrate 12 may be thinned to any acceptable thickness (*e.g.*, as thin as 100 μm in some embodiments, as thin as 50 μm in other embodiments, and even thinner substrates are contemplated as encompassed by the invention). In embodiments where imager 10 already includes contact plugs 64′, the contact plugs 64′ may be exposed as substrate 12 is thinned, potentially eliminating the need for the additional processing described in reference to FIGs. 3 through 7.

Once substrate 12 has a desired thickness, features may be fabricated on backside 16. An embodiment of such a back side fabrication process is depicted in FIGs. 2-9.

As illustrated in FIG. 2, imager 10 may be secured, dielectric film 50-down, to a carrier 200. In some embodiments, carrier 200 may comprise a glass substrate, while in other embodiments, carrier 200 may comprise a fabrication substrate (*e.g.*, a silicon wafer). Dielectric film 50 may, in these and other embodiments of carrier 200, be secured to carrier 200 by way of a suitable adhesive material (*e.g.*, a polymeric adhesive, etc.) that will withstand the fabrication temperatures (*e.g.*, up to about 250° C) to which imager 10 will be subsequently exposed. In still other embodiments, carrier 200 may be an electrostatic carrier, such as a carrier of the type described in Bock, K., et al., "Characterization of electrostatic carrier substrates to be used as a support for thin semiconductor wafers," Fraunhofer Institute for Reliability and Microintegration IZM-M (no date available) to which imager 10 is secured by electrostatic forces.

In FIG. 3, in embodiments where contact holes 60, dielectric liners 61, and conductive plugs 64 (FIG. 1A) were not formed before securing imager 10 dielectric film 50-down to carrier 200, or in embodiments where additional contact holes 60, dielectric liners 61, and contact plugs 64 are desired, contact holes 60 may be formed from through substrate 12, from back side 16 thereof, toward active surface 14, to expose features 65 (*e.g.*, source/drain regions, etc.) that, in conventional fabrication processes, would have been exposed by forming contact holes through dielectric film 50. The distance (*e.g.*, diameter, etc.) across a contact hole 60 may be about 200 nm or less. In some embodiments, the distance across a contact hole 60 may be as small as about 100 nm, about 50 nm, or less. Contact holes 60 may be fabricated by known processes, such as by laser ablation or mask and etch processes. When mask and etch processes are used, a suitable mask (*e.g.*, a transparent carbon mask, a hard mask, a photomask, etc.) (not shown) may be formed over back side 16 of substrate and material may be removed from substrate 12 through the mask (*e.g.*, by dry etch processes).

As contact holes 60 extend directly to very small features 65 (*e.g.*, features that, in some embodiments, correspond to conductive line widths of about 100 nm or less) (*e.g.*, source/drain regions, etc.) at active surface 14, contact holes 60 may have

correspondingly small dimensions. As noted above, in some embodiments contact holes 60 may be about 200 nm or less across, or in diameter. In other embodiments, contact holes may be about 100 nm or less across, or in diameter.

As shown in FIG. 4, contact holes 60 may be lined with dielectric material to electrically isolate conductive features, such as contact plugs 64 (FIG. 7), which are also referred to herein as "interconnects," and other conductive features, that are to be subsequently fabricated within contact holes 60 from substrate 12. In a specific embodiment, the dielectric material lining contact holes 60 may comprise silicon dioxide with trace amounts of aluminum. Dielectric liners 62 (FIGs. 5 and 6) may be formed by forming a thin dielectric film 61 within each contact hole 60. Known processes may be used to form dielectric film 61. In some embodiments, pulsed layer deposition (PLD) processes may be used to form dielectric film 61. In other embodiments, dielectric film 61 may be formed by low silane oxide (LSO) deposition processes.

In embodiments where the dielectric film 61 covers features 65 to which electrical contacts are to be made, dielectric film 61 is removed from features 65 to re-expose the same to contact holes 60, as depicted in FIGs. 5 and 6.

In some embodiments, such re-exposure may be effected by way of a so-called "spacer etch," which is a dry etch in which portions of an etched film that are oriented in substantially the same direction as (*i.e.*, substantially parallel to) that in which the etch is to be effected (*e.g.*, portions of dielectric film 61 (FIG. 4) on the side walls of contact holes 60) remain substantially unetched, while portions of the etched film that are oriented differently (*i.e.*, substantially transverse to the direction of the etch) are removed. More specifically, portions of dielectric film 61 on features 65 are removed and, as shown in FIG. 5, portions of dielectric film 61 on back side 16 of substrate 12 may also be removed, leaving dielectric liners 62 on surfaces of contact holes 60.

Alternatively, in other embodiments, a mask (*e.g.*, a photomask, a hard mask, a transparent carbon mask, any combination of the foregoing, etc.) (not shown) of a type known in the art may be formed over dielectric film 61 (FIG. 4). Apertures of the mask may be configured and aligned so as to facilitate exposure of portions of dielectric film 61 that cover features 65, with which electrical contact is to be established, to a suitable, known anisotropic etchant (*e.g.*, a dry etchant). When imager 10, the mask, and regions of dielectric film 61 that are exposed through the mask are contacted, by

known techniques, by the isotropic etchant, material is removed from the contacted regions of dielectric film 61, re-exposing features 65. Following the re-exposure of features 65 through dielectric film 61, the mask may be removed. Regions of dielectric film 61 that remain on surfaces of contact holes 60 form dielectric liners 62, while regions of dielectric film 61 that overlie back side 16 of substrate 12 may remain as a back side dielectric layer 66, as shown in FIG. 6.

Conductive features, including contact plugs 64, may then be formed in contact holes 60, as shown in FIG. 7. Known processes may be used to fabricate contact plugs 64 and conductive features within contact holes 60. Thus, in some embodiments, diffusion barriers (*e.g.,* titanium nitride, tungsten nitride, etc.) and/or interconnects (*e.g.,* metal silicides) may be formed in contact holes 60 to provide desirable electrical connectivity between a contact plug 64 and a contacted feature, without undesirable interdiffusion between the materials of contact plug 64 and the contact feature. Regardless of whether diffusion barriers or interconnects are fabricated within contact holes 60, known processes (*e.g.,* chemical vapor deposition (CVD), PLD, atomic layer deposition (ALD), etc.) may be used to introduce conductive material into contact holes 60 and, thus, to form contact plugs 64 within contact holes 60.

Some embodiments of contact plugs 64 may be formed by filling or substantially filling contact holes 60 with conductive material (*e.g.,* by known deposition processes). Other embodiments of contact plugs 64 may be fabricated by forming (*e.g.,*. by deposition processes) one or more films, or coatings, of conductive material (*e.g.,* polysilicon, etc.) on a surface of each contact hole 60 (*i.e.,* on dielectric liner 62, a diffusion barrier, an interconnect, etc.), then filling (*e.g.,* by deposition processes, plating processes, etc.) any void remaining within the contact hole 60 with a conductive material (*e.g.,* polysilicon, tungsten, etc.) or a dielectric material.

In embodiments where the material layer or layers from which contact plugs 64 are formed are electrically isolated from back side 16 of substrate 12 by back side dielectric film 66 (*see, e.g.,* FIG. 6), the material layer or layers may remain on back side dielectric film 66 for further processing, or they may be removed by known processes (*e.g.,* CMP, wet etching, etc.).

In other embodiments, where back side 16 of substrate 12 was not covered by a back side dielectric layer 66 prior to the fabrication of contact plugs 64 (*see, e.g.,* FIG. 5), any conductive material remaining on back side 16 is removed.

Known processes, such as CMP and/or or wet etching, may be used to remove conductive material from back side 16.

In such embodiments, as well as in imager 10 embodiments in which contact plugs 64′ are formed through active surface 14 of substrate 12 rather than through back side 16 thereof, such as the embodiment shown in FIG. 1A, one or more layers of dielectric material may be formed on (*e.g.,* by thermal growth, deposition techniques, etc.) or applied to (*e.g.,* by spin-on techniques, etc.) back side 16. Contact plugs 64 may then be exposed (*e.g.,* by mask and etch processes) through the resulting layer of dielectric material. The result is a back side dielectric layer 66, as shown in FIG. 8.

Next, as shown in FIG. 9, conductive lines 68 that are connected to contact plugs 64 and that extend laterally over back side 16 may be fabricated. In embodiments where one or more layers of conductive material already overlie back side dielectric layer 66, conductive lines 68 may be fabricated from the one or more layers of conductive material and any associated material layers. Alternatively, one or more material layers, including one or more layers of conductive material, may be formed over dielectric layer 66, as known in the art (*e.g.,* by deposition processes, etc.), to facilitate fabrication of conductive lines 68. Once the appropriate material layer or layers are present on dielectric layer 66, laterally extending conductive lines 68 may be fabricated by known processes (*e.g.,* mask and etch techniques).

Further processing may continue, as known in the art, to form additional interlayer dielectric films 70, 74, laterally extending conductive lines 72, 76, interlayer contacts or interconnects 71, 73, and any other desired semiconductor device features, as well as a protective layer 78 and external contacts 79 (*e.g.,* bond pads), to fabricate a completed imager 10 with back side integrated circuitry 80, as shown in FIG. 10.

Referring now to FIG. 11, once back side integrated circuitry 80 has been fabricated, imager 10 may be removed from carrier 200 (FIG. 10) and, if necessary or desired, cleaned. As illustrated, in some embodiments, including embodiments in which color filter arrays and/or microlenses were not previously formed, a color filter array 85 may be formed on or applied to imager 10, over at least image sensing element 20 thereof. CFA 85 may be disposed upon imager 10 by known processes. Likewise, known processes may, if desired, be used to form or place a microlens 90 over image sensing element 20.

As at least some conductive lines 68, 72, 76 and external contacts 79 are carried by back side 16 of substrate 12, they may extend across locations that are opposite from image sensing element 20 and, thus are not confined to the periphery of imager 10. Consequently, electrical and other design constraints may be eased with back side integrated circuitry 80, while the overall size of the chip may be reduced relative to state-of-the-art imagers. Further, backside integrated circuitry 80 eliminates the additional processes and costs associated with fabricating conductive features, such as edge-bound conductive traces or TWIs or conductive vias, to reroute circuitry from above the active surface of an imager substrate to its back side.

Additionally, by placing such metallization on back side 16, in some embodiments, the features that are fabricated on active surface 14 of substrate 12 of imager 10 protrude only a small distance from active surface 14 (*e.g.,* about one-half micron or less in embodiments where no conductive lines extend over photocell capacitor 25 or imager transistors 30-45) and, thus, above image sensing element 20. When compared with the typical seven to ten microns that features of state-of-the-art imagers protrude from the active surfaces of the substrates of such imagers, the distance, or focal length F, between image sensing element 20 and any optical elements (*e.g.,* CFA 85, microlens 90, glass, lenses, filters, etc.) to be positioned thereover is significantly reduced. In some embodiments, the reduction in focal length F may be sufficient to eliminate the use of a microlens array over image sensing element 20. Accordingly, some embodiments of imagers 10 of the present invention neither include nor require microlenses.

While the foregoing description is limited to embodiments of photoimagers with contact openings that extend exclusively through the substrate, embodiments of photoimagers that additionally include contact openings that extend through features fabricated over the active surfaces thereof are also within the scope of the present invention.

With reference to FIG. 12, an electronic device 100 that includes a photoimager 10 according to embodiments of the present invention is depicted. Photoimager 10 is electrically connected to a carrier 102, such as a circuit board, that communicates with or carries other semiconductor devices 104, such as a processor, memory, and the like, as well as with a power source, input/output devices (*e.g.,* wired and wireless communications ports, etc.), a video display, and a variety of other devices

known in the art. In some embodiments, electronic device 100 may include one or more optical elements 106, such as glass, one or more lenses, filters, or the like. Without limiting the scope of the present invention, in specific embodiments, the electronic device 100 may comprise a camera, a cellular telephone, a personal digital assistant (PDA), a personal computer, or any other device into which a camera may be incorporated.

Although the foregoing description includes many specifics, these should not be construed as limiting the scope of the present invention but, merely, as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions and modifications to the invention as disclosed herein which fall within the meaning and scope of the claims are to be embraced thereby.

CLAIMS

What is claimed:

1. A method for fabricating an imaging device, comprising:

fabricating at least one image sensing element at an active surface of a fabrication substrate;

fabricating at least one transistor or at least one capacitor associated with the at least one image sensing element at the active surface of the fabrication substrate;

disposing an imperforate dielectric layer over the at least one transistor or capacitor; and

forming at least one contact opening through a back side of the fabrication substrate with the dielectric layer remaining imperforate.

2. The method of claim 1, wherein disposing the dielectric layer comprises disposing the dielectric layer to have a thickness of about a half a micron or less.

3. The method of claim 1, further comprising:

planarizing a surface of the imperforate dielectric layer.

4. The method of claim 3, wherein planarizing is effected before forming the at least one contact opening.

5. The method of claim 3, further comprising:

securing a planarized surface of the imperforate dielectric layer to a carrier.

6. The method of claim 5, wherein securing is effected before forming the at least one contact opening.

7. The method of claim 5, further comprising:

removing material from a back side of the fabrication substrate.

8. The method of claim 6, wherein removing material comprises grinding the back side of the fabrication substrate.

9. The method of claim 1, comprising fabricating at least one transistor and wherein forming the at least one contact opening comprises forming the at least one contact opening to extend to a source or drain of the at least one transistor or to a gate of the at least one transistor.

10. The method of claim 9, wherein fabricating the at least one transistor comprises fabricating at least one of a transfer gate, a reset gate, a source follower gate, and a row select gate associated with at least one photodiode of the array.

11. The method of claim 1, comprising fabricating a capacitor and wherein forming the at least one contact opening comprises forming the at least one contact opening to communicate with an electrode of the capacitor.

12. The method of claim 1, further comprising:
introducing conductive material into the at least one contact opening.

13. The method of claim 12, further comprising:
fabricating at least one laterally extending conductive element over the back side of the fabrication substrate and in communication with the conductive material in the at least one contact opening.

14. The method of claim 13, further comprising:
fabricating at least one contact adjacent to or in communication with the at least one laterally extending conductive element.

15. The method of claim 1, wherein fabricating the at least one image sensing element comprises fabricating an array of photodiodes in the active surface of the fabrication substrate.

16. A photoimager, comprising:

a substrate;

at least one image-sensing element at an active surface of the substrate;

at least one transistor in communication with the at least one image-sensing element on the active surface; and

at least one contact plug extending from an element of the at least one transistor, through the substrate, to a back side of the substrate.

17. The photoimager of claim 16, further comprising:

at least one laterally extending conductive element carried by the back side of the substrate and in communication with the at least one contact plug.

18. The photoimager of claim 17, further comprising:

at least one contact adjacent to and in communication with the at least one laterally extending conductive element.

19. The photoimager of claim 18, wherein at least one of the at least one laterally extending conductive element and the at least one contact is located at least partially beneath the at least one image-sensing element.

20. The photoimager of claim 16, further comprising:

a dielectric layer overlying the at least one transistor and the at least one image-sensing element.

21. The photoimager of claim 20, wherein the dielectric layer has a planar surface.

22. The photoimager of claim 20, wherein a distance between a surface of the dielectric layer and the active surface at which the at least one image-sensing element is located is at most about one half micron.

23. The photoimager of claim 22, lacking a microlens that corresponds to the at least one image-sensing element.

24. The photoimager of claim 20, wherein no contact openings are located in the dielectric layer.

25. An electronic device, comprising:

a carrier substrate including terminals in a pattern on a surface thereof; and

at least one photoimager according to any of claims 16 through 24.

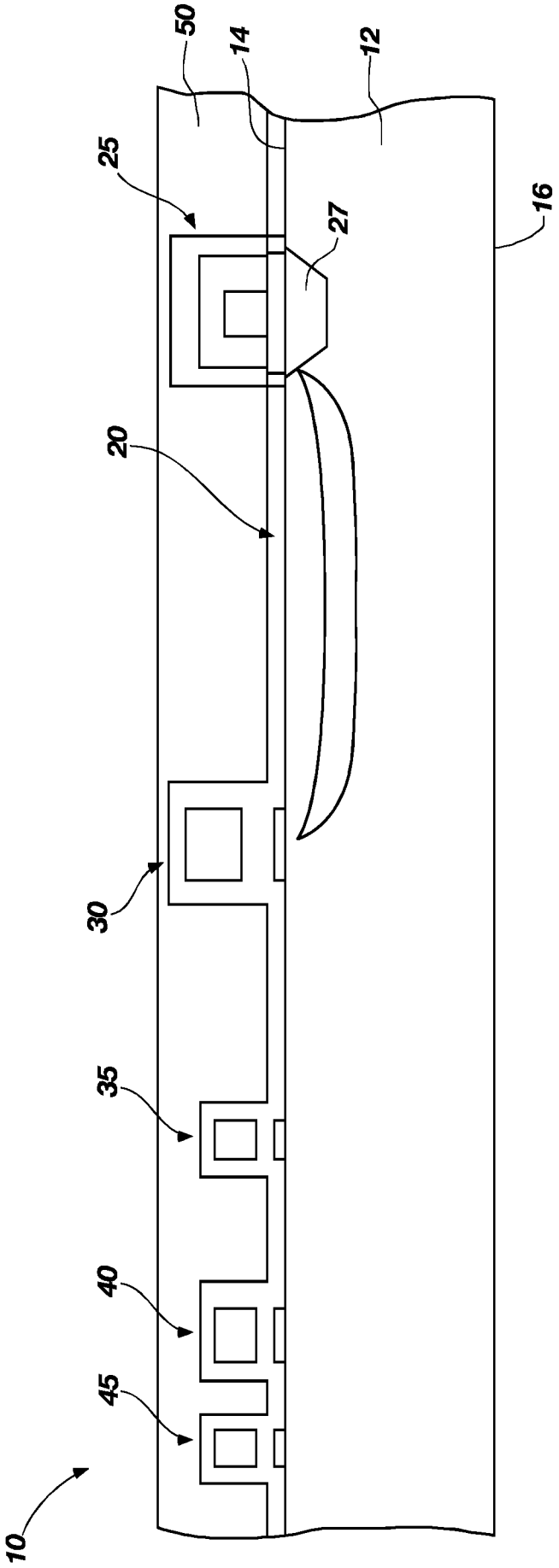


FIG. 1

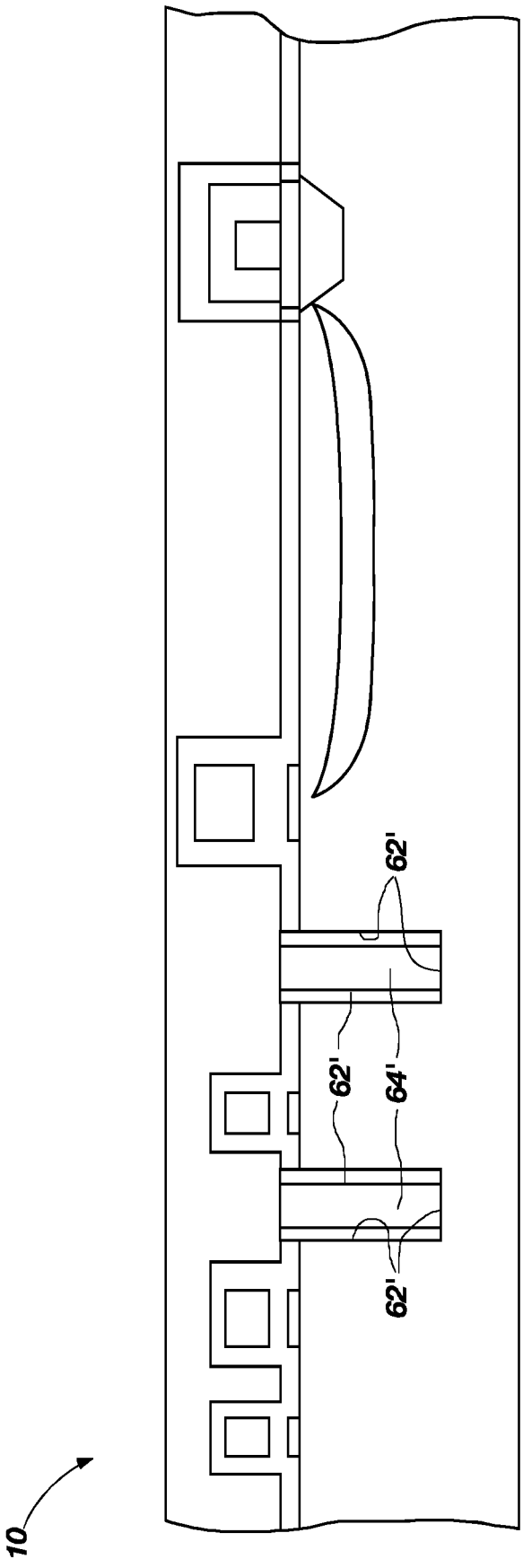


FIG. 1A

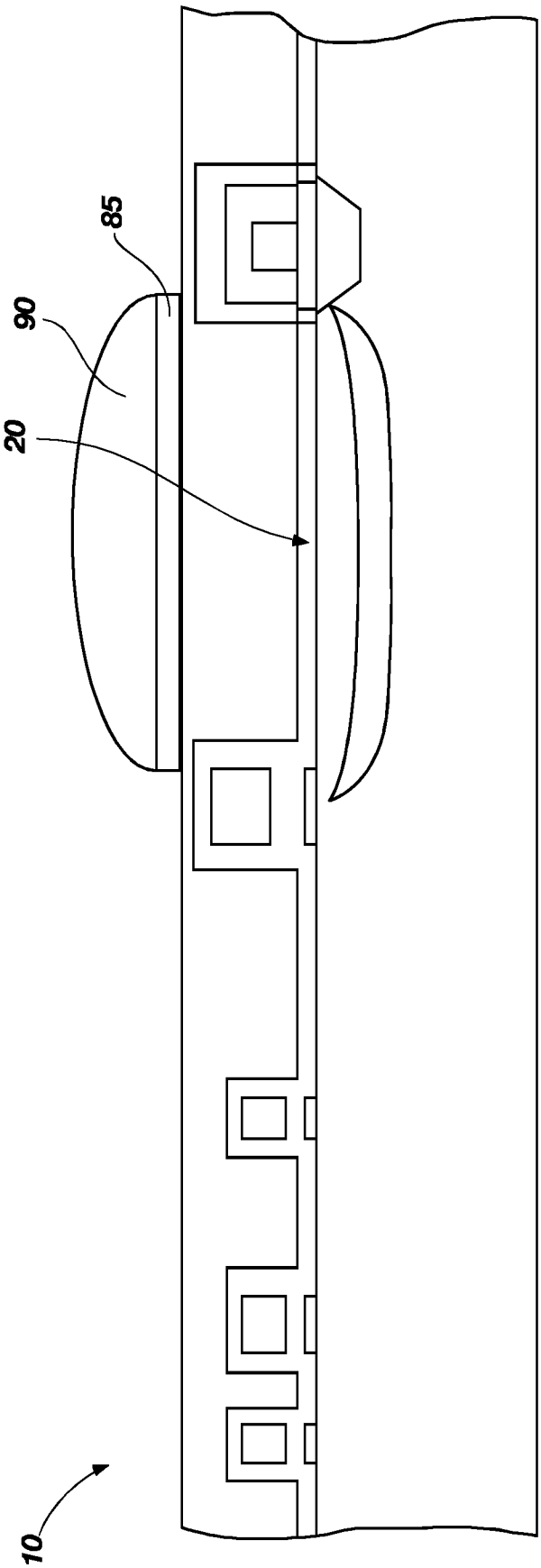


FIG. 1B

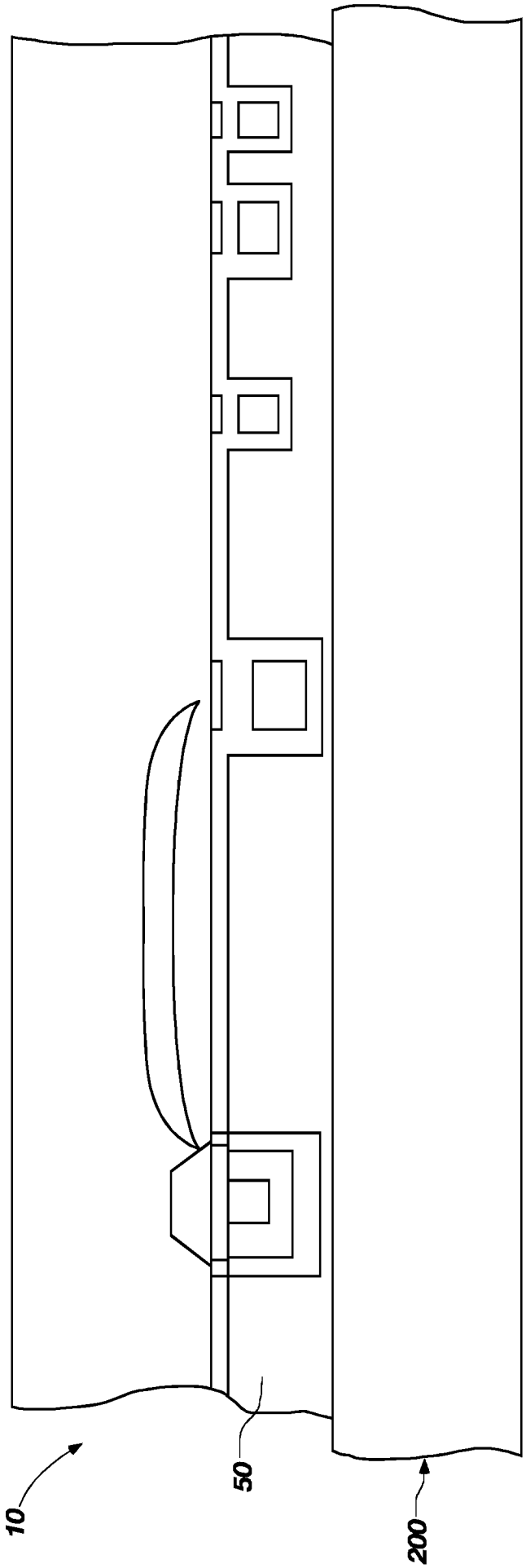


FIG. 2

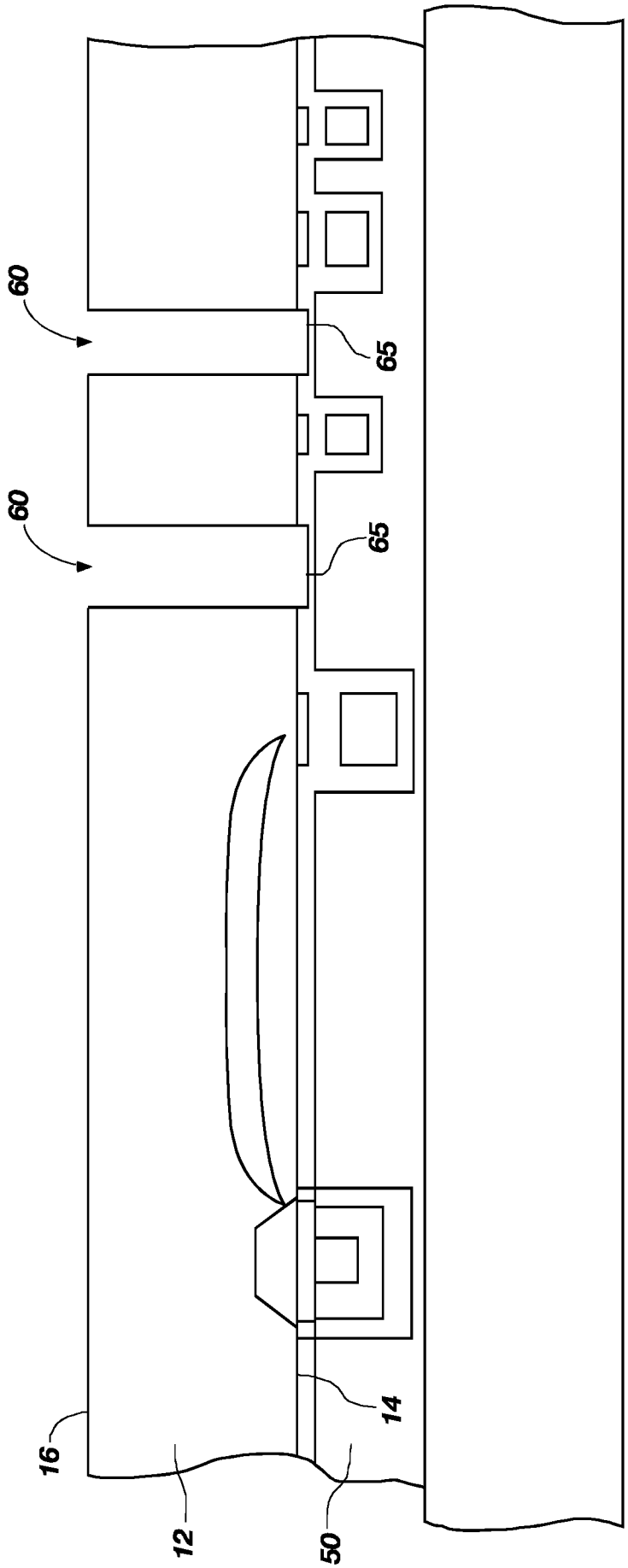


FIG. 3

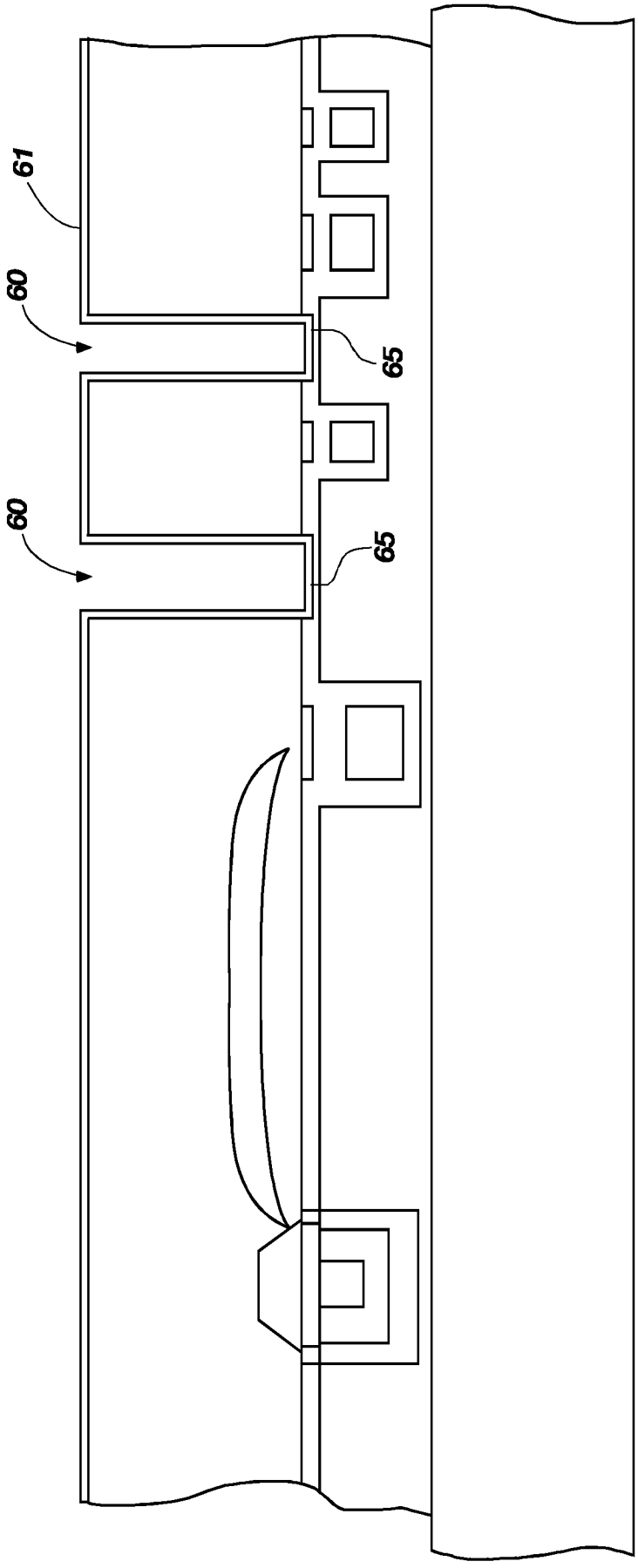


FIG. 4

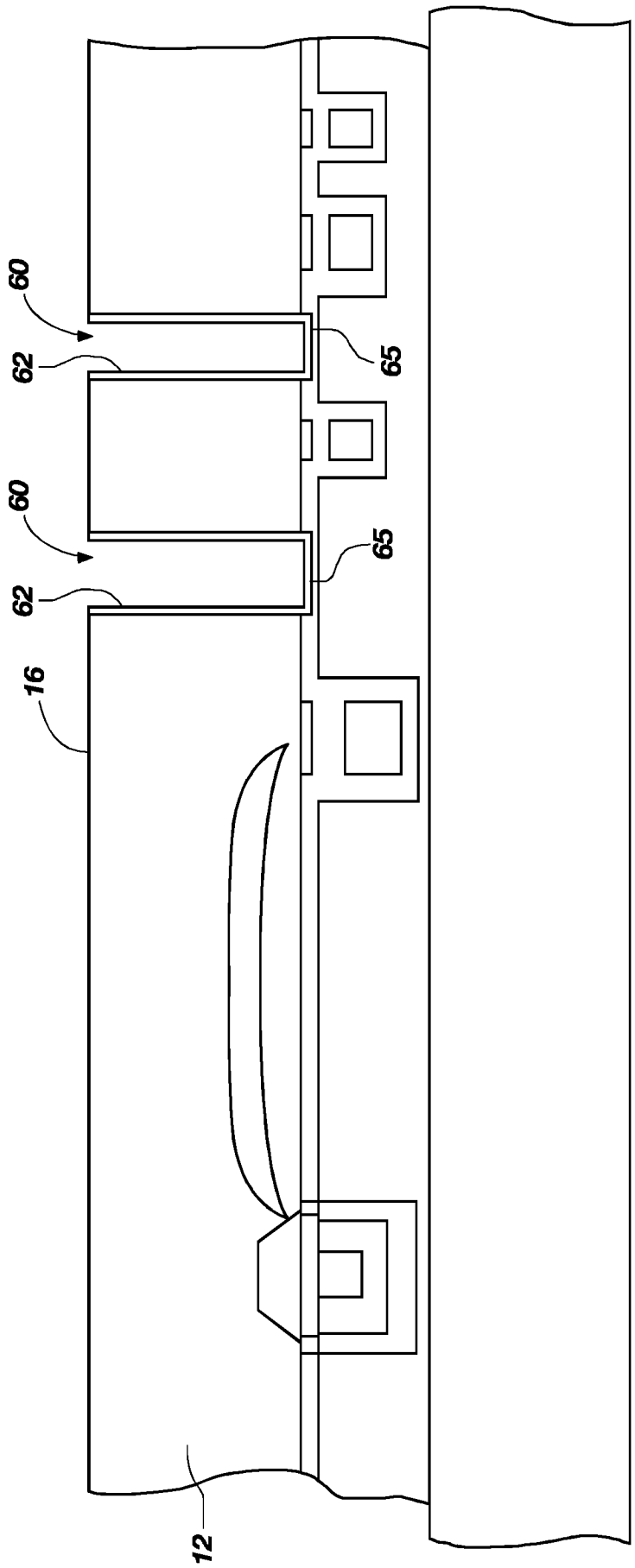


FIG. 5

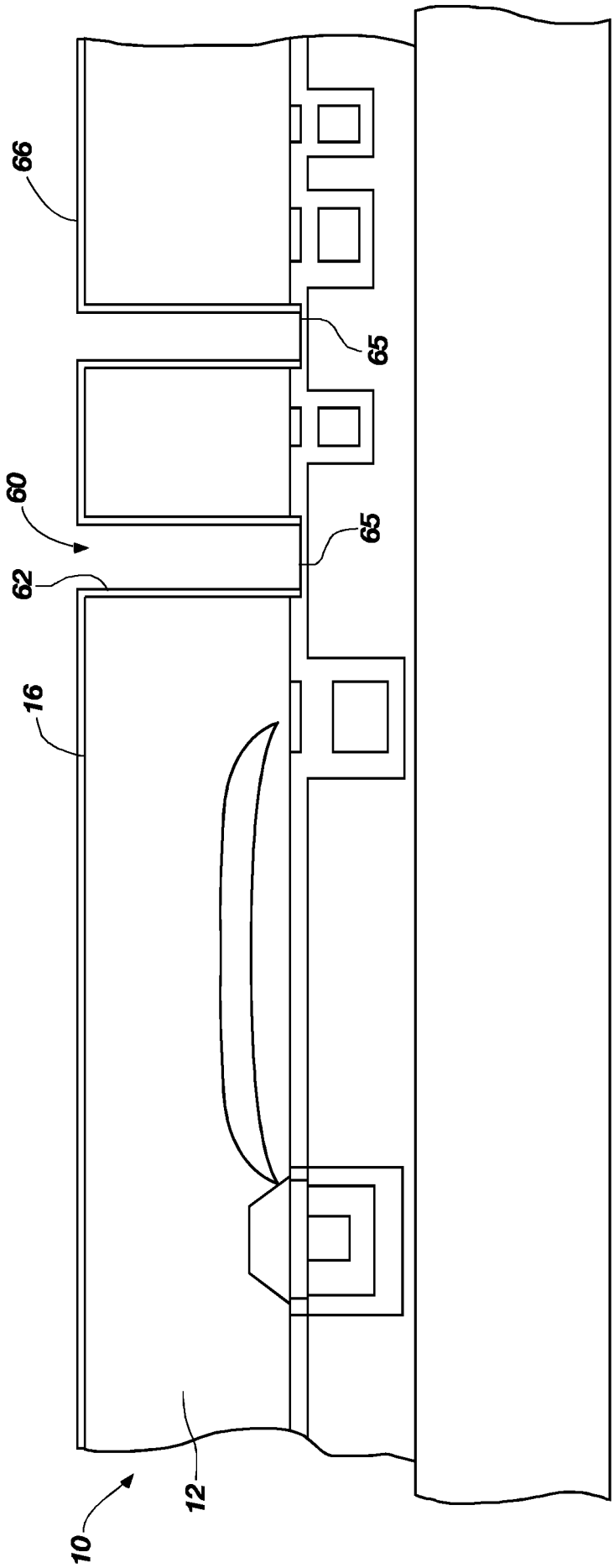


FIG. 6

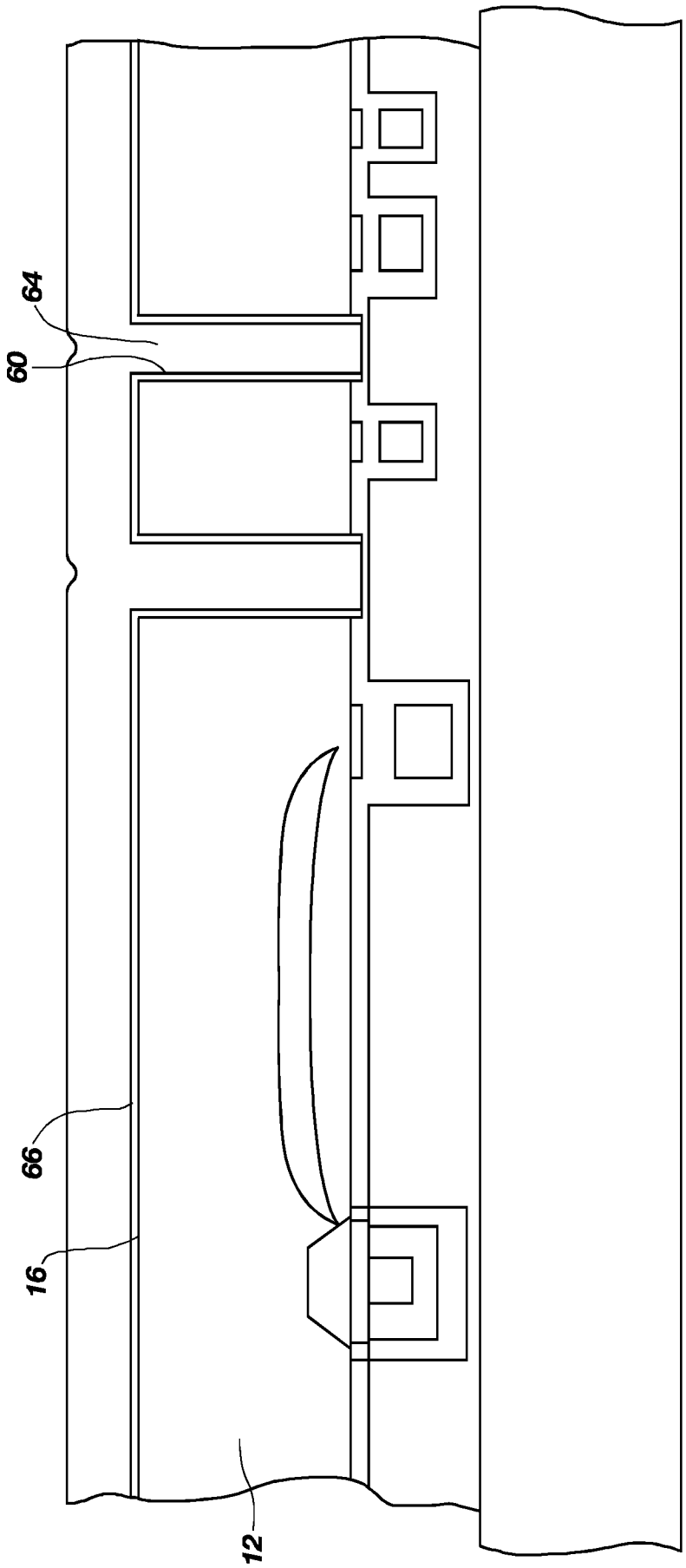


FIG. 7

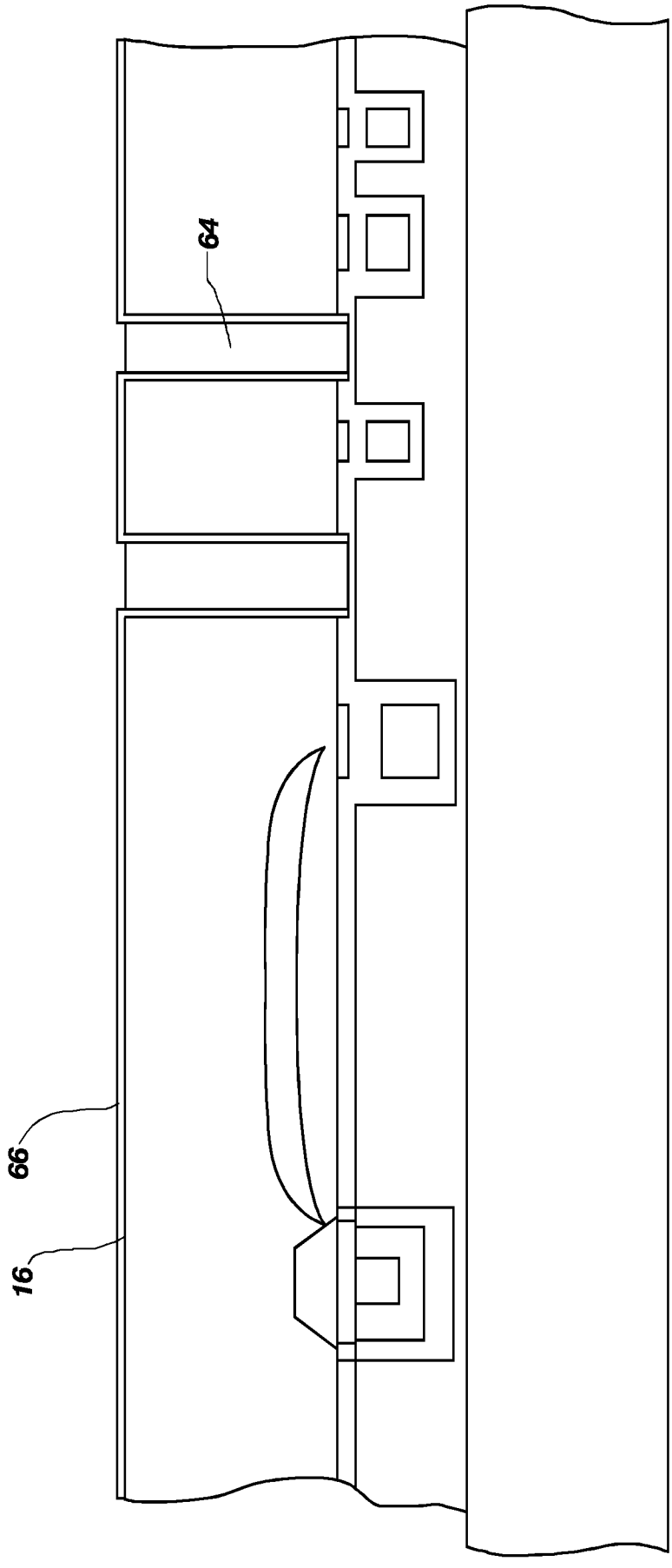


FIG. 8

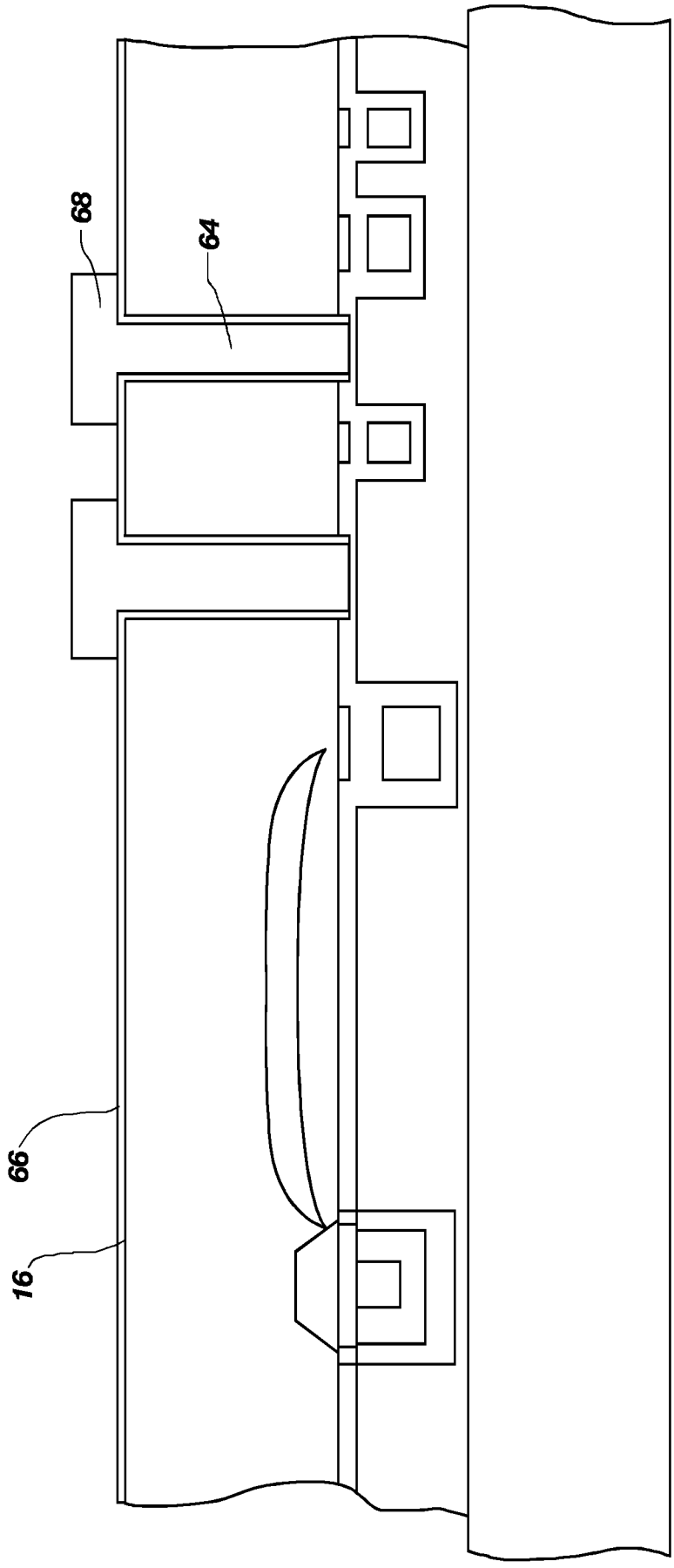


FIG. 9

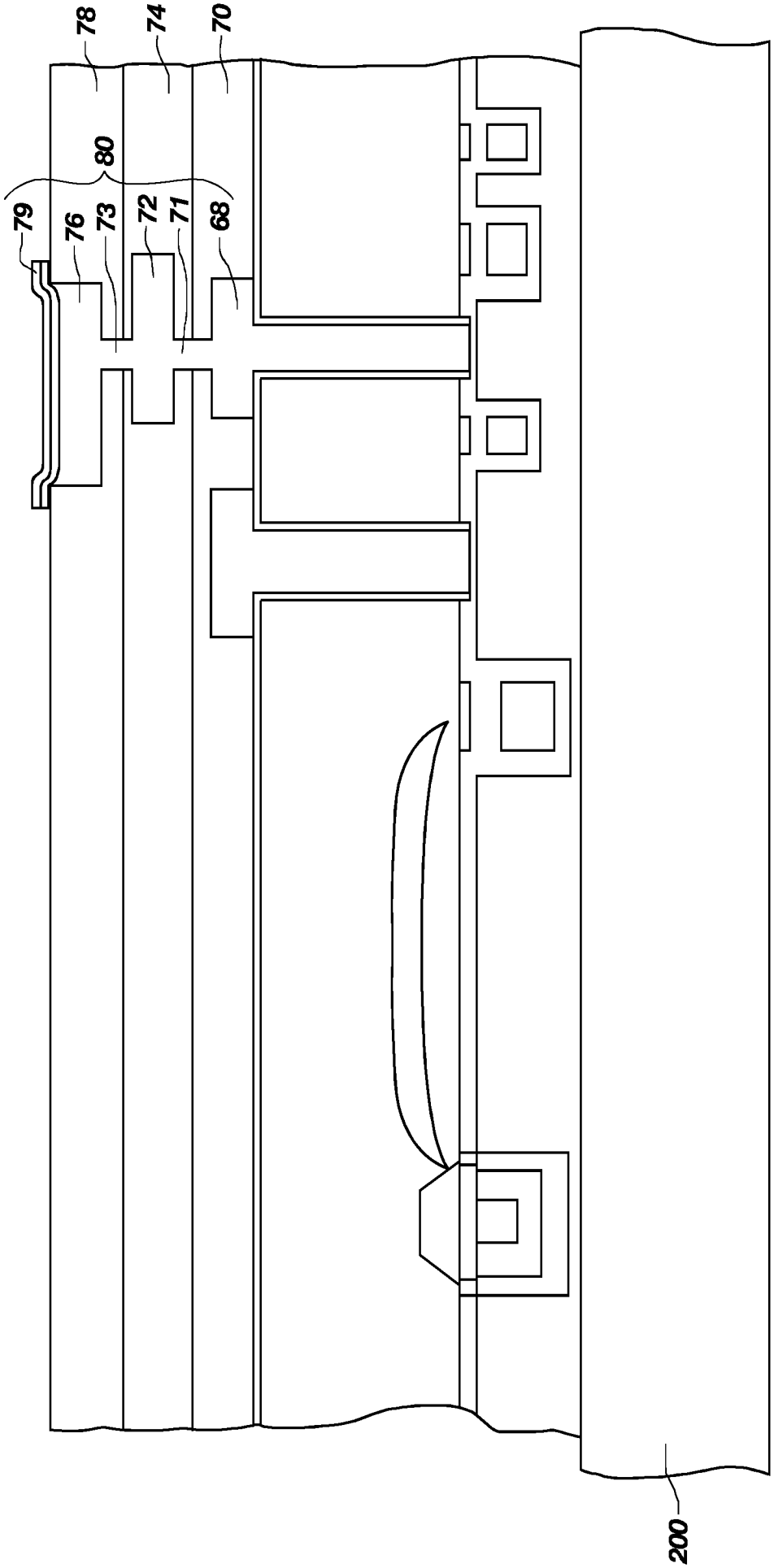


FIG. 10

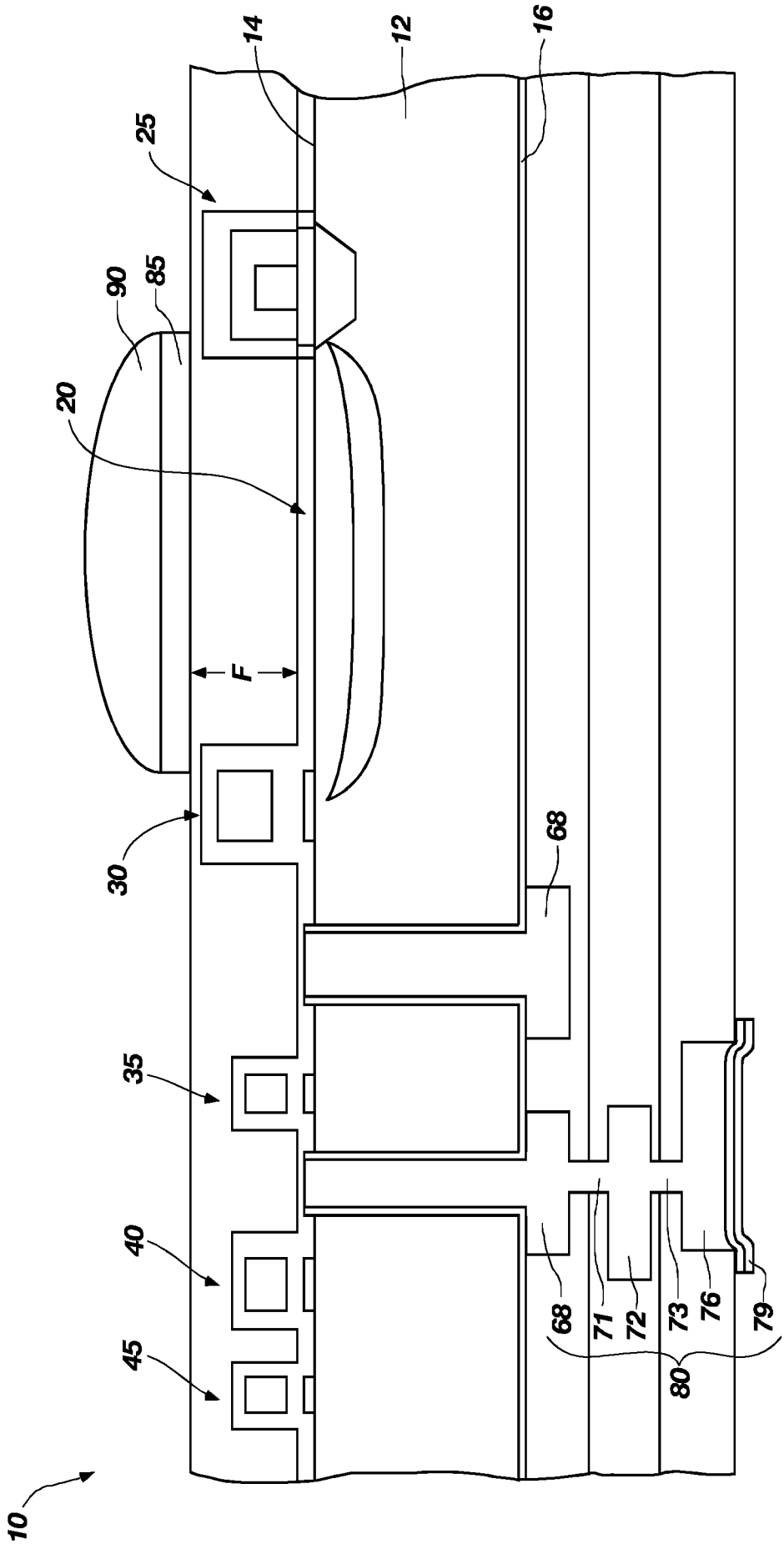


FIG. 11

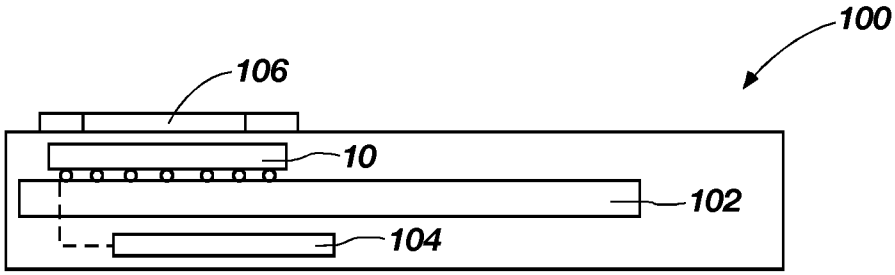


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/066489

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : H01L 27/146

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "imager","image","sensor","through","contact","fill-factor"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0052056 A1 (T. Doi et al.), 08 MARCH 2007 See the abstract, paragraphs [0021]-[0035], figures 1-3	1-25
A	US 6169319 B1 (Y. Malinovich et al.), 02 JANUARY 2001 See the abstract, column 8 line 64 - column 10 line 9, figure 5	1-25
A	US 2007-0007556 A1 (K. Shibayama), 11 JANUARY 2007 See the abstract, paragraphs [0045]-[0059], figure 1	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 OCTOBER 2008 (21.10.2008)	**21 OCTOBER 2008 (21.10.2008)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
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Facsimile No. 82-42-472-7140

Authorized officer

Kim, Young Jin

Telephone No. 82-42-481-5771

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2008/066489

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0052056 A1	08.03.2007	NONE	
US 6169319 B1	02.01.2001	US 6168965 B1	02.01.2001
US 2007-0007556 A1	11.01.2007	KR 10-2006-0064560 A US 7420257 B2	13.06.2006 02.09.2008