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(54) Title: SEED LAYERS FOR INTERCONNECTS AND METHODS AND APPARATUS FOR THEIR FABRICATION

(57) Abstract: One embodiment of the present invention is a method for making metallic interconnects including: (a) forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening; (b) depositing a barrier layer over the field and inside surfaces of the at least one opening; (c) depositing a first seed layer over the barrier layer using a first deposition technique; (d) depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and (e) electroplating a metallic layer over the second seed layer, the electroplated metallic layer including a material selected from a group consisting of Cu, Ag, or alloys including one or more of these metals.

Seed Layers for Interconnects and Methods and Apparatus for Their Fabrication

This is a continuation-in-part of a patent application entitled "Seed Layers for Interconnects and Methods for Their Fabrication" which was filed on October 2, 1999, Ser. No. 09/410,898.

Technical Field of the Invention

The present invention pertains to the field of electroplating metals or alloys for filling high aspect ratio openings, such as trenches and vias, for semiconductor metallization interconnects, thin film heads, or micromachined Microelectromechanical Systems (MEMS) devices. In particular, embodiments of the present invention provide improved seed layers for electroplating copper or silver interconnects in semiconductor devices, and methods and apparatus for fabricating such improved seed layers. The improved seed layers facilitate reliable, void-free filling of small openings with high aspect ratios for so called "Damascene" and "Dual Damascene" copper and/or silver interconnects.

Background of the Invention

As is well known in the prior art, filling trenches and/or vias formed on a wafer by electroplating copper metal to form semiconductor device interconnects (often referred to as a "Damascene" or a "Dual Damascene" process) requires that a metallization layer (often referred to in the art as a seed layer or a base layer) be formed over the wafer surface. As is also well known in the prior art, the seed layer is required: (a) to provide a low-resistance electrical path (to enables uniform electroplating over the wafer surface); (b) to adhere well to the wafer surface (usually to an oxide-containing a dielectric film such as SiO_2, SiO_X, or SiO_XN_Y); and (c) to be compatible with subsequent electroplating copper thereon.

As is well known, the requirement of providing a low-resistance electrical path is fulfilled by choosing the seed layer to be comprised of an adequately thick, low-resistivity material.

As is further well known, since copper has a rather poor adhesion to oxide surfaces, the requirement of adhering well to the wafer surface is typically fulfilled by disposing an intermediary barrier (or adhesion) metallic layer having a

strong affinity for oxygen atoms under the seed layer. As is well known in the prior art, the barrier metallic layer is formed prior to the seed layer to provide good adhesion: (a) to the oxide surface underneath it (the barrier layer provides good adhesion to the oxide surface by sharing oxygen atoms) and (b) to the seed layer above it (the barrier metallic layer provides good adhesion to the seed layer by metal to metal bonds). The barrier layer is often also referred to as an "adhesion layer" or a "liner". In addition to providing good adhesion, the barrier layer also serves to mitigate copper out-diffusion directly into the device, or indirectly (through an insulating or a dielectric layer) into the device. As is well known in the prior art, the barrier layer is usually chosen from the refractory metals or their alloys, such as for example, Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials.

As is still further well known, the requirement of being compatible with electroplating copper is fulfilled by choosing a seed layer that does not react spontaneously (i.e., by displacement) with copper electrolyte used during the electroplating. This is satisfied by requiring that the seed layer does not comprise a metal or alloy that is less noble than copper.

Typically, a seed layer comprises a copper layer that is deposited by a "dry" technique, such as by physical vapor deposition ("PVD"), including but not limited to sputtering, ion plating, or evaporation, or by chemical vapor deposition ("CVD"). However, the seed layer may also be deposited by a "wet" electroless plating process. In such cases, the copper seed layer thickness is typically in a range of about 300Å to about 2,000Å on the field (i.e., the top surface of the wafer outside trenches and via openings). In such cases, the barrier layer is typically deposited to a thickness of about 50Å to about 500Å (on the field) by either a PVD or a CVD technique.

The PVD techniques include, for example and without limitation, techniques such as evaporation, ion plating, and various sputtering techniques, such as DC and/or RF plasma sputtering, bias sputtering, magnetron sputtering, or Ionized Metal Plasma (IMP) sputtering. As is well known in the art, in general, due to their anisotropic and directional ("line of sight") nature, the PVD techniques produce non-conformal deposition. For a comprehensive description of sputtering techniques and

their applications, see for example an article entitled "Sputter Deposition Processes" by R. Parsons, pp. 177-208 in Thin Film Processes II, edited by J. L. Vosen and W. Kern, Academic Press (1991). However, some of the PVD techniques (such as ion plating) may produce, under certain conditions, a relatively more conformal deposition. For a comprehensive description of the ion plating technique and its applications, see for example an article entitled "The Cathodic Arc Plasma Deposition of Thin Films" by P. C. Johnson, pp. 209-285 in Thin Film Processes II, edited by J. L. Vosen and W. Kern, Academic Press (1991). The CVD techniques include, for example and without limitation, thermal CVD, Plasma Enhanced CVD ("PECVD"), Low Pressure CVD ("LPCVD"), High Pressure CVD ("HPCVD"), and Metallo Organic CVD ("MOCVD"). For a comprehensive description of CVD techniques and their applications, see for example an article entitled "Thermal Chemical Vapor Deposition" by K. F. Jensen and W. Kern, pp. 283-368 in Thin Film Processes II, edited by J. L. Vosen and W. Kern, Academic Press (1991). For example, one precursor used for CVD Cu is Cupraselect™, which precursor is sold by Schumacher, Inc. Another precursor is Cu(II) hexafluoroacetylacetonate. The latter can be reacted with hydrogen gas to obtain high purity copper. As is well known in the art, in general, due to their isotropic and non-directional nature, the CVD and the electroless techniques produce conformal deposition, with substantially uniform thickness over the entire surface, including over the field and the bottom and sidewall surfaces of the openings.

Aspect ratio ("AR") is typically defined as a ratio between a vertical dimension, D (depth), of an opening and its smallest lateral dimension, W (width, or diameter): AR = D/W. Usually, in electroplating metals or alloys to fill patterns having high aspect ratio openings (for example, in an insulator or a dielectric), the electroplating rate inside openings is slower than the rate outside openings (i.e., on the field). Further, the higher the AR of the openings, the slower the electroplating rate is inside. This results in poor or incomplete filling (voids) of high AR openings, when compared with results achieved with low AR openings. To overcome this problem in the prior art, commercial copper electrolytes contain additives that adsorb and locally inhibit (or suppress) growth outside the openings (i.e., on the field). Further, growth inhibition inside the openings is decreased from that achieved outside the openings due

to slow replenishment of the additives inside the openings as compared with replenishment of the additives on the field. As a result, the deposition rate inside the openings is faster than outside, thereby facilitating void-free copper fill. Other well known reasons for voids in copper electrofill include discontinuous (or incomplete coverage of) seed layers inside the openings, and pinching-off of opening walls (for example, by overhangs of the top corners) prior to plating.

The openings may consist of vias, trenches, or patterned photoresist. As is well known, in damascene or dual damascene processes, an insulating or a dielectric layer is pattern-etched to form openings therein. Next, a barrier (or an adhesion) metallic layer and a seed layer are deposited over the insulating layer to metallize its field (the surface surrounding openings), as well as the sidewalls and bottom surfaces of the openings. Next, copper electroplating is performed over the entire metallized surface, including the top surface (the field) surrounding the openings, and inside the patterned openings. Finally, excess plated copper overlying the openings and the top surface (the field) of the insulating layer, as well as the barrier and seed layers on the field, are removed, for example, by a mechanical polishing or by a chemical mechanical polishing ("CMP") technique. The end result is copper filled openings (trenches and vias), including bottom and sidewall surfaces lined by the barrier and seed layers. In today's most advanced copper filling processes for trenches and vias, the openings have ARs as high as 5:1 (D = 1.25μm; W = 0.25μm). Future trenches and vias openings will likely require W = 0.10 - 0.18μm, or narrower, and AR = 6:1 – 15:1, or larger.

As semiconductor device dimensions continue to shrink, there is an ever increasing demand for narrower interconnect cross-sections and, thus, smaller openings and larger aspect ratios (AR) during the copper electrofill. To ensure void-free copper filling, the seed layer inside the openings must completely cover the bottom and the sidewall surfaces inside the openings without discontinuities, or else there will be voids in the copper electrofill. On the other hand, the seed layer must not be so thick on the sidewalls that it pinches-off the very narrow openings and should not overhang the top corners of the openings so that it pinches-off the very small openings. Similarly, the barrier layer must also be continuous inside the openings. In contrast to

these requirements with respect to the openings, the seed layer must be sufficiently thick on the top surface (the field) to provide a low-resistive electrical path that facilitates uniform plating across the surface of the wafer. That is, the seed layer must be sufficiently thick (for example, a Cu seed layer should preferably be at least about 1,000Å) on the field to avoid radial non-uniformity across the wafer caused by a voltage (or IR) drop between a contact at the edge of the wafer to the center of the wafer. Any voltage drop (and resulting non-uniformity therefrom) becomes more severe as the resistance of the seed layer increases due to high resistivity and/or insufficient thickness. To ensure a sufficiently low-resistance seed layer, it is now common to deposit a copper seed layer to a thickness of about 1,000Å to about 2,000Å on the top surface (field) by a PVD technique. On the other hand, the typical thickness of about 300Å to about 1,000Å (on the field), deposited by the CVD techniques, may not be sufficient.

However, neither of these techniques satisfies all of the above-identified requirements. The non-conformal PVD techniques, while providing adequate thickness on the field, fail to provide continuous and complete step coverage inside very narrow openings with large AR. They also result in substantial overhangs at the top corners of the openings. The conformal CVD or electroless techniques, on the other hand, while providing continuous and complete step coverage of the seed layer inside very narrow openings, pinch-off the small openings when used at thicknesses required on the field for a low-resistance electrical path. As a result, typical conformal CVD or electroless seed layers are too thin on the field and too thick inside the very narrow openings.

As one can readily appreciate from the above, a need exists in the art for a method and apparatus to produce a continuous seed layer on the sidewalls and bottom of the openings, while maintaining sufficient thickness on the field to facilitate void-free copper electrochemical filling of very narrow openings having high aspect ratios.

Summary of the Invention

Embodiments of the present invention advantageously satisfy the above-identified need in the art and provide a method and apparatus to produce seed layers

used to produce void-free copper or silver electrochemical filling of small openings having high aspect ratios.

One embodiment of the present invention is a method for making metallic interconnects comprising: (a) forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening; (b) depositing a barrier layer over the field and inside surfaces of the at least one opening; (c) depositing a first seed layer over the barrier layer using a first deposition technique; (d) depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and (e) electroplating a metallic layer over the second seed layer, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

In another embodiment of the invention, a substantially conformal and a substantially non-conformal seed layers are deposited in a single tool, without breaking vacuum, or without exposing the wafer to the atmosphere between the deposition of the two seed layers. The single deposition tool may comprise two or more chambers, at least one chamber for the deposition of the conformal seed layer and at least another chamber for the deposition of the non-conformal seed layer.

In yet another embodiment, a single deposition tool comprises a single chamber in which both the conformal and the non-conformal seed layers are deposited utilizing either: (a) two or more distinct steps, wherein the deposition conditions (or parameters) during the first step are suitable for the deposition of a substantially conformal (or a non-conformal) seed layer and the deposition conditions during the second step are suitable for the deposition of a substantially non-conformal (or a conformal) seed layer, or (b) wherein the deposition conditions are varied continuously or gradually, thereby changing the nature of the seed layer from substantially conformal to substantially non-conformal, or vice versa, or (c) a combination of at least one distinct step and at least one gradual variation of the deposition conditions.

Brief Description of the Figures

FIG. 1 shows a cross-sectional view of an inventive structure formed in accordance with a preferred embodiment of the present invention wherein a first,

conformal seed layer is deposited over a barrier layer, followed by a second, non-conformal seed layer deposited over the first, conformal seed layer;

FIG. 2 shows a cross-sectional view of the inventive structure of FIG. 1 after removing excess plated copper or silver overlying an opening and the field, as well as removing the seed layers and barrier layer overlying the field surrounding the opening;

FIG. 3 shows a cross-sectional view of an inventive structure formed in accordance with an alternative embodiment of the present invention wherein a first, non-conformal seed layer is deposited over a barrier layer, followed by a second, conformal seed layer deposited over the first, non-conformal seed layer;

FIG. 4 shows a cross-sectional view of the inventive structure of FIG. 3 after removing excess plated copper or silver overlying an opening and the field, as well as removing the seed layers and barrier layer overlying the field surrounding the opening;

FIG. 5 shows a scanning electron microscope ("SEM") photograph of a cleaved cross-section (with a tilt angle of 30°) of a trench (the trench is ~0.10μm wide, ~1.4μm deep, and has an aspect ratio of ~14:1) having seed layers formed in accordance with one embodiment of the present invention;

FIG. 6 shows an SEM photograph of the trench shown in FIG. 5 without a tilt, and with a larger enlargement; and

FIG. 7 shows a schematic (not to scale) top view of a cluster tool apparatus, and a frontal view of its controller (e.g. computer), in accordance with a preferred embodiment of the invention.

Detailed Description

FIG. 1 shows a cross-sectional view of an inventive structure formed in accordance with a preferred embodiment of the present invention wherein a first, conformal seed layer is deposited over a barrier layer, followed by a second, non-conformal seed layer deposited over the first, conformal seed layer. The conformal seed layer provides continuous and complete step coverage inside the openings, while the non-conformal seed layer provides a low resistance electrical path over the top surface (field) surrounding the openings to enable uniform plating across the substrate

(or wafer). To enable the uniform plating, it is preferable that the thickness of the combined seed layers be at least about 1,000Å on the field.

In accordance with the preferred embodiment of the inventive method of the present invention, barrier layer 18 is deposited over the entire surface of wafer 10, including over patterned insulating layer 12 (having had opening 16 patterned therein in accordance with any one of a number of methods that are well known to those of ordinary skill in the art), using a conformal Chemical Vapor Deposition ("CVD") technique. Although the term barrier layer is used, it should be understood by those of ordinary skill in the art that the term barrier layer includes examples wherein: (a) the barrier layer acts both as an adhesion layer and as a barrier layer; (b) a barrier layer separate from an adhesion layer is used; and (c) a multiplicity of layers is used, some acting as adhesion layers, some acting as barrier layers, or some acting as both. Further, although the term wafer is used, this also includes the term substrate as it is used in the art. Still further, although the present invention is described in the context of opening 16, in practice, a multiplicity of openings are patterned and filled in accordance with the present invention.

Advantageously, in accordance with the present invention, the use of a CVD technique to deposit barrier layer 18 ensures substantially complete and continuous coverage of the bottom and sidewall surfaces inside opening 16. However, it is within the scope of the present invention that barrier layer 18 may also be deposited using a Physical Vapor Deposition ("PVD") technique that provides continuous bottom and sidewall coverage. In accordance with the present invention, barrier layer 18 may comprise, for example and without limitation, a material selected from Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials. Further, the thickness of barrier layer 18 can be in a range of about 30Å to about 500Å, and more preferably in a range of about 50Å to about 300Å. Since barrier layer 18 occupies a certain fraction of interconnects formed in accordance with the present invention, and since barrier layer 18 has a relatively large resistivity, its thickness should be minimized. However, the thickness of barrier layer 18 should be sufficiently large to mitigate copper out-diffusion and to provide complete bottom and

sidewall coverage inside opening 16. Many CVD techniques and PVD techniques are well known to those of ordinary skill in the art for forming barrier layer 18.

Next, conformal seed layer 20 is deposited over barrier layer 18. Conformal seed layer 20 can be preferably deposited by using a CVD technique, but it can also be deposited by using an electroless technique or any other substantially conformal deposition technique. Many CVD techniques and electroless techniques are well known to those of ordinary skill in the art for forming conformal seed layer 20. The thickness of conformal seed layer 20 can be in a range of about 50Å to about 500Å, and more preferably in a range of about 100Å to about 300Å. Finally, non-conformal seed layer 22 is deposited over conformal seed layer 20. Non-conformal seed layer 22 can be preferably obtained using a PVD technique. Many PVD techniques are well known to those of ordinary skill in the art for forming non-conformal seed layer 22. The thickness of non-conformal seed layer 22 can be in a range of about 100Å to about 3,000Å, and more preferably in a range of about 500Å to about 1,800Å (in the field).

In accordance with the present invention, the conformal and non-conformal seed layers may comprise the same material, or they may comprise different materials. Although copper is commonly used as a seed layer, a highly conductive silver (Ag) layer can also be used. In fact, Ag has lower resistivity than that of Cu and, therefore, can be formed with a smaller thickness than that required when using Cu. Thus, conformal seed layer 20 and non-conformal seed layer 22 may comprise, for example, a material selected from Cu, Ag, or alloys comprising one or more of these metals.

Due to the non-directional, isotropic nature of CVD deposition techniques, the thickness of the CVD layers is substantially uniform over the entire surface (i.e., conformal), including over field 14, and over bottom and sidewall surfaces inside opening 16. In reality, however, even the best conformal CVD layers are thicker over the field than inside the openings. In fact, it is quite common for CVD Cu seed layers inside openings to have a thickness of about 80% of that over the field. In addition, the thickness of a CVD barrier layer inside the openings is typically only

about 50% of that over the field. Thus, even the best CVD layers exhibit some overhang at the top corners of the openings.

Example 1

The following presents an example of a preferred embodiment of the inventive method for 0.18μm wide vias or trenches. In accordance with the preferred embodiment, one deposits, by a CVD technique, a barrier layer comprised of about 200Å of TaN_X or WN_X, then one deposits, by a CVD technique, a conformal seed layer comprised of about 300Å of Cu, finally one deposits, by a PVD technique, a non-conformal seed layer comprised of about 900Å of Cu (as measured on the field). This will result in a total combined (including the barrier) thickness of about 400Å inside the openings: {Cu(PVD~50Å)/Cu(CVD~250Å)/TaN_X(CVD~100Å)} and a total combined Cu seed layer and barrier layer thickness of about 1,400Å on the field: {Cu(PVD~900Å)/Cu(CVD~300Å)/TaN_X(CVD~200Å}. Advantageously, in accordance with the present invention, the inventive "two-step" seed layer deposition ensures a continuous seed layer having excellent step coverage, and a low-resistance electrical path on the field to ensure uniform copper plating across the wafer. It may be noted that although the combined thickness of the copper seed layers inside the openings is only about 300Å, due to the very short distance to the field (typically about 1μm), a voltage drop from the field to the inside of the openings is negligible. Thus, the thickness of the "two-step" seed layer inside the openings is adequate for copper plating therein. In fact, if necessary, the thickness of the "two-step" seed layer inside the openings can be further decreased (to a range from about 100Å to about 200Å) to enable void-free copper filling of even smaller openings (for example, below 0.10 - 0.13μm). In the above example, the combined thicknesses of the barrier and seed layers at the sidewalls of the openings is about 400Å on each side, thus occupying about 800Å of the 1,800Å opening. This leaves enough room (~1,000Å) to facilitate electroplating inside the opening without sealing or pinching-off of the top corners.

After depositing seed layers 20 and 22 shown in FIG. 1, substrate 10 is placed in a copper electroplating bath, and electroplating is carried out in accordance with any one of a number of methods that are well known to those of ordinary skill in the art to deposit a thickness of copper sufficient to fill patterned opening 16, with

some excess, and to cover field 14 surrounding opening 16. Finally, excess plated copper overlying opening 16 and overlying field 14, as well as seed layers 20 and 22 and barrier layer 18 overlying field 14, are removed using any one of a number of techniques that are well known to those of ordinary skill in the art, for example, using a mechanical polishing or a chemical mechanical polishing (CMP) technique. Other removal techniques, such as wet or dry etching techniques may also be used to remove excess plated copper overlying opening 16 and field 14, and to remove seed layers 20 and 22 and barrier metallic layer 18 overlying field 14. It should be clear to those of ordinary skill in the art that removal may also be accomplished using a combination of techniques, including those identified above.

Although the detailed description above refers to filling opening 16 by electroplating copper, it is within the scope of the present invention to electrofill opening 16 with any low resistivity material, such as a material selected from Cu, Ag, or an alloy comprising one or more of these metals. In fact, silver (Ag) has lower resistivity than that of Cu, and may be attractive for further reducing the dimensions of the interconnects.

FIG. 2 shows a cross-sectional view of the inventive structure of FIG. 1 after removing excess plated copper (or silver) 24 overlying opening 16 and field 14, and removing seed layers 20 and 22 and barrier layer 18 overlying field 14 surrounding opening 16. FIG. 2 illustrates the filling of openings (trenches and vias) with electroplated copper (or silver) 24, as well as the lining of the bottom and sidewall surfaces of opening 16 by barrier layer 18 and seed layers 20 and 22. As shown in FIG. 2, all metallic layers were removed from field 14 of insulating layer 12 which surrounds embedded electroplated copper (or silver) interconnect 24.

FIG. 3 shows a cross-sectional view of an inventive structure formed in accordance with an alternative embodiment of the present invention wherein a first, non-conformal seed layer is deposited over a barrier layer, followed by a second, conformal seed layer deposited over the first, non-conformal seed layer. The non-conformal seed layer provides a low resistance electrical path over the top surface (field) surrounding the openings to enable uniform plating across the substrate (or

wafer), while the conformal seed layer provides continuous and complete step coverage inside the openings.

In accordance with the alternative embodiment of the inventive method of the present invention, barrier layer 118 is deposited over the entire surface of wafer 110, including over patterned insulating layer 112 (having had opening 116 patterned therein in accordance with any one of a number of methods that are well known to those of ordinary skill in the art), using a conformal Chemical Vapor Deposition ("CVD") technique. Although the term barrier layer is used herein, it should be understood by those of ordinary skill in the art that the term barrier layer includes examples wherein: (a) the barrier layer acts both as an adhesion layer and as a barrier layer; (b) a barrier layer separate from an adhesion layer is used; and (c) a multiplicity of layers is used, some acting as adhesion layers, some acting as barrier layers, or some acting as both. Further, although the term wafer is used, this also includes the term substrate as it is used in the art. Still further, although the present invention is described in the context of opening 116, in practice, a multiplicity of openings are patterned and filled in accordance with the present invention.

Advantageously, in accordance with the present invention, the use of a CVD technique to deposit barrier layer 118 ensures complete and continuous coverage of the bottom and sidewall surfaces inside opening 116. However, it is within the scope of the present invention that barrier layer 118 may also be deposited using a Physical Vapor Deposition ("PVD") technique that provides continuous bottom and sidewall coverage. In accordance with the present invention, barrier layer 118 may comprise, for example and without limitation, a material selected from Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials. Further, the thickness of barrier layer 118 can be in a range of about 30Å to about 500Å, and more preferably in a range of about 50Å to about 300Å. Since barrier layer 118 occupies a certain fraction of interconnects formed in accordance with the present invention, and since barrier layer 118 has a relatively large resistivity, its thickness should be minimized. However, the thickness of barrier layer 118 should be sufficiently large to mitigate copper out-diffusion and to provide complete bottom and

sidewall coverage inside opening 116. Many CVD techniques and PVD techniques are well known to those of ordinary skill in the art for forming barrier layer 118.

Next, non-conformal seed layer 126 is deposited over barrier layer 118. Non-conformal seed layer 126 can be preferably obtained using a PVD technique. Many PVD techniques are well known to those of ordinary skill in the art for forming non-conformal seed layer 126. The thickness of non-conformal seed layer 126 can be in a range of about 100Å to about 3,000Å, and more preferably in a range of about 500Å to about 1,800Å (on the field). Finally, conformal seed layer 128 is deposited over non-conformal seed layer 126. Conformal seed layer 128 can be preferably obtained using a CVD or electroless technique or any other substantially conformal deposition technique. Many CVD techniques and electroless techniques are well known to those of ordinary skill in the art for forming conformal seed layer 128. The thickness of conformal seed layer 128 can be in a range of about 50Å to about 500Å, and more preferably in a range of about 100Å to about 300Å.

In accordance with the present invention, the conformal and non-conformal seed layers may comprise the same material, or they may comprise different materials. Although copper is commonly used as a seed layer, a highly conductive silver (Ag) layer can also be used. Non-conformal seed layer 126 and conformal seed layer 128 may comprise, for example, a material selected from Cu, Ag, or alloys comprising one or more of these metals.

After depositing seed layers 126 and 128 shown in FIG. 3, substrate 110 is placed in a copper electroplating bath, and electroplating is carried out in accordance with any one of a number of methods that are well known to those of ordinary skill in the art to deposit a thickness of copper sufficient to fill patterned opening 116, with some excess, and to cover field 114 surrounding opening 116. Finally, excess plated copper overlying opening 116 and field 114 of insulating layer 112, as well as seed layers 126 and 128 and barrier layer 118 overlying field 114, are removed using any one of a number of techniques that are well known to those of ordinary skill in the art, for example, using a mechanical polishing or a chemical mechanical polishing (CMP) technique. Other removal techniques, such as wet or dry etching techniques may also be used to remove excess plated copper overlying opening 116 and field 114, and to

remove seed layers 126 and 128 and barrier layer 118 overlying field 114. It should be clear to those of ordinary skill in the art that removal may also be accomplished using a combination of techniques, including those identified above.

Although the detailed description above refers to filling opening 116 by electroplating copper, it is within the scope of this invention to electrofill opening 116 with any low resistivity material, such as a material selected from Cu, Ag, or alloys comprising one or more of these metals. In fact, silver (Ag) has lower resistivity than that of Cu, and may be attractive for further reducing the dimensions of the interconnects.

FIG. 4 shows a cross-sectional view of the inventive structure of FIG. 3 after removing excess electroplated copper (or silver) 130 overlying opening 116 and field 114, and removing seed layers 126 and 128 and barrier layer 118 overlying field 114 surrounding opening 116. FIG. 4 illustrates the filling of openings (trenches and vias) with electroplated copper (or silver) 130, as well as the lining of the bottom and sidewall surfaces of opening 116 by barrier layer 118 and seed layers 126 and 128. As shown in FIG. 4, all metallic layers were removed from field 114 of insulating layer 112 which surrounds embedded electroplated copper (or silver) interconnect 130.

Example 2

FIGs. 5 and 6 show scanning electron microscope ("SEM") photographs of a cross-section of a 0.10 μm wide trench having a Cu seed layer prepared in accordance with a preferred embodiment of the invention. In accordance with this embodiment, a pattern of trenches was formed in a SiO_2 insulating layer. The trenches were about 0.10 μm wide and about 1.4 μm deep (thereby having an aspect ratio of about 14:1). Next, a barrier layer (WN_X) was deposited using a CVD technique. Next, a relatively thin, conformal Cu seed layer was deposited using a CVD technique. The barrier layer and thin, conformal Cu seed layer is seen at 501 in FIG. 6. In accordance with this embodiment, the combined thickness of the barrier and the CVD Cu seed layer was about 500Å on the field, and about 400-500 Å on the sidewalls and bottom of the trenches. Next, a non-conformal PVD Cu seed layer having a thickness of about 1,400 Å (on the field) was deposited by sputtering. In this embodiment, the non conformal PVD Cu seed layer was applied in two steps and is seen at 510 in FIG. 6.

The end result, as shown in FIGs. 5 and 6, was a combined thickness (including the barrier and the Cu seed layers) of only about 400-500Å on the sidewalls and bottom of the trench (with excellent continuity and uniformity there), and about 1,900Å on the field, without pinching-off of the trench. One should note that, while FIG. 5 shows the cross-section with a tilt of about 30° and an enlargement of 20,000X (thus providing also a partial view of the top surface), FIG. 6 shows the same cross-section with an enlargement of 40,000X and without a tilt.

Example 3

Similar to Example 2 above, trenches ~0.10 μm wide and ~1.4 μm deep (thereby having an aspect ratio of ~14:1) were formed in a SiO_2 insulating layer. Next, a barrier layer (WN_X) was deposited using a CVD technique. Next, a relatively thin, conformal Cu seed layer was deposited using a CVD technique. The combined thickness of the barrier layer and the CVD Cu layer was ~500 Å on the field, and ~400-500 Å on the sidewalls and bottom of the trenches. Next, a non-conformal PVD Cu seed layer having a thickness of ~500 Å (on the field) was deposited by sputtering. The end result was a combined thickness (including the barrier layer and the Cu seed layers) of only about 400-500 Å on the sidewalls and bottom of the trenches (with excellent continuity and uniformity), and about 1,000 Å on the field, without pinching-off the trenches.

It should be understood that the scope of the present invention is not limited to the embodiments described above with respect to FIG. 1 and FIG. 3. For example, in accordance with further embodiments of the present invention, a relatively thin ("Flash") PVD seed layer can be deposited first, followed by a conformal CVD or electroless seed layer, and finally followed by a (relatively thick) PVD seed layer to produce three separately deposited seed layers.

Adhesion of a metallo-organic CVD (MOCVD) deposited Cu seed layer to underlying barrier layer is rather poor, and may not be adequate for use in devices when chemical mechanical polishing (CMP) processing follows Cu plating. In addition, when an MOCVD Cu layer is deposited directly over a barrier layer containing a refractory metal, further problems arise. In particular, the morphology, uniformity, and electrical resistivity of the MOCVD Cu layer may not be adequate for

use in devices. It is believed that these problems are due to the high affinity of the refractory metal in the barrier layer to oxygen and/or carbon atoms. Specifically, during the initial stages of MOCVD Cu deposition, the refractory metal of the barrier layer spontaneously reacts with carbon or oxygen containing species (from the organic part of the metallo-organic compound) to form an oxide, carbide, or a mixed oxide-carbide interfacial layer between itself and the depositing Cu. Such an intermediate layer adversely impairs the adhesion of the MOCVD Cu layer. Cu (as well as other noble metals) does not adhere well to oxide or carbide layers, and requires a clean metal-to-metal bond in order to adhere well to another metal. Similarly, the oxide, carbide, and/or oxide-carbide interfacial layer impairs proper nucleation of the MOCVD Cu on the refractory metal barrier layer. This adversely affects the morphology, uniformity, and resistivity of the deposited MOCVD Cu seed layer.

In accordance with one embodiment of the present invention, at least an initial stage of CVD Cu deposition is carried out utilizing high purity, inorganic Cu compounds (precursors), such as, for example and without limitation, chlorides or fluorides, which do not contain oxygen or carbon atoms. The resulting clean metal-to-metal interface between a barrier layer containing a refractory metal and the depositing copper ensures good adhesion, morphology, uniformity, and low electrical resistivity of the CVD Cu layer. In a further embodiment, the entire CVD Cu layer can be deposited using the inorganic precursors. In a still further embodiment, only the initial stage of the CVD Cu is carried out using inorganic precursors, switching later to an MOCVD Cu deposition process, to form the rest of the CVD Cu layer.

In accordance with a still further embodiment of the present invention that solves the problems involved with the deposition of an MOCVD Cu layer on a barrier layer containing a refractory metal, a first, relatively thin, "Flash" PVD seed layer is deposited to enhance adhesion to the barrier layer and/or to improve grain morphology and uniformity of a subsequently deposited CVD seed layer.

Exposure of wafers to the atmosphere during transport from one deposition chamber to another may cause deleterious oxidation and/or contamination of the surface of barrier and/or seed layers. Such exposure should, therefore, be avoided or minimized.

In accordance with one embodiment of the present invention, conformal and non-conformal seed layers are deposited in an apparatus where the conformal and non-conformal seed layer deposition steps can be carried out without breaking vacuum, or without exposing the wafer to the atmosphere between the deposition steps. In accordance with this embodiment, the apparatus may comprise two or more chambers, at least one chamber for deposition of the conformal seed layer, and at least another chamber for deposition of the non-conformal seed layer. In a preferred embodiment of the present invention, the apparatus further comprises a chamber for deposition of the barrier layer, preferably by a CVD technique. The barrier layer may be deposited in a separate chamber or it may be deposited in one of the chambers used to deposit either the conformal, or the non-conformal, seed layers.

FIG. 7 shows apparatus 7000 that is fabricated in accordance with a preferred embodiment of the invention. As shown in FIG. 7, apparatus 7000 comprises cluster tool 70 which operates in accordance with input from controller 80 in a manner that is well known to those of ordinary skill in the art. As further shown in FIG. 7, cluster tool 70 includes input loadlock 71 and output loadlock 72. As is well known to those of ordinary skill in the art, loadlocks 71 and 72 enable wafers to be inserted into and removed from cluster tool 70, respectively. Although FIG. 7 shows separate input and output loadlocks, it is also within the spirit and scope of the present invention to use a single loadlock for both input and output of wafers.

As is well known to those of ordinary skill in the art, once wafer 74 is inserted into transfer chamber 73 of cluster tool 70, it can be transferred between the various processing chambers (for example, processing chambers 75-79) without breaking vacuum, or without exposure to the atmosphere. As is shown in FIG. 7, cluster tool 70 comprises CVD barrier layer deposition chamber 76, PVD Cu seed layer deposition chamber 77, and CVD Cu seed layer deposition chamber 78. In addition, FIG. 7 shows several other processing, for example, processing chambers 75 and 79, which can be used for other processing steps that are well known to those of ordinary skill in the art, such as pre-cleaning, cooling, or as extra deposition chambers. Although FIG. 7 shows separate CVD chambers for depositing a barrier layer and Cu

seed layers, it is also within the scope of the invention to deposit both types of layers in the same CVD chamber.

Controller 80 is apparatus which is well known to those of ordinary skill in the art that is used to control the operation of cluster tool 70. As such, controller 80 determines the sequence and duration of movements and stays of wafer 74: (a) to and from loadlocks 71 and 72; and (b) to and from the various processing chambers 75-79. As is also well known to those of ordinary skill in the art, controller 80 controls the specific process sequence and process parameters for operation of the various ones of processing chambers 75-79, sometimes referred to in the art as "recipes." For example, in PVD Cu seed layer deposition chamber 77, among other things, controller 80 controls the duration of the sputter deposition, the background pressure, the sputtering gas (such as Argon) pressure and flow rate, the cathodic voltage and power, and/or bias voltage applied to the wafer. Lastly, as is also well known to those of ordinary skill in the art, controller 80 performs these functions in accordance with specific recipes which are data structures that dictate the operation of controller 80 software. The data structures are typically stored on computer readable media that are input to controller 80 under the control of operation software, which operation software itself is typically stored on a computer readable medium. In accordance with a preferred embodiment of the present invention, recipes are input to controller 80 to cause it to control cluster tool 70 to process wafers in the manner described above to deposit a Cu barrier layer and Cu seed layers without breaking vacuum or exposing a wafer to the atmosphere.

In one embodiment of the present invention, the apparatus comprises a chamber in which both conformal and non-conformal seed layers are deposited utilizing: (a) two or more distinct steps, wherein the deposition variables (or conditions or parameters) during the first step are suitable for the deposition of a substantially conformal (or a non-conformal) seed layer, and the deposition conditions during the second step are suitable for the deposition of a substantially non-conformal (or a conformal) seed layer; (b) wherein at least one of the deposition variables is varied (or ramped) continuously or gradually, thereby changing the nature of the seed layer from substantially conformal to substantially non-conformal, or vice versa; or (c) a combination of at least one distinct step of depositing a substantially conformal (or a

non-conformal) seed layer and at least one gradual variation (or ramping) of at least one deposition variable towards a substantially non-conformal (or a conformal) seed layer, and vice versa.

As is well known to those of ordinary skill in the art, the nature of certain deposition techniques, such as ion plating or other PVD techniques, can be made more conformal, or less conformal, by varying the deposition parameters (or variables, or conditions). For example, increasing the (partial) pressure during ion plating and other PVD techniques, tends to increase scattering of the depositing atoms (or ions), thereby making the deposition more isotropic and conformal. Similarly, biasing the substrate has a effect on the nature of the deposit. For example, in ionized metal plasma (IMP) and ion plating, increasing the (negative) bias voltage further accelerates positive ions (of the depositing metal) towards the substrate, thereby improving the filling of small openings. At the same time, the higher (negative) bias also increases the removal rate (or back-sputtering) from the top corners of the openings and the field, thereby rendering the deposition to be more conformal. Conversely, decreasing the negative bias, or even using positive bias, can render the deposition to be less conformal. Deposition rate (or power density) can also affect the nature of the deposition.

Similarly, as is known to those of ordinary skill in the art, the nature of certain CVD techniques can be made less conformal, or more conformal, by changing the deposition variables. For example, increasing the substrate temperature tends to shift the deposition from a surface-reaction, rate-controlled deposition at low temperature, to a transport, rate-controlled deposition at higher temperature. As a result, increasing the substrate temperature tends to render the deposition to be less conformal. Conversely, decreasing the temperature, tends to render the deposition to be more conformal. Similarly, increasing the precursor and/or the reacting gas partial pressure (or flow rate) tends to shift the deposition to be a more surface-reaction, rate-controlled deposition, thereby tending to render the deposition to be more conformal. Conversely, decreasing the partial pressure and/or flow rate of the precursor and/or a reacting gas, tends to render the deposition to be a more transport, rate-controlled

deposition and, therefore, less conformal. The plasma variables in PECVD, such as the power density, may also have significant effects on the nature of the deposition.

In accordance with one embodiment of the present invention, cluster tool 70 comprises the following chambers: a CVD deposition chamber for depositing a barrier layer (for example, Ta, TaN_X, W, or WN_X); a PVD deposition chamber for depositing a PVD Cu seed layer; and a CVD deposition chamber for depositing a CVD Cu seed layer. Single wafers are transferred in-situ in cluster tool 70, from one chamber to another, without exposing the wafers to the atmosphere prior to the deposition of the top Cu seed layer. The CVD barrier and the CVD Cu seed layers can be deposited in the same CVD chamber by using different gases and chemistries for the respective layers. However, a separate CVD chamber for each layer (i.e., the barrier and the CVD Cu layers) is preferred in order to minimize cross-contamination. Using cluster tool 70, cluster tool controller 80 would cause a deposition process such as the following to be carried out in accordance with a recipe specified, for example in the form of a data structure or software or program code: (a) (in accordance with a first portion of the data structure or a first portion of the software or computer code) introducing wafer 74 into CVD barrier layer deposition chamber 76 and depositing on wafer 74 a CVD barrier layer (about 200-400Å thick) comprising TaN_X or WN_X; (b) (in accordance with a second portion of the data structure or a first portion of software or computer code) transferring wafer 74 through transfer chamber 73, without exposing wafer 74 to the atmosphere, to PVD Cu seed layer deposition chamber 77 and depositing on wafer 74 a relatively thin (about 100-500 Å) "Flash" PVD Cu layer; (c) (in accordance with a third portion of the data structure or a first portion of software or computer code) transferring wafer 74 through transfer chamber 73, without exposing wafer 74 to the atmosphere, to CVD Cu seed layer deposition chamber 78 and depositing on wafer 74 a CVD Cu layer (about 100-500Å thick); and (d) (in accordance with a fourth portion of the data structure or a first portion of software or computer code) transferring wafer 74 through transfer chamber 73, without exposing it to the atmosphere, to PVD Cu seed layer deposition chamber 77 and depositing on wafer 74 a relatively thick PVD Cu layer (about 500-1,800Å thick). Other ancillary

steps include introducing wafer 74 into and removing wafer 74 from cluster tool 70 through loadlocks 71 and 72, respectively.

Another embodiment of a three-step combination may include a first deposited CVD seed layer, followed by a relatively thick PVD seed layer, and finally followed by a second deposited CVD seed layer. Other combinations may comprise even more steps in the deposition of the seed layer. In this embodiment, the three (or more) separately deposited seed layers may comprise the same metal or alloy or they may comprise, for example and without limitation, different materials chosen from Cu, Ag, or alloys comprising one or more of these metals.

Those skilled in the art will recognize that the foregoing description has been presented for the sake of illustration and description only. As such, it is not intended to be exhaustive or to limit the invention to the precise form disclosed.

What is claimed is:

1. A method for making metallic interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the field and inside surfaces of the at least one opening;

depositing a first seed layer over the barrier layer using a first deposition technique;

depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and

electroplating a metallic layer over the second seed layer, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

2. The method of claim 1 wherein the electroplated metallic layer comprises Cu.

3. The method of claim 1 wherein the electroplated metallic layer comprises Ag.

4. The method of claim 2 further comprising:

substantially removing electroplated copper overlying the opening and overlying the field, and removing the seed layers and the barrier layer overlying the field, wherein the removing comprises one or more of a mechanical polishing technique, a chemical mechanical polishing technique, a wet etching technique, and a dry etching technique.

5. The method of claim 1 wherein the first deposition technique comprises a conformal deposition technique and the second deposition technique comprises a non-conformal deposition technique, said second seed layer being thicker than said first seed layer over the field.

6. The method of claim 5 wherein:

the conformal deposition technique comprises a chemical vapor deposition (CVD) technique or an electroless technique; and

the non-conformal deposition technique comprises a physical vapor deposition (PVD) technique.

7. The method of claim 5 wherein the conformal deposition technique is a chemical vapor deposition (CVD) technique.

8. The method of claim 1 wherein the first deposition technique comprises a non-conformal deposition technique and the second deposition technique comprises a conformal deposition technique, said first seed layer being thicker than said second seed layer over the field.

9. The method of claim 8 wherein:

the non-conformal deposition technique comprises a physical vapor deposition (PVD) technique; and

the conformal deposition technique comprises a chemical vapor deposition (CVD or an electroless technique.

10. The method of claim 8 wherein the conformal deposition technique is a chemical vapor deposition (CVD) technique.

11. The method of claim 1 wherein the first and second seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

12. The method of claim 5 wherein the first seed layer and the second seed layer comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

13. The method of claim 8 wherein the first seed layer and the second seed layer comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

14. The method of claim 1 wherein the first and second seed layers comprise Cu.

15. The method of claim 5 wherein the first and second seed layers comprise Cu.

16. The method of claim 8 wherein the first and second seed layers comprise Cu.

17. The method of claim 5 wherein the first seed layer has a thickness in a range of about 50Å to about 500Å over the field and the second seed layer has a thickness in a range of about 100Å to about 2,000Å over the field.

18. The method of claim 5 wherein the first seed layer has a thickness in a range of about 100Å to about 300Å over the field and the second seed layer has a thickness in a range of about 300Å to about 1,000Å over the field.

19. The method of claim 8 wherein the first seed layer has a thickness in a range of about 100 Å to about 2,000Å over the field and the second seed layer has a thickness in a range of about 50Å to about 500Å over the field.

20. The method of claim 8 wherein the first seed layer has a thickness in a range of about 300Å to about 1,000Å over the field and the second seed layer has a thickness in a range of about 100Å to about 300Å over the field.

21. The method of claim 1 wherein the barrier layer is selected from a group consisting of Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, or alloys comprising one or more of these materials.

22. The method of claim 1 wherein the barrier layer is deposited by a chemical vapor deposition technique.

23. The method of claim 1 wherein the barrier layer is deposited by a physical vapor deposition technique.

24. The method of claim 1 wherein the barrier layer has a thickness in a range of about 30Å to about 500Å.

25. The method of claim 1 wherein the barrier layer has a thickness in a range of about 50Å to about 300Å.

26. A method for making copper interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the patterned insulating layer including overlying the field and inside surfaces of the at least one opening, the barrier layer comprising a refractory metal or an alloy comprising a refractory metal;

chemical vapor depositing a first copper seed layer over the barrier layer, the first copper seed layer substantially continuously covering inside surfaces of the at least one opening;

physical vapor depositing a second copper seed layer over the first copper seed layer, said second seed layer being thicker than said first seed layer over the field; and

electroplating copper over the second seed layer.

27. A method for making copper interconnects comprising:

forming a patterned insulating layer over a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the patterned insulating layer including overlying the field and inside surfaces of the at least one opening, the barrier layer comprising a refractory metal or an alloy comprising a refractory metal;

physical vapor depositing a first copper seed layer over the barrier layer;

chemical vapor depositing a second copper seed layer over the first copper seed layer, said first seed layer being thicker than said second seed layer over the field; and

electroplating copper over the second seed layer.

28. The method of claim 1 wherein the first deposition technique comprises a conformal deposition technique and the second deposition technique comprises a non-conformal deposition technique and further comprising depositing at least one additional seed layer over the second seed layer prior to electroplating.

29. The method of claim 1 wherein the first deposition technique comprises a conformal deposition technique and the second deposition technique comprises a non-conformal deposition technique and further comprising depositing at least one additional seed layer under the first seed layer.

30. The method of claim 28 wherein depositing at least one additional seed layer comprises using a conformal deposition technique.

31. The method of claim 29 wherein depositing at least one additional seed layer comprises using a non-conformal deposition technique.

32. The method of claim 30 wherein the first deposition technique comprises a chemical vapor deposition technique, the second deposition technique comprises a physical vapor deposition technique, and depositing at least one additional seed layer comprises using a chemical vapor deposition technique.

33. The method of claim 31 wherein depositing at least one additional seed layer comprises using a physical vapor deposition technique.

34. The method of claim 1 wherein the first deposition technique comprises a non-conformal deposition technique and the second deposition technique comprises a conformal deposition technique and further comprising depositing at least one additional seed layer over the second seed layer prior to electroplating.

35. The method of claim 34 wherein depositing at least one additional seed layer comprises using a non-conformal deposition technique.

36. The method of claim 35 wherein the first deposition technique comprises a physical vapor deposition technique, the second deposition technique comprises a chemical vapor deposition technique, and depositing at least one additional seed layer comprises using a physical vapor deposition technique.

37. A method for making metallic interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the field and inside surfaces of the at least one opening;

depositing two or more seed layers over the barrier layer using two or more different deposition techniques; and

electroplating a metallic layer over the two or more seed layers, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

38. Copper filled via or trench interconnects on a substrate comprising:

a patterned insulating layer formed on the substrate, the patterned insulating layer including at least one opening;

a barrier layer formed over the patterned insulating layer, including inside surfaces of the at least one opening;

a first seed layer deposited over the barrier layer, including inside surfaces of the at least one opening;

a second seed layer deposited over the first seed layer; and

an electroplated metallic layer deposited over the second deposited seed layer, said metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

39. An apparatus for depositing seed layers on a substrate, said apparatus comprising:

at least one conformal deposition chamber adapted to deposit a substantially conformal seed layer on the substrate; and

at least one non-conformal chamber adapted to deposit a substantially non-conformal seed layer on the substrate, wherein said seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

40. The apparatus of claim 39 wherein said at least one conformal deposition chamber comprises a CVD seed chamber and said at least one non-conformal deposition chamber comprises a PVD seed chamber.

41. The apparatus of claim 40 which further comprises a transfer chamber adapted to transfer the substrate from said CVD seed chamber to said PVD seed chamber, and vice versa, without exposing the substrate to atmosphere.

42. The apparatus of claim 41 which further comprises a transfer chamber adapted to transfer the substrate from said CVD seed chamber to said PVD seed chamber, and vice versa, without breaking vacuum.

43. The apparatus of claim 40 further comprising a barrier chamber adapted to deposit a barrier layer.

44. The apparatus of claim 43 wherein said barrier layer comprises a material selected from the group consisting of Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials.

45. The apparatus of claim 43 wherein said barrier chamber comprises a CVD deposition chamber.

46. The apparatus of claim 43 wherein said barrier chamber comprises a PVD deposition chamber.

47. The apparatus of claim 40 wherein the CVD seed chamber is further adapted to deposit a CVD barrier layer.

48. The apparatus of claim 40 wherein the PVD seed chamber is further adapted to deposit a PVD barrier layer.

49. An apparatus for depositing seed layers on a substrate, said apparatus comprising a deposition chamber adapted to deposit a substantially conformal seed layer on the substrate and a substantially non-conformal seed layer on the substrate, wherein said seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

50. The apparatus of claim 49 wherein the apparatus is adapted to deposit at least two seed layers in at least two distinct steps in succession, inside a deposition chamber, wherein deposition parameters used to control the deposition chamber in one of the distinct steps produce a substantially conformal seed layer and deposition parameters used to control the deposition chamber in another one of the distinct steps produce a substantially non-conformal seed layer.

51. The apparatus of claim 50 wherein the apparatus causes at least one of the deposition parameters to be varied continuously or gradually, thereby changing the nature of the depositing seed layer from a substantially conformal seed layer to a substantially non-conformal seed layer, or vice versa, inside the same deposition chamber.

52. The apparatus of claim 50 wherein the apparatus controls at least one of the deposition parameters in a manner to provide a combination of at least one distinct step of depositing a substantially conformal or a non-conformal seed layer and at least one gradual variation of the at least one deposition parameter towards a

substantially non-conformal or a conformal seed layer, respectively, or vice versa, inside the same deposition chamber.

53. The apparatus of claim 39 which further comprises a controller which causes the apparatus to transfer the substrate between the conformal deposition chamber and the non-conformal deposition chamber, or vice versa, and wherein said controller also causes the conformal deposition chamber to deposit the substantially conformal seed layer on the substrate, and the non-conformal chamber to deposit the substantially non-conformal seed layer on the substrate.

54. The apparatus of claim 49 which further comprises a controller which causes at least one deposition parameter to vary in a manner to deposit a substantially conformal seed layer on the substrate and a substantially non-conformal seed layer on the substrate, inside the same deposition chamber.

55. A computer readable medium which comprises a data structure which causes a controller to cause a deposition apparatus comprising a conformal deposition chamber and a non-conformal deposition chamber to deposit a substantially conformal and a substantially non-conformal seed layers, respectively, wherein said substantially conformal and substantially non-conformal seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals, and wherein said data structure comprises:

a first data portion that causes the controller to cause the apparatus to deposit a substantially conformal seed layer; and

a second data portion that causes the controller to cause the apparatus to deposit a substantially non-conformal seed layer.

56. A computer readable medium which comprises a data structure which causes a controller to cause a deposition apparatus comprising a conformal deposition chamber and a non-conformal deposition chamber to deposit a substantially conformal and a substantially non-conformal seed layers, respectively, wherein said substantially conformal and substantially non-conformal seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals, and wherein said data structure comprises:

a first data portion that causes the controller to cause the apparatus to deposit a substantially non-conformal seed layer; and

a second data portion that causes the controller to cause the apparatus to deposit a substantially conformal seed layer.

57. A computer readable medium which comprises a data structure which causes a controller to cause a deposition apparatus comprising a deposition chamber adapted to deposit a substantially conformal seed layer on a substrate and a substantially non-conformal seed layer on the substrate, wherein said substantially conformal and substantially non-conformal seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals, and wherein said data structure comprises:

a first data portion that causes the controller to cause the apparatus to deposit a substantially conformal seed layer; and

a second data portion that causes the controller to cause the apparatus to deposit a substantially non-conformal seed layer.

58 A computer readable medium which comprises a data structure which causes a controller to cause a deposition apparatus comprising a deposition chamber adapted to deposit a substantially conformal seed layer on a substrate and a substantially non-conformal seed layer on the substrate, wherein said substantially conformal and substantially non-conformal seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals, and wherein said data structure comprises:

a first data portion that causes the controller to cause the apparatus to deposit a substantially non-conformal seed layer; and

a second data portion that causes the controller to cause the apparatus to deposit a substantially conformal seed layer.

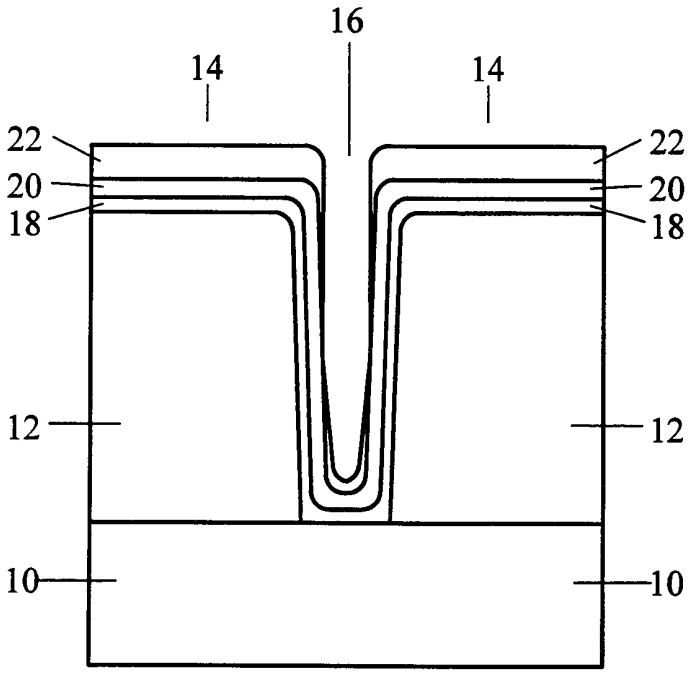

Figure 1

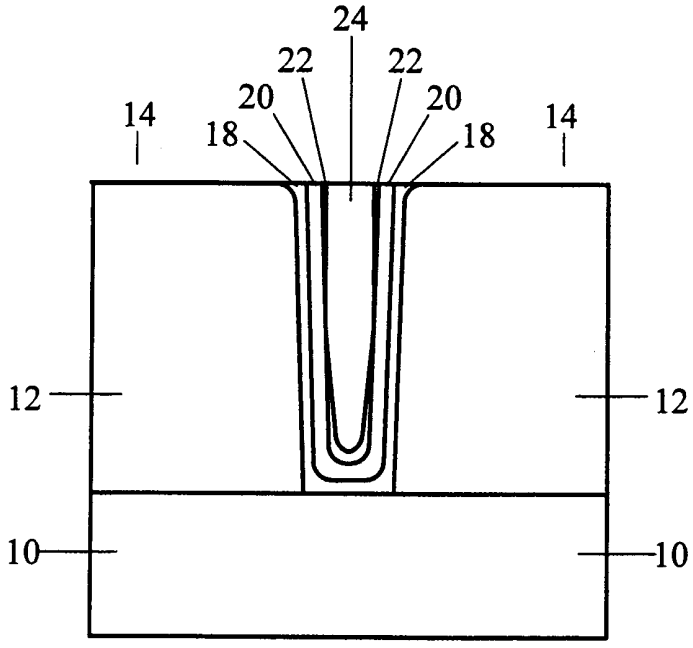

Figure 2

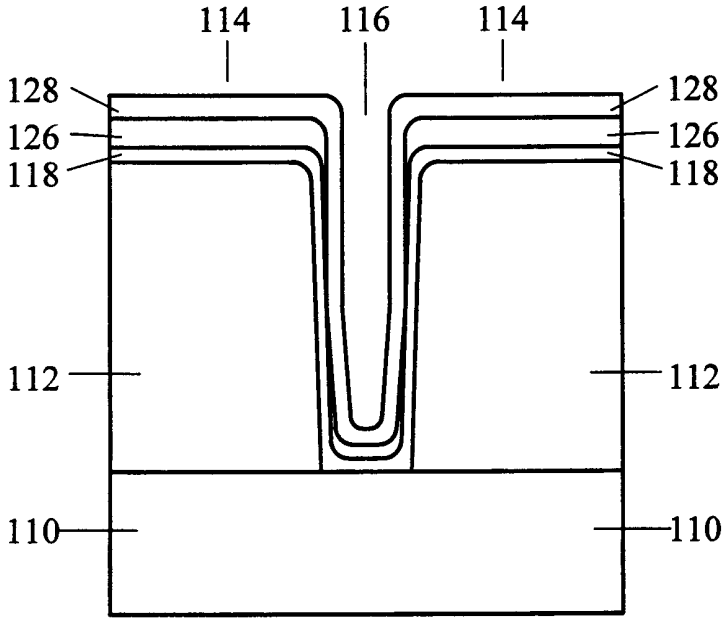

Figure 3

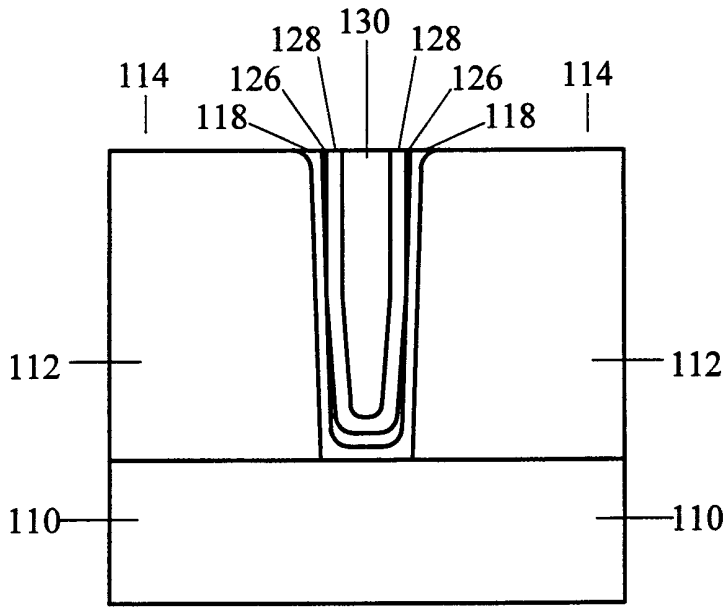

Figure 4

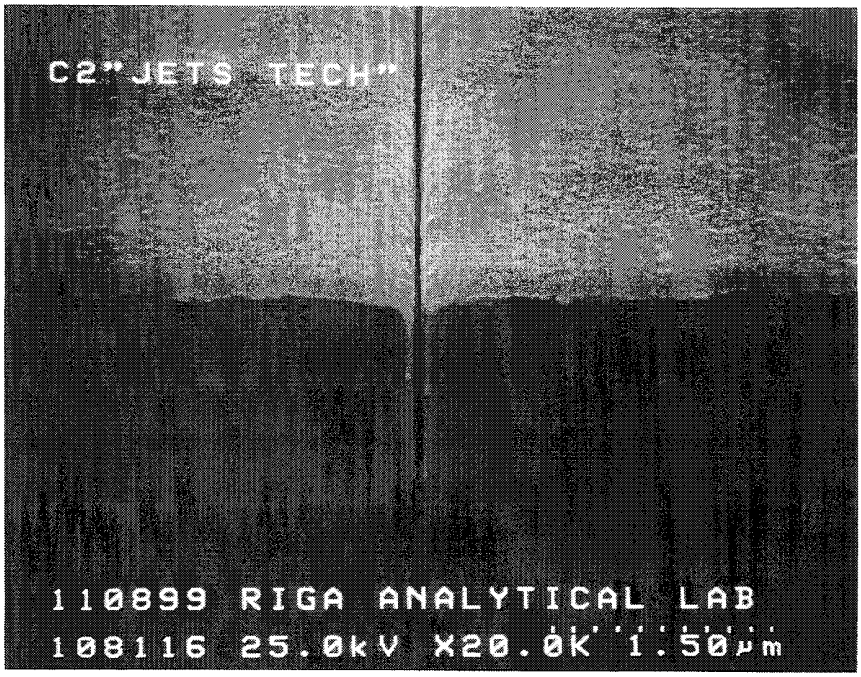

Figure 5. SEM of a trench ~0.10µm wide; ~1.4µm deep; AR ~ 14.0:1; Combined barrier and seed layers: ~400-500Å on sidewalls and ~1,800-1,900Å on field. 30° tilt.

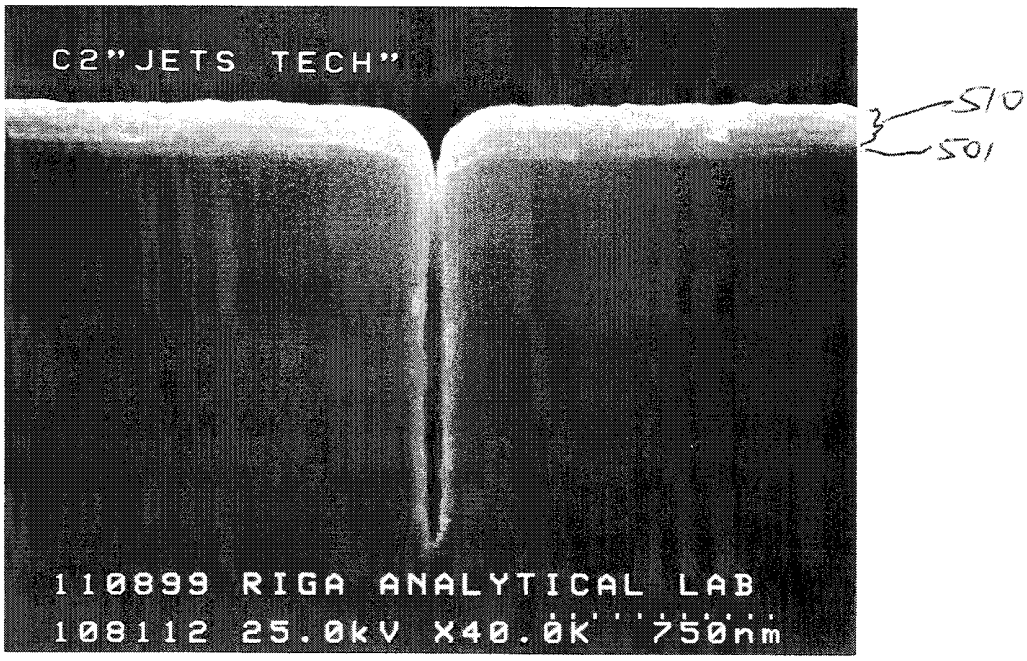

Figure 6. SEM of a trench ~0.10µm wide; ~1.4µm deep; AR ~ 14.0:1; Combined barrier and seed layers: ~400-500Å on sidewalls and ~1,800-1,900Å on field. No tilt.

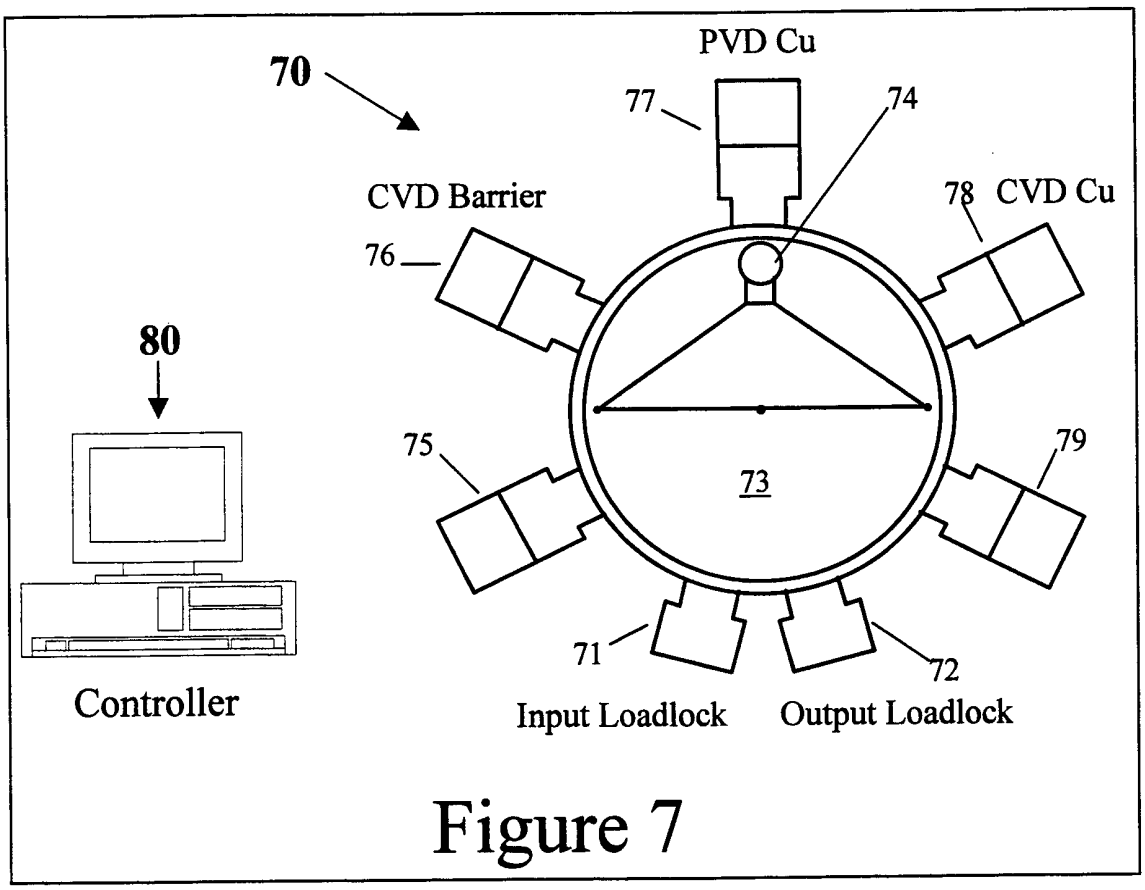
70
PVD Cu
77
74
CVD Barrier
78 CVD Cu
76
80
75
79
73
71
72
Controller
Input Loadlock
Output Loadlock

Figure 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/40983

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/629, 652, 687, 643, 644, 763; 118/715, 719, 900; 700/123; 709/100

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6,087,711 A (GIVENS) 11 July 2000 (11.07.2000), col. 4, lines 20-65.	1-58
A,P	US 6,069,068 A (RATHORE et al) 30 May 2000 (30.05.2000), col. 8, lines 1-65.	1-58

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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