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[54] **PROGRAMMED TIME DIVISION MULTIPLEXED CODED TONE TRANSMISSION SYSTEM**

[75] Inventors: **Carl F. Klein; Lawrence B. Korta; Michael B. McLean,** all of Milwaukee, Wis.

[73] Assignee: **Johnson Service Company,** Milwaukee, Wis.

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[52] **U.S. Cl.** ..... **340/409 R,** 340/413 R
[51] **Int. Cl.** **G08b 29/00**
[58] **Field of Search** ..... 340/413 R, 409 R

[56] **References Cited**

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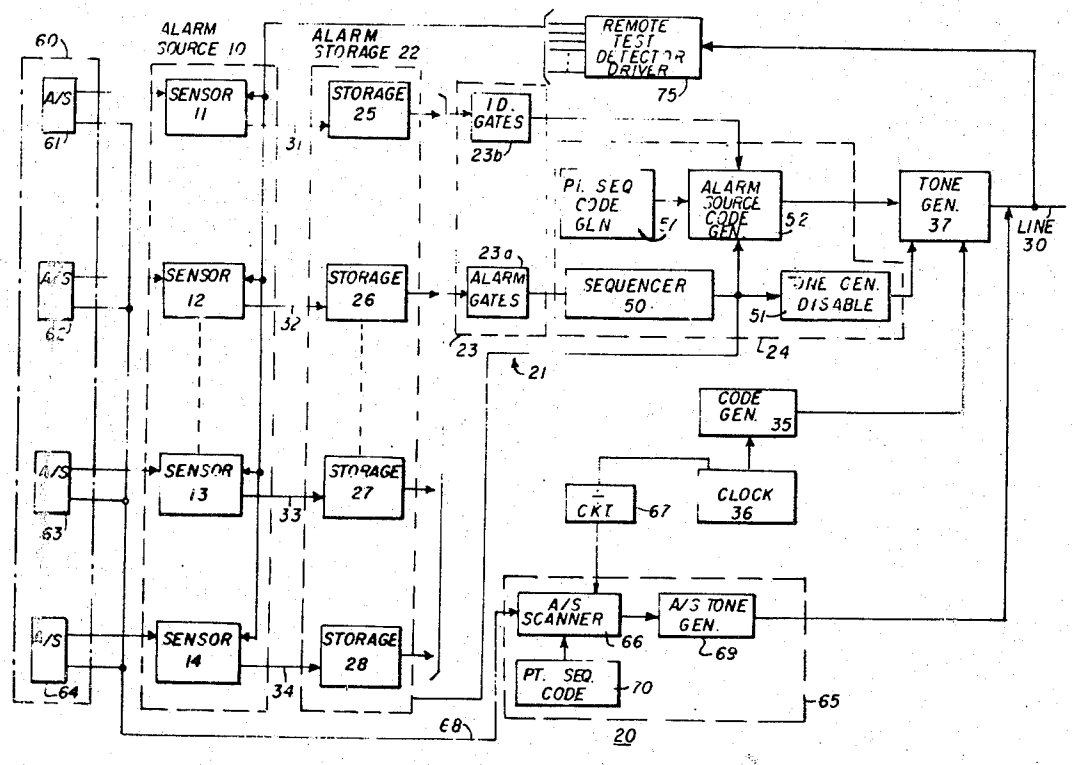
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Primary Examiner—Harold I. Pitts
Attorney, Agent, or Firm—Johnson, Dienner, Emrich, Verbeck & Wagner

[57] **ABSTRACT**

An alarm transmission system for transmitting alarm information provided by a plurality of alarm sources to a central monitor over a common transmission line includes zone monitoring circuits having a code generator for generating a monitor code comprised of a continuous sequence of bits for transmission over the transmission line to the central monitor, alarm multiplexing circuits including alarm storage circuits which provide separate storage locations for storing alarm outputs provided by each alarm source and a sequencing circuit controlled by the alarm data storage circuits in response to the receipt of an alarm output provided by an alarm sensor to generate a plurality of control signals in a predetermined time sequence, including a control signal for enabling an inhibit circuit to inhibit the transmission of the monitor code to the central monitor and a further control signal for enabling an alarm source identification code generator to effect readout of the alarm storage circuits to generate an alarm source identification code comprised of a sequence of coded bits, each bit of which represents the condition of a different alarm sensor, for transmission over the transmission line to the central monitor to enable identification of the source of the alarm.

43 Claims, 13 Drawing Figures



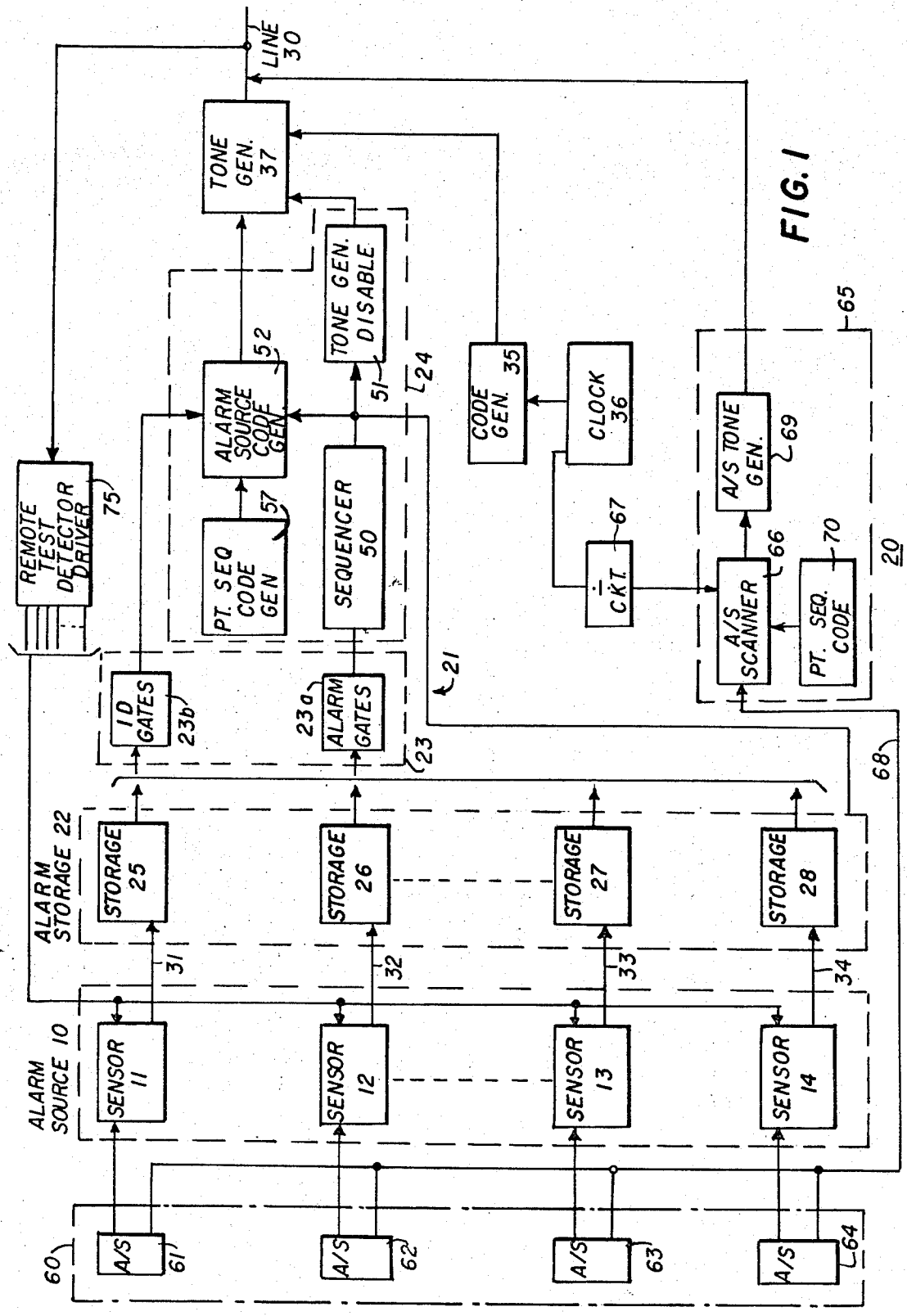
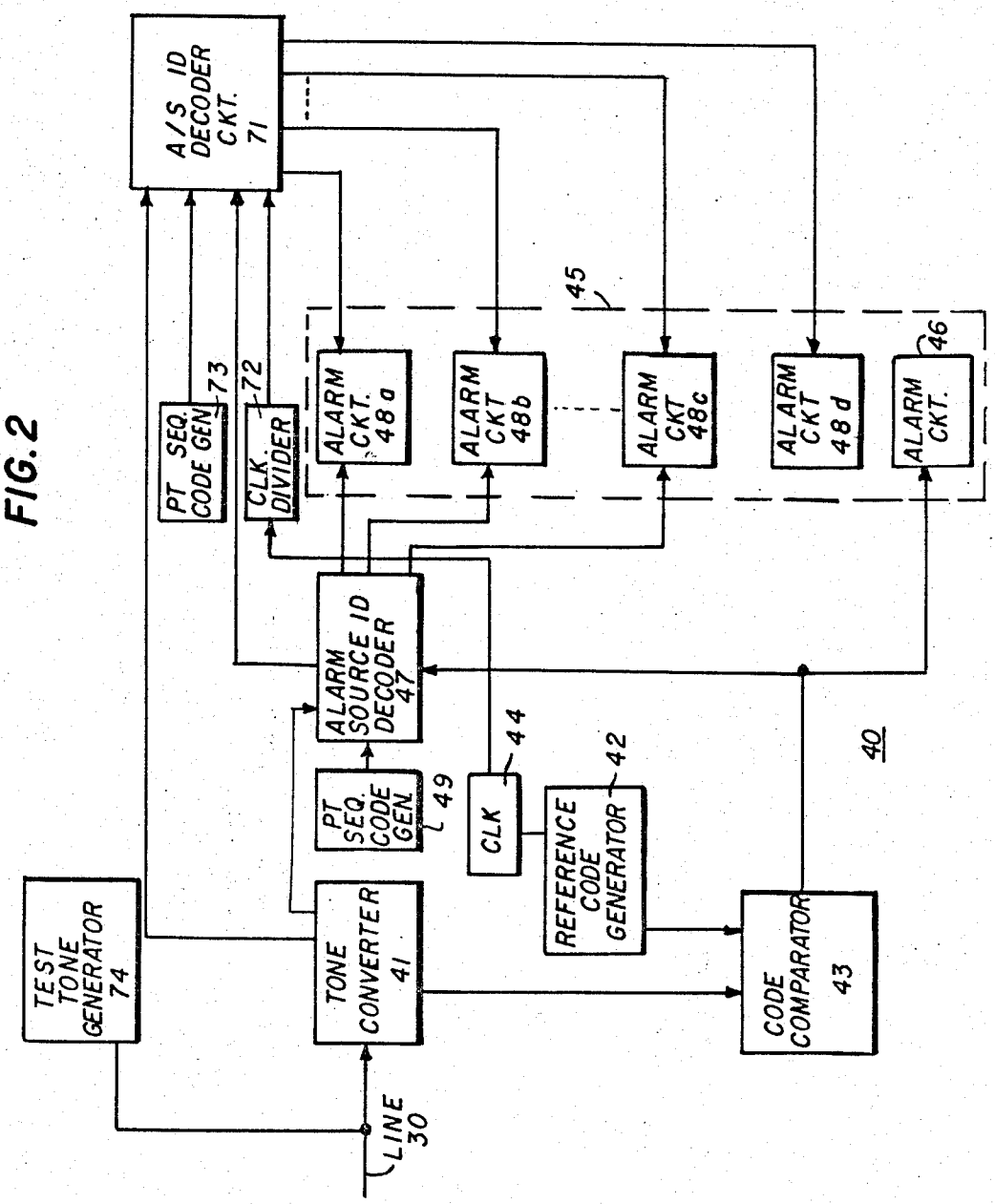

LINE 30
TONE GEN. 37
TONE GEN. DISABLE
ALARM SOURCE CODE GEN.
52
51
24
CODE GEN. 35
CLOCK 36
65
A/S TONE GEN. 69
REMOTE TEST DETECTOR DRIVER 75
PT. SEQ CODE GEN 57
SEQUENCER 50
67
CKT.
A/S SCANNER 66
PT. SEQ. CODE 70
20
21
ID GATES 23b
23a ALARM GATES
23
68
ALARM STORAGE 22
STORAGE 25
STORAGE 26
STORAGE 27
STORAGE 28
31
32
33
34
ALARM SOURCE 10
SENSOR 11
SENSOR 12
SENSOR 13
SENSOR 14
60
A/S 61
A/S 62
A/S 63
A/S 64

FIG. 1

FIG. 2


A/S ID DECODER CKT. 71
PT SEQ. CODE GEN 73
CLK. DIVIDER 72
ALARM CKT. 48a
ALARM CKT 48b
ALARM CKT 48c
ALARM CKT 48d
ALARM CKT. 46
45
ALARM SOURCE ID DECODER 47
PT SEQ. CODE GEN 49
CLK 44
REFERENCE CODE GENERATOR 42
40
TEST TONE GENERATOR 74
TONE CONVERTER 41
CODE COMPARATOR 43
LINE 30

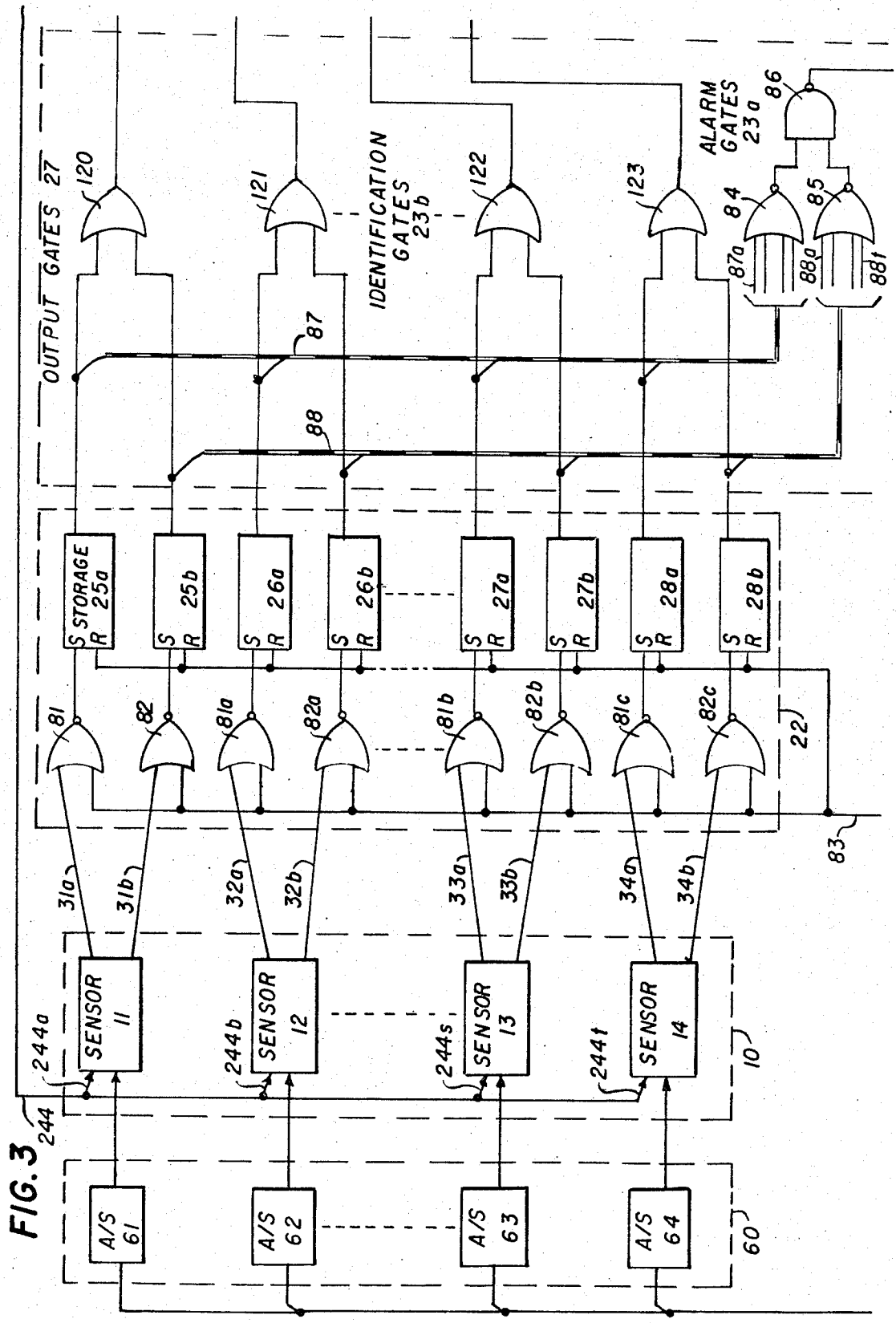

OUTPUT GATES 27
IDENTIFICATION GATES 23b
ALARM GATES 23a
120
121
122
123
84
85
86
87
88
87a
88a
88t
S STORAGE R 25a
S R 25b
S R 26a
S R 26b
S R 27a
S R 27b
S R 28a
S R 28b
81
82
81a
82a
81b
82b
81c
82c
22
83
31a
31b
32a
32b
33a
33b
34a
34b
SENSOR 11
SENSOR 12
SENSOR 13
SENSOR 14
244a
244b
244s
244t
244
10
A/S 61
A/S 62
A/S 63
A/S 64
60

FIG. 3

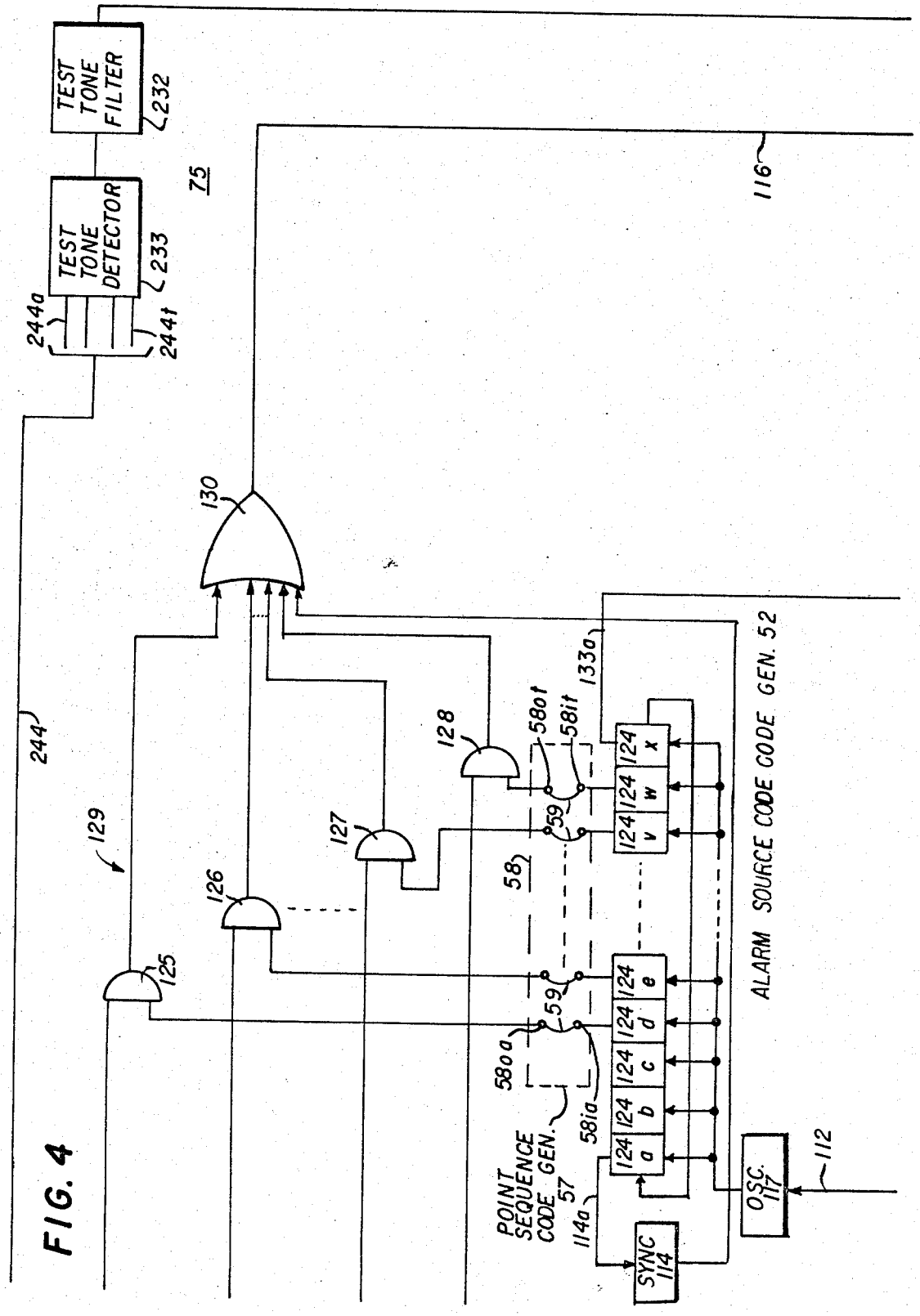

TEST TONE FILTER
232
TEST TONE DETECTOR
233
75
116
244a
244t
244
130
129
125
126
127
128
58
59
58oa
58ia
58ot
58it
133a
124 a
124 b
124 c
124 d'
124 e
124 v
124 w
124 x
ALARM SOURCE CODE GEN. 52
POINT SEQUENCE CODE GEN. 57
114a
SYNC 114
OSC. 117
112

FIG. 4

FIG. 5

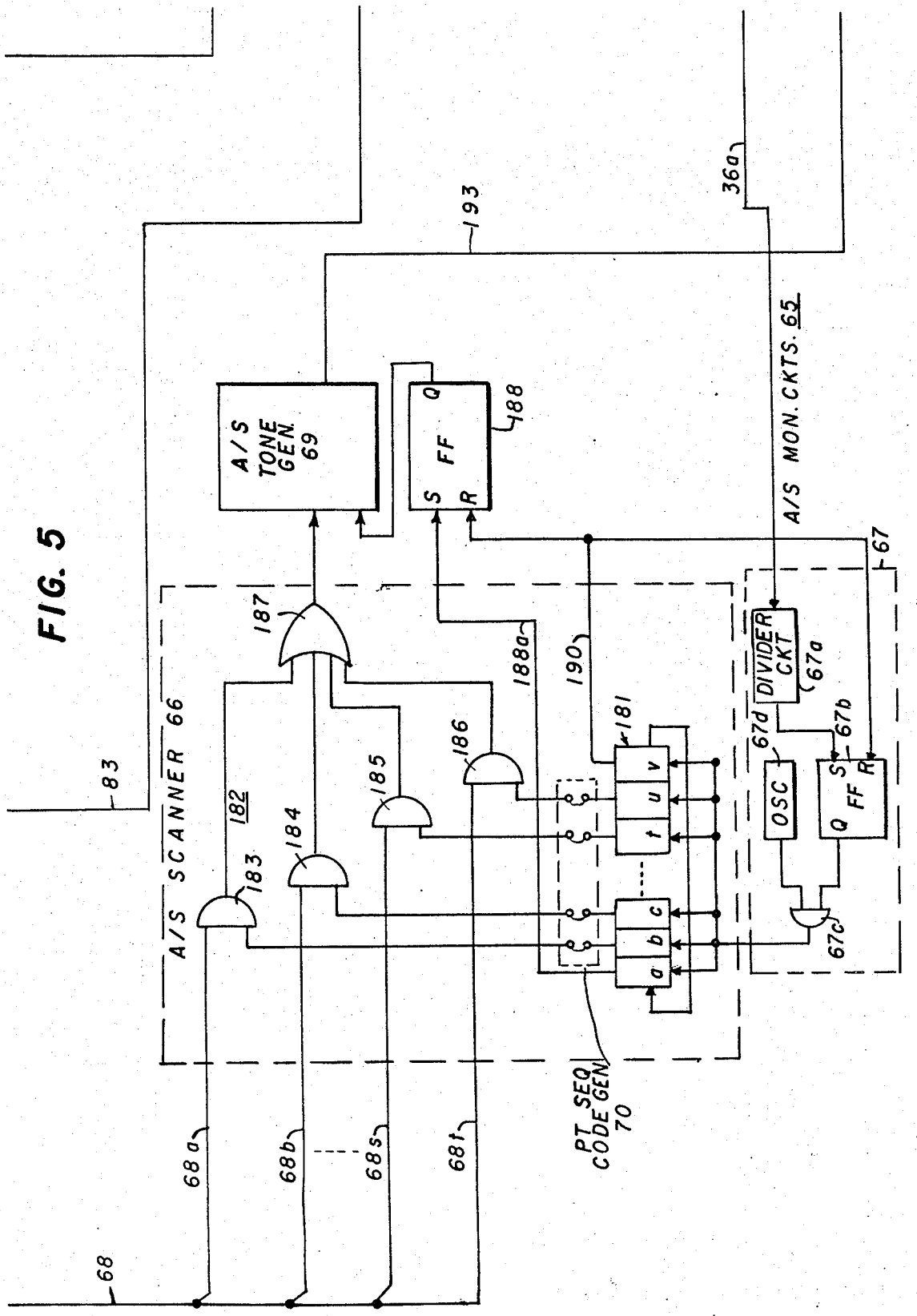

A/S TONE GEN. 69
FF
S
R
Q
188
193
36a
A/S MON. CKTS. 65
67
A/S SCANNER 66
187
188a
190
181
186
185
184
183
182
83
DIVIDER CKT
67a
67d
67b
OSC
FF
67c
PT. SEQ. CODE GEN. 70
68a
68b
68s
68t
68

FIG. 6

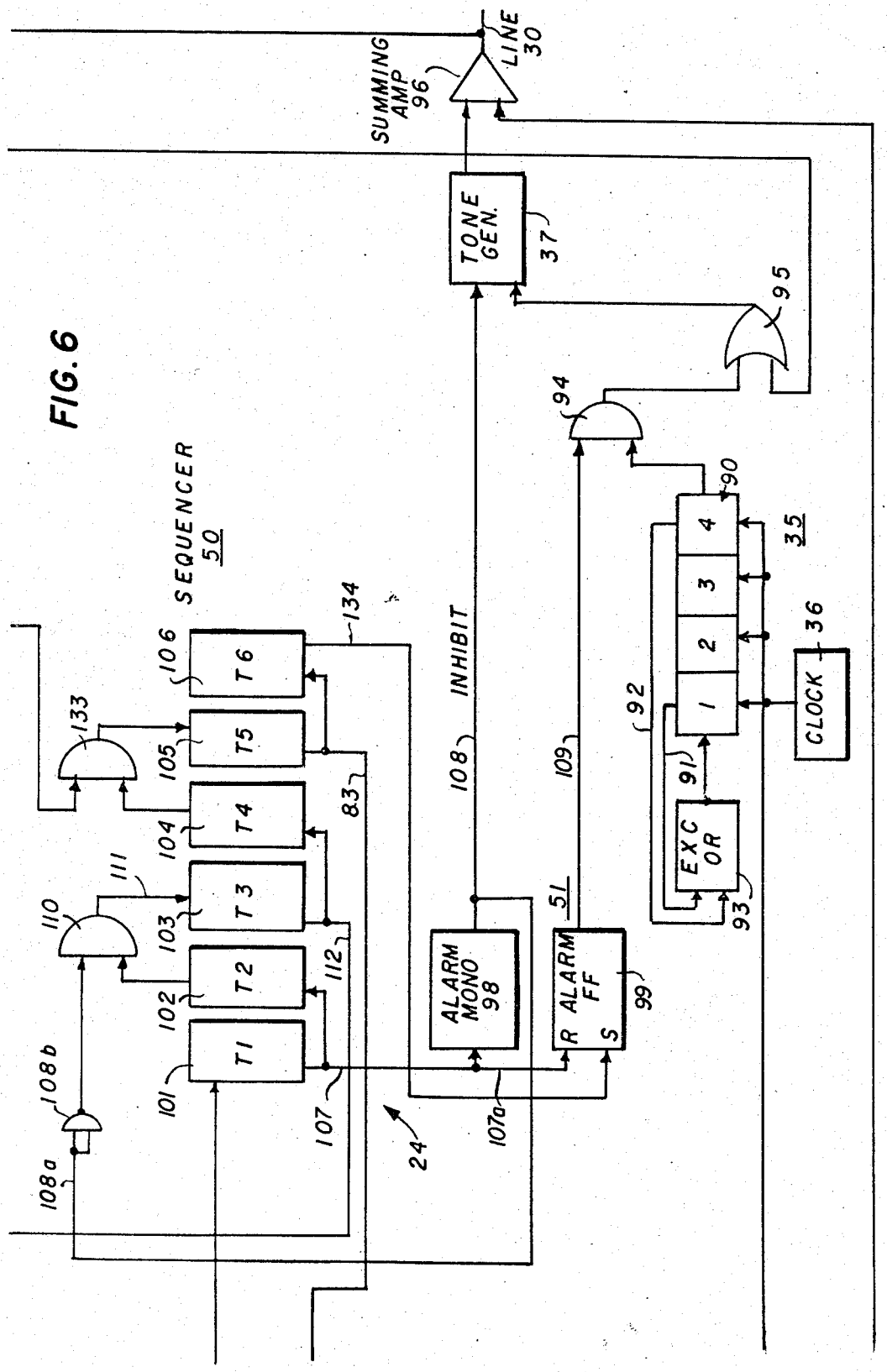

SUMMING AMP 96
LINE 30
TONE GEN. 37
95
94
90
4
3
2
1
35
92
91
EXC OR
93
CLOCK 36
SEQUENCER 50
106
T6
105
T5
104
T4
103
T3
102
T2
101
T1
134
133
111
110
108b
108a
83
112
107
107a
24
108 INHIBIT
109
ALARM MONO 98
R ALARM FF S
51
99

FIG. 7

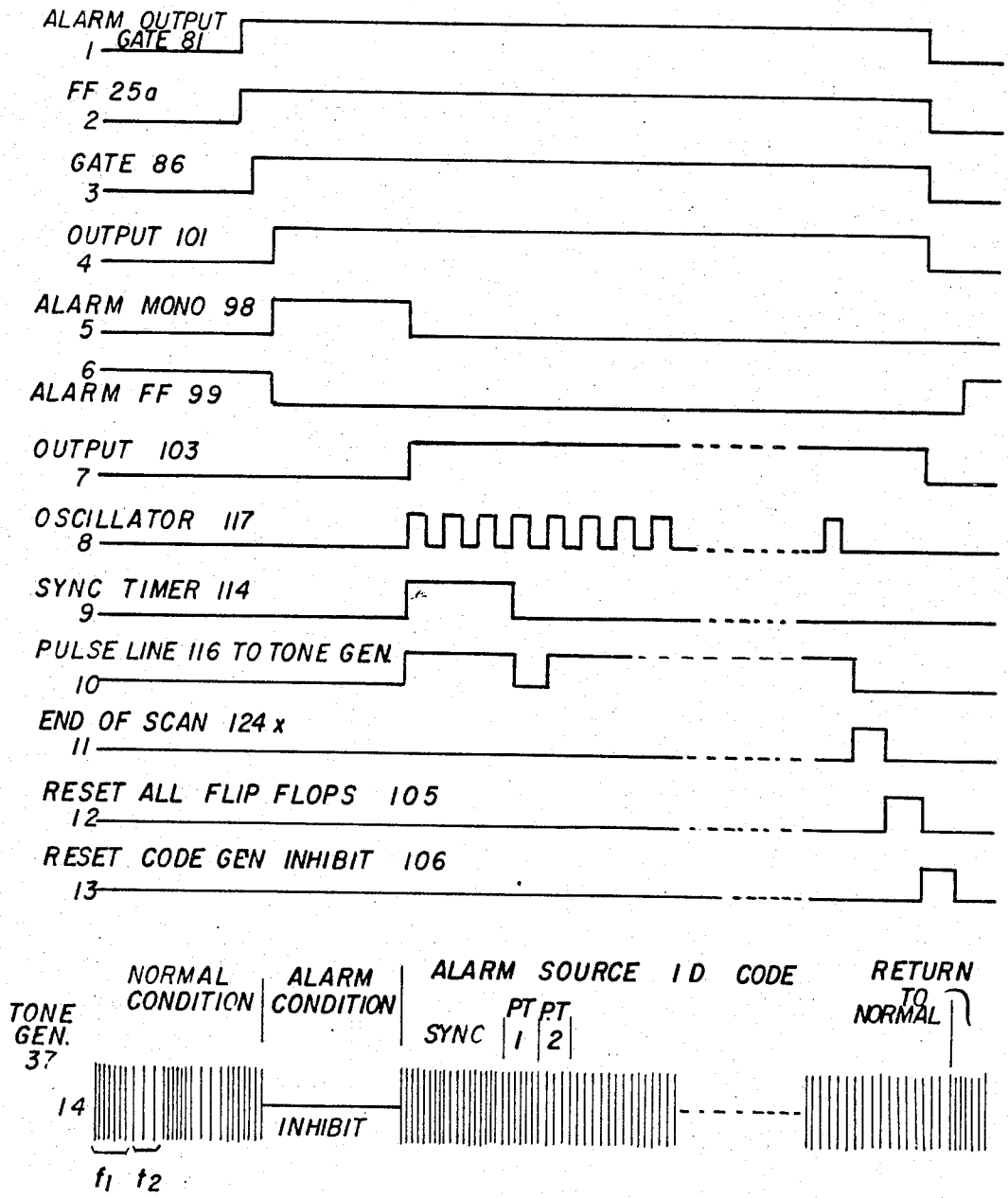

ALARM OUTPUT GATE 81
1
FF 25a
2
GATE 86
3
OUTPUT 101
4
ALARM MONO 98
5
6
ALARM FF 99
OUTPUT 103
7
OSCILLATOR 117
8
SYNC TIMER 114
9
PULSE LINE 116 TO TONE GEN.
10
END OF SCAN 124x
11
RESET ALL FLIP FLOPS 105
12
RESET CODE GEN INHIBIT 106
13
TONE GEN. 37
NORMAL CONDITION
ALARM CONDITION
ALARM SOURCE I D CODE
SYNC
PT 1
PT 2
RETURN TO NORMAL
14
INHIBIT
f1
t2

FIG. 8

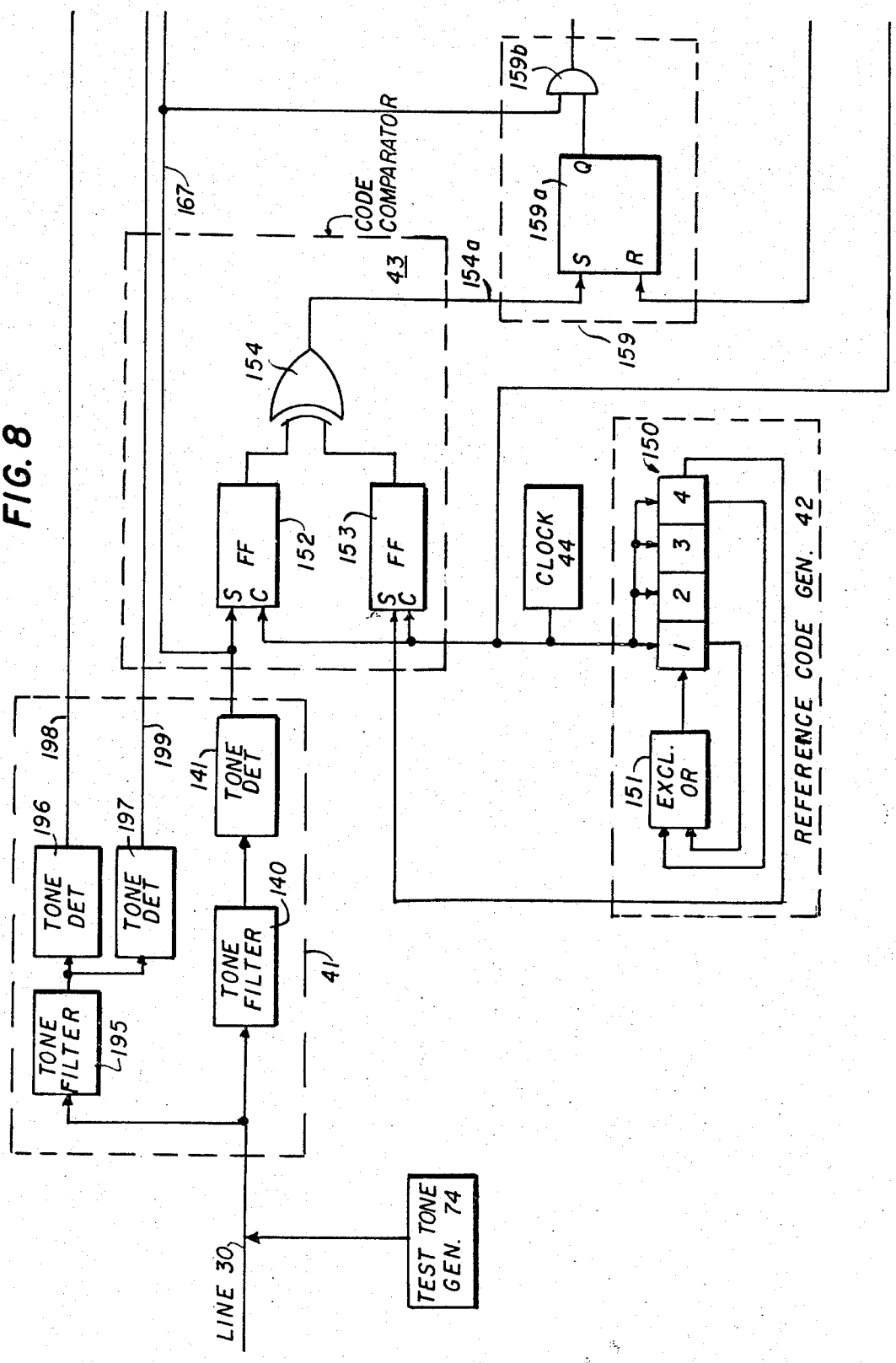

LINE 30
TEST TONE GEN. 74
TONE FILTER
195
TONE DET
196
TONE DET
197
198
199
TONE FILTER
140
TONE DET
141
41
CODE COMPARATOR
167
43
154
154a
FF
S
C
152
FF
S
C
153
159b
159a
Q
S
R
159
CLOCK 44
150
4
3
2
1
EXCL. OR
151
REFERENCE CODE GEN. 42

FIG. 9

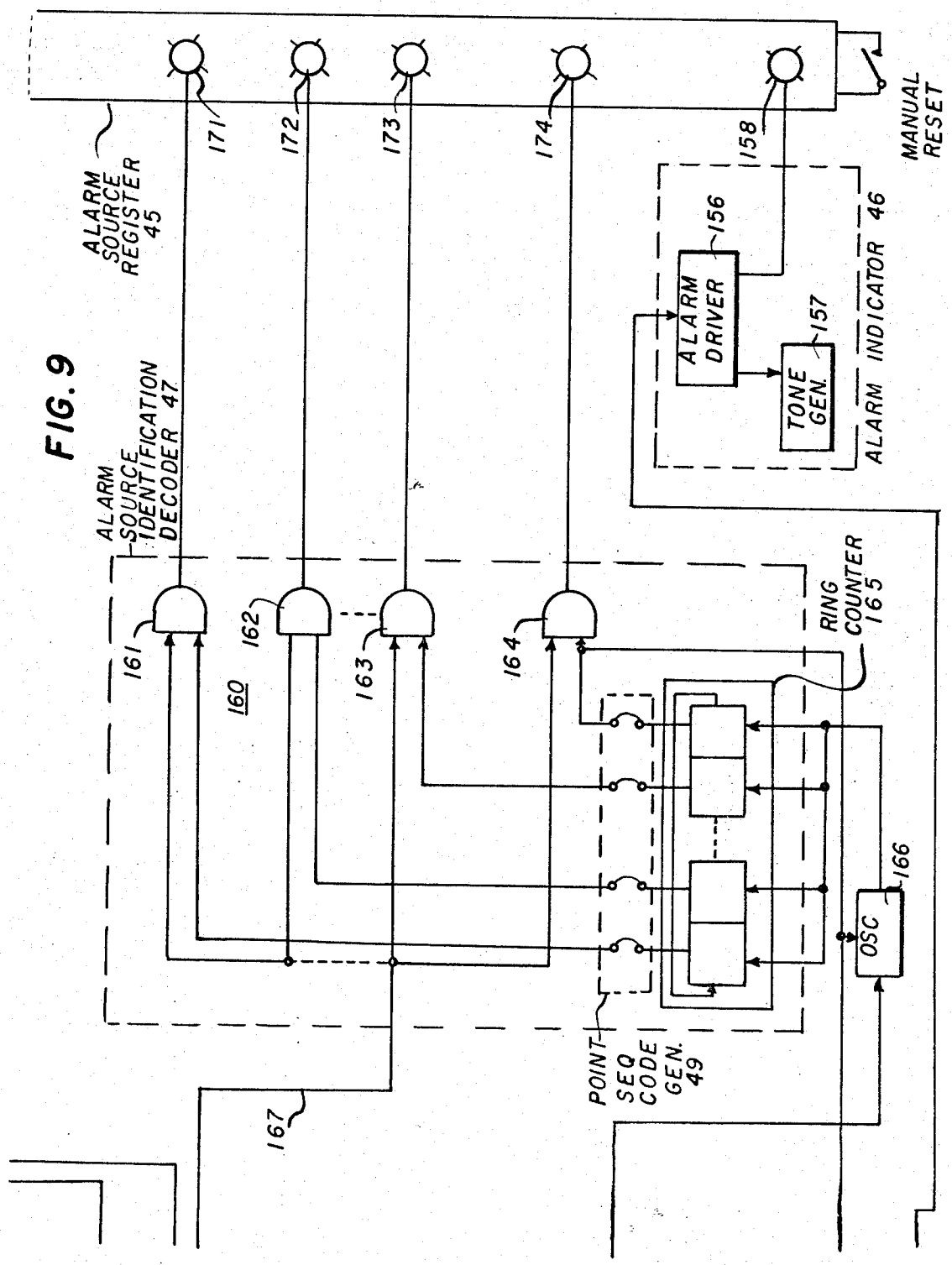
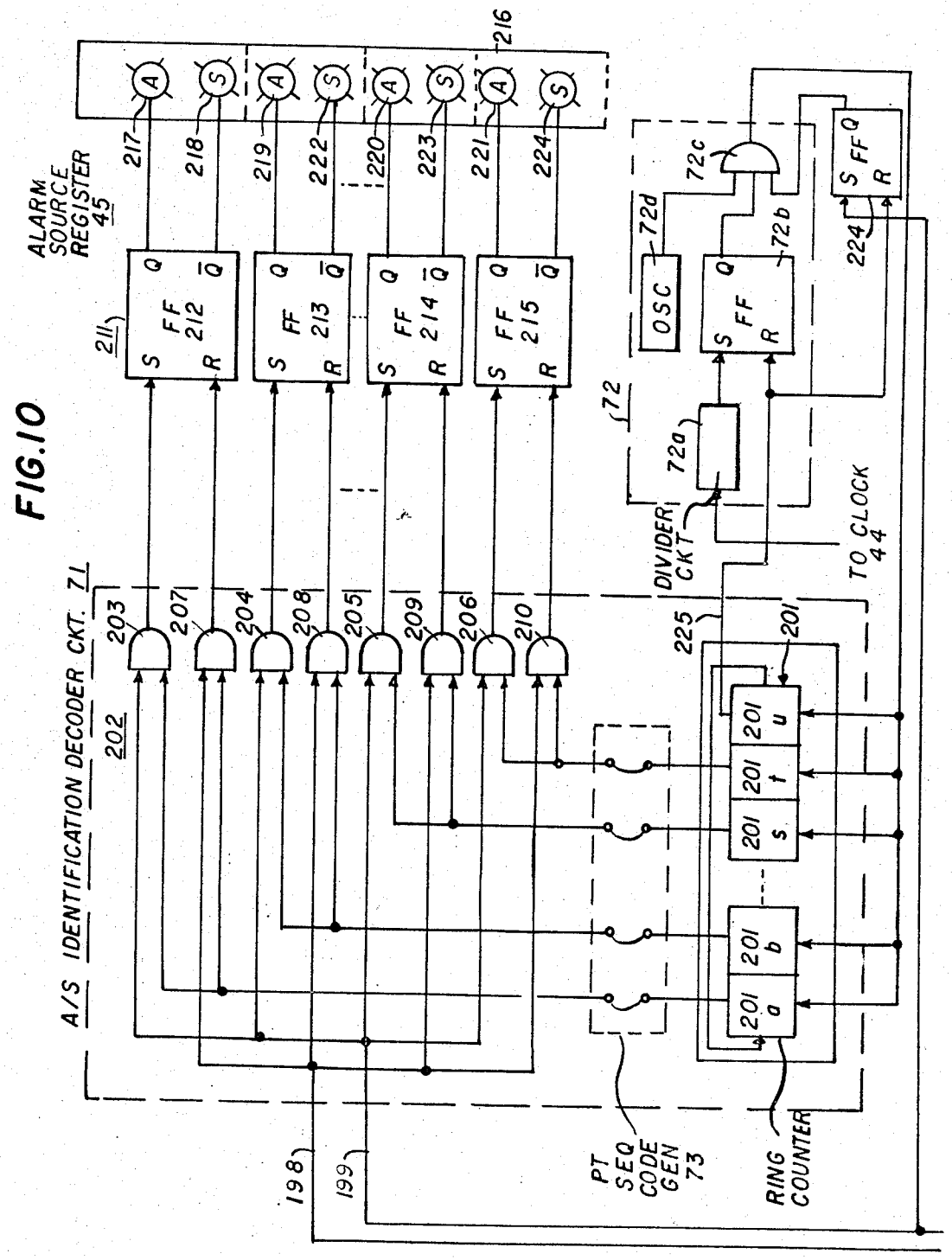

ALARM SOURCE REGISTER 45
171
172
173
174
158
MANUAL RESET
ALARM DRIVER
156
TONE GEN.
157
ALARM INDICATOR 46
ALARM SOURCE IDENTIFICATION DECODER 47
160
161
162
163
164
RING COUNTER 165
OSC
166
POINT SEQ CODE GEN. 49
167

FIG. 10


ALARM SOURCE REGISTER 45
A/S IDENTIFICATION DECODER CKT. 71
DIVIDER CKT
TO CLOCK 44
PT SEQ CODE GEN 73
RING COUNTER
OSC
FF 212
FF 213
FF 214
FF 215
FF
216
217
218
219
220
221
222
223
224
225
198
199
201
202
203
204
205
206
207
208
209
210
211
72
72a
72b
72c
72d

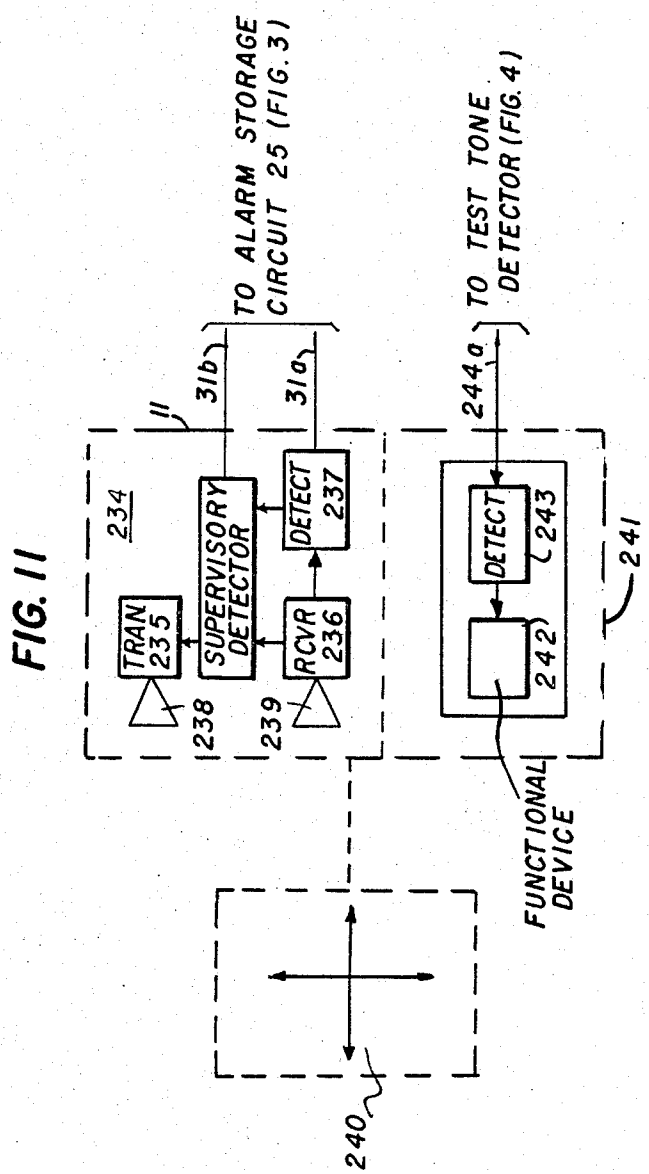


FIG. 11

FIG. 12

FIG. 3	FIG. 4
FIG. 5	FIG. 6

FIG. 13

	FIG. 10
FIG. 8	FIG. 9

PROGRAMMED TIME DIVISION MULTIPLEXED CODED TONE TRANSMISSION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to remote alarm monitoring systems, and, more particularly, to a multiplexed alarm transmission system wherein alarm information from a plurality of alarm sensors is transmitted to a central monitor over a single transmission line.

2. Description of the Prior Art

In security systems, it is frequently necessary to interconnect a multiplicity of alarm sensors to one central monitor. Typically, the alarm sensors are separated by relatively short distances as, for example, when the alarm sensors are employed for detecting unauthorized entry of classrooms in a school, while the central monitor could be a relatively large distance away from any of the sensors as, for example, when located in the school administration building.

When the distance over which alarm information must be transmitted is great, some form of line supervision is required for the transmission lines which carry such alarm data, the degree of supervision being a function of the level of system security required. To minimize alarm data transmission costs and to enhance the security of the alarm transmission system when alarm data must be transmitted over long distances, it is desirable to minimize the number of transmission lines which must be connected between the central monitor and the locations of the alarm sensors. Therefore, there exists a need for a supervised alarm data transmission system which couples multiple alarm sensors to a central monitor over a single secured transmission line while transmission line complexity and costs of associated supervision and alarm transmission circuits are minimized.

Such system may employ a multiplexing arrangement using either frequency division multiplexing or time division multiplexing techniques to transmit data from a plurality of sources to the central monitor.

Frequency division multiplexing systems require a plurality of tone generators including an individual tone generator for each alarm data source. Alarm data provided by different alarm sources is coded by tones of different frequencies, and the coded tones, representing the data from all of the alarm sources, transmitted simultaneously to the central monitor over a common transmission line. Filter circuits are required at the central monitor to separate the coded tones provided by the different alarm sources in separate signal channels and a separate tone detector in each channel detects the tones transmitted from an associated alarm source.

In time division multiplexing systems, information from a plurality of alarm data sources is transmitted over a common transmission line on a shared time basis. Accordingly, only one tone generator and tone detector are required, and thus, the cost of the data transmission circuits is less than those required in systems employing frequency division multiplexing.

However, the use of time division multiplexing has not found much acceptance in the security area. There is a prevailing feeling that a necessary condition for maximum security requires continuous monitoring of all protected areas. Thus, any time division multiplexing system which inherently results in a brief interruption between an alarm sensor and the central monitor to provide a time interval for interleaving of the signals from a plurality of alarm sensors has not been well accepted. Part of this disfavor results from the fear that a momentary alarm indication provided by a given sensor may occur between the two instants at which the output of such alarm sensor is sampled and that such alarm indication may not be detected.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a secured intrusion alarm data transmission system wherein alarm data provided by a plurality of intrusion sensors is transmitted to a central monitor over a common alarm transmission line in order to minimize complexity and both installation and operating costs of the system.

A further object of the invention is to provide a secured data transmission system which utilizes coded tone transmission wherein information provided by a plurality of alarm sensors is transmitted to a central monitor in a programmed time sequence.

Another object is to provide a secured data transmission system which transmits at least two fundamentally different types of alarm information, namely an indication of an alarm and the identification of the source of such alarm.

A further object is to provide an intrusion alarm data transmission system in which the alarm sensors are selectively operable in either an active or standby mode and wherein data representing the active or standby status of each alarm sensor is periodically transmitted to the central monitor over the alarm transmission line.

Another object is to provide a time multiplexed alarm transmission system which, by virtue of an alarm storage means, maintains essentially continuous surveillance over all alarm sensors.

Another object is to provide an extremely flexible, secured data transmission system which can easily be expanded in terms of both the number of alarm sensors monitored and the amount in types of information transmitted for each alarm sensor.

Yet another object is to provide a secured multiplex alarm data transmission system in which the operation of each alarm sensor can be tested upon command from the central monitor.

In accordance with an exemplary embodiment, the secured intrusion alarm data transmission system provided by the present invention includes zone monitoring means for monitoring the status of a plurality of alarm sensors, each located in a different area to be protected and for effecting the transmission of alarm information provided by the sensors to a central monitor over an alarm line. The zone monitoring means includes alarm multiplexing means having alarm storage means for providing separate storage locations for storing alarm outputs provided by each sensor and alarm data readout means responsive to alarm outputs provided by one or more of the alarm sensors to effect the transmission of alarm information into the central monitor indicating an alarm condition for one or more of the protected areas and the source of the alarm.

The zone monitoring means further includes code generator means for generating a monitor code comprised of a known sequence of code bits for transmis-

sion over the transmission line to the central monitor to normally indicate that the transmission line is secure and that all protected areas are secure.

Whenever an alarm indication is provided by one or more of the alarm sensors, the alarm multiplexing means is operable to substitute the alarm code for the monitor code to indicate the presence of the alarm and permit identification of the source of the alarm at the central monitor. The alarm code includes an alarm indication followed by an alarm source identification code sequence which is comprised of a plurality of bits, each bit of which represents the condition of a different one of the alarm sensors.

The central monitor includes alarm line monitoring means having reference code generator means for generating a sequence of code bits which is identical with the bit sequence normally provided by the code generator means of the zone monitoring means. The central monitor also includes comparator means which accepts the coded bits transmitted to the central monitor over the transmission line and compares each bit of the received code with the corresponding bit of the reference code generated by the reference code generator means. Under normal conditions, that is, whenever the transmission line and all of the protected areas are secure, the sequence of bits received from the zone monitoring means is identical with the sequence of bits provided by the reference code generator means.

However, whenever an alarm code is being transmitted from the alarm multiplexing means, the alarm code will fail to compare with the corresponding bits of reference code sequence, and accordingly an alarm indication will be provided at the central monitor. Thereafter, alarm source identification decoding means of the central monitor is enabled to be responsive to the bits of the alarm source identification code which represent the conditions of the alarm sensors for determining the source of the alarm.

Thus, the alarm transmission system of the present invention provides an alarm indication at the central monitor whenever an alarm is provided by any one or more of the alarm sensors. Thereafter, the origin of the alarm is determined through readout of the alarm storage means to effect the generation of an alarm source identification word comprised of a plurality of bits, each bit of which represents the status of a different alarm sensor.

In a described embodiment of the invention, the code generator means and the reference code generator means are each operable to provide code bits in a known yet pseudo-random sequence. Since the line monitor code thus provided cannot easily be anticipated, the system provides protection from tampering with the alarm transmission line. Severing of the transmission line or the injection of signals onto the line will cause the system to indicate an alarm.

In accordance with a feature of the invention, the alarm multiplexing means is operable in a programmed sequence during a plurality of time slots. The alarm multiplexing means includes sequencing means which is enabled whenever an alarm output is provided by one or more of the alarm sensors to generate signals during different time slots for controlling the sequencing of operations of the alarm multiplexing means.

The alarm multiplexing means further includes means responsive to a first control output provided by the sequencing means to inhibit the transmission of the monitor code to the central monitor so as to indicate that an alarm has been provided by one or more of the alarm sensors. Thereafter, an alarm source identification means of the alarm multiplexing means is enabled by a further output of the sequencing means to generate the alarm source identification code.

The sequencing means further provides a delay in the sequencing of operations of the alarm multiplexing means to enable the transmission of the alarm indication to the central monitor and a further delay for enabling the transmission of the alarm source identification code to the central monitor.

After the alarm code has been transmitted to the central monitor, the sequencing means provides control outputs for restoring the zone monitoring means to the idle condition.

In accordance with a further feature of the invention, the alarm source identification means may include point sequence code generator means which enables preselection of the sequence in which the bits representing the status of the alarm sensors are provided such that the alarm source identification code bits cannot be attributed to a given alarm sensor. A similar point sequence code generator provided at the central monitor allows proper decoding of the point sequence code representing the identification of the alarm sensor providing an alarm output.

The zone monitoring means further includes accesssecure means for permitting the alarm sensors to be selectively operable in either an active or a standby mode and for providing information for transmission to the central monitor to indicate the access-secure status of each alarm sensor.

In a described embodiment of the invention, the alarm transmission system includes remote test generator means at the central monitor selectively operable to provide signals for transmission to the locations of the alarm sensors to selectively enable the alarm sensors so that the performance of each alarm sensor can be tested upon command from the central monitor.

The system provided by the present invention may employ tone generator means operable to provide coded tones to represent the alarm data and the access secure data, the frequencies of the tone signals which comprise such sequences being different to enable simultaneous transmission of the information over a common transmission line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** and **2**, when arranged in a side-by-side relationship, show a block diagram of the multiplexed coded tone transmission system provided by the present invention;

FIGS. **3–6**, when assembled as shown in FIG. **12**, show a schematic representation of the zone monitoring circuits and the alarm sensors associated therewith of the system shown in FIGS. **1** and **2**;

FIG. **7** is a timing diagram showing the relationships for signals provided by circuits of the zone monitoring circuits shown in FIGS. **3–6**;

FIGS. **8–10**, when assembled as shown in FIG. **13**, show a schematic representation of the line monitoring circuits of the system shown in FIGS. **1** and **2**;

FIG. **11** is a schematic representation of one of the alarm sensors of the system shown in FIGS. **1** and **2**;

FIG. **12** shows how FIGS. **3–6** are to be assembled; and

FIG. 13 shows how FIGS. 8–10 are to be assembled.

DESCRIPTION OF A PREFERRED EMBODIMENT

General Description

FIGS. 1 and 2 when arranged in a side-by-side relationship show a block diagram of an exemplary embodiment for a secured intrusion alarm transmission system provided by the present invention. The system comprises zone monitoring circuits **20** shown in FIG. **1**, for effecting the transmission via a transmission line **30** of alarm information provided by a plurality of alarm sources **10** to transmission line monitoring circuits **40** (FIG. **2**) at a central location which is remote from the locations of the alarm sources **10**.

The alarm sources **10** include a plurality of alarm sensors, such as sensors **11–14** shown in FIG. **1**, each located in a different area to be protected. Typically the protected areas may be rooms of a building. Each of the alarm sensors **11–14** may, for example, be an intrusion detector which provides an alarm output in response to the detection of an unauthorized entry of an area protected by such intrusion detector.

The zone monitoring circuits **20** include alarm multiplexing circuits **21** having alarm data storage circuits **22** and associated output gating circuits **23**, and programmed alarm data readout circuits **24**. The alarm data storage circuits **22** comprise a plurality of bistable storage circuits, such as storage circuits **25–28** each associated with a different one of the alarm sensors such as alarm sensors **11–14**, respectively for storage circuits **25–28**. The bistable storage circuits **22**, such as storage circuit **25**, is set by each alarm output provided by the associated alarm sensor, sensor **11** for storage circuit **25**, and will remain set until alarm data indicating that an alarm has been provided by such alarm sensor has been transmitted to the central monitor.

The alarm sensors **11–14** are connected to an associated alarm storage circuits **25–28** via DC supervised lines **31–34**, respectively. Such supervision provides for an alarm responsive to a change of more than 5 percent in a DC current which continuously flows in the lines **31–34**. Thus, opening or shorting of any one of the lines **31–34** will immediately result in an alarm. Alarm information may be provided in the form of contact closures, as is customary in security systems.

The zone monitoring circuits **20** further include a monitor code generator **35** which is driven by a clock **36** at a predetermined rate to generate a line supervisory or monitor code, comprised of a known pseudo-random sequence of logic 1 and logic 0 bits. The monitor code bit sequence provided at the output of the code generator **35** is extended to a tone generator **37** which converts the logic level bits of the line monitor code into tone signals of first and second frequencies coded to represent the monitor code. The sequence of coded tones thus provided is normally continuously transmitted over the transmission line **30** to the transmission line monitoring circuits **40**, shown in FIG. **2**, and the reception of the monitor code by the line monitoring circuits **40** indicates that the transmission line is secure.

Referring to FIG. **2**, the transmission line monitoring circuits **40** include a tone converter circuit **41**, a reference code generator **42** and a code comparator circuit **43**. The tone sequence transmitted from the zone monitoring circuits **20** is received by the tone converter circuit **41** and converted into logic 1 and logic 0 level bits representing the line monitor code generated by code generator **35**.

The reference code generator **42** is driven by clock pulses provided by a clock **44** to generate a reference code which is comprised of a known sequence of bits in which each bit is normally identical with corresponding bits of the line monitor code at any given time. The bits of the line monitor code received from the zone monitoring circuits **20** are compared with corresponding bits of the reference code by the code comparator circuit **43** and under normal conditions, the bits of the monitor and reference codes which are compared will be the same, indicating that the transmission line **30** is secure and that all protected areas are secure.

Due to the pseudo-random nature of the monitor code, it is highly improbable that the monitor code could be duplicated by a person attempting to defeat the system. Thus, tampering with the transmission line **30** such as by cutting the line **30** or attempting to substitute another code for the monitor code, will result in the registration of an alarm at the central monitor.

Referring again to FIG. **1**, whenever an unauthorized intrusion is detected in one or more of the protected areas, such as the area protected by alarm sensor **11**, for example, the alarm sensor **11** will provide an alarm output over the DC line **31** which is connected between alarm sensor **11** and alarm storage circuit **25** which is associated with alarm sensor **11**. The bistable circuit **25** is normally in a reset condition, providing a first logic level output indicating that the corresponding protected area is secure. The bistable circuit **25** is responsive to each alarm output provided by alarn sensor **11** to be switched to a set condition, thereby providing a second logic level output indicating an alarm condition for the corresponding protected area.

The outputs of all of the alarm data storage circuits **22**, including storage circuit **25**, are extended over alarm gates **23a** of the output gating circuits **23** to the alarm data readout circuits **24** and whenever an alarm output is provided by one or more of the alarm sensors **10**, the logic level output of the alarm data storage circuit associated with such alarm sensor will enable the alarm data readout circuits **24** to effect transmission of an alarm indication to the central monitor.

The alarm multiplexer circuits **21** of the zone monitoring circuits **20** are operable to continuously monitor the alarm status of all of the alarm sensors **10** and whenever an alarm output is provided by one or more of the alarm sensors, the alarm multiplexer circuits effect the transmission of alarm data to the central monitor to indicate an alarm condition for one of the protected areas and the source of the alarm.

The alarm multiplexing circuits **21** are operable in a programmed sequence during seven time slots as summarized in Table I.

TABLE I

TIME SLOT	OPERATION
T0	Monitor alarm sensors
T1	Inhibit monitor code transmission
T2	Transmit alarm indication
T3	Initiate alarm source identification
T4	Transmit alarm source identification data
T5	Reset alarm data storage circuits
T6	Reinitiate monitor code transmission

During the first time slot T0 which represents the idle condition for the alarm multiplexing circuits **21**, the alarm sensors **10**, including alarm sensor **11**, are continuously monitored, and the monitor code generated by monitor code generator **35** is transmitted to the central monitor.

The alarm output provided by any of the alarm sensors, such as alarm sensor **11**, responsive to an intrusion of the area protected by such alarm sensor is provided during time **T0**. Such alarm output effects the setting of the corresponding alarm data storage circuit, storage circuit **25** for alarm sensor **11**, to provide an enabling output for the alarm data readout circuits **24**. The alarm data readout circuits **24**, under the control of a sequencing circuit **50**, effect the generation of an alarm code which includes an output indicating that an alarm has been provided by one or more of the alarm sensors **10** and an alarm source identification bit sequence for indicating the source of the alarm. The alarm code is substituted for the monitor code during times T1–T6, to permit transmission of the alarm information to the central monitor.

The sequencing circuit **50** is responsive to an alarm output extended thereto over the output gating circuits **23***a* to provide a series of control signals during time slots T1–T6, for controlling a tone generator disable circuit **51** and an alarm source identification code generator circuit **52** of the alarm data readout circuits **24**.

Thus, for example, assuming alarm sensor **11** provides an alarm output indicating an unauthorized intrusion of the area protected by alarm sensor **11**, the corresponding alarm data storage circuit **25** will be set, providing an alarm indicating output during time slot **T0**. The alarm indicating output of storage circuit **25** is extended over the alarm gates **23***a* of the output gating circuits **23** to the sequencing circuit **50** of the alarm data readout circuits **24**. The sequencing circuit **50** is responsive to such output to generate a control signal at time T1 for the tone generator disable circuit **51** which is operable to disconnect the output of the code generator **35** from the input of the tone generator **37** during times T1–T6, thereby interrupting the transmission of the monitor code to the central monitor and to inhibit the tone generator for a predetermined time interrupting the transmission of tone signals to the central monitor during time slot T2.

At time T3, the sequencing circuit **50** provides an output for enabling the alarm source identification code generating circuit **52** to generate an alarm source identification code for transmission to the central monitor during time T4. The alarm source identification circuit **52** may comprise a parallel-to-serial converter which scans the alarm data storage circuits, including circuits **25–26** to provide a logic level output as each alarm data storage circuit is scanned, with each output provided representing the condition of the alarm storage circuit being scanned.

The alarm data storage circuits **22** may be scanned in sequence such that successive bits of the point identification code represent the data stored in consecutive storage circuits **25, 26, . . . 27, 28,** or, alternatively, a point sequence generator circuit **57** may be employed for controlling the alarm source identification circuit **52** to scan the data storage circuits **22** in a non-consecutive order, but in a known sequence to make the identification of the alarm source being scanned more difficult to a person attempting to compromise the alarm transmission system.

The bits of the alarm source identification code provided by the identification code generator **52** are extended to the tone generator **37** to effect the generation of tone signals of first and second frequencies in a sequence coded to represent the alarm source identification code. The tone sequence provided by the tone generator is transmitted to the central monitor over the transmission line **30**.

Referring to FIG. **2**, whenever the transmission of tone signals is interrupted as the result of an alarm output provided by one or more of the alarm sensors **10**, the loss of tone, when detected at the central monitor, will cause the code comparator circuit **43** of the line monitoring circuits **40** to provide an output for enabling an alarm circuit **46** of an alarm module **45** to indicate an alarm condition for one or more of the protected areas. Thereafter, the tone sequence representing the alarm source identification code is received by the tone converter **41**, converted to a logic level sequence and passed to an alarm source identification decoder **47** to enable decoding of the alarm source identification bit code sequence transmitted to the central monitor from the zone monitoring circuits **20** and the identification of the source of the alarm.

The alarm source identification decoder circuit **47** may comprise a serial-to-parallel converter which is operable to gate successive bits of the alarm source identification code to different alarm circuits, including alarm circuits **48***a–48d*, of the alarm module **45**. A separate alarm circuit, such as circuits **48***a–48d* is provided for each of the alarm sensors, such as alarm sensors **11–14** respectively. The bits of the alarm source identification code which represent the status of an alarm sensor, such as alarm sensor **11**, which is providing an alarm output, will enable the alarm circuit associated with such alarm sensor to provide an alarm indication at the central monitor to thereby indicate the source of the alarm. It is pointed out that if a point sequence code generator **57** is used at the zone monitoring circuits **20** to modify the sequence in which the alarm data storage circuits **22** are scanned, the alarm source identification decoder circuit **47** would have associated therewith a further point sequence generator **49**, which is identical with point sequence generator **57**, for enabling proper decoding of the alarm source identification code.

Referring again to FIG. **1**, after all of the point identification code bits have been transmitted to the central monitor, the sequencer circuit **50** provides an output during time slot T5 for effecting the reset of all of the alarm storage circuits **22** and thereafter at **T6**, reset of the code generator disable circuit **51**, thereby returning the alarm multiplexing circuits **21** to the idle condition and reinitiating the transmission of the monitor code to the central monitor.

In the foregoing general description of the alarm transmission system, the alarm sensors **10** and associated zone monitoring circutis **20** were described as being operable in a secure mode, and as such, were responsive to the detection of any human movement within the corresponding protected area to provide an alarm output for effecting the registration of an alarm at the central monitor. During certain periods of time, however, it may be necessary to permit movement of an authorized person within a given protected area while the alarm system is energized. For example, when

the alarm transmission system is used in an application for monitoring the conditon of rooms in a school, an authorized person, such as a janitor or a repairman, should be allowed access to the protected area at night.

Accordingly, the zone monitoring circuits **20** includes a plurality of access-secure switches **60** including an individual access-secure switch for each of the alarm sensors. Thus, for example, alarm sensors **11–14** have associated therewith access-secure switches **61–64,** respectively. Each access-secure switch such as access secure switch **61,** is a limited access two-position switch, which is located at the site of the alarm sensor **11,** as for example, on a wall outside of a room protected by alarm sensor **11.** The access-secure switch **61** controls the associated alarm sensor **11** to be operable in either a secure mode of an access mode. Whenever the switch **61** is set in the secure position, the alarm sensor **11** will be responsive to any human movement within the area protected by the alarm sensor **11** to provide an alarm output indicative of the detection of an unauthorized intruder within the protected area, and the movements of such intruder will cause the registration of an alarm at the central monitor in the manner described in the foregoing.

However, when the access-secure switch **61** is set to the access position, the alarm sensor **11** associated with access-secure switch **61** will be disabled and will not respond to movements detected with the protected area.

In order to enable the access-secure status of the alarm sensors, including alarm sensors **11–14,** to be made known at the central monitor, the zone monitoring circuits **20** include access-secure condition-monitoring circuits **65** which periodically scan the access-secure switches **60** and generate a sequence of tone signals coded to represent the status of all of the access-secure switches **60** and hence of the alarm sensors **10.**

The access-secure condition monitoring circuits **65** include a scanner circuit **66** controlled by clock pulses provided over a pulse divider circuit **67** from the clock **36** which controls the code generator **35.** Since the access-secure information does not have the same degree of importance as the alarm information provided by the alarm multiplexer **21,** the conditions of the access-secure switches **60,** including switches **61–64,** are scanned at a slower rate than the rate at which the bits of the monitor code are generated. The slower rate is provided through the use of the clock pulse divider circuit **67.** The access-secure switches **60,** including access-secure switches **61–64,** are connected to the scanner **66** over a cable **68** which provides separate paths for each switch to the scanner **66.** Each access secure switch is adapted to provide a first output over cable **68** when such switch is set in the access mode position and a second output when such switch is set in the secure mode position.

As each access-secure switch is scanned, the scanner **66** extends the output representative of the condition of the switch being scanned to an access-secure tone generator **69** which provides a tone output of a first frequency for each output representing an access mode position for a switch being scanned, a tone output of a second frequency for each output representing a secure mode for a switch being scanned. The tone sequence thus provided represents the access-secure status of all of the switches **60** being scanned. The access-secure switches **60** may be scanned sequentially, i.e., switch **61,** then switch **62, . . . 63, 64,** or alternatively, through the use of a point sequence code generator **70,** the switches **60** may be scanned in a non-consecutive yet known sequence and accordingly, the access-secure information as transmitted from the zone monitoring circuits **20** could not be attributed to a specific alarm sensor location.

In order to enable simultaneous transmission of the tone sequence representing access-secure data provided by the access-secure condition monitoring circuits **65** to the central monitor over a common transmission line, the frequencies of the tone signals provided by the tone generator **69** of the access-secure monitoring circuits **65** are chosen to be different from the frequencies of the tone signals provided by the tone generator **37** of the alarm multiplexer circuits.

The tone sequence representing the access-secure code generated by the access-secure monitoring circuits **65** is transmitted over transmission line **30** to the central monitor and is received by the tone converter circuit **41** of the transmission line monitoring circuits **40.** The tone converter circuit **41** converts the received tone sequence to a sequence of logic level signals and extends the sequence of logic level bits to an access-secure decoder circuit **71** which routes each bit of the access-secure code to a different alarm circuit of the alarm module **45.** The access secure decoder **71** is controlled by clock pulses supplied thereto over pulse divider **72** from clock pulse generator **44** and is operable at the same rate as the scanner **66** at the zone monitoring circuits **20.**

The alarm module **45** includes a separate access-secure indicator for each alarm sensor. The access-secure indicators are enabled as a function of the bits of the access-secure code received from the zone monitoring circuits **20.** Thus, as the sequence of bits representing the status of the access-secure switches **60,** and correspondingly alarm sensors **10,** is received, the access-secure decoder **71** (under the control of the point sequence code generator **73,** if point sequence code generator **70** is used at the zone monitoring circuits **20**) will provide a separate output for each alarm circuit of the alarm module **45,** including alarm circuits **48***a*–**48***d* corresponding to alarm sensors **11–19,** respectively, such that the alarm circuit associated with a given alarm sensor will provide a first indication whenever the corresponding alarms sensor is operating in the secure mode and a second indication whenever the corresponding alarm sensor is operating in the access mode.

The alarm transmission system also includes provision for remote testing of the alarm sensors **10** to determine if all of the alarm sensors are operating properly. Accordingly, a remote test signal generator **74** at the central monitor is operable, when enabled, to transmit a test command signal over the transmission line **30** to the alarm multiplexing circuit **21** at the locations of the alarm sensors **10.** The frequency of the test signal is different from the frequencies of the signals provided by the tone generator **37** of the alarm multiplexing circuits **21** and the tone generator **69** of the access-secure condition monitoring circuits **65.**

The alarm multiplexing circuits **21** include a test signal detecting circuit **75** which receives the test signals and is responsive to each test signal extended thereto

to extend enabling signals to each of the alarm sensors **10** to simulate intrusions in the areas protected by the alarm sensors **10.**

Each of the alarm sensors **10,** including sensors **11–14,** is responsive to the enabling signals extended thereto to provide an alarm output. The alarm outputs thus provided effect the generation of an alarm code by the alarm multiplexing circuits **21** for transmission to the control monitor to register appropriate alarm indications at the central monitor in the manner set forth in the foregoing.

DETAILED DESCRIPTION

A schematic representation of the zone monitoring circuits **20** and the alarm sensors **10** associated therewith is shown in FIGS. **3–6** when arranged in a side-by-side relationship as shown in FIG. **14.** For purposes of illustration of the operation of the zone monitoring circuits **20,** including the slarm multiplexing circuits **21** and the access-secure condition monitoring circuits **65** it is assumed that the zone monitoring circuits **20** monitor twenty alarm sensors, including sensors **11–14** shown in FIG. **3.**

The nature of many commercially available alarm sensors is such that separate alarm indications (as represented, for example, by changes in relay contact states) are available for intruder detection and for supervisory indication of sensor component malfunctions. The alarm multiplexing circuits **21** include alarm storage circuits **22** which provide separate storage for both types of sensor information.

Accordingly, the alarm storage circuits **22** include flip flops **25***a*–**28***a* which store intrusion alarm outputs provided by sensors **11–14,** respectively in response to the detection of an unauthorized entry of the areas protected by sensors **11–14,** and flip flops **25***b*–**28***b*, which store supervisory alarm outputs provided by sensors **11–14** as the result of component malfunctions of sensors **11–14.**

The intrusion alarm output of sensor **11** is connected over a DC supervised line **31***a* and a NOR gate **81** to the set input of the alarm flip-flop **25***a* associated with sensor **11.** The supervisory output of the sensor **11** is connected over a DC supervised line **31***b* and a NOR gate **82** to the set input of the supervisory flip flop **25***b* associated with sensor **11.**

Similarly, the alarm outputs of sensors **12–14** ar connected over respective D.C. supervised lines **32***a*–**34***a* and NOR gates **81***a*–**81***c* to the set inputs of alarm flip flops **26***a*–**28***a*, and the supervisory outputs of sensors **12–14** are connected over respective D.C. lines **32***b*–**34***b* and NOR gates **82***a*–**82***c* to the set inputs of supervisory flip flops **26***b*–**28***b*, respectively.

A logic 1 level signal on lines **31***a*–**34***a* or **31***b*–**34***b* represents a normal condition, and a logic 0 level on one or more of the lines **31***a*–**34***a* or **31***b*–**34***b* indicates that an intrusion or supervisory alarm indication is being provided by the sensor connected to such line.

An enabling signal at a logic 0 level is normally extended over conductor **83** from the alarm data readout circuits **24** to each of the NOR gates including gates **81, 81***a*–**81***c*, **82***a*–**82***c*, **82.** Accordingly, whenever one or more of the alarm sensors, such as alarm sensor **11,** provides an intrusion alarm output over conductor **31***a* or a supervisory alarm output over conductor **31***b*, such alarm outputs will enable the NOR gates **81** or **82** connected to conductors **31** and **31***b*, respectively. Whenever NOR gate **81** is enabled, the alarm flip flop **25***a* will be set and whenever NOR gate **82** is enabled the supervisory flip flop **25***b* will be set. The alarm flip flop **25***a* and the supervisory flip flop **25***b*, when set in response to an alarm indication by the associated sensor **11,** will remain set, storing such alarm indications until reset by the alarm data readout circuits **24.** Thus, an alarm indication provided by any of the alarm sensors **10,** such as sensor **11,** will be stored in the alarm storage circuits **22** until the alarm indication has been transmitted to the central monitor.

Each of the alarm storage flip flops, including flip flops **25***a*–**28***a*, and each of the supervisory flip flops, including flip flops **25***b*–**28***b*, normally provide a logic **0** output whenever associated alarm sensors **11–14** are not providing an alarm output.

The outputs provided by the alarm storage flip flops **25***a*–**28***a* and the supervisory flip flops **25***b*–**28***b* are combined by alarm gates **23***a*, including gates **84–86,** of the output gating circuits **23.** For example, the outputs of the alarm flip flops, such as flip flops **25***a*–**28***a*, are extended via cable **87** to separate inputs of a NOR gate **84.** The outputs of the supervisory flip flops, such as flip flops **25***b*–**28***b*, are extended via cable **88** to separate inputs of a NOR gate **85.** The outputs of NOR gates **84** and **85** are individually connected to inputs of a NAND gate **86.**

Whenever all of the alarm storage flip flops, including flip flops **25***a*–**28***a*, and all of the supervisory flip flops, including flip flops **25***b*–**28***b*, are in a reset condition, representing an idle condition for the alarms multiplexing circuits **21,** NOR gates **84** and **85** will be enabled to thereby enable alarm gate **86.** NOR gate **84** will be disabled to thereby disable alarm gate **86** whenever an alarm output is stored in one or more of the alarm flip flops, and NOR gate **85** will be disabled to thereby disable alarm gate **86** whenever an alarm output is stored in one or more of the supervisory flip flops. The alarm multiplexing circuits **21** are operable in the alarm mode whenever alarm gate **86** is disabled.

Whenever alarm gate **86** is disabled, gate **86** provides an output which enables the alarm data readout control circuits **24** (FIG. **6**) to generate an output indicating that an alarm has been provided and to thereafter effect readout of the alarm data stored in the alarm data storage circuits **22** and the transmission of such data to the central monitor to permit identification of the source of the alarm.

CODE GENERATOR

Whenever all of the protected areas are secure and all of the alarm sensors, such as alarm sensors **11–14,** are operating properly, the alarm multiplexing circuits **21** are operable in the idle mode during time slot TO, and accordingly, the monitor code generated by the monitor code generator **35** shown in FIG. **6,** is transmitted over the transmission line **30** to the central monitor.

One code generator suitable for this purpose is described in the copending application U.S. Ser. No. 193,450 of John C. Donovan, Ramesh Krishnaiyer and Frank J. Esser, which was filed on Oct. 28, 1971.

In an exemplary embodiment, the code generator **35** includes a four stage shift register **90** having feedback connections over conductors **91** and **92** from the first and fourth stages, respectively, connected through an

Exclusive OR circuit **93** to the input of the first stage. The Exclusive OR circuit **93** provides a logic 0 output whenever the two inputs to the Exclusive OR circuit are at the same logic level, and provides a logic 1 output whenever the inputs are at different logic levels. Code generator **35** preferably includes at least a sixteen stage register and may be as much as a thirty-two stage register capable of generating a pseudo-random sequence of bits, the length of the sequence being given by the relationship 2^n-1, where N is the number of stages which comprise the shift register **90** of the code generator circuit **35.** In the present example, for convenience only, a four stage register **90** is shown, and 15 bits are provided.

To illustrate the operation of the code generator **35,** it is assumed that initially all stages of the register **90** store logic 1 level bits and that the register **90** is thereafter cycled under the control of clock pulses provided by a clock pulse generator **36.** The sequence of words given in Table II will appear in the stages of the shift register **90** as successive clock pulses are provided.

TABLE II

	Register Stage	1	2	3	4
	(Initial)	1	1	1	1
Clock Pulse					
1		0	1	1	1
2		1	0	1	1
3		0	1	0	1
4		1	0	1	0
5		1	1	0	1
6		0	1	1	0
7		0	0	1	1
8		1	0	0	1
9		0	1	0	0
10		0	0	1	0
11		0	0	0	1
12		1	0	0	0
13		1	1	0	0
14		1	1	1	0
15		1	1	1	1

Since initially the first and fourth stages both contain binary ones, the Exclusive OR circuit **93** provides a logic 0 output which is gated into the first stage of the shift register **90** with receipt of the first clock pulse as can be seen in Table II. The clock pulse also shifts the logic 1's from the first to third stages to the second to fourth stages, respectively. When the second clock pulse is received, the outputs of the first and fourth stages are different, and accordingly the "Exclusive Or" circuit **93** will provide a logic 1 output which will be gated into first stage of the shift register **90.**

The random bit sequence generated by the code generator **35** is extended to an input of an AND gate **94** which has a second input connected to the output of an alarm flip flop **99** of the tone generator disabling circuit **51.**

Under normal conditions, that is, whenever no alarm indications are being provided by the alarm sources **10,** the alarm flip flop **99** is set, providing an enabling input for AND gate **94** whereby AND gate **94** follows the bits of the monitor code provided by code generator **35** and provides a logic 1 level output for each logic 1 level bit of the monitor code sequence and a logic 0 level output for each logic 0 level bit of the monitor code sequence.

The sequence of logic 1 and logic 0 level bits provided at the output of the AND gate **94** is extended over an OR gate **95** to the input of the tone generator **37.**

The tone generator **37** may comprise a conventional frequency shift keyed oscillator (FSK) which normally provides a tone output of a first frequency F*a*, whenever a control signal at a logic 0 level is supplied to the input of the oscillator circuit. The oscillator circuit is responsive to a control signal at a logic 1 level to provide a tone output which is shifted in frequency by a predetermined amount F*a* + F*o* providing a signal of a second frequency F*b*. Thus, the FSK oscillator is responsive to coded sequence of logic 1 and logic 0 level bits supplied thereto by the code generator **35** to provide tones of frequencies F*a*and F*b* in a sequence coded to represent the bits of the monitor code for transmission to the central monitor over the transmission line **30.**

The transmission line **30** may, for example, comprise a pair of standard 4 KHz bandwidth telepone lines. Since such lines have a transmission frequency range of 500 Hz to 3KHz, the base frequency F*a* of the oscillator and the second frequency F*b* are selected to be within the range of 500 Hz to 3KHz.

The output of the tone generator **37** is connected to an input of a summing amplifier **96,** the output of which is connected to the transmission line **30** to pass the tone sequence to the line **30** for transmission to the central monitor. The monitor code tone sequence will be transmitted to the central monitor as long as all the protected areas are secure.

On the other hand, whenever an alarm output is provided by one of the alarm sensors **10,** such as alarm sensor **11,** the associated alarm flip flop **25***a* for sensor **11** will be set, providing a logic 1 output which is extended via conductor **87***a* of cable **87** to NOR gate **84,** enabling gate **84.** Whenever gate **84** is enabled, the gate **84** provides a logic 0 output which disables alarm gate **86.** The logic 1 output provided whenever NAND gate **86** is disabled, is extended to the sequencing circuit **50** of the alarm data readout circuits **24.**

Sequencing Circuit

The sequencing circuit **50** provides enabling signals defining time slots T1–T6 to permit the generation of the alarm code including an alarm indication output and an alarm data output sequence representing the status of each of the alarm sensors **10.** The sequencing circuit **50** includes a plurality of logic timing elements **101–106,** shown in block form in FIG. **6,** which provide a set of enabling pulses in a programmed sequence during time slots T1–T6 for controlling the operation of the alarm data readout circuits **24** while the alarm multiplexing circuits **21** are operable in the alarm mode. The logic timing elements **101–106** may, for example, be monostable multivibrators of the type SN74121 commercially available from Texas Instruments.

Referring to the timing diagram given in FIG. **7,** in response to an alarm output provided by alarm sensor **11** over line **31***a* during time slot TO, NOR gate **81** will be enabled, providing a logic 1 level output (shown in line **1** of FIG. **7**). The logic 1 level output provided by gate **81** sets the alarm storage flip flop **25***a* which then provides a logic 1 level output (line **2,** FIG. **7**) to effect enabling of alarm gate **86.** The output of gate **86** (shown in line **3** of FIG. **7**) is extended to a monostable circuit **101** of the sequencing circuits **50** which after a short transition delay provides an output (FIG. **7,** line **4**) over conductor **107** defining time slot T1, for en-

abling the alarm monostable circuit **98** and the alarm flip-flop **99.**

The alarm monostable circuit **98** when enabled, provides an output (line **5,** FIG. **7**) of a predetermined duration over conductor **108** which output disables the tone generator **37** and inhibits the generation of a tone output by the tone generator **37** for the duration of the monostable circuit **98** as indicated in line **14** of FIG. **7.** Such absence is indicative of an alarm condition at the zone monitoring circuits **20** as will become apparent hereinafter.

The enabling signal provided by monostable **101** over conductor **107** is also extended over conductor **107***a* to alarm flip flop **99,** resetting flip flop **99** providing a logic 0 output over conductor **109** as shown in line **6** of FIG. **7.** The logic 0 output provided by the alarm flip flop **99** over conductor **109** disables AND gate **94** to thereby preclude the passage of code bits provided by the code generator **35** to the tone generator **37.** The output on conductor **107** is also extended to a monostable **102** which provides a delay during time slot T2, for the duration of the output of the monostable circuit **98,** to permit transmission of the alarm condition, as indicated by a loss of tone, to the central monitor.

The output of monostable **102** is extended to a first input of an AND gate **110** which has a second input provided by the output of monostable circuit **98** over conductors **108** and **108***a* and an inverter **108***b*. Gate **110** will be enabled when the monostable **98** times out. At such time, the output **111** of gate **110** will be extended to a monostable **108** which provides an output (line **7,** FIG. **7**) over conductor **112,** defining time slot T3, for enabling the alarm source identification code generating circuit **52.** The output of monostable **103** is also extended to an input of monostable circuit **104** enabling monostable **104** to provide a logic 1 level output which is extended to an input of an AND gate **133.**

Alarm Source Identification Circuit

The alarm source identification code generating circuit **52** is operable to effect readout of the contents of the alarm flip flops, such as flip flops **25***a*–**28***a*, and the supervisory flip flops, such as flip flops **25***b*–**28***b* which comprise the alarm storage data circuits **22.** The outputs of all the alarm data flip flops **22** are extended over output identification gates **23***b* to the alarm source identification generator circuit **52.**

The output identification gates **23***b* comprise a plurality of OR gates, including OR gates **120–123** shown in FIG. **3.** The output identification gates **23***b* provide a separate OR gate for each pair of alarm data storage flip flops, the output of each OR gate providing a scan point for the data stored in an associated pair of flip flops. Thus, for example, the outputs of the alarm storage flip flop **25***a* and the corresponding supervisory storage flip flop **25***b* associated with alarm sensor **11** are connected to separate inputs of OR gate **120.** Similarly, the outputs of alarm flip flop **26***a* and supervisory storage flip flop **26***b*, associated with alarm sensor **12,** are connected to inputs of OR gate **121,** etc.

Each output identification gate, such as gates **120–123,** provides a logic 0 output whenever both inputs are at logic 0 level (representing an idle condition for the corresponding alarm sensor) and a logic 1 output whenever either output is at a logic 1 level (representing an alarm condition for the corresponding alarm sensor).

The alarm source identification code generating circuit **52** comprises a parallel-to-serial converter, which is comprised of a multi-stage shift register **124** and a plurality of gate circuits **129,** including AND gates **125–128** shown in FIG. **4** and an OR gate **130.** In the present example, wherein the data stored in 20 pairs of flip flops, such as flip flops **25***a* and **25***b*, is to be readout, the alarm source identification code generating circuit **52** includes 20 AND gates **129,** four of which are shown in FIG. **4,** each AND gate being individually associated with one of the output OR gates **23***b*.

The output of each of the OR gates **23***b* is individually extended to an input of a different one of the AND gates **129** of the alarm source identification code generating circuit **52.** For example, the outputs of OR gates **120–123** are individually connected to first inputs of AND gates **125–128,** respectively. The outputs of the AND gates **129** are individually connected to a separate input of OR gate **130.**

In an exemplary embodiment, the shift register **124** comprises a 24 stage shift register connected as a ring counter having the output stage **124***x* fed back to the input stage **124***a*. Each of the stages of the register **124,** including stages **124***a*–**124***e* and **124***v*–**124***x*, shown in FIG. **4,** have clock inputs connected to an output of an oscillator circuit **117** to receive clock pulses provided by the oscillator **117** whenever the oscillator **117** is enabled. The oscillator is enabled at time T3 by an output extended to an input of the oscillator **117** over conductor **112** from monostable circuit **103.**

An output **114***a* of the first stage **124***a* of the register **124** is connected to an input of a sync pulse generator circuit **114.** The sync pulse generator circuit **114** may, for example, be a monostable circuit operable when enabled to provide a pulse (shown on line **9** of FIG. **7**) of a predetermined duration, the duration of three clock pulses in the present example. The sync pulse, provided by sync pulse generating circuit **114,** is extended over OR gate **130,** a pulse line **116** and or gate **95** to the input of the tone generator **37.** The sync pulse enables the tone generator **37** to generate an output tone at frequency F*b*, for example, (as indicated in line **14** of FIG. **7**), the duration of the tone being determined by the width of the sync pulse provided by the sync pulse generating circuit **114.**

The sync tone is transmitted to the central monitor over the transmission line **30** to enable the alarm source identification decoder circuit **47** of the line monitoring circuits **40** to be responsive to the bits of the alarm source identification code provided by the alarm source identification code generating circuit **52.**

Intermediate stages of the register including stages **124***d*, **124***e*, **124***v* and **124***w* shown in FIG. **4,** have outputs individually connected over a point sequence code generator **57** to second inputs of a different one of the twenty AND gates, gates **125–129,** respectively. An output **133***a* of the last stage **124***x* of the register **124** is connected to an input of AND gate **133** which has a second input connected to the output of monostable circuit **104.**

In operation, one of the stages of the ring counter **124** normally contains a logic 1 level bit, and the remaining stages normally contain logic 0 level bits. The logic 1 level bit, which is assumed to be initially stored in the last stage **124***x* of the register **124** is shifted to the first stage **124***xa* of the register **124** when the first clock

pulse is provided by oscillator **117** when the oscillator is enabled at T3 by an output on conductor **112** and is thereafter shifted sequentially from stage to stage responsive to further pulses supplied to the clock inputs of the ring counter stages by the oscillator circuit **117** during time T4.

Accordingly, with the receipt of the first clock pulse, the logic 1 level bit is shifted into the first stage **124***a* of register **124**, and the logic 1 level output provided by stage **124***a* will enable the sync pulse generating circuit **114** to provide a sync pulse, which is extended over OR gate **130**, bit line **116** and OR gate **95** to the tone generator **37**. The tone generator **37** will be responsive to the sync pulse to generate a tone of frequency F*b* for transmission to the central monitor over the transmission line **30**. The logic 1 level bit stored in stage **124***a* will be shifted to stages **123***b* and **123***c* responsive to the second and third clock pulses, respectively, providing a delay while the synce pulse is being transmitted to the central monitor.

When the fourth clock pulse is provided, the sync pulse will have terminated and the logic 1 level bit stored in the third stage **124***c* of the register **124** will be shifted to the fourth stage **124***d* of the register. Accordingly, a logic 1 level output of the fourth stage **124***d* of the register **124** will provide an enabling input for AND gate **125**, permitting the logic 1 or logic 0 output supplied to AND gate **125** by identification gate **120** to be gated to OR gate **130**.

In the present example, it is assumed that only alarm sensor **11** is providing an alarm output, and accordingly, the output of identification gate **120** associated with alarm sensor **11** will be at a logic 1 level, and the outputs of the remaining identification gates, including gates **121–123** will be at logic 0 levels.

Thus, when AND gate **125** is enabled by the logic 1 level output provided by register **124**, the logic 1 level bit will be gated to an input of OR gate **130**.

Thereafter, with successive clock pulses, the logic 1 level bit stored in the shift register **124** will be shifted from stage to stage sequentially enabling the remaining AND gates of the alarm source identification circuits **52** including AND gates **126–128** to gate the logic 0 level outputs supplied to each of the AND gates **125–128** from the corresponding identification gates **121–123** to an input of OR gate **130**.

The sequence of logic 1 and logic 0 pulses provided at the output of OR gate **130** as a result of the scanning of the alarm storage circuits **22** by the alarm source identification generator **52** represents an alarm source identification code indicating the alarm status of all of the alarm sensors **10**. The logic 1 and logic 0 bits of the alarm source identification code are extended over pulse line **116** and OR gate **95** to the input of the tone generator **37**. The bits of the alarm source identification code control the tone generator **37** to provide an output tone sequence comprised of tones of frequencies F*a* and F*b* in a sequence coded to represent the logic 0 and logic 1 bits, respectively, of the alarm source identification code. The alarm source identification code tone sequence (shown in line **14** of FIG. 7) thus provided is transmitted over the transmission line **30** to the central monitor.

Point Sequence Code Generator

In order to provide additional security for the alarm sensor identification information while such information is being transmitted from the zone monitoring circuits **20** to the central monitor, the alarm multiplexing circuits **21** may include a point sequence code generator **57** for altering the sequence in which alarm output data points (outputs of output identification gates **23***b*).

Thus, in accordance with an exemplary embodiment the point sequence code generator **57** may comprise a plug board **58** having a plurality of input terminals **58***ia–58it* and a plurality of output terminals **58***oa–58ot*, interconnected in pairs by a plurality of straps **59**. Each of the input terminals **58***ia–58it* is individually connected to the output of one of the intermediate stages (i.e., the fourth through twenty-third stages) of the shift register **124**. Each of the output terminals **58***oa–58ot* is individually connected to the input of one of the AND gates **129**, including gates **125–128**, of the alarm source identification generator **52**.

In the exemplary illustration of the point sequence code generator **57** shown in FIG. **4**. The input terminals **58**ia-**58**it and the output terminals **58***oa–58ot* are shown interconnected to provide consecutve enabling of the AND gates **125, 126, . . . 127, 128**, and thus consectuive readout of the alarm data storage circuits **22**. However, the sequence in which the alarm data output points are scanned can be altered by modifying the connections between the input and output terminals of the plug board **58**.

With this feature, the identification of the information provided by a particular alarm sensor is rendered virtually impossible.

While the point sequence code generator **57** is shown in one embodiment as a plug board **58** including removable interconnecting straps **59**, the point sequence code generator may also comprise an arrangement of switches or some other mechanically or electrically alterable connections scheme or a card reader, depending upon the number of scan points provided by the alarm storage **22**.

Reset of Alarm Multiplexer

The alarm data bits are read out by the alarm source identification generator **52** during time slot T4 and transmitted to the central monitor in the form of coded frequency signals (line **14**, FIG. 7) provided by the tone generator **37** under the control of the output of the alarm source identification generator **52**.

In the present example wherein it is assumed there are 20 alarm sensors, such as sensors **11–14** and correspondingly 20 alarm data storage locations such as storage circuits **25–28**, all of the data storage locations of the alarm storage circuits **22** will have been scanned and the alarm data provided transmitted to central monitor after the 23 clock pulse is provided by the oscillator **117**. At the 24 clock pulse, an output of the last stage **124***x* of the register **124**, representing end of scan, will be extended to gate **133** which has a second input provided by a monostable circuit **104** to enable gate **133**. Monostable **104**, which is enabled at time slot T3 by an output of monostable **103** is providing a logic 1 level signal at one input of gate **133**. Accordingly, gate **133** provides an output for enabling a monostable circuit **105** to provide an output over conductor **83** for resetting the alarm data storage flip flops **22** during time slot T5.

The output of monostable **105**, shown in line **12** of FIG. **7**, is extended over conductor **83** to the NOR gates, including gates **81**, **81***a*–**81***c* and **82**, **82***a*–**82***c*, which are connected to the set inputs of the alarm data storage flip flops **22**, disabling the NOR gates. The output on conductor **83** is further extended over conductor **83***a* to the reset inputs of all of the alarm data storage flip flops **22** causing the flip flops to be reset.

Thus, as shown in line **2** of FIG. **7**, the alarm storage flip flop **25***a* associated with alarm sensor **11** will be reset by the output provided by monostable **105** at time T**5**, and the output of flip flop **25***a* will return to a logic 0 level. It is pointed out that even though the alarm output of alarm sensor **11**, ceased prior to the transmission of the entire alarm code by the alarm multiplexing circuits **21**, the corresponding alarm flip flop **25***a* remained set until the reset signal was supplied by the sequencing circuit **50**.

When the alarm data storage flip flops **22** are reset, the output of monostable circuits **101** and **103** (lines **4** and **7**, respectively of FIG. **7**) go to logic 0 level, and at such time, oscillator **117** is deenergized and no further clock pulses are provided as shown in line **8** of FIG. **7**.

The output of monostable **105** is also extended to a monostable **106** which then provides an output over conductor **134** at time T**6**. The output of monostable **106**, shown in line **13** of FIG. **7**, is extended over conductor **134** to the set input of the alarm flip flop **99**, setting the alarm flip flop **99** which provides a logic 1 level output as shown in line **6** of FIG. **7**, to enable AND gate **94** to connect the output of the code generator **35** to the input of the monitor tone generator **37** over OR gate **95**. Accordingly, the alarm multiplexing circuits are returned to the idle condition and the monitor code is again transmitted to the central monitor.

It is pointed out that if the alarm sensor **11**, or any other alarm sensor, were providing an alarm output at the end of time slot T**5**, the alarm storage device **25***a* will not be responsive to the set signal supplied by monostable circuit **105** and the alarm data readout sequence, beginning with time slot T**1**, will be reinitiated.

Alarm Monitoring Circuits

The coded tone sequences, including the monitor code and the alarm code sequences, provided by the zone monitoring circuits **20** are transmitted via transmission line **30** to the transmission line monitoring circuits **40** (FIGS. **8**–**10**) at the central monitor.

Referring to FIG. **8**, the transmission line monitoring circuits **40** comprise a tone converter circuit **41** including a tone filter circuit **140** having an input connected to the transmission line **30** and a tone detecting circuit **141** connected to the output of the tone filter **140**. The tone filter **140** is tuned to pass only signals of frequencies F*a* and F*b* and the tone detecting circuit **141** is responsive to each signal at frequency F*b* to provide a logic 1 level output.

The output of the tone detector **141** is extended to a code comparator circuit **43** which compares the bits of the received sequence of code bits with corresponding bits of a reference code provided by a reference code generator **42**. The reference code generator **42** is similar to the code generator **35** of the zone monitoring circuit **20** and operates in synchronism with code generator **35** to provide a sequence of random bits in which each bit is normally identical with a corresponding bit of the random bit sequence at any given time. In an exemplary embodiment, the reference code generator **42** comprises a four-stage shift register **150** having outputs of the first and fourth stages fed back over an Exclusive OR circuit **151** to the input of the first stage. The reference code generator **42** is driven by clock pulses provided by a clock pulse generator **44** to provide the sequence of random bits shown in Table II that is provided by the code generator **35**.

The code comparator circuit **43** includes a pair of flip flops **152**, **153**, and an Exclusive OR gate **154**. The set input of flip flop **152** is connected to the output of tone detector circuit **141**. The set input of flip flop **153** is connected to the output of the reference code generator **42**. Clock inputs *c* of flip flops **152** and **153** are connected to the output of the clock pulse generator **44**. The outputs of the flip-flops **152** and **153** are extended to separate inputs of the Exclusive OR gate **154**.

The Exclusive OR gate **154** of the code comparator circuit **43** provides logic 0 output whenever corresponding bits of the reference code and the code received from the zone monitoring circuits **20** are the same, and a logic output whenever the compared bits are different. Exclusive OR gate **154** controls an alarm indication circuit **46** (FIG. **9**) which, for example, may provide an audible and a visual alarm indication at the central monitor in response to an alarm.

As each bit of the monitor code received is extended over the tone converter **41** to the set input of the flip flop **152**, the corresponding bit of reference code generated by the reference code generator **42** is extended to the set input of flip flop **153**. The code bits at the set inputs of flip flops **152** and **153** are clocked into the flip flops **152** and **153** by clock pulses from clock pulse generator **46**. Under normal conditions the bits extended to the inputs of the flip flops **152** and **153** will be identical with the bit extended to flip flop **153**, and accordingly the Exclusive OR gate **154** will provide a logic 0 level output.

Whenever the zone monitoring circuits **20** are providing an alarm code the intial portion of which is indicated by the interruption of tone transmission over line **30** for a predetermined time, to indicate that an alarm output has been provided by one or more of the alarm sources **10**, the tone detector **141** will fail to provide a logic 1 output during such time to the input of flip flop **152**.

Consequently the bits clocked into flip flops **152** and **153** will be different for one or more bits of the reference code, and the Exclusive OR gate **154** will provide a logic 1 level output. The logic 1 level output provided by the Exclusive OR gate **154** enables an alarm driver **156** of the alarm indication circuit **45** to energize an alarm tone generator **157**, which generates an audible alarm tone, and lights an alarm lamp **158** at the central monitor.

The logic 1 level output of the Exclusive OR circuit **154** is also extended to an enable circuit **159** of the alarm source identification decoder circuit **47** (FIG. **9**) to enable the alarm source identification circuit **47** to be responsive to the sync tone generated by the sync circuit **114** of the alarm multiplexing circuits **21** and to thereafter be responsive to the bits of the alarm source identification code transmitted to the control monitor from the zone monitoring circuits **20**.

The enable circuit **159** includes a flip flop **159***a* having a set input connected to the alarm output line **154***a* at the output of the code comparator circuit **43**, and an AND gate **159***b* having a first input connected to the positive output Q of the flip flop **159***a* and a second input connected over conductor **167** to the output of the tone detector circuit **141**.

The output of gate **159***b* is connected to an input of an oscillator **166** which is operable when enabled to supply clock pulses for the alarm source identification decoder circuit **47**.

The alarm source identification decoder circuit **47** is similar to the alarm source identification generator **52** of the alarm multiplexing circuits **21** and may comprise a plurality of AND gates **160**, including gates **161–164**, and a multi-stage ring counter **165** which provides outputs for selectively enabling the AND gates **160**. In the present example, wherein the alarm source identification code comprises 20 bits representing the status of twenty alarm sensors **10**, the alarm source identification decoder **47** includes 20 AND gates **160**, such as gates **161–164** and the ring counter **165** has twenty stages, each having an output connected to a different one of the gates **160** for providing enabling inputs for the AND gates **160** in a predetermined sequence. A second input of each of the AND gates is connected to the output of the tone detector circuit **141**.

The alarm source identification decoder circuit **47** is operable similar to the alarm source identification code generator **52**. A logic 1 level bit, assumed initially to be stored in the first stage of the ring counter **165** is stepped from stage to stage of the ring counter **165** responsive to pulses supplied to the ring counter **165** from the oscillator circuit **166**.

The oscillator circuit **166**, enabled by the sync pulse gated over gate **159**b of the enable circuit **159** to the input of the oscillator circuit **166**, is operable to provide a series of square wave pulses of the same frequency as the pulses supplied by the oscillator **117** of the alarm multiplexing circuits **21** whenever an alarm code is received at the central monitor. The series of pulses provided by the oscillator **166** shift the logic 1 bit stored in the ring counter **165** from stage to stage of the counter **165** to provide enabling inputs for AND gates **160**, to thereby enable successive bits of the alarm source identificaton code to be gated over gates **160** to individual inputs of the alarm source register **45**.

The AND gate to which the enabling input is supplied will be enabled if the bit of the alarm source identification code extended to the second input of such gate from the tone detector circuit **141** is at logic 1 level. However, such gate will remain disabled if the alarm source code bit is at logic 0 level.

The alarm source register **45** includes a plurality of alarm lamps, including alarm lamps **171–174**, each connected to the output of a different one of the AND gates **160**, and each individually associated with a different one of the alarm sources **10** to indicate the alarm status of an associated alarm sensor. Thus, for example, alarm lamps **171–174** are connected to outputs of AND gates **161–164**, respectively, and indicate the alarm status of alarm sensors **11–14**, respectively.

The alarm lamps, such as alarm lamp **171**, are normally unlit, but will be lit whenever the corresponding AND gate, gate **161** for lamp **171**, is enabled and remains lit until the associated register circuit is manually reset.

It is pointed out that if the alarm source identification generator **52** (FIG. 4) includes a point sequence code generator **57**, described in the foregoing as comprising a plugboard **58** connected between the output of the register **124** and the inputs of the AND gates **129** associated with the register **124**, the alarm source identification decoder circuit **47** will also include an identical point sequence code generator **49** connected between the output of the ring counter **165** and the inputs of the AND gates **160** to effect enabling of AND gates **160** in the same order that gates **129** are enabled to permit proper decoding of the alarm source identification code sequence transmitted from the zone monitoring circuits **20**.

In operation, as the bits of the monitor code transmitted by the zone monitoring circuits **20** are received by the tone converter circuit **41** of the transmission line monitoring circuits **40**, the bits of the monitor code will compare with corresponding bits of the reference code.

At the time the alarm sensor **11** provides an alarm output, the output of the sequencing circuit **50** at T1 will inhibit the tone generator **37** so that no tones will be received at the central monitor for the duration of the output of the alarm monostable circuit **98**. The loss of tone is detected by the code comparator circuit **43**, enabling the alarm register **46** to provide an audio and visual alarm indication at the central monitor. In addition, the code comparator circuit **43** provides an enabling output for the enabling circuit **159**, setting flip flop **159***a*, which provides an enabling input signal for gate **159***b*. Accordingly, when the sync tone generated by the sync circuit **114** is received, gate **159***b* of the enabling circuit **159** is already set to provide a path for the sync pulse to energize the oscillator circuit **166** associated with the alarm source identification decoder **47**, and to thus effect the generation of sequential enabling signals for the AND gates **160** as the bits of the alarm source identification code are extended to the inputs of gates **160**.

In the exemplary example, wherein it is assumed that alarm sensor **11** has provided the alarm output and that the other nineteen sensors, including sensors **12–14** are indicating that corresponding protected areas are secure, the first bit of the alarm source identification code sequence will be at a logic 1 level and the other 19 bits of the code will be at logic 0 levels.

Thus, as the first bit (logic 1 level) of the alarm source identification bit sequence is provided at the output of the tone detecting circuit and extended over conductor **167** to the inputs of all of the AND gates **160**, including gate **161**, the logic 1 level output provided by the first stage of the ring counter **165** is extended to the second input of the AND gate **161**. Accordingly, AND gate **161** will be enabled, providing an output for energizing lamp **171** of the alarm source register **47**, to indicate that an alarm has been provided by alarm sensor **11**.

Therefter, as subsequent bits of the alarm source identification code are received and passed to the alarm source identification decoder circuit **47**, the logic 1 enabling output provided by the ring counter **165** will be extended in sequence to inputs of the other AND gates **160** of the alarm source identification circuit **47**, including gates **162–164**. However, since it is

assumed that only alarm sensor **11** is providing an alarm output, the identification bits representing the conditions of the other 19 alarm sensors, including sensors **12–14**, will be logic 0. Accordingly, as each of the subsequent bits of the alarm source identification code are received the AND gates, such as gates **162, 163** and **164** of the alarm source identification circuits **47** associated with such sensors will not be enabled. After all of the gates **160** have been enabled in sequence, a logic 1 level output provided by the output stage of the ring counter register **165** is extended to the oscillator **166**, and to the reset input of flip flop **159**a, disabling the oscillator **166** and resetting the enable circuit **159.**

Access Secure Circuitry

Referring again to FIG. **5**, the access-secure circuits **65**, including A/S scanner **66** and the A/S tone generator **69**, are operable to periodically scan the access-secure switches **60**, including switches **61–64** associated with the alarm sensors **10**, to provide a tone sequence including serial information regarding the access-secure status of the alarm sensors **10.**

The scanner **66** may comprise a ring counter **181** and associated enabling gates **182**, including AND gates **183–186** and an OR gate **187.** The ring counter **181** includes an input stage **181**a having an output connected over a conductor **188***a* to a set input of a scan initiate flip flop **188** which has a positive output Q connected to an input of the A/S tone generator **69.** Intermediate stages **181***b*–**181***u* are individually connected to inputs of the AND gates **182.** Each of the AND gates **182** has a second input connected over a cable **68** to an individual access secure switch. Thus, for example, an input of gate **182** is connected over a conductor **68***a* of cable **68** to A/S switch **61.** Similarly, gates **184–186** are connected over conductors **68***b*, **68***s* and **68***t*, respectively to A/S switches **62–64.** The outputs of the AND gates **182** are connected to individual inputs of the OR gate **187.** The output of the OR gate **187** is connected to an input of the tone generator **69.**

The scanner **66** has associated therewith a pulse divider circuit **67.** The pulse divider circuit **67** supplies clock pulses of a predetermined frequency and at predetermined time intervals (relative to the time base as established by clock **36**) to the ring counter **181** enabling the ring counter to provide outputs for effecting sequential enabling of the AND gates **182.**

The pulse divider circuit **67** includes a divider circuit **67***a* having an input connected over conductor **36***a* to the output of the clock **36** and an output connected to the set input of a flip flop **67***b*. The positive output Q of the flip flop **67***b* is connected to a first input of an AND gate **67**c. A second input of AND gate **67***c* is connected to the output of an oscillator circuit **67***d*.

The ring counter **181** has an output stage **181***v* connected over conductor **190** to the reset input of flip flop **67***b* of the pulse divider circuit and over conductor **190***a* to the reset input of the scan initiate flip flop **188.**

The access-secure scan is periodic, with the rate of scan being controlled by the zone monitoring circuits **20** through the clock **36** of the zone monitoring circuit **20** and the frequency of the signals provided by oscillator **67***d*. More specifically, the access-secure scan is initiated periodically by a signal resulting from the appropriate division of the clock frequency by pulse divider circuit **67.** A scan of the A/S switches **60** may be initiated once each minute, for example, depending upon the number of alarm sensors and the scanning rate as determined by the pulse divider circuit **67.**

Referring to FIG. **3**, each of the access secure switches **60** may, for example, comprise a key-operated switch having contacts connected to suitable voltage sources to provide a first logic level output whenever the switch is set in the secure mode. For example, a logic 1 level output may indicate access mode, and a logic 0 level output may indicate secure mode. The logic level outputs provided by all of the access secure switches **60** are extended over cable **68** to individual inputs of the AND gates **182** of the A/S scanner **66.**

The A/S scan cycle is initiated in the following manner. The divider circuit **67***a* is responsive to a predetermined number of sequential clock pulses extended over conductor **36***a* to provide a set input for flip flop **67**b. When set, flip flop **67***b* enables AND gate **67***c*, permitting pulses provided by free-running oscillator **67***d* to be gated to the clock inputs of the ring counter **181.** With the receipt of the first oscillator pulse over gate **67***c*, a logic 1 level output, provided by the first stage of register **181**, sets the scan initiate flip flop **188.** Flip flop **188**, when set, provides a logic 1 level output which is extended to an input of the A/S tone generator **69**, causing power to be applied to the A/S tone generator circuit **69.** Accordingly, tone generator **69** will generate a scan initiate tone of a predetermined frequency Fc for transmission to the central monitor. The scan initiate signal is passed over a cable **193** and summing amplifier **96** to the transmission line **30** for transmission to the central monitor.

As successive clock pulses are gated from the oscillator **67**d to the clock inputs of the stages of the ring counter **181**, the logic 1 level bit is shifted from stage to stage of the ring counter **181** such that each stage of the ring counter **181** provides an output for sequentially enabling an associated one of the AND gates **182** of the scanner **66**, thereby gating the outputs, respresentative of the status of access-secure switches **60**, extended to the gates **182** from the A/S switches **60** over the OR gate **187** to the input of the A/S tone generator **68.**

The tone generator **69** may be a conventional frequency shift keyed oscillator which is similar to the tone generator **37** associated with the alarm multiplexing circuits **21.** The tone generator **69** is operable when enabled by flip flop **188** to be responsive to each logic 1 level input supplied thereto to provide an output tone of a first frequency Fc and responsive to each logic 0 level input supplied thereto to provide a tone output of a second frequency F*d* which is shifted from the base frequency Fc by a preselected amount. Thus, as the AND gates **182** of the A/S scanner **66** are sequentially enabled by output s supplied by the ring counter **181**, the tone generator **69** generates tone bursts of frequencies Fc and F*d* in a sequence coded to represent the status of the access-secure switches **60.**

Access Secure Monitoring Circuits

Referring to FIG. **8**, the tone sequence of frequencies Fc and F*d* provided by the access-secure monitoring circuits **65** is received by the tone converter circuits **41** at the central monitor. The tone converter circuits **41** include a tone filter **195** and a pair of tone detector circuits **196** and **197.** The tone filter **195** is tuned to pass

signals of frequencies Fc (logic 0) and Fd (Logic 1) which are provided by the access-secure tone generator **69** and to block passage of tones of frequencies F*a* and F*b* provided by the monitor tone generator **37.** The output of the tone filter **195** is extended to the inputs of the tone detector circuits **196** and **197.** Tone detector **196** is responsive to tone signals of frequency Fc to provide a logic 1 level output, and tone detector **197** is responsive to signals of frequency F*d* to provide a logic 1 level output. The outputs of the tone detector circuits **196** and **197** are extended over conductors **198** and **199,** respectively, to inputs of the access-secure identification decoder circuit **71,** shown in FIG. **10.**

The access-secure decoder circuit **71** may comprise a serial-to-parallel decoder circuit, which is similar to the scanner circuit **66** of the access-secure circuitry **65** of the zone monitoring circuits **20.**

The A/S decoder circuit **71** is operable to extend the bits of the A/S monitor code supplied over conductors **198** and **199** to inputs of the alarm source register **45** to effect selective lighting of A/S indicating lamps **216** of the alarm source register **45.** The alarm source register **45** provides a pair of A/S lamps, such as lamps **217** and **218,** for each of the A/S switches **60,** such as A/S switch **61.** Lamp **217,** when lit, indicates that A/S switch **61** is set in the access position and that the corresponding alarm sensor **61** is operating in the access mode. Lamp **218,** when lit, indicates that A/S switch **61** is set in the secure position and that the corresponding alarm sensor **11** is operating in the secure mode.

The A/S decoder **71** includes a plurality of AND gates **202,** including gates **203–210,** having a pair of gates such as gates **203** and **207,** individually associated with each of the access-secure switches **60,** such as A/S switch **61.** The A/S decoder **71** further includes a ring counter **201** for sequentially enabling the AND gates in pairs.

One of the gates of each pair, including gates **203–206** has a first input commonly connected to conductor **199** which conducts logic 1 bits (access condition) of the A/S code and the other gates, including gates **207–210,** have a first input commonly connected to conductor **198** which conducts logic 0 bits (secure condition) of the A/S code. Each pair of gates, such as gates **203** and **207** has a second input commonly connected to an output of a different stage of a ring counter **201,** such as stage **201**a for gates **203** and **207.**

The output of gate **203** is extended to the set input of a flip flop **212** and the output of gate **207** is extended to the reset input of flip flop **212.** The positive output Q of flip flop **212** is connected to the access condition indicating lamp **217** associated with A/S switch **61** (and alarm sensor **11**) and the negative output $\bar{Q}$ of flip flop **212** is connected to the secure condition indicating lamp **218** associated with A/S switch **61.** Whenever flip flop **212** is set, the access condition indicating lamp **217** will be lit, and whenever flip flop **212** is reset, the secure condition indicating lamp will be lit.

Similarly, the outputs of gates **204-206** are connected to the set inputs of flip flops **213–215,** respectively, and the outputs of gates **208–210** are connected to the reset inputs of flip flops **213–215,** respectively. The positive outputs Q of flip flops **213–215** control the energization of access condition indicating lamps **219–221,** respectively, associated with alarm sensors **12–14,** respectively. The negative outputs $\bar{Q}$ of flip flops **213–215** control the energization of secure condition indicating lamps **222–224,** respectively, associated with alarm sensors **12–14,** respectively.

The ring counter **201** initially stores a logic **1** bit in the first stage **201***a* of the counter register. In response to clock pulses supplied to the ring counter **201** from the pulse divider circuit **72** (under the control of clock **44**), the logic 1 level bit is shifted from stage to stage to sequentially enable each pair of AND gates, such as the pair of gates **203** and **207** associated with A/S switch **61,** as the bit of the access-secure code representing the A/S condition of the corresponding A/S switch **61** is received at the central monitor.

Clock pulses are supplied to the ring counter **201** whenever the clock pulse dividing circuit is enabled. The clock pulse divider circuit **72** is similar to the clock pulse divider circuit **67** of the zone monitoring circuits **20.** Clock pulse divider circuit **72** includes a divider circuit **72***a* having an input connected to the output of the clock **44** and an output connected to the set input of a flip flop **72***b*. Flip flop **72***b* has a positive output Q connected to an input of an AND gate **72***c*. A second input of AND gate **72***c* is connected to an output of a free running oscillator **72***d*. A third input of AND gate **72**c is connected to the positive output Q of an enable flip flop **224** which has a set input connected to conductor **199.** The reset inputs of flip flops **726** and **224** are connected to the output stage **201**m.

In operation, the scan initiate tone, at frequency Fd, transmitted from the A/S monitoring circuits **65** is received by tone converter circuit **41** and passed over tone filter **195** to the tone detectors **196** and **197.** Tone detector **197** will be responsive to the scan initiate tone to provide a logic 1 level output which is extended over conductors **199** and **199**a to the A/S decoder enable flip flop **224,** setting flip flop **224.** When flip **224** is set, a logic 1 level provided at the positive output Q of the flip flop **224** will be extended to one input of AND gate **72***c* of the clock pulse divider circuit **72.** Moreover, divider circuit **72***a* is responsive to a predetermined number of clock pulses supplied from clock **44** to provide an output for setting flip flop **72***b* of the clock pulse dividing circuit **72** which provides an enabling input at a logic 1 level to a further input of AND gate **72***c*. When flip flops **72***b* and **224** are both set, AND gate **72***c* will be enabled to follow the output pulses provided by oscillator **72***d* to thereby supply clock pulses to the ring counter **201.**

The A/S decoder circuit **71** operates in synchronism with the scanning circuit **66** and accordingly, the AND gates **202** of the decoder **71** will be enabled in sequence with the enabling of AND gates **182** of the A/S scanner **66.**

Since initially a logic 1 level bit is stored in the first stage **201***a* of the ring counter **201,** an enabling signal will be provided for AND gates **203** and **207** as the first bit of the access-secure code is received.

Accordingly, if access-secure switch **61** associated with alarm source **11** is in the secure position, the first bit of the access-secure code will be a tone signal of frequency Fc, representing a logic 0 level, which will be received by the tone converter circuit **41** at the central monitor, passed over tone filter circuit **195** enabling tone detector **196** to provide a logic 1 level output over conductor **198.** Therefore, gate **207** will be enabled, causing flip flop **212** to be reset and lamp **218** to be lit indicating a secure condition for access-secure switch

61. On the other hand, if access-secure switch 61 were set in the access position, the first bit of the access-secure code will be a tone at a frequency F*d*, indicating a logic 1 level, which tone will be received by the tone converter circuit 41 and passed over tone filter 195 to enable tone detector 197. Tone detector 197 will provide a logic 1 output level over conductor 199 to enable AND gate 203, setting flip flop 212 and causing lamp 217 to be energized, thereby indicating an access condition for an access secure switch 61.

When the ring counter 181 (FIG. 5) is stepped to enable AND gate 184 to provide an input to the A/S tone generator 69 generating the second bit of the A/S code, a shift pulse supplied to ring counter 202 over pulse divider circuit 72 will shift the logic 1 level bit of counter 202 to the second stage 201b, enabling AND gates 204 and 208 to be responsive to the second bit of the A/S code for controlling the associated flip flop 212 effecting energization of lamps 219 or 222 in accordance with the status of A/S switch 62.

Thereafter, as the ring counter 181 of the A/S scanner 66 is stepped by successive shift pulses to sequentially enable the AND gates 182 to effect the generation of the remaining eighteen bits of the A/S code, the ring counter 201 of the A/S decoder 71 will also be stepped in synchronism with counter 181, to enable decoding of the A/S code, and the registration of the A/S information in the alarm source register 48.

When the last bit of the access secure code is received, the logic 1 level bit will have been shifted to stage 201*t* of the ring counter 201 to enable either AND gate 206 or 210, lighting either lamp 221 or 224 to indicate the access-secure status of A/S switch 64.

The next clock pulses extended to the ring counter 201 from the pulse divider circuit 72 will cause the logic 1 level bit stored in the register 201 to be shifted to the output stage 201*u* of the register 201. The logic 1 output of stage 201*u* is extended over conductor 225 to the reset inputs of flip flop 72*b* and 224, effecting reset of the pulse divider circuit 72 and the A/S decoder scan initiate flip flop 224 inhibiting the passage of further clock pulses to the ring counter 201 and returning the A/S decoder circuit 71 to an idle condition.

The A/S scanner 66 (FIG. 5) and the A/S decoder 71 (FIG. 10) at the central monitor may include point sequence code generators 70, 73 which are similar to the point sequence code generator 57 associated with the alarm multiplexing circuits 21 to permit a coded selection of the sequence in which the A/S switches 60 are scanned. By such provision, the access-secure information transmitted over the transmission line 30 cannot be attributed to the A/S status of a particular alarm sensor. The scan sequence may, for example, be modified at both the zone monitoring circuits 20 and the central monitor by a programmable plug board, in the manner described in the foregoing.

Remote Test Circuits

Referring to FIG. 8, in addition to the signal receiving aspects of the central monitor, the transmission line monitoring circuits 40 at the central monitor may also include a remote test signal generator 74 to enable testing of the operation of the alarm sensors 10 such as alarm sensors 11–14, from the central monitor. The remote test signal generator 70 generates a test command signal of a predetermned frequency, which is transmitted over the transmission line 30 to the alarm multiplexing circuits 21. The frequency of the test command is selected to be different from the frequencies of signals provided by the monitor tone generator 37 and the A/S tone generator 69.

The alarm multiplexing circuits 21 include a test signal detecting circuit 75 (FIG. 4) which includes a bandpass filter 232 and a tone detector circuit 233. The bandpass filter 232 is tuned to pass only signals which are of the frequency of the test command signals provided by the test signal generator 74 to the test signal detector circuit 233.

The test signal detector circuit 233 is responsive to signals passed by the test signal filter 232 to provide control signals over conductors 244*a*–244*t* of cable 244 for each of the alarm sensors 10.

In an exemplary system the alarm sensors 10, such as alarm sensor 11, may comprise a microwave motion detector circuit 234, shown in FIG. 11.

Referring to FIG. 11, the microwave motion detector 234, which may be of the type which is conventional in the art, includes a transmitter 235, a receiver 236, and an alarm signal detecting circuit 237. The transmitter 235 generates microwave signals at a predetermined frequency for radiation via transmitter antenna 238 into the area protected by the motion detector 234. Such radiated signals will be reflected off objects within the protected area and the reflected signals will be received by an antenna 239 of the receiver 236. When the transmitted signals are reflected off a human intruder, indicated generally at 240, moving within the protected area, the frequency of the received signals will be shifted from the frequency of the transmitted signals providing Doppler signals which are related in amplitude and frequency to characteristics of an object, such as a human intruder, moving within the protected area. When the moving object 240 is a human intruder, the Doppler signals detected by the receiver 236 will be passed to the alarm signal detecting circuit 237 which will correspondingly provide an alarm output over alarm line 31a which is connected over OR gates 81 (FIG. 3) to an input of alarm storage flip flop 25*a*.

To enable the testing of each alarm sensor, the alarm sensors 10, such as alarm sensor 11, have associated therewith a motion simulation output generating circuit such as motion simultation circuit 241 for alarm sensor 11.

The motion simulation output generating circuit 241, includes a drive circuit 243 which is responsive to each control output signal provided over conductor 244*a* by the test signal detecting circuit 233 to control an associated functional device 242 to produce a signal output representative of human motion for enabling the corresponding alarm sensor 11 to produce alarm output if the alarm sensor 11 is functioning properly. The motion simulation signal may well be a frequency signal, but that frequency is selected for its motion simulation characteristics, and does not necessarily bear any relationship to the frequency of the remote test signal.

The performance of the microwave motion detector 234 which comprises alarm sensor 11 can be tested through the use of various electrical or mechanical functional devices 242 activated by enabling of the drive circuit 243 by the test signal detector circuit 233. Examples of mechanical motion simulators include a small fan placed in the detection field of the sensor 11

and a piezoelectric element placed within the receiver antenna structure **239.** Electrical motion simulators include the application of a low frequency modulation signal to the transmitter oscillator (conveniently, 60 Hz is most appropriate for motion detectors operating in the GHz region as this frequency corresponds to that generated by normal human motion) or the excitation of a small neon bulb within the antenna structure (**238, 239**). This latter approach is quite convenient in the case of an avalance diode oscillator which requires DC voltage as high as that used for neon bulb excitation. The movement of the ionized gases in the neon bulb can be then utilized to electrically simulate intruder motion. A diode (point contact, Schottky or PIN structure) can also be placed within the antenna structure and driven at a low 60 Hz or lower is convenient) frequency to modulate the microwave beam as in human motion. Finally, switching transients in the supply circuit of the transmiter **235** can be used to simulate transient motion conditions.

The functional device **242,** when activated by the drive circuit **243,** thus effects modulation of the microwave signals radiated into the protected area, as would occur when such microwave signals are reflected off a human target moving within the protected area. The modulated microwave signals, thus produced, are detected by the receiver **236** and passed to the alarm signal detecting circuit **237,** enabling the alarm signal detecting circuit **237** to provide an alarm output on alarm line **31a.**

The alarm output thus provided over line **31*a*** will set the corresponding alarm flip flop **25*a*** (FIG. **3**) thereby effecting the generation of an alarm code by the alarm multiplexing circuits **21** (FIGS. **4** and **6**) in the manner described hereinabove for transmission to the central monitor. The receipt at the central monitor of such alarm code in response to the transmission of a test signal from the central monitor will indicate that alarm sensor **11** is functioning properly. On the other hand, a malfunction in the alarm sensor **11** will be indicated by the failure to receive an alarm code after the test signal has been transmitted to the locations of the alarm source monitoring circuits **20.**

Since test command signals are extended simultaneously to individual motion simulator circuits associated with all of the alarm sensors **10,** each alarm sensor will provide an alarm output over a corresponding alarm line. Accordingly, the alarm code generated by the alarm multiplexing circuits **21** will include bits indicating that alarm outputs have been provided by all of the alarm sensors **10** if all alarm sensors are operating properly.

While the remote test system described employs a single test signal for effecting a remote test of all alarm sensors **10,** it is evident that through the use of a multiple frequency generator at the central monitor and the additon of appropriate tone detector circuits at the zone monitoring circuits **20,** an individual test signal could be provided for each alarm sensor, enabling the alarm sensors **10** to be selectively tested upon command from the central monitor.

Modifications

While in the foregoing description an exemplary embodiment of a programmed time multiplexed alarm transmission system was operable to monitor 20 alarm sensors and transmit alarm information indicating the conditions of twenty alarm sensors, it is apparent that more alarm sensors could be monitored through the provision of additional alarm data storage circuits, gating circuits, counter register stages and alarm registers. In addition, while in the exemplary embodimeht only one alarm code bit was provided for each alarm sensor to indicate the status of such sensor, the alarm source multiplexing circuits could be modified, by the addition of appropriate gating circuits and counter register stages, to provide, a plurality of alarm bits for each alarm sensor so as to enable transmission of information regarding the specific nature of an alarm indication, that is, an intrusion, a component failure, tampering with an alarm sensor or an attempt to compromise the system or an alarm detector.

Moreover, rather than inhibitng the transmission of the monitor code in the event of an alarm condition, the bits of the monitor code could be selectively modified to indicate an alarm indication and the identification of the source of the alarm.

We claim:

1. In a security system including a transmission line for carrying alarm information from a plurality of protected areas within a predetermined zone to a central monitor that is remote from the protected areas, zone monitoring means including code generating means for continuously generating a line monitor code comprised of a known sequence of coded bits, means for enabling said monitor code to be transmitted over said transmission line to said central monitor, alarm multiplexing means including alarm storage means having separate storage locations for each protected area for storing a first data bit whenever the corresponding protected area is secure and a second data bit to indicate an alarm condition for the corresponding protected area, sequencing means controlled by said alarm data storage means in response to the storage of a second data bit therein to inhibit the transmission of said monitor code to said central monitor and means controlled by said sequencing means to effect the generation of an alarm source identification code comprised of a plurality of bits in a sequence coded to represent the conditions of all of the protected areas for transmission over said transmission line to said central monitor.

2. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an intrusion detector for each protected area, normally enabled to be operable in a secure mode to provide an alarm output in response to an intrusion of the corresponding protected area, alarm source monitoring means including means responsive to an alarm output provided by at least one of said intrusion detectors to generate an alarm code for transmission over said transmission line to said central monitor, said alarm code comprising an alarm indication followed by a plurality of bits in a sequence coded to represent the conditions of all of the intrusion detectors to thereby indicate the source of the alarm, access-secure means including an individual access switch means for at least certain ones of said intrusion detectors for individually disabling an associated intrusion detector to cause said intrusion detector to be operable in an access mode to thereby permit an intrusion of a corresponding protected area without providing an alarm output, said access-secure means including condition indicating

means for continuously providing a plurality of output signals over a plurality of outputs thereof, each of said output signals indicating the mode of operation of a different one of said intrusion detectors, and access-secure monitoring means for scanning said output of said access-secure means to generate an access-secure code for transmission over said transmission line to said central monitor, said access-secure code being comprised of a plurality of signals coded to represent the mode of operation of each of said intrusion detectors.

3. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor for each protected area, each of said alarm sensors being normally operable in a source mode to provide an alarm output signal in response to an intrusion of an associated area, alarm source monitoring means including code generating means for continuously generating a line monitor code comprised of a known sequence of code bits which is normally transmitted over said transmission line to said central monitor to indicate that all protected areas are secure, alarm multiplexing means including alarm storage means having an individual storage means for each alarm sensor for receiving the alarm output signals provided by an associated alarm sensor, and alarm data readout means including sequencing means enabled by said alarm storage means whenever an alarm output signal is provided by one of said alarm sensors to generate a plurality of control signals in a predetermined time sequence, means responsive to a first control signal to inhibit the transmission of the monitor code to said central monitor, means responsive to a second control signal to thereafter effect readout of the alarm storage means to generate an alarm code comprised of a plurality of bits which represent the conditions of the alarm sensors for transmission over said transmission line to said central monitor to enable the identification of the source of the alarm.

4. A system as set forth in claim **3** wherein said alarm source monitoring means includes access switch means for individually disabling said alarm sensors, whereby said alarm sensors are operable in an access mode to permit an intrusion of a corresponding protected area without providing an alarm output, said access switch means including condition indicating means for continuously providing a plurality of output signals over a plurality of outputs thereof, each of said output signals indicating the mode of operation of a different one of said alarm sensors and access-secure monitoring means including scanner means for periodically scanning said outputs to generate an access-secure code for transmission over said transmission line to said central monitor, said access-secure code being comprised of a plurality of bits in a sequence coded to represent the mode of operation of each of said alarm sensors.

5. A system as set forth in claim **4** wherein said alarm source monitoring means include clock pulse generating means for providing pulses for controlling said code generating means to generate the bits of the monitor code at a predetermined rate, and clock pulse dividing means for extending pulses from said clock pulse generating means to said scanner means for enabling said scanner means to generate said access-secure code at a rate slower than said predetermined rate.

6. A system as set forth in claim **4** wherein said scanner means includes an output gate circuit having a plurality of input and an output, and a plurality of scan gate circuits, each of said scan gate circuits having a first input individually connected to one of the outputs of said condition indicating means and an output individually connected to one of the inputs of said output gate circuit, and enabling means for extending an enabling signal to a second input of each of said scan gate circuits in a preselected sequence to gate the output signals provided by said condition indicating means to said output gate circuit to thereby provide said access-secure code at the output of said output gate circuit.

7. A system as set forth in claim **6** wherein said scanner means includes output point sequence code generator means for controlling said enabling means to thereby preselect the sequence in which said scan gates are enabled.

8. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from a protected areas, alarm source means including an alarm sensor for each protected area, each of said alarm sensors being operable to provide an alarm output signal to indicate an alarm condition for an associated protected area, code generating means for continuously generating a line monitor code comprised of a known sequence of coded signals which are normally transmitted over said transmission line to said central monitor, alarm multiplexing means including sequencing means enabled in response to the receipt of an alarm output signal provided by an alarm sensor to provide a plurality of control signals in a predetermined time sequence, inhibit means responsive to a first control signal provided by said sequencing means to inhibit the passage of said monitor code sequence to said transmission line, and alarm source identification means responsive to a second control signal provided by said sequencing means to provide an alarm source identification code comprised of a plurality of bits in a sequence coded to represent the conditions of said protected areas for transmission over said transmission line to said central monitor.

9. A system as set forth in claim **8** wherein said alarm multiplexing means includes alarms storage means having separate alarm output storage means for each of said alarm sensors for storing the alarm output signals provided by the alarm sensors.

10. A system as set forth in claim **9** wherein each of said alarm sensors are further operable to provide a supervisory alarm output signal in responsive to a component failure of the alarm sensors, and wherein said alarm storage means further includes separate supervisory storage means for each of said alarm sensors for storing supervisory alarm outputs provided by the alarm sensors, said sequencing means being responsive to either an alarm output signal or a supervisory output signal to provide said control signals for effecting the transmission of alarm information to said central monitor.

11. A system as set forth in claim **10** wherein each of said alarm output storage means comprises a first normally reset bistable data storage circuit and each of said supervisory storage means comprises a second normally reset bistable data storage circuit, a first data storage circuit being set whenever an alarm output signal is provided by an associated alarm sensor and a sec-

ond data storage circuit being set whenever a supervisory alarm output signal is provided by an associated alarm sensor.

12. A system as set forth in claim **8** wherein said alarm multiplexing means includes alarm storage means including a separate alarm flip flop for each alarm sensor, each alarm flip flop being normally reset to provide an output bit at a first logic level and being set in response to an alarm output signal provided by an associated alarm sensor to provide an output bit at a second logic level.

13. A system as set forth in claim **12** wherein said alarm source identification means comprises parallel-to-serial converter means including a plurality of gate circuits, each of said gate circuits being individually connected to the output of a different one of said alarm flip flops, output gating means having a plurality of inputs individually connected to an output of a different gate circuit, and enabling means responsive to said second control signal to sequentially enable said gate circuits to pass the bits stored in the alarm flip flops of said alarm storage means to said output gating means to thereby provide a sequence of bits at an output of said gating means representing the alarm data stored in all of said alarm flip flops.

14. A system as set forth in claim **13** wherein said alarm source identification means further includes point sequence code generator means for controlling said enabling means to enable preselection of the sequence in which said gate circuits are enabled and thus the sequence in which the bits stored in the alarm flip flops are passed to said output gating means.

15. A system as set forth in claim **13** which includes line monitoring means at said central monitor having reference code generating means for generating a reference code comprised of a sequence of coded bits, each bit of which is normally identical with corresponding bits of the monitor code at any given time, code comparator means for receiving the bits of the monitor code and comparing the monitor code bit sequence with the reference code bit sequence, alarm indicating means controlled by said code comparator means for providing an alarm indication whenever corresponding bits of the sequences are different and decoder means responsive to the bits of an alarm source identification code to determine the source of the alarm.

16. A system as set forth in claim **15** wherein said alarm data readout means further includes means responsive to a control signal provided by said alarm source identification means as enabled, to provide a sync signal, prior to the readout of the alarm flip flops of said alarm storage means, for transmission over said transmission line to said central monitor to enable said decoder means to be responsive to the bits of the alarm source identification code to identify the source of the alarm.

17. A system as set forth in claim **13** wherein said sequencing means includes means enabled by said enabling means of said alarm source identification means after the bits stored in all of the alarm flip flops have been gated to said output gating means to provide a reset signal for resetting all of the alarm flip flops.

18. A system as set forth in claim **17** wherein said sequencing means includes means enabled by said reset signal to provide a signal for disabling said inhibit means to thereby reinitiate the transmission of said monitor code to said central monitor.

19. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor for each protected area, each of said alarm sensors being normally operable in a secure mode to provide an alarm output in response to an intrusion of a corresponding protected area, code generating means for continuously generating a line monitor code comprised of a continuous sequence of logic level bits, tone generating means responsive to the bits of the monitor code to generate tone signals of first and second frequencies in a sequence coded to represent the bits of the minitor code for transmission over said transmission line to said central monitor, alarm multiplexing means including alarm storage means for storing the alarm outputs provided by the alarm sensors, and readout means including sequencing means controlled by said alarm data storage means in response to the receipt of an alarm output signal provided by an alarm sensor to provide a control signal for inhibiting the passage of said monitor code bit sequence to said tone generating means, and alarm source identification means responsive to a further control signal provided by said sequencing means to effect readout of the alarm data source means to provide an alarm source identification code comprised of a sequence of logic level bits, each bit of which represents the condition of a different protected area, for controlling said tone generating means to generate a further tone sequence comprised of tone signals of said first and second frequencies coded to represent the conditions of the protected areas for transmission over said transmission line to said central monitor, access-secure means for rendering each of said alarm sensors individually operable in an access mode to enable intrusions of a corresponding protected area without providing an alarm output, and access-secure monitoring means operable to periodically scan said access-secure means to generate an access-secure code for transmission over said transmission line to said central monitor, said access-secure code being comprised of a sequence of bits, each bit of which indicates the mode of operation of a different one of the alarm sensors.

20. A system as set forth in claim **19** wherein said access-secure means comprises a plurality of access-secure switch means including an access-secure switch means individually associated with each alarm sensor for selecting the mode of operation of a corresponding alarm sensor, each of said access-secure switch means being operable to provide an output at a first logic level signal whenever the corresponding alarm sensor is operating in the access mode and an output at a second logic level signal whenever the corresponding alarm sensor is operating in the secure mode, said access-secure monitoring means including scanner means for providing a sequential scan of all of said access-secure switch means to provide a sequence of bits comprised of the logic level signals being provided by access-secure switch means.

21. A system as set forth in claim **20** wherein said access-secure monitoring means includes further tone generator means responsive to each output at said first logic level to provide a tone signal of said third frequency and responsive to each output bit at the second logic level to provide a tone signal at said fourth frequency.

22. A system as set forth in claim 21 including line monitoring means at said central monitor including tone detecting means for receiving the access-secure tone sequence and providing a sequence of logic level bits coded to represent the access-secure code, and access-secure decoding means responsive to the bits of the access-secure code to provide an indication of the acccess-secure mode of operation for each of said alarm sensors.

23. A system as set forth in claim 22 wherein said scanner means includes means for enabling said further tone generator means to provide a scan initiate signal of one of the frequencies of said further pair, for transmission over said transmission line to said central monitor to enable said access-secure decoding means to be responsive to the bits of the access-secure code.

24. A system as set forth in claim 22 wherein said access-secure decoding means includes a plurality of indicator means, including first and second indicator means for each alarm sensor, said first indicator means being operable when enabled to indicate the corresponding alarm sensor is operating in the access mode and said second indicator means being operable when enable to indicate the corresponding alarm sensor is operating in the secure mode, control means including a plurality of control circuits each individually associated with a different pair of indicator means for selectively enabling the associated indicator means, and gating means for gating each bit of the access-secure code to a different control circuit to effect enabling of one of the indicator means associated with each control circuit.

25. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an individual alarm sensor being operable to provide an alarm output signal in response to an unauthorized intrusion of an associated area, alarm source monitoring means including code continuously generating means for generating a line monitor code comprised of a continuous sequence of logic level bits, tone generating means, bit gating means normally enabled to gate the bits of the monitor code to said tone generating means to effect the generation of tone signals of first and second frequencies in a sequence coded to represent the monitor code for transmission over said transmission line to said central monitor, alarm multiplexing means including alarm storage means for storing the alarm outputs provided by the alarm sensors, and readout means including sequencing means controlled by said alarm data storage means in response to the receipt of an alarm output signal provided by an alarm sensor to provide a control signal for disabling said bit gating means to thereby inhibit the passage of said monitor code bit sequence to said tone generating means, and alarm source identification means responsive to a further control signal provided by said sequencing means to effect readout of the alarm data storage means to provide an alarm source identification code comprised of a sequence of logic level bits, each bit of which represents the condition of a different protected area for controlling said tone generating means to provide a further tone sequence comprised of tone signals of said first and second frequencies in a sequence coded to represent the conditions of said protected areas for transmission over said transmission line to said central monitor.

26. A system as set forth in claim 25 wherein said alarm data readout circuits include tone generator disable means, including means responsive to said first control signal to provide a disabling signal for said tone generator means to inhibit the generation of tone signals for a predetermined time.

27. A system as set forth in claim 25 wherein said alarm source identification means includes means for providing a bit at a first logic level to represent an alarm condition for a protected area in which a corresponding alarm sensor is providing an alarm output signal and a bit at a second logic level to represent a secure condition for a protected area, and output means for extending the bits of the alarm source identification code to the tone generator means to effect the generation of a tone signal at said first frequency for each bit of alarm source identification code at said first logic level and a tone signal of said second frequency for each bit of the alarm source identification code at said second logic level.

28. A system as set forth in claim 25 including line monitoring means at said central monitor having tone detecting means responsive to the tone sequences provided by said alarm source monitoring means to provide sequences of logic level bits at an output thereof, reference code generating means for generating a reference code comprised of a coded sequence of logic level bits, each bit of which is normally identical with corresponding bits of the monitor code at any given time, code comparator means for receiving the bit sequence provided by said tone detecting means and comparing the monitor code bit sequence with the reference code bit sequence, alarm indicating means controlled by said code comparator means for providing an alarm indication whenever corresponding bits of the sequences are different, and alarm source identification decoder means response to the bits of the alarm source identification bit sequence to determine the source of the alarm.

29. A system as set forth in claim 28 wherein said alarm data readout means further includes means responsive to a signal provided by said alarm source identification means prior to the readout of said alarm data storage means, to generate a sync pulse of a predetermined duration for enabling said tone generator means to generate a sync tone of one of said frequencies for transmission over said transmission line to said central monitor, said alarm source identification decoder means including decoder means and decoder enable means responsive to said sync tone to enable said decoder means to be responsive to the bits of the alarm source identification code.

30. A system as set forth in claim 29 wherein said tone detecting means is responsive to said sync tone to provide a logic level sync pulse, and wherein said decoder enable means includes gating means and bistable switching means, said bistable switching means being set responsive to the inhibiting of the transmission of said monitor code to enable said gating means to pass the sync pulse provided by said tone detecting means to said decoder means.

31. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an

individual alarm sensor for each protected area, each of said alarm sensors being operable to provide an alarm output signal in response to an unauthorized intrusion of an associated area, code continuously generating means for generating a line monitor code comprised of a known sequence of coded bits, bit gating means for normally passing the bits of the monitor code to the transmission line for transmission to said central monitor, alarm multiplexing means including alarm data storage means for storing alarm output signals provided by the alarm sensors, and readout means including alarm source identification means operable when enabled to effect sequential readout of the alarm data storage means to provide an alarm source identification code comprised of a plurality of bits in a sequence coded to represent the conditions of all of the alarm sensors, and sequencing means including first means responsive to an alarm output signal provided by at least one of said alarm sensors to provide a first control signal for disabling said bit gating means to thereby inhibit the transmission of said monitor code to said central monitor, second means for providing a second control signal for enabling said alarm source identification means to generate said alarm source identification code for transmission to said central monitor, and line monitoring means at said central monitor including reference code generating means for generating a reference code comprised of a sequence of coded bits, each bit of which is normally identical with corresponding bits of the monitor code at any given time, input means for receiving the monitor code, code comparator means controlled by said input means for comparing the bits of the monitor code with the bits of the reference code, alarm indicator means controlled by said code comparator means for providing an alarm indication whenever the compared bits are different, and alarm source identification decoder means including gating means for receiving the alarm source identification code and alarm source indicating means controlled by said gating means to indicate the source of the alarm.

32. A system as set forth in claim **31** wherein said alarm data storage means includes a plurality of alarm storage flip flops including a separate alarm storage flip flop for each alarm sensor, each alarm storage flip flop being normally reset to provide an output at first logic level, and each alarm storage flip flop being set responsive to an alarm output signal provided by an associated alarm sensor to provide an output at a second logic level.

33. A system as set forth in claim **32** wherein said alarm multiplexing means includes output gating means having a plurality of inputs, each input being individually connected to an output of a different one of said alarm storage flip flops, and an output connected to an input of said sequencing means, said output gating means including an alarm gate, enabled by an output at said second logic level provided by one of said alarm storage flip flops to enable said first means of said sequencing means to provide said first control signal.

34. A system as set forth in claim **33** wherein said alarm data readout circuits include a control flip flop normally providing an output for enabling said bit gating means, said control flip flop being responsive to said first control signal to provide a further output for disabling said bit gating means.

35. A system as set forth in claim **32** wherein said alarm source identification means includes output gating means and a plurality of gate circuits, each of said gate circuits having an input individually connected to an output of one of said alarm storage flip flops and an output individually connected to an input of said output gating means, and enabling means, responsive to said further control signal to enable said gate circuits in a preselected sequence to extend the logic level outputs of said alarm storage flip flops to said output gating means, whereby said output gating means provides a sequence of logic level outputs representing the conditions of all of said alarm sensors.

36. A system as set forth in claim **35** wherein said alarm multiplexing circuits includes sync pulse generating circuit means enabled by said enabling means prior to the enabling of said gate circuits to provide a sync signal for transmission to said central monitor to enable the alarm source identification decoder means to be responsive to the bits of the alarm source identification code.

37. A system as set forth in claim **36** wherein said alarm source indicating means comprises a plurality of indicator circuits including an indicator circuit corresponding to each alarm sensor, said gating means of said alarm source identification decoder means including a plurality of decoder gate circuits, each having inputs commonly connected to an output of said input means and an output individually connected to one of said indicator circuits, and further enabling means responsive to aid sync pulse to enable said decoder gate circuits in a preselected sequence in synchronism with the enabling of the gating circuits of said alarm source identification means whereby each of the bits of the alarm source identification code is gated over said decoder gating means to a different indicating circuit.

38. A system as set forth in claim **37** wherein said alarm source identification means includes point sequence code generator means for controlling said enabling means to preselect the sequence in which said gating circuits are enabled, and wherein said alarm source identification decoder means includes further point code generator means, which is identical to said first point sequence code generator means for controlling the further enabling means of said alarm identification decoder means to preselect the sequence in which the decoder gate circuits are enabled.

39. In an alarm transmission system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including individual intrusion detector means for each protected area, each intrusion detector means being operable to provide an alarm output in response to the detection of movement of an intruder within the corresponding protected area, alarm source monitoring means including means for continuously generating a line monitor code comprised of a selected sequence of tone signals of predetermined frequencies for transmission over said transmission line to said central monitor and alarm multiplexing means including means responsive to each alarm output for inhibiting the transmission of said monitor code to said central monitor and means for generating an alarm source identification code which indicates the conditions of all of the protected areas for transmission over said transmission line to said central monitor, and line monitoring means at

said central monitor including means enabled whenever the transmission of said monitor code is inhibited to provide an alarm indication at said central monitor and means reponsive to the alarm source identification code to indicate the source of the alarm, and test signal generating means operable to provide a test signal for transmission over said transmission line to said alarm source monitoring means, said alarm source monitoring means further including test signal detecting means responsive to each test signal provided by said test signal generating means to enable at least one of said intrusion detector means to provide an alarm output.

40. An alarm transmission system as set forth in claim **39** wherein at least said one intrusion detector means comprises microwave motion detection means having means operable to produce Doppler alarm signals of frequencies within a predetermined range whenever a human intruder is moving within the corresponding protected area, alarm signal detecting means response to each of said Doppler alarm signals to provide an alarm output, and motion simulator means enabled a test signal provided by said test signal detecting means to generate signals of a frequency within said predetermined range to enable said motion detection means to provide an alarm output.

41. In a security system including a transmission line for carrying alarm information from a plurality of protected areas to a central monitor that is remote from the protected areas, alarm source means including an alarm sensor for each protected area, each of said alarm sensors being operable to provide an alarm output signal to indicate an alarm condition for a corresponding protected area, alarm source monitoring means including means for continuously generating a line monitor code comprised of a selected sequence of coded signals for transmission over said transmission line to said central monitor, and alarm multiplexing means including means responsive to an larm output signal for inhibiting the transmission of said monitor code and for generating an alarm source identification code indicating the conditions of all of the protected areas for transmission to said central monitor.

42. A system as set forth in claim **41** wherein at least certain ones of said alarm sensors include an intrusion detector normally operable in a secure mode to provide an alarm output in response to an intrusion of a corresponding protected area and operable in an access mode to permit intrusion of the protected area without providing an alarm output, and authorized entry switch means at the location of said intrusion detectors for enabling selection of the mode of operation of said intrusion detectors.

43. A system as set forth in claim **42** including access-secure monitoring means for periodically scanning said authorized entry switch means and providing an access-secure code for transmission to said central monitor for indicating the mode of operation of each of said intrusion detectors.

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