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(54) **Resistive switching memory cell**

(57) A resistive switching memory cell (100) comprises a stack of a first electrode (110), a first inner region (120), a second inner region (130), and a second electrode (140). The first inner region (120) comprises one or more metal oxide layers. The second inner region (130) comprises one or more insulating, semi-insulating or semiconductive layer, wherein the second inner region (130) is in direct contact with the first inner region (120) and can scavenge oxygen from the first inner region (120), and the second inner region (130) has a nonlinear charge carrier dominant conduction mechanism under an applied voltage or electric field.

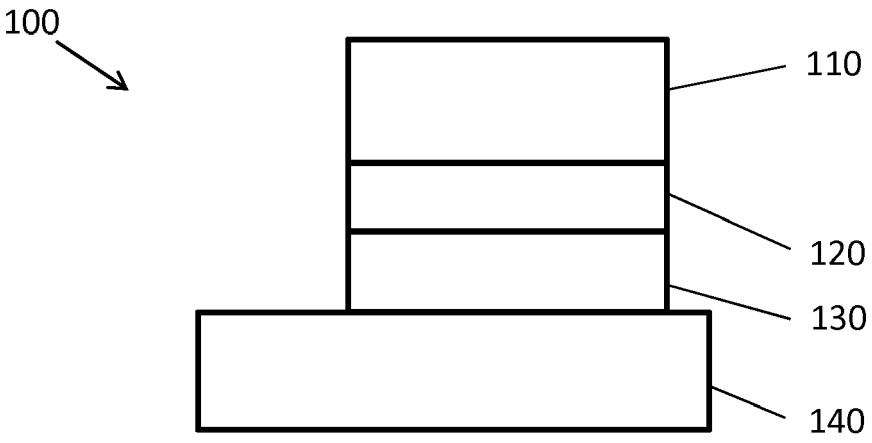

FIG. 1

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Description

Field of the invention

[0001] The invention relates to the field of memory cells. More specifically it relates to resistive switching memory cells comprising CMOS compatible materials and processes.

Background of the invention

[0002] The use of resistive random access memory (RRAM) has numerous advantages: RRAM is operated at low voltages and with low power, it has fast read/write access (fast switching time), it is stable over a long time, and it is scalable.

[0003] Implementation of large nonvolatile RRAM arrays, however, lags behind device research advances due to the lack of an appropriate selector element and/or due to unavailability of a resistive self-rectifying (hence selectorless) switching memory cell with highly nonlinear current-voltage characteristics, which can fit in a pitch-size cross-point array, or in a vertical RRAM string. The problem is made even more stringent when, considering limitations in switching current levels imposed by addressing large memory arrays or by power consumption, the requirement of operating at low switching currents, in the range of μA or below, is added.

[0004] Suitable selector elements could be introduced by means of transistors or rectifying diodes, which would block sneak currents in memory array. However, introducing such elements increases the size of the unit memory cell as well as the processing complexity. For instance, when using a select-transistor in a memory cell, an extra terminal is introduced, which makes the cell size increase above $4F^2$ (F-being the feature size) and also increases the complexity of the RRAM array fabrication, as well as its driving circuitry.

[0005] Therefore there is a need for highly-nonlinear self-rectifying RRAM cells.

Summary of the invention

[0006] It is an object of embodiments of the present invention to provide resistive switching memory cells which are non-linear, and self-rectifying and of a method of operating the same.

[0007] The above objective is accomplished by a method and device according to embodiments of the present invention.

[0008] In a first aspect, the present invention provides a resistive switching memory cell, the memory cell comprising a stack of a first electrode, a first inner region, a second inner region and a second electrode. The first inner region comprises one or more metal oxide layers, and the second inner region comprises one or more insulating, semi-insulating or semiconductive layers, whereby the second inner region is in direct contact with the first inner region (meaning that there are no other layers in between) and can scavenge oxygen from the first inner region. The second inner region has a nonlinear charge carrier conduction dominant mechanism under an applied voltage or electric field.

[0009] It is an advantage of embodiments of the present invention that the resistive switching memory cell can be placed between a word line and a bit line and that no extra transistor nor rectifying diode is required for operating the memory cell. The reason therefore is the self-rectifying behavior of resistive switching memory cells according to embodiments of the present invention. It is an advantage of embodiments of the present invention that basic CMOS compatible materials can be used. It is an advantage of embodiments of the present invention that resistive switching memory cells have an improved cycle-to-cycle and device-to-device uniformity compared to devices exhibiting filamentary switching. This may even hold for small cells such as 40 nm cells (area 40 nm x 40 nm) or below. It is an advantage of embodiments of the present invention that the resistive switching memory cells have the ability to endure at least 1000 switching cycles while maintaining stable ON/OFF states. It is an advantage of embodiments of the present invention that no forming of the resistive switching memory cell is required. Embodiments of the present invention do not rely on filament forming to create an ON state. It is an advantage of embodiments of the present invention that a resistive memory cell can switch to an arbitrary-value off-state resistance, controllable by externally applying a suitable voltage. The switching process is controlled by the voltage applied between the first electrode and the second electrode. It is an advantage that the resistive switching memory cells according to embodiments of the present invention feature non-linear current-voltage behavior in both low- and high-resistive states.

[0010] It is an advantage that resistive switching memory cells according to embodiments of the present invention do not require application of an external compliance to control the switching process. Resistive switching memory cells according to embodiments of the present invention have low switching current levels, typically between 50 μA and 1 μA for a 40 x 40 nm^2 cell size, and reducing with decreasing cell area. In embodiments of the present invention the resistive switching memory cells can be read-out by applying a voltage of the same polarity as the voltage required to reset the memory cell.

[0011] In a resistive switching memory cell according to embodiments of the present invention, the metal of the at least one metal oxide layer of the first inner region may be a transition metal. It is an advantage of embodiments of the present invention that transition metal oxides have weaker metal-oxygen bonds and therefore allow easier oxygen vacancy formation.

[0012] In a resistive switching memory cell according to embodiments of the present invention, the second inner region may comprise at least one amorphous, or predominantly amorphous layer. In such embodiments,

there are less grain boundaries within the second inner region than in a polycrystalline structure. This implies less leaky current paths, as the presence of grain boundaries may give rise to leaky current paths. As these leaky current paths may compromise the device behavior it is an advantage that they are decreased. Furthermore, in case of a-Si, for example, amorphous nature leads to an increase in the bandgap and consequently barrier height, which is beneficial for current decrease and nonlinearity increase.

[0013] In a resistive switching memory cell according to embodiments of the present invention, the second inner region may contain at least one layer which is not intentionally doped. Doping may require a higher thermal budget which might be incompatible with BEOL limitations. Therefore it is an advantage of embodiments of the present invention that the thermal budget may be lowered by having a second inner region which contains at least one layer which is not intentionally doped. Moreover, it is an advantage of embodiments of the present invention that large fluctuations in the doping level of a layer can be avoided by having a layer which is not intentionally doped. Doping in small volumes can lead to severe device to device fluctuations. When for instance a layer of 10x10x10 nm^3 is considered, and a doping density of e.g. 1e18/cm^3, this means that in that layer there has to be on the average 1 dopant atom. Changes in the number of dopant atoms therefore have an extreme impact on the device behavior. It is an advantage of embodiments of the present invention that this impact can be avoided or at least reduced by not intentionally doping at least one layer in the second inner region.

[0014] In a resistive switching memory cell according to embodiments of the present invention, at least one layer of the second inner region may be formed of Si, $SiGe_x$, SiN_x, Al_2O_3, MgO, AlN, Si_3N_4, SiO_2, HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, $GdAlO_x$, $DyScO_x$, Ta_2O_5, each in stoichiometric or off-stoichiometric composition, or a combination thereof, such that a Si, or a Si-containing layer is in direct contact with the first inner region.

[0015] In a resistive switching memory cell according to embodiments of the present invention, at least one layer of the first inner region may be formed in stoichiometric or off-stoichiometric MgO, Al_2O_3, TiO_2, HfO_2, ZrO_2, Ta_2O_5, TaO_2, Nb_2O_5, NbO_2, V_2O_5, VO_2, or a combination thereof, and the first inner region may be doped with N, Mg, Al, Si, Ge, or a combination thereof.

[0016] In a resistive switching memory cell according to embodiments of the present invention, the first inner region has a thickness extending between a surface between the first inner region and the second inner region and a surface between the first inner region and one of the electrodes, whereby the thickness of the first inner region may be between 2 nm and 30 nm, preferably between 2 nm and 15 nm.

[0017] In a resistive switching memory cell according to embodiments of the present invention, the second inner region has a thickness extending between a surface between the first inner region and the second inner region and a surface between the second inner region and one of the electrodes, whereby the thickness of the second inner region may be between 2 nm and 30 nm, preferably between 2 nm and 15 nm.

[0018] In a resistive switching memory cell according to embodiments of the present invention, the first electrode and the second electrode may be formed by one or more layers, each layer comprising one or more metals or metallic compound layers, selected from Ti, Ta, Hf, W, Mo, Ru, Ir, Ni, Cu, Al, Mg, TiN, TaN, TiCN, TaCN, TiAlN, or from heavily p, or n-type doped semiconductor materials such as Si, Ge, GaAs, InGaAs or of a combination thereof.

[0019] In a second aspect, the present invention provides a method for manufacturing a resistive switching memory cell. The method comprises providing a stack of a first electrode, a first inner region, a second inner region and a second electrode, such that the first inner region comprises one or more metal oxide layers in contact with the second inner region, and the second inner region comprises an insulating, semi-insulating or semiconductive layer, in contact with the first inner region, whereby the insulating, semi-insulating or semiconductive layer can scavenge oxygen from the first inner region, and whereby the insulating, semi-insulating or semiconductive layer has a nonlinear charge carrier transport behavior when a voltage or electric field is applied.

[0020] It is an advantage of embodiments of the present invention that a BEOL-compatible thermal budget is possible. It is an advantage of embodiments of the present invention that the electrode regions and the inner regions can be formed in materials that are compatible with CMOS technology.

[0021] A method according to embodiments of the present invention may comprise providing the first inner region and the second inner region in between the first electrode and the second electrode which are located in different substantially parallel planes such that the first electrode and the second electrode cross one another.

[0022] A method according to embodiments of the present invention may comprise providing the first inner region and the second inner region parallel with the first electrode.

[0023] A method according to embodiments of the present invention may comprise forming the first and second inner regions through a conformal coating process.

[0024] In a third aspect, the present invention provides a resistive switching memory cell according to embodiments of the first aspect, whereby the resistive switching memory cell is integrated in a cross-point array or in a vertical RRAM string.

[0025] It is an advantage of embodiments of the present invention that cross-point arrays or vertical RRAM strings can be realized that have a low thermal budget, a fast read/write access, a long time stability and a low voltage operation. The resistive switching memory cells according to embodiments of the present invention

are self-rectifying. Therefore it is an advantage of embodiments of the present invention that no extra elements are required such as transistors or rectifying diodes to reduce the sneak currents in cross-point arrays of vertical RRAM strings made with these resistive memory cells. Thereby the complexity (in case of a transistor an extra terminal would be required), the power dissipation, and the size can be reduced.

[0026] In a further aspect the present invention provides a method for operating a resistive switching memory cell (100) according to embodiments of the first aspect of the present invention. The method comprises
a writing step comprising

- a reset step wherein a first positive voltage is applied on the first electrode for bringing the resistive switching memory cell to a high resistive state, or
- a set step wherein a negative voltage is applied on the first electrode for bringing the cell to a low resistive state, and

a read-out step wherein a second positive voltage is applied to the first electrode for reading out the resistive state of the cell, whereby the second positive voltage is smaller than the first positive voltage.

[0027] It is an advantage of embodiments of the present invention that for the reset step a continuous range of positive voltages can be applied. The read-out voltage (the second positive voltage) should be below the voltage used at the reset step (the first positive voltage). It is an advantage of embodiments of the present invention that no forming step is required.

[0028] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

[0029] These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

Brief description of the drawings

[0030]

FIG. 1 shows a schematic cross-section of a resistive switching memory cell according to an embodiment of the present invention.
FIG. 2 shows a resistive switching memory cell integrated in a cross-point array in accordance with embodiments of the present invention.
FIG. 3 shows the current-voltage characteristic of a 40 nm size (meaning device area W x L = 40 nm x 40 nm) resistive switching memory cell according to an embodiment of the present invention.
FIG. 4 shows the analog behavior of a resistive switching memory cell according to an embodiment of the present invention.
FIG. 5 shows the current voltage characteristic of a 50 nm size resistive switching memory cell according to an embodiment of the present invention.
FIG. 6 shows the raw current voltage data of a sequence of 5 sweeps on a 40 nm size resistive switching memory cell according to an embodiment of the present invention. It shows averaged IV sweeps for 5 consecutive DC set/reset cycles, over a plurality of devices tested, and is illustrative for cycle-to-cycle uniformity.
FIG. 7 shows the raw current-voltage data on a plurality of 40 nm resistive switching memory cells according to an embodiment of the present invention. It shows raw and averaged data for a particular set or reset sweep and is illustrative for device-to-device uniformity.
FIG. 8 shows the raw current voltage data of a sequence of 5 sweeps on a 120 nm size resistive switching memory cell according to an embodiment of the present invention. It shows averaged IV sweeps for 5 consecutive DC set/reset cycles, over a plurality of devices tested, and is illustrative for cycle-to-cycle uniformity.
FIG. 9 shows the raw current voltage data on a plurality of 120 nm resistive switching memory cells according to an embodiment of the present invention. It shows raw and averaged data for a particular set or reset sweep and is illustrative for device-to-device uniformity.
FIG. 10 shows the on/off resistances in function of the cell size of resistive switching memory cells in accordance with embodiments of the present invention.
FIG. 11 shows a schematic cross-section of a resistive switching memory cell from a vertical RRAM string, in accordance with embodiments of the present invention.
Fig. 12 shows resistive memory cells integrated in vertical RRAM strings in accordance with embodiments of the present invention.

[0031] The drawings are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0032] Any reference signs in the claims shall not be construed as limiting the scope.

[0033] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of illustrative embodiments

[0034] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size

of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

[0035] The terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

[0036] Moreover, the terms top, under and the like in the description and the claims are used for descriptive purposes and not necessarily for describing relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other orientations than described or illustrated herein.

[0037] It is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0038] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[0039] Similarly it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

[0040] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[0041] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[0042] In the context of the present invention, an RRAM device is a type of nonvolatile random access memory device that operates by reversibly changing the resistance across a solid-state material or combination of materials.

[0043] In the context of the present invention, a vacancy is a type of point defect in a crystalline, polycrystalline or amorphous lattice, in which an atom, such as O, is missing from one of the lattice sites.

[0044] In the context of the present invention, a high resistive state corresponds with an OFF-state and a low resistive state corresponds with an ON-state.

[0045] In the context of the present invention, the Gibbs free energy of a vacancy is defined as the standard free energy required (absorbed or released), for forming a vacancy in a material or a material system, in accordance with specific chemical or redox reactions.

[0046] In a first aspect, the present invention relates to a resistive switching memory cell 100, an example whereof is schematically illustrated in FIG. 1. FIG. 1 shows the cross-section of a resistive memory cell which may be integrated in a cross-point array. An example of such cross-point array is illustrated in FIG. 2. Elements like word line drivers, bit line drivers, controllers etc. are not illustrated in the drawing and are not described here in more detail, as they are standard and known to a person skilled in the art. The dotted lines in FIG. 2 show the cross-section which is depicted in FIG. 1. The resistive switching memory cell 100 comprises a stack of a first inner region 120, and a second inner region 130, in between a first electrode 110 and a second electrode 140. These are all shown in the exemplary embodiments of the present invention illustrated in FIG. 1 and FIG. 2.

[0047] The first electrode 110, also referred to as top electrode (TE), may be made from a conductive material layer, such as metals or metallic compounds, for instance a transition metal e.g. Ru, W, or a transition metal nitride, e.g. TiN, TaN. Preferably the conductive material layer is compatible with standard CMOS processes. The ma-

terial of the top electrode influences the ON-OFF levels of the resistive switching memory cell 100. The first electrode 110 forms a Schottky barrier with the first inner region 120 underneath it. The top electrode preferably has a workfunction of midgap to p-type. By choosing, for the first electrode 110, a different material with a higher work function, the Schottky barrier height between the top electrode and the neighboring layer can be increased, and thus current levels can be decreased.

[0048] In the embodiment illustrated in FIG. 1, the first inner region 120 is provided adjacent the first electrode 110, but the invention is not limited thereto. In alternative embodiments (not illustrated) the location of the first inner region 120 and second inner region 130 can be inversed with respect to the top and bottom electrodes 110, 140.

[0049] The first inner region 120 serves as a switching layer and may for instance be a titanium dioxide layer (TiO_2). The material of the first inner region 120 may be a metal oxide or a transition metal oxide, which preferably easily forms oxygen vacancies by deposition or under thermal treatment, i.e. when the Gibbs free energy of oxygen vacancy formation under such conditions becomes negative. The metal oxides or transition metal oxides may be selected from the following list: Ta_2O_5, Nb_2O_5, HfO_2, ZrO_2, V_2O_5, MgO, Al_2O_3, Gd_2O_3, Sc_2O_3, LaO, or a combination of materials thereof. This list is non-exhaustive. Also a deviation from the stoichiometry is possible. It is also possible that the first inner region 120 comprises oxides with metals having different oxidation states, such as Ta_2O_5 and TaO_2, Nb_2O_5 and NbO_2 or V_2O_5 and VO_2. The first inner region 120 may comprise a stack of multiple layers. For instance, the first inner region 120 may comprise a TiO_2 layer with on top thereof a modified insulating (semiconductive) interface with the first electrode 110 by insertion of one or more insulating/semiconductive layers or by purpose modifying the material by doping or chemical/thermal treatments, such as for example nitridation and anneals, so as to suitably adjust its physical-chemical properties and morphology. In embodiments of the present invention the thickness of the first inner region 120 may be between 2 and 25 nm, such as between 3 and 20 nm, for instance about 8 nm.

[0050] The second inner region 130 is provided in between the first inner region 120 and the second electrode 140. The second inner region 130 is able to fulfill a double role:

- that of an nonlinear electron transport barrier, which modulates the RRAM cell conductivity in both low and high resistance states
- and, at the same time, that of an oxygen scavenger, able to induce an oxygen vacancy reservoir in the first inner region 120, where switching between the two memory states takes place. The reservoir is thereby large enough such that it cannot be emptied by processing or electrical manipulation.

[0051] In embodiments of present invention the second inner region 130 is amorphous and is not intentionally doped. The second inner region 130 may be an amorphous silicon (a-Si; having a higher bandgap than crystalline silicon) layer or any other layer (for instance comprising SiNx, or transition metal oxides) that can scavenge oxygen from the first inner region 120. The second inner region 130 may also be a SiGe alloy which can scavenge oxygen from the first inner region 120. Preferably the SiGe alloy is not doped. The second inner region 130 may comprise multiple materials. These materials may be organized in layers or as an alloy. In embodiments of the present invention the second inner region may comprise an Al_2O_3/a-Si layer. In embodiments of the present invention the thickness of the second inner region 130 is such that a barrier exists which makes the behavior of the resistive switching memory cell 100 non-linear. The thickness of the second inner region 130 may be between 2 and 25 nm, for instance between 4 and 20 nm, such as e.g. about 8 nm. The second inner region 130 should have a thickness which is sufficient to make the IV characteristics of the device non-linear. In an exemplary embodiment of the present invention the second inner region may have a thickness t_1. The electron barrier height between the second electrode 140 and the inner region 130 may be B1. In this example the material of the second inner region 130 could be replaced by another material, comprising insulating, semi-insulating or semiconductive layers that can scavenge oxygen from the first inner region (120), whereby the new material has a thickness $t_2 = t_1*(B_1/B_2)^{3/2}$ where B_2 is the electron barrier height between second electrode 140 and the inner region 130, implemented by the other material.

[0052] The second electrode 140 adjacent the second inner region 130, also referred to as bottom electrode (BE), may be made from a conductive material layer, such as a transition metal e.g. Ru, W, Ti, Ta, or a transition metal nitride, e.g. TiN, TaN. The first electrode 110 and second electrode 140 may be implemented in same, similar or different materials. The number of layers in first 110 and second electrode 140 may be the same or different. The second electrode 140 may be for instance be a titanium nitride layer (TiN). The second electrode may form a Schottky barrier with the second inner region.

[0053] Resistive switching memory cells according to embodiments of the present invention provide a stable switching. The set current and the reset current are dependent on the area of the resistive switching memory cell. For example: a resistive switching memory cell with a size of 40 nm may have a reset current of between 10 and 30 μA, for instance about 20 μA. This reset current can be controlled by process modification, such as nitridation or thermal treatment, or by appropriate design of the cell, for example suitable choice of the layer thickness or the inner regions. The set current may be a few μA, for example 1-5 μA.

[0054] In embodiments of the present invention the ratio between the read-out current in the ON state and the

read-out current in the OFF state may be bigger than 20. In an exemplary embodiment the read-out current in the ON state is 1 μA and the read-out current in the OFF state is 50 nA. This corresponds with a resistance in the ON state of 3 MΩ and a resistance in the OFF state of 60 MΩ. Hence in this exemplary embodiment an on/off window of 20 can be obtained. In embodiments of the present invention the on/off window may be between 1 and 1000, for example between 3 and 100.

[0055] In embodiments of the present invention the resistive switching memory cell may be operated at 5V DC or in pulse mode with pulse widths of 1ms or shorter, preferably 1μs, or shorter than that, for example 100 ns or even shorter than 10 ns. Shorter pulse widths will, however, require an increased voltage.

[0056] In particular embodiments of the present invention the resistive switching memory cell 100 may comprise:

- a first electrode 110 made of TiN,
- a first inner region 120 comprising a layer of Al_2O_3,
- a second inner region 130 comprising a layer of a-Si, a layer of TiO_2 and a layer of Al_2O_3,
- a second electrode 140 made of TiN.

Thus in this particular example, the following cell 100 is obtained: TiN/Al_2O_3/a-Si/TiO_2/Al_2O_3/TiN.

[0057] In embodiments of the present invention, switching memory cells 100 may be organized in a cross-point array as illustrated in FIG. 2, where each memory cell 100 is designed in a horizontal stack of layers. Alternatively, as illustrated in FIG. 11, a switching memory cell 100 may be configured in a vertical RRAM string, where each cell 100 is designed in a stack of vertical layers.

[0058] FIG. 12 shows a 3D-view of resistive switching memory cells integrated in vertical RRAM strings in accordance with embodiments of the present invention. The $A_1A_2A_3A_4$ cross-section of this figure is shown in FIG. 11. FIG. 12 shows a first inner region 120, a second inner region 130 against a first electrode 110 against a second inner region 130, against a first inner region 120. In FIG. 12 the first inner region and second inner region are drawn as one layer, for ease of drawing only. The detail of FIG. 11 shows the different layers 120, 130. In the exemplary embodiment of FIG. 12 the first electrode 110, the first inner region 120 and the second inner region 130 are organized in vertical layers. In the exemplary embodiment it are vertical bars. The first inner region 120 and the second inner region 130 are thereby parallel with the first electrode 110. The second electrodes in FIG. 12 are oriented orthogonal to the first inner region 120. In the exemplary embodiment of FIG. 12 the second electrodes 140 are in contact with the first inner regions 120.

[0059] In a second aspect, the present invention relates to a method for manufacturing a resistive switching memory cell according to embodiments of the first aspect of the present invention. The method comprises providing a bottom electrode (second electrode) 140, on top thereof providing a second inner region 130, on top thereof providing a first inner region 120 and on top thereof providing a first electrode, also called top electrode 110. The first electrode 110 thereby forms a Schottky barrier with the first inner region 120. The first inner region 120 comprises a metal oxide or a transition metal oxide that can easily form oxygen vacancies, and the second inner region 130 comprises an optionally amorphous, not intentionally doped insulating, semi-insulating or semiconductor layer which can scavenge oxygen from the first inner region 120 and which exceeds a minimal thickness such that the IV behavior of the memory cell becomes non-linear.

[0060] In embodiments of the present invention the second inner region may be deposited using a conformal coating method, such as e.g. chemical vapor deposition (CVD) or atomic layer deposition (ALD), or using a non-conformal coating method, such as e.g. physical vapor deposition (PVD). Other deposition methods are for example metal oxide chemical vapor deposition (MOCVD), pulsed laser deposition (PLD). It is an advantage that resistive switching memory cells 100 which are fabricated using a conformal coating method can be fabricated in a vertical array.

[0061] In embodiments of the present invention oxygen vacancies are induced into the first inner region 120 by annealing. Alternatively the oxygen vacancies can be created during deposition, through a variety of techniques, such as but not limited to physical vapor deposition, plasma treatments, and other techniques, which allow sputtering materials with off-stoichiometric composition.

[0062] A post-deposition anneal (PDA) step may be carried out after deposition of the first inner region 120 and before provision of the first electrode layer 110. This anneal step may be used for preparing the cell 100 in a pre-defined state (ON/OFF) or for adjusting the switching current levels. The PDA condition in relation to stack design determines whether the cell 100 is initially ON or initially OFF. For example in a resistive switching memory cell 100 comprising a stack of a first electrode 110 on top of a first inner region 120, on top of a second inner region 130, on top of a second electrode 140, annealing can induce more defects (vacancies) in the stack. These defects may be induced in a sub-region of the first inner region 120 (e.g. at the interface with the second inner region 130), or they may extend throughout the first inner region 120. Depending on the film thickness this may produce a memory cell which initially is either in the OFF or in the ON state. Furthermore, the density of generated vacancies may raise or reduce the switching current - exemplified as 20 μA earlier, or of the ON/OFF states, exemplified as 3 MOhm and 60 MOhm earlier.

[0063] In a third aspect, the present invention relates to the use of a resistive switching memory cell 100 according to embodiments of the first aspect in a cross-point array or in a vertical RRAM string. It is an advantage

of embodiments of the present invention that the resistive switching memory cells 100 are self-rectifying switching memory cells for which a selector is not required. These resistive switching memory cells 100 can fit into a pitch size cross-point array or in a vertical RRAM string.

[0064] In a fourth aspect, the present invention relates to a method for operating a resistive switching memory cell 100 according to aspects of the first embodiment of the present invention. The method comprises writing steps during which a value, represented by a high resistive (OFF-state) or a low resistive cell state (ON-state), is written into the cell, and readout steps, during which the value, represented by the high resistive or a low resistive cell state, is read out from the cell. A writing step comprises either one of

- a reset step wherein a first positive voltage is applied between the first electrode 110 (the top electrode) and the second electrode 140 (the bottom electrode), for example the second electrode 140 may be grounded and a positive voltage may be applied to the first electrode 110, for bringing the resistive switching memory cell to a high resistive state, or
- a set step wherein a negative voltage is applied between the first electrode 110 (the top electrode) and the second electrode 140 (the bottom electrode), for example the second electrode 140 may be grounded and a negative voltage may be applied to the first electrode 110 for bringing the cell to a low resistive state.

[0065] During the read-out step a second positive voltage is applied between the first electrode 110 (the top electrode) and the second electrode 140 (the bottom electrode), for example the second electrode 140 may be grounded and a positive voltage may be applied to the first electrode 110 (the top electrode) for reading out the resistive state of the cell, whereby the second positive voltage is smaller than the first positive voltage.

[0066] In the embodiment illustrated in FIG. 3, initially, i.e. after processing the resistive switching memory cell 100, the resistive switching memory cell 100 is in the ON-state (low resistive state).

[0067] The ratio between the OFF-state resistance and the ON-state resistance defines the ON/OFF window. The ON/OFF window is typical for a particular stack and can be derived from the IV sweeps. In embodiments of the present invention the pulsed Set or Reset voltage is higher than the DC Set or Reset voltage. For each decade the pulses are shortened, the Set or Reset voltage increases with a predetermined delta value. The Set or Reset voltage is depending on the stack (first electrode, first inner region, second inner region, second electrode) and on the stack materials of the resistive switching memory cell. The Set or Reset voltage is also depending on the Set and Reset operation. In an exemplary embodiment of the present invention the Reset voltage is 5.5 V in DC. In this example the trade-off between the voltage and pulse length is 0.2 V/decade. In embodiments of the present invention DC corresponds with a pulse length of 1 ms. For pulses longer than 1 ms there is no difference in Set and Reset voltages. In this example the Reset voltage for a 1 μs pulse is therefore about 5.5 V + 3 decades * (0.2 V/decade) which is equal to 6.1 V. For a pulse length of 100 ns the Reset voltage becomes 6.3 V. A similar reasoning can be maintained for a Set pulse.

[0068] First a reset step is applied. The voltage of the reset step is depending on the stack structure and on the process (e.g. annealing). The voltage is moreover depending on the applied pulse width. In an exemplary embodiment of the present invention the voltage of the reset step may be between 7 Volt and 5.5. V for a pulse width of the reset pulses between 1 ms and 10 ns. In the same exemplary embodiment the voltage during a subsequent set step is reduced down to -4 V for pulse widths between 1 ms and 10 ns.

[0069] By changing the voltage difference between the first electrode 110 (the top electrode) and the second electrode 140 (the bottom electrode) the oxygen vacancy distribution in the first inner region 120 and the second inner region 130 can be modified.

[0070] FIG. 3 shows the current through a resistive switching memory cell 100 versus the applied voltage difference between the top electrode 110 of and the bottom electrode 140 of the resistive switching memory cell (in the example the bottom electrode 140 is grounded. The vertical axis shows the current through the cell, expressed in Ampere. The horizontal axis shows the voltage applied to the cell, expressed in Volt. The resistive switching memory cell 100 in this example has a feature size of 40 nm (i.e. an area of $40*40nm^2$). The figure shows a number of consecutive, alternating Set/Reset sweeps whereby the shown data is raw data. The reset current is obtained by applying a voltage with positive polarity, the set current is obtained by applying a voltage with negative polarity on the top electrode, while grounding the bottom electrode. This example is given for 40 nm cells; however, the present invention is not limited thereto. Smaller sized resistive switching memory cells 100 are also possible.

[0071] In embodiments of the present invention the set as well as the reset current voltage (IV) characteristics are continuous for any cell size and do not exhibit sharp transitions (as for example shown in the IV characteristic of FIG. 3), which are typically indicative of filamentary switching.

[0072] In embodiments of the present invention, the switching currents during the writing (set or reset) operations, as well as during the read operations, depend on the cell size, and more specifically on the cell area, with a slope of 1:1 (as shown for example in FIG. 10). This behavior is caused by a switching mechanism and cell state which involve the whole or most of the cell cross-section area and is not localized in a particular cell region. The latter is typical for resistive memory cells where conductive filaments are formed.

[0073] In embodiments of the present invention the forming operation is not required. There is no distinct behavior for subsequent sweeps at higher voltages. In prior art resistive memory cells filaments are formed at higher voltages whereas the present invention does not rely on filament forming.

[0074] In embodiments of the present invention the operation of the resistive switching memory cell is forming voltage irrelevant. An example thereof is illustrated in FIG. 3 showing a different first IV trace at low biases.

[0075] FIG. 4 shows three different current voltage (IV) characteristics of a resistive switching memory cell 100 in accordance with embodiments of the present invention. The vertical axis shows the current expressed in Ampere. The horizontal axis shows the voltage expressed in Volt. Each of the reset IV characteristics has a different stop voltage, i.e. a voltage where the up going voltage sweep ends and starts to decrease again. Only the parts of the IV characteristics having a positive voltage polarity are shown. For graph 310, the stop voltage equals 4V, for graph 320 the stop voltage equals 5V and for graph 330 the stop voltage equals 6V. The downward part of the most left graph 310 fully overlaps with the upward part of the middle graph 320. Also the downward part of the middle graph 320 fully overlaps with the upward part of the most right graph 330. The reset state is thus continuously controllable by the stop voltage. A similar control is achievable for the set state. It is thus an advantage that resistive switching memory cells 100 according to embodiments of the present invention have an analog switching behavior. It is an advantage of embodiments of the present invention that multiple off states can be obtained for a resistive switching memory cell. This allows to use the resistive switching memory cells in a multi-level cell (MLC) configuration. The measurements in FIG. 4 are done on a 40 nm memory cell. The analog switching behavior moreover has as advantage that the resistive switching memory cell 100 according to embodiments of the present invention may be used for implementing electronic synapses for neuromorphic computing circuits/chips.

[0076] The reset voltage of the 40 nm resistive switching memory cell, of which the IV characteristic is illustrated in FIG. 3, goes up to 5.5 V in DC. The set voltage goes down to -4V in DC. Read-out of the current may for example be done at 3 V as shown by the double arrow 310 in FIG. 3. In the exemplary 40 nm embodiment, which is not intended to be limiting for the present invention, this leads to a current of around 1 μA when the resistive switching memory cell is in the ON state and to about 50 nA when the resistive switching memory cell is in the OFF state. The non-linearity is around 100 when it is defined as the ratio of the current at the maximum reset voltage and the current at half of the maximum reset voltage and around 500 when it is defined as the ratio of the current at the maximum reset voltage and the current at a third of the maximum reset voltage.

[0077] The switching currents increase with increasing size of the resistive switching memory cell. This is illustrated by comparison of FIG. 3, and FIG. 5. The vertical axis of FIG. 3, and FIG. 5 shows the current expressed in Ampere. The horizontal axis shows the voltage expressed in Volt. FIG. 3 shows the raw IV data of a number of sweeps for a resistive switching memory cell with a size of 40 nm. FIG. 5 shows a graph measured on a resistive switching memory cell 100 with a size of 50 nm. The graphs of FIG. 3, and FIG. 5 show multiple sweeps thereby illustrating the cycle-to-cycle uniformity of the resistive switching memory cells.

[0078] FIG. 7 and FIG. 9 show raw and averaged data for a particular set or reset sweep and are illustrative for the device-to-device uniformity. It is therefore an advantage of embodiments of the present invention that a uniform device to device behavior can be realized. FIG. 6, and FIG. 8 are averaged IV sweeps for 5 consecutive DC set/reset cycles, over a plurality of devices tested and are illustrative for the cycle-to-cycle uniformity.

[0079] For FIG. 8 and FIG. 9 the resistive switching memory cells 100 had a size of 120 nm. The vertical axis in FIG. 6-FIG. 9 represents the current through the switching memory cell 100 and is expressed in μA, the horizontal axis represents the voltage over the switching memory cell 100 and is expressed in V.

[0080] In embodiments of the present invention resistive switching memory cells have cell sizes with features below 200 nm, preferably below 50 nm, for instance between 5 nm and 40 nm, such as between 5 nm and 20 nm. [DenK1]As can be seen from FIG. 6 to FIG. 9 the cell currents increase with the device size.

[0081] As illustrated in FIG. 10, also on/off resistances scale with cell area: the smaller the cell size the higher the resistances. FIG. 10 shows the cell resistance (in Ω, in the particular embodiment illustrated measured at 3 V) in function of the cell area (in nm^2). The cell resistance is shown for cells in the OFF state (highest graph) as well as for cells in the ON state (lowest graph). It can be seen that both the ON and the OFF state resistances scale with the cell area in a 1:1 ratio. The graph illustrates a clear separation between the resistance values in the OFF state and the resistance values in the ON state.

Claims

1. A resistive switching memory cell (100), the memory cell comprising a stack of a first electrode (110), a first inner region (120), a second inner region (130) and a second electrode (140),
   wherein,

   - the first inner region (120) comprises one or more metal oxide layers
   - the second inner region (130) comprises one or more insulating, semi-insulating or semiconductive layers, whereby the second inner region (130) is in direct contact with the first inner region

(120) and can scavenge oxygen from the first inner region (120), and the second inner region (130)has a nonlinear charge carrier conduction dominant mechanism under an applied voltage or electric field.

2. A resistive switching memory cell (100) according to claim 1, whereby the metal of the at least one metal oxide layer of the first inner region (120) is a transition metal.

3. A resistive switching memory cell (100) according to any of the previous claims, whereby the second inner region (130) comprises at least one amorphous, or predominantly amorphous layer.

4. A resistive switching memory cell (100) according to any of the previous claims, whereby the second inner region (130) contains at least one layer which is not intentionally doped.

5. A resistive switching memory cell according to any of the previous claims, whereby at least one layer of the second inner region (130) is formed of Si, $SiGe_x$, SiN_x, Al_2O_3, MgO, AlN, Si_3N_4, SiO_2, HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, $GdAlO_x$, $DyScO_x$, Ta_2O_5, each in stoichiometric or off-stoichiometric composition, or a combination thereof, such that a Si, or a Si-containing layer is in direct contact with the first inner region (120).

6. A resistive switching memory cell (100) according to any of the previous claims, whereby at least one layer of the first inner region (120) is formed in stoichiometric or off-stoichiometric MgO, Al_2O_3, TiO_2, HfO_2, ZrO_2, Ta_2O_5, TaO_2, Nb_2O_5, NbO_2, V_2O_5, VO_2, or a combination thereof, and whereby the first inner region (120) may be doped with N, Mg, Al, Si, Ge, or a combination thereof.

7. A resistive switching memory cell (100) according to any of the previous claims, the first inner region (120) having a thickness extending between a surface between the first inner region (120) and the second inner region (130) and a surface between the first inner region (120) and one of the electrodes (110, 140), whereby the thickness of the first inner region (120) is between 2 nm and 30 nm, preferably between 2 nm and 15 nm.

8. A resistive switching memory cell (100) according to any of the previous claims, the second inner region (130) having a thickness extending between a surface between the first inner region (120) and the second inner region (130) and a surface between the second inner region (130) and one of the electrodes (110, 140), whereby the thickness of the second inner region (130) is between 2 nm and 30 nm, preferably between 2 nm and 15 nm.

9. A resistive switching memory cell (100) according to any of the previous claims, whereby the first electrode (110) and the second electrode (140) are formed by one or more layers, each layer comprising one or more metals or metallic compound layers, selected from Ti, Ta, Hf, W, Mo, Ru, Ir, Ni, Cu, Al, Mg, TiN, TaN, TiCN, TaCN, TiAlN, or from heavily p, or n-type doped semiconductor materials such as Si, Ge, GaAs, InGaAs or of a combination thereof.

10. A method for manufacturing a resistive switching memory cell, the method comprising providing a stack of a first electrode (110), a first inner region (120), a second inner region (130) and a second electrode (140), such that

- the first inner region (120) comprises one or more metal oxide layers in contact with the second inner region (130),
- and the second inner region (130) comprises an insulating, semi-insulating or semiconductive layer, in contact with the first inner region (120), whereby the insulating, semi-insulating or semiconductive layer can scavenge oxygen from the first inner region (120), and whereby the insulating, semi-insulating or semiconductive layer has a nonlinear charge carrier transport behavior when a voltage or electric field is applied.

11. A method according to claim 10, the method comprising providing the first inner region (120) and the second inner region (130) in between the first electrode (110) and the second electrode (140) which are located in different substantially parallel planes such that the first electrode (110) and the second electrode (140) cross one another.

12. A method according to claim 10, the method comprising providing the first inner region (120) and the second inner region (130) parallel with the first electrode (110).

13. A method according to any of claims 10 to 12, wherein the first and second inner regions (120, 130) are formed through a conformal coating process.

14. Use of a resistive switching memory cell (100) according to any of the claims 1 to 9, whereby the resistive switching memory cell is integrated in a cross-point array or in a vertical RRAM string.

15. A method for operating a resistive switching memory cell (100) according to any of the claims 1 to 9, the method comprising:

a writing step comprising

- a reset step wherein a first positive voltage is applied on the first electrode (110) for bringing the resistive switching memory cell to a high resistive state, or
- a set step wherein a negative voltage is applied on the first electrode (110) for bringing the cell to a low resistive state, and

a read-out step wherein a second positive voltage is applied to the first electrode (110) for reading out the resistive state of the cell, whereby the second positive voltage is smaller than the first positive voltage.

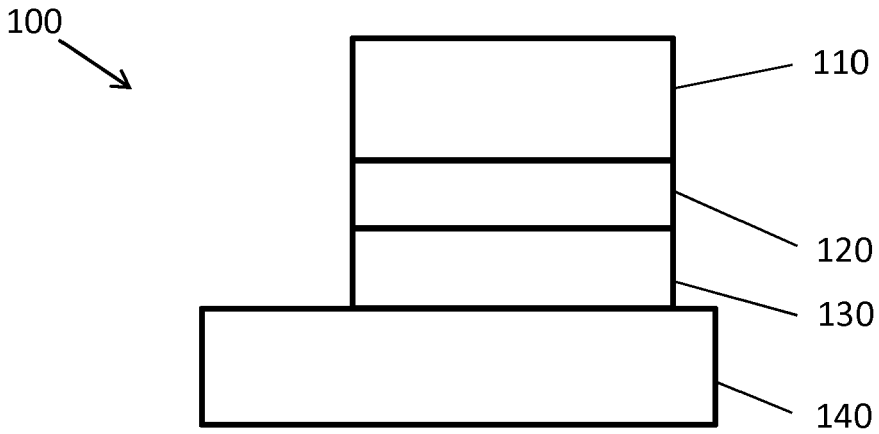

FIG. 1

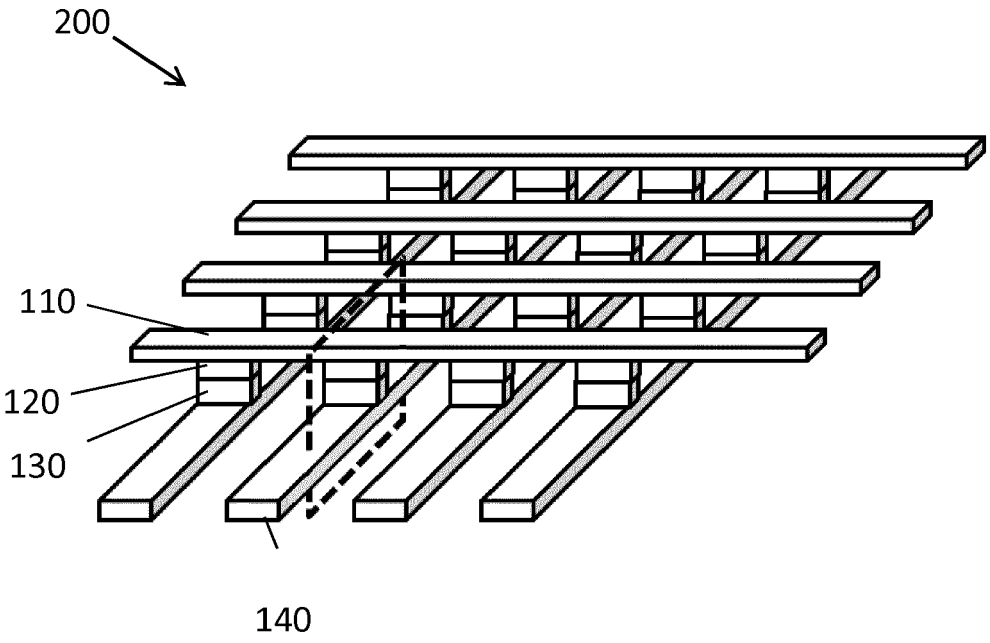

FIG. 2

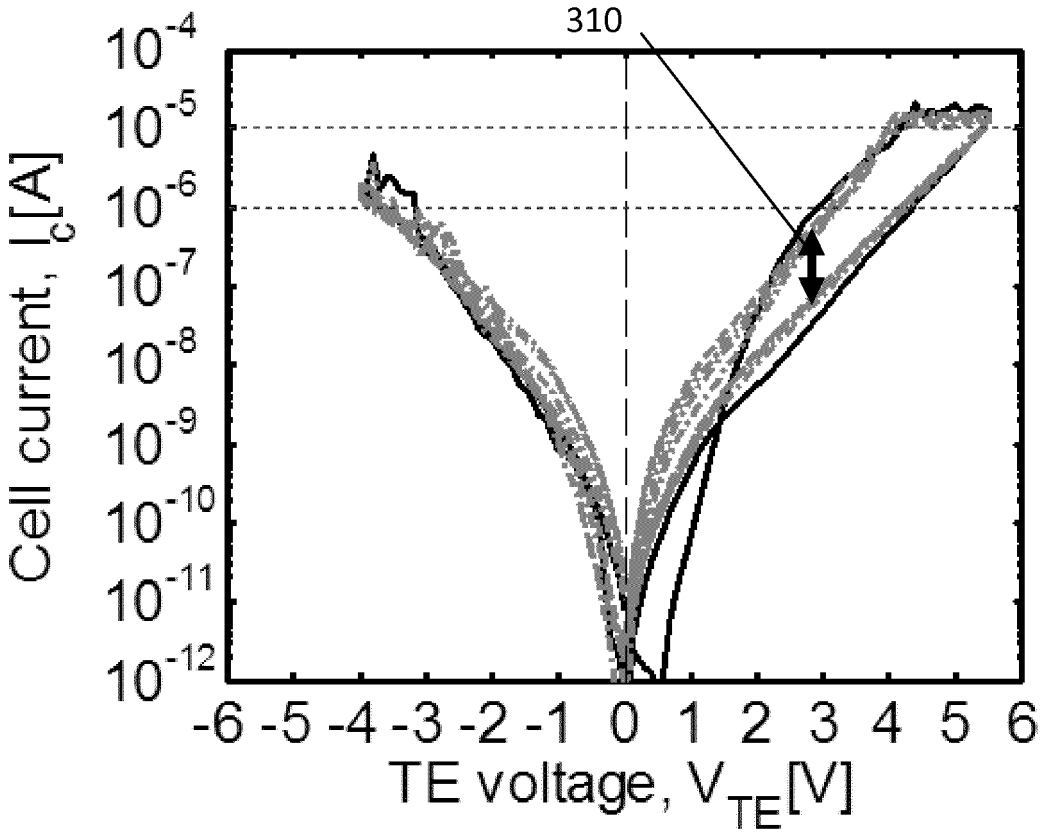
310
Cell current, I_c[A]
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
TE voltage, V_{TE}[V]

FIG. 3

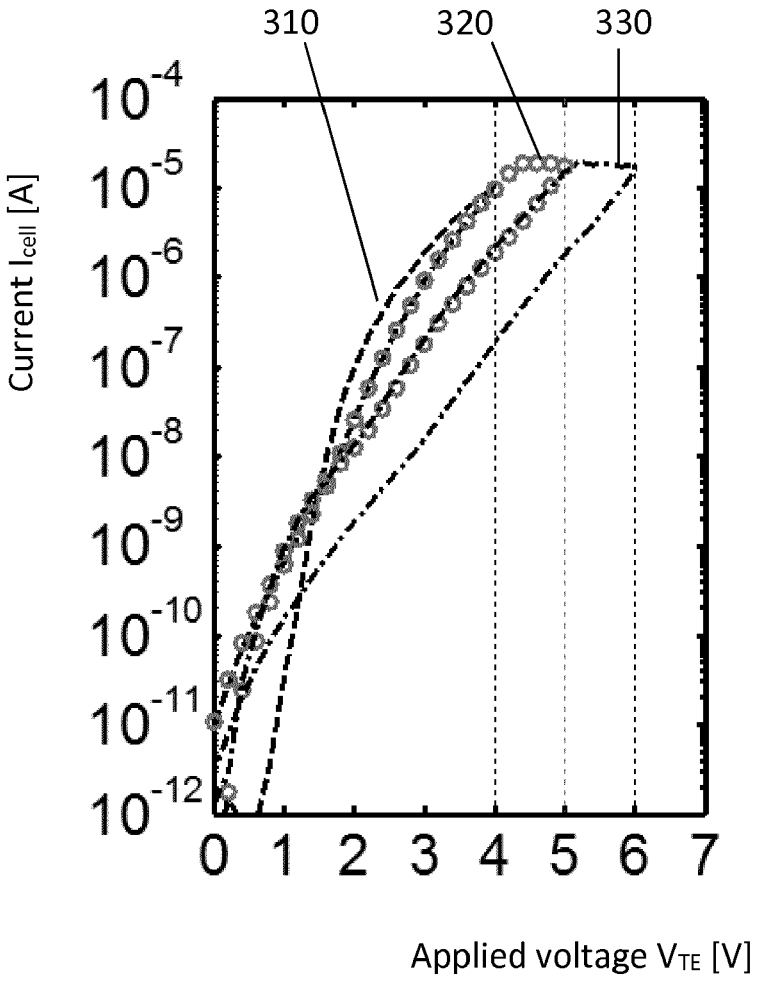
310
320
330
Current I_{cell} [A]
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
0 1 2 3 4 5 6 7
Applied voltage V_{TE} [V]

FIG. 4

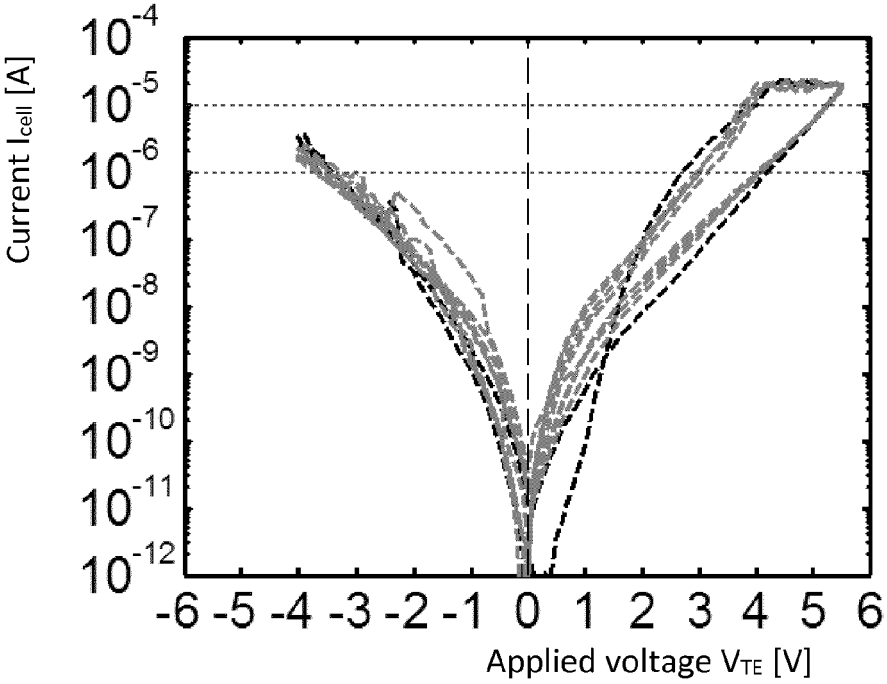
Current I_{cell} [A]
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Applied voltage V_{TE} [V]

FIG. 5

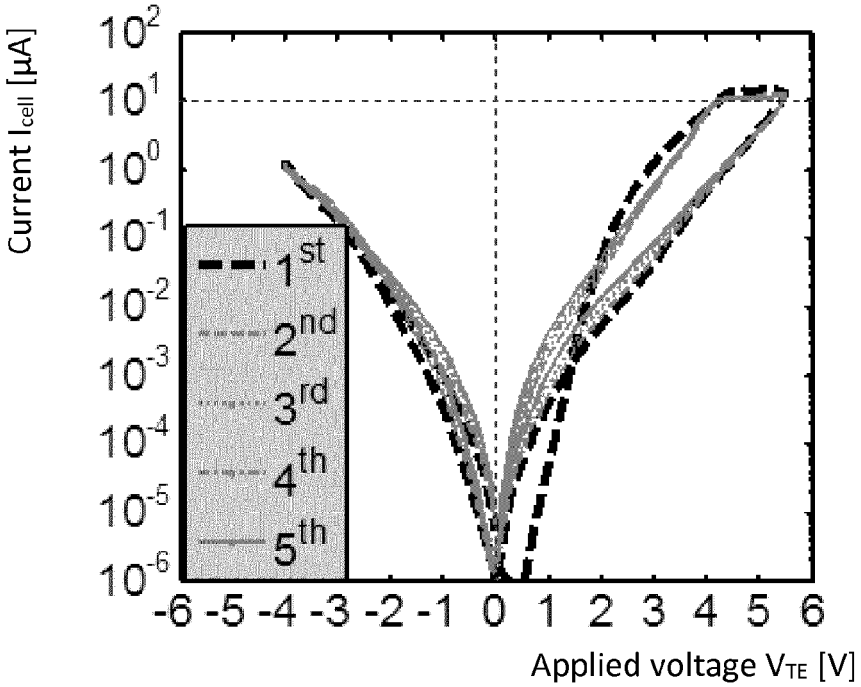
Current I_{cell} [μA]
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
1st
2nd
3rd
4th
5th
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Applied voltage V_{TE} [V]

FIG. 6

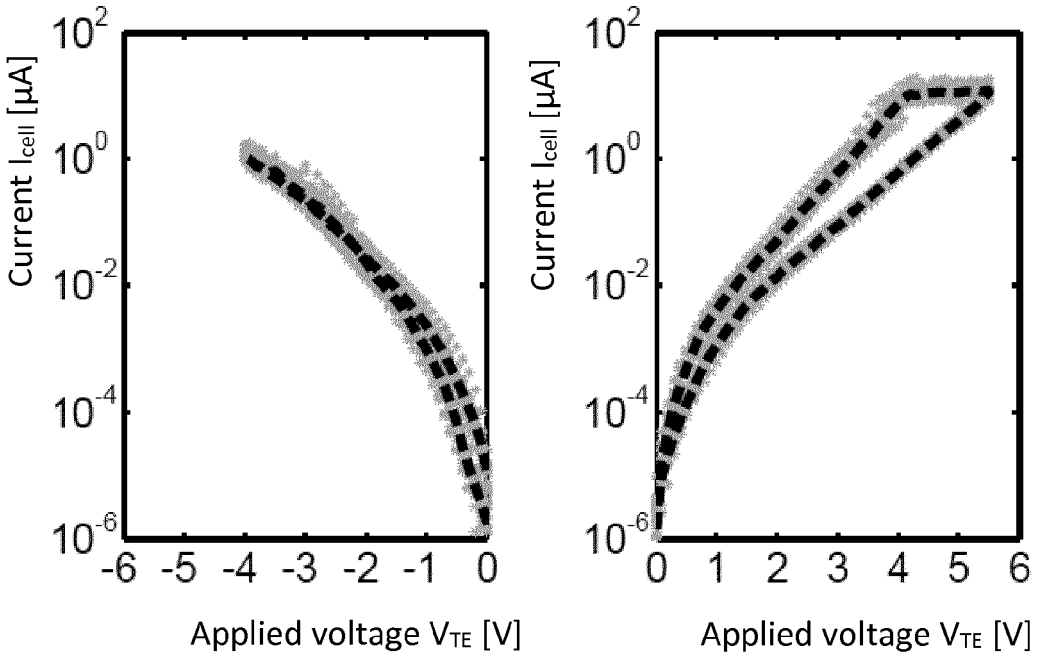
Current I_{cell} [μA]
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
-6 -5 -4 -3 -2 -1 0
Applied voltage V_{TE} [V]
Current I_{cell} [μA]
10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}
0 1 2 3 4 5 6
Applied voltage V_{TE} [V]

FIG. 7

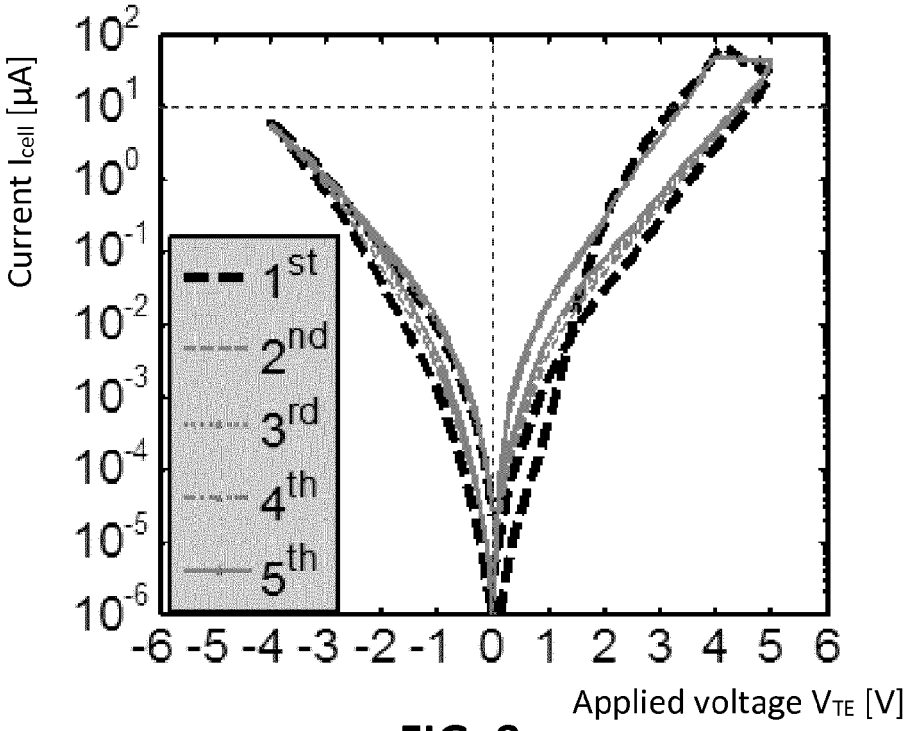
Current I_{cell} [μA]
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
1st
2nd
3rd
4th
5th
-6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6
Applied voltage V_{TE} [V]

FIG. 8

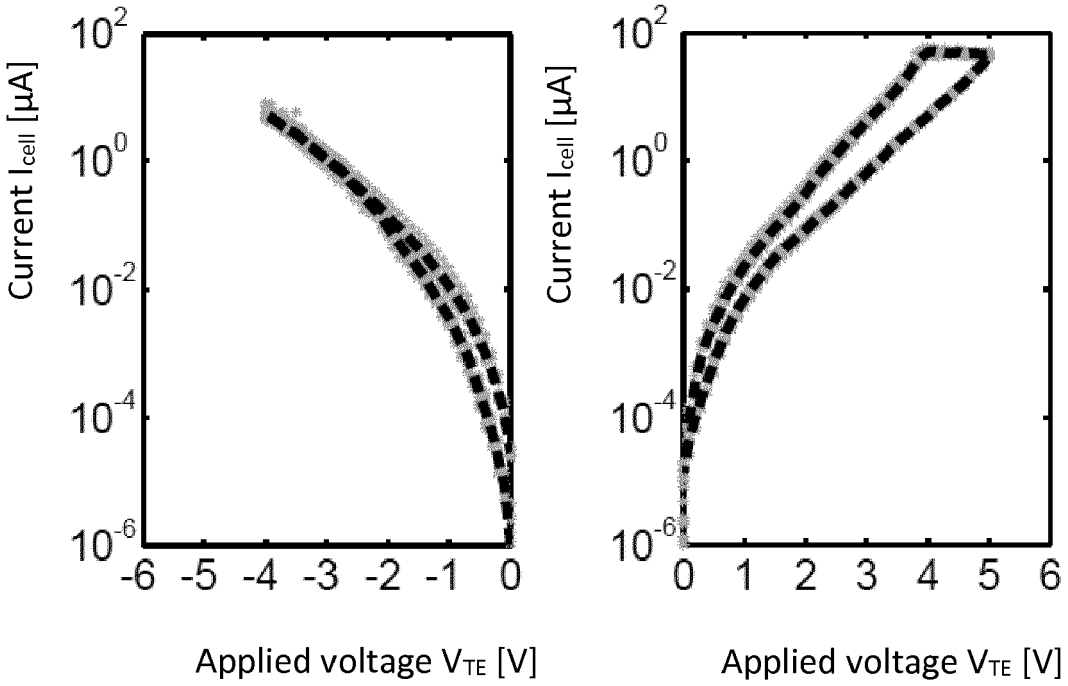
Current I_{cell} [μA]
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
-6 -5 -4 -3 -2 -1 0
Applied voltage V_{TE} [V]
Current I_{cell} [μA]
10^2
10^0
10^{-2}
10^{-4}
10^{-6}
0 1 2 3 4 5 6
Applied voltage V_{TE} [V]

FIG. 9

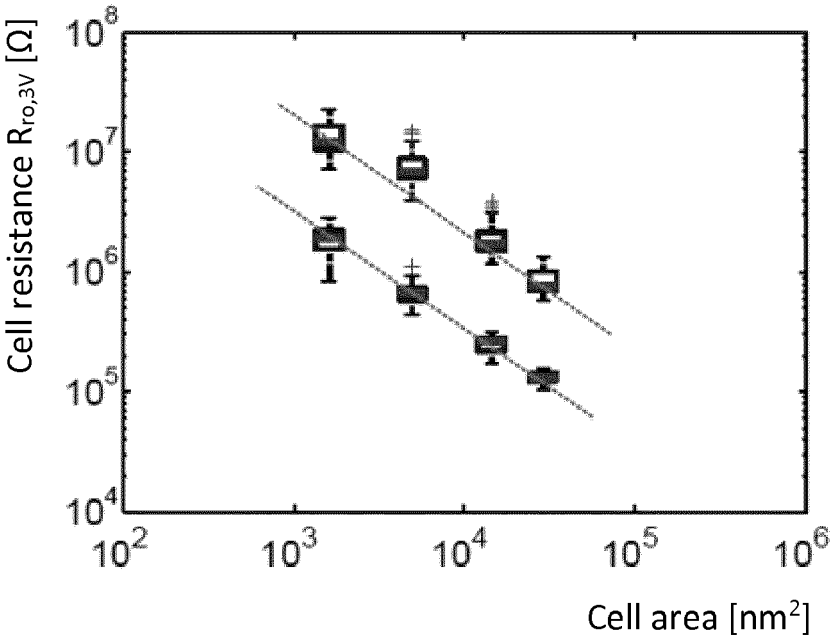
Cell resistance $R_{ro,3V}$ [Ω]
10^8
10^7
10^6
10^5
10^4
10^2 10^3 10^4 10^5 10^6
Cell area [nm^2]

FIG. 10

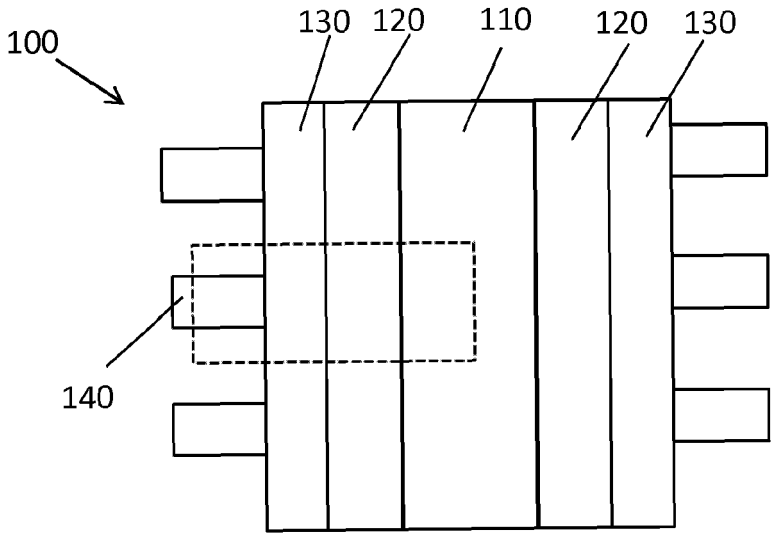

FIG. 11

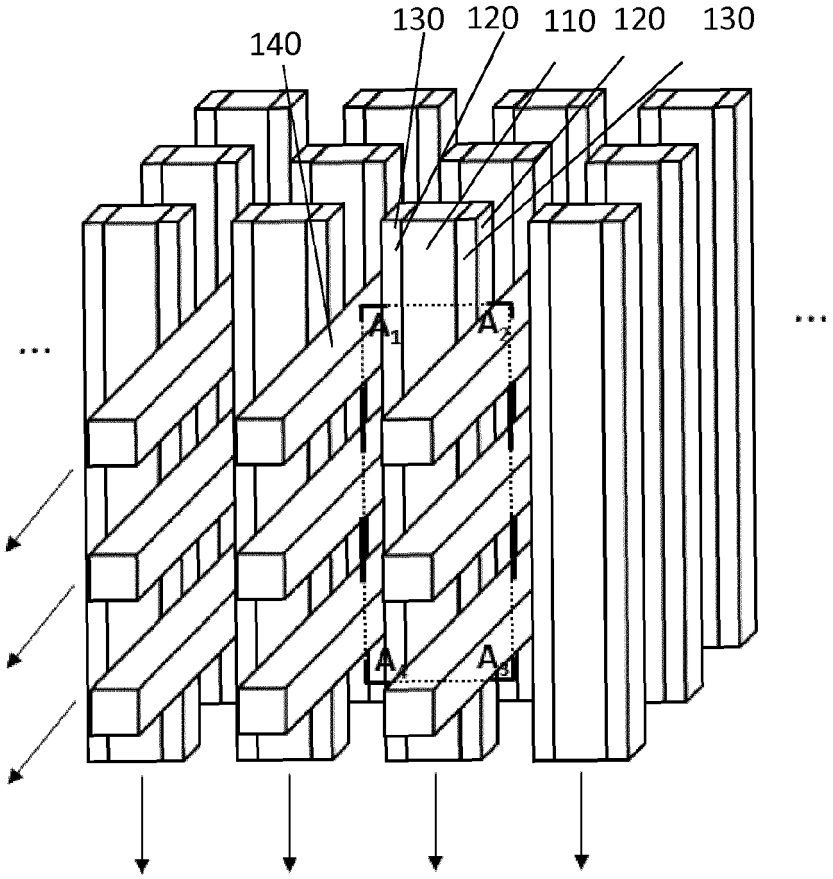

FIG. 12

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EUROPEAN SEARCH REPORT

Application Number
EP 15 15 1313

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2014/268993 A1 (CHIANG TONY P [US] ET AL) 18 September 2014 (2014-09-18) * paragraph [0057] - paragraph [0058]; figure 6 * * paragraph [0044] * * paragraph [0052] - paragraph [0053] * * paragraph [0033] - paragraph [0037]; figure 3 * * figures 4,5 *	1-15	INV. H01L45/00 G11C13/00 H01L27/24
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X	US 2012/091427 A1 (CHEN YUNG-TIN [US] ET AL) 19 April 2012 (2012-04-19) * paragraph [0039] - paragraph [0068]; figures 1,2 *	1-15	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	27 April 2015	Gröger, Andreas

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27-04-2015

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