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(71) Applicant *(for all designated States except US)*: **SILICONFILE TECHNOLOGIES INC.** [KR/KR]; 9F Yewon Bldg, 75-1, Yangjae-dong, Seocho-gu, Seoul 137-130 (KR).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **LEE, Do Young** [KR/KR]; 402-1002 Hansol-Apt, 102 Jungja-dong, Bundang-gu, Seongnam-si, Kyeungki-do 463-833 (KR).

(74) Agent: **LEE, Cheol Hee**; Guardian International Patent &, Law Office, 2F, Woo Kyeong Bldg., 156-13, Samseong-dong, Kangnam-ku, Seoul 135-090 (KR).

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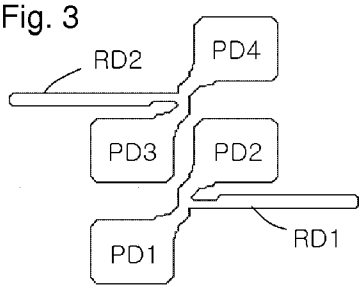
(54) **Title:** 4T-2S STEP & REPEAT UNIT PIXEL

Fig. 3



(57) **Abstract:** Disclosed is a 4T-2S step & repeat unit cell obtained by combining four image sensor unit cells each having four transistors into a single unit. A 4T-2S step & repeat unit cell includes a first photodiode diffusion area pattern, a second photodiode diffusion area pattern, a third photodiode diffusion area pattern, a fourth photodiode diffusion area pattern, a first image signal conversion circuit diffusion area pattern, and a second image signal conversion circuit diffusion area pattern. The second photodiode diffusion area pattern is formed in a diagonal direction from the first photodiode diffusion area pattern. The third photodiode diffusion area pattern is formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern. The fourth photodiode diffusion area pattern is formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern. The first image signal conversion circuit diffusion area pattern is formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern. The second image signal conversion circuit diffusion area pattern is formed above the third photodiode diffusion area pattern beside the fourth photodiode diffusion area pattern.

Description

4T-2S STEP & REPEAT UNIT PIXEL

Technical Field

[1] The present invention relates to a step & repeat unit cell, and more particularly, to a 4T-2S step & repeat unit cell obtained by combining four image sensor unit cells each having four transistors into a single unit.

Background Art

[2] An image sensor is implemented by arranging a plurality of image sensor unit cells in a two-dimensional array structure. That is, a horizontal image sensor unit line is formed by repeatedly arranging a single type of image sensor unit cells in a horizontal direction through a step & repeat process, and then, a vertical image sensor unit line is formed by repeatedly arranging in a vertical direction image sensor unit cells extended from each image sensor unit cell of the horizontal image sensor unit line, thereby implementing a single image sensor. The image sensor unit cell used in such a process is called a step & repeat unit cell.

[3] Although the term, step & repeat unit cell is generally used in a layout stage, the concept of the step & repeat unit cell will be described using a circuit diagram rather than a layout diagram.

[4] FIG. 1 is a circuit diagram for describing a process of forming a 4T-2S step & repeat unit cell by combining two image sensor circuits each having four transistors.

[5] Referring to FIG. 1, the 4T-2S step & repeat unit pixel 100 shown in the right-hand side is obtained by combining two step & repeat unit cells 10 and 20 shown in the left-hand side, each having four transistors. A first step & repeat unit cell 10 includes a single photodiode PD1 and an image signal conversion circuit for converting image signals generated from the photodiode PD1 into electric signals. The image signal conversion circuit has four transistors M11, M12, M13, and M14. While the second step & repeat unit cell 20 has a similar structure to the first step & repeat unit cell 10, the reference numerals of its components are differently denoted just for a distinguishing purpose.

[6] The 4T-2S step & repeat unit pixel 100 is obtained by sharing a reset transistor M12 or M22, a conversion transistor M13 or M23, and a selection transistor M14 or M24 between two 4T step & repeat unit cell 10 and 20 each having four transistors. The 4T-2S step & repeat unit cell 100 detects and transmits charges corresponding to image signals generated from two photodiodes PD1 and PD2 using two transmission transistors M11 and M21 and three transistors MC2, MC3, and MC4 that are commonly shared.

[7] The reset signal Rx12 applied to the gate of the reset transistor MC2 is enabled once at a corresponding time period when either of the charge transmission control signal Tx1 or Tx2 applied to the gate of the transmission transistor M11 or M21 is enabled. This fact is reflected in the reference numeral "12" of Rx12. Similarly, the reference numeral "12" of the selection signal Sx12 applied to the gate of the selection transistor MC4 is named for the same reason.

[8] As described above, the 4T-2S step & repeat unit cell obtained by combining two step & repeat unit cells each having four transistors can be laid out in various manners. However, the most important thing to be considered when the 4T-2S step & repeat unit cell is laid out is an aperture ratio.

Disclosure of Invention

Technical Problem

[9] The present invention provides a layout pattern of a 4T-2S step & repeat unit cell having an improved aperture ratio.

Technical Solution

[10] According to an aspect of the present invention, there is provided a 4T-2S step & repeat unit cell comprising a first photodiode diffusion area pattern, a second photodiode diffusion area pattern, a third photodiode diffusion area pattern, a fourth photodiode diffusion area pattern, a first image signal conversion circuit diffusion area pattern, and a second image signal conversion circuit diffusion area pattern. The second photodiode diffusion area pattern is formed in a diagonal direction from the first photodiode diffusion area pattern. The third photodiode diffusion area pattern is formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern. The fourth photodiode diffusion area pattern is formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern. The first image signal conversion circuit diffusion area pattern is formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern. The second image signal conversion circuit diffusion area pattern is formed above the third photodiode diffusion area pattern beside the fourth photodiode diffusion area pattern.

[11] According to another embodiment of the present invention, there is provided a 4T-2S step & repeat unit cell comprising a first photodiode diffusion area pattern, a second photodiode diffusion area pattern, a third photodiode diffusion area pattern, a fourth photodiode diffusion area pattern, a first image signal conversion circuit diffusion area pattern, and a second image signal conversion circuit diffusion area pattern. The second photodiode diffusion area pattern is formed in a diagonal direction from the first photodiode diffusion area pattern. The third photodiode diffusion area pattern is

formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern. The fourth photodiode diffusion area pattern is formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern. The first image signal conversion circuit diffusion area pattern is formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern. The second image signal conversion circuit diffusion area pattern is formed beside the third photodiode diffusion area pattern below the fourth photodiode diffusion area pattern above the second photodiode diffusion area pattern.

Advantageous Effects

[12] A 4T-2S step & repeat unit cell according to the present invention is advantageous in that an aperture ratio can be improved in comparison with a conventional unit cell by alternately arranging image signal conversion circuits for converting image signals detected from each photodiode into electric signals in the unit of a line.

Brief Description of the Drawings

[13] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

[14] FIG. 1 is a circuit diagram for describing a process of forming a 4T-2S step & repeat unit cell by combining two image sensor circuits each having four transistors;

[15] FIG. 2 is a circuit diagram illustrating a 4T-2S step & repeat unit cell according to the present invention;

[16] FIG. 3 is a layout diagram illustrating arrangement of active diffusion areas defining a 4T-2S step & repeat unit cell according to an embodiment of the present invention;

[17] FIG. 4 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 3 and gate layer patterns formed thereon;

[18] FIG. 5 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention;

[19] FIG. 6 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 5 and gate layer patterns formed thereon;

[20] FIG. 7 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention;

[21] FIG. 8 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 7 and gate layer patterns formed thereon;

[22] FIG. 9 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention;

[23] FIG. 10 is a layout diagram for showing arrangement of the active diffusion areas of

FIG. 9 and gate layer patterns formed thereon;

[24] FIG. 11 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 3;

[25] FIG. 12 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 5; and

[26] FIG. 13 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 7.

Best Mode for Carrying Out the Invention

[27] According to the present invention, a step & repeat unit cell is defined by combining four image sensor unit cells into a single unit, and the layout pattern of the defined unit cell is optimized. It is possible to readily implement an image sensor area by arranging the layout pattern of the defined unit cell in both of horizontal and vertical directions. Now, circuitry corresponding to the layout pattern will be described first to facilitate understanding of the layout pattern pertaining to the present invention.

[28] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[29] FIG. 2 is a circuit diagram illustrating a 4T-2S step & repeat unit cell according to the present invention.

[30] Referring to FIG. 2, a 4T-2S step & repeat unit cell includes a first subordinate unit cell (i.e., an upper portion with respect to a dotted line) and a second subordinate unit cell (i.e., a lower portion with respect to a dotted line). In the first subordinate unit cell, a reset transistor M13, a conversion transistor M14, and a selection transistor M15 are shared by two image sensors. Photodiodes PD3 and PD 4 of each image sensor are connected to transmission transistors M11 and M12. Similarly, in the second subordinate unit cell, a reset transistor M3, a conversion transistor M4, and a selection transistor M5 are shared by two image sensors. Also, photodiodes PD1 and PD2 of each image sensor are connected to transmission transistors M1 and M2.

[31] Unlike a conventional 4T-2S step & repeat unit cell of FIG. 1 defined by combining two image sensor unit cells into a single unit, a 4T-2S step & repeat unit cell of FIG. 2 according to the present invention is defined by combining four image sensor unit cells.

[32] Operation of an image sensor unit cell and a typical 4T-2S step & repeat unit cell sharing an image signal conversion circuit are well known in the art, and thus, description of their operation and electric characteristics will be omitted.

[33] FIG. 3 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to an embodiment of the present invention.

[34] Referring to FIG. 3, the active diffusion areas of the 4T-2S step & repeat unit cell

include areas for four photodiodes PD1, PD2, PD3, and PD4 and areas for image signal conversion circuits RD1 and RD2. A second photodiode PD2 is implemented in a right diagonal direction from a first photodiode PD1, and a third photodiode PD3 is implemented in a left-hand side of the second photodiode PD2 above the first photodiode PD1. A fourth photodiode PD4 is implemented in a diagonal direction from the third photodiode PD3 above the second photodiode PD2.

[35] A diffusion area pattern for a first image signal conversion circuit RD1 is implemented in a right-hand side of the first photodiode PD1 below the second photodiode PD2, and a diffusion area pattern for a second image signal conversion circuit RD2 is implemented in a left-hand side of the fourth photodiode PD4 above the third photodiode PD3.

[36] Diffusion area patterns of the first photodiode PD1, the second photodiode PD2, and the first image signal conversion circuit RD1 are connected to one another in a single pattern. Similarly, diffusion area patterns of the third photodiode PD3, the fourth photodiode PD4, and the second image signal conversion circuit RD2 are connected to one another in a single pattern.

[37] FIG. 4 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 3 and gate layer patterns formed thereon.

[38] Referring to FIG. 4, an upper right corner of the first photodiode PD1 is connected to a lower left corner of the second photodiode PD2 by extension. A first transmission transistor M1 for transmitting charges detected from the first photodiode PD1 and a second transmission transistor M2 for transmitting charges detected from the second photodiode PD2 are implemented on this extension area. Also, a first reset transistor M3, a first conversion transistor M4, and a first selection transistor M5 are implemented on the diffusion area pattern of the first image signal conversion circuit RD1.

[39] An upper right corner of the third photodiode PD3 is connected to a lower left corner of the fourth photodiode PD4 by extension. A third transmission transistor M11 for transmitting charges detected from the third photodiode PD3 and a fourth transmission transistor M12 for transmitting charges detected from the fourth photodiode PD4 are implemented on this extension area. Also, a second reset transistor M13, a second conversion transistor M14, and a second selection transistor M15 are implemented on the diffusion area pattern RD2 of the second image signal conversion circuit.

[40] FIG. 5 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention.

[41] Referring to FIG. 5, diffusion area patterns of the first and second image signal conversion circuits RD1 and RD2 are separated from the diffusion area patterns of the corresponding photodiodes unlike those shown in FIG. 3. While the diffusion area

patterns integrated in a single pattern of FIG. 3 are electrically connected, the diffusion area patterns of FIG. 4 are separated from one another. Therefore, they are connected in a subsequent wiring process. Specifically, contacts are formed on corresponding portions of two diffusion area patterns, and a metal line pattern is formed on the contacts, so that the two diffusion area patterns can be electrically connected to each other.

[42] FIG. 6 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 5 and gate layer patterns formed thereon.

[43] The arrangement of the diffusion area patterns and the gate layer formed thereon shown in FIG. 4 is similar to the diffusion area patterns and the gate layer formed thereon shown in FIG. 6 except for a fact that the diffusion area patterns of the first and second image signal conversion circuits RD1 and RD2 are separated from the diffusion area patterns of the extension between corresponding photodiodes. Therefore, detailed description of FIG. 6 will be omitted.

[44] FIG. 7 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention.

[45] The arrangement of the active diffusion areas shown in FIG. 7 according to another embodiment is similar to that shown in FIG. 3 except for a fact that the diffusion area pattern of the second image signal conversion circuit RD2 connected to the extension between the upper right corner of the third photodiode PD3 and the lower left corner of the fourth photodiode PD4 is located on a right-hand side rather than a left-hand side.

[46] FIG. 8 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 7 and gate layer patterns formed thereon.

[47] Referring to FIG. 8, an upper right corner of the first photodiode PD1 is connected to a lower left corner of the second photodiode PD2 by extension. A first transmission transistor M1 for transmitting charges detected from the first photodiode PD1 and a second transmission transistor M2 for transmitting charges detected from the second photodiode PD2 are implemented on this extension area. Also, a first reset transistor M3, a first conversion transistor M4, and a first selection transistor M5 are implemented on the diffusion area pattern of the first image signal conversion circuit RD1.

[48] An upper right corner of the third photodiode PD3 is connected to a lower left corner of the fourth photodiode PD4 by extension. A third transmission transistor M11 for transmitting charges detected from the third photodiode PD3 and a fourth transmission transistor M12 for transmitting charges detected from the fourth photodiode PD4 are implemented on this extension area. Also, a second reset transistor M13, a second conversion transistor M14, and a second selection transistor M15 are implemented on the diffusion area pattern RD2 of the second image signal conversion circuit.

[49] FIG. 9 is a layout diagram illustrating active diffusion areas defining a 4T-2S step & repeat unit cell according to another embodiment of the present invention.

[50] The diffusion area patterns of the first and second image signal conversion circuits RD1 and RD2 are separated from the diffusion area patterns of the corresponding photodiodes unlike those shown in FIG. 3. Since understanding of difference between embodiments shown in FIGS. 3 and 5 can be similarly applied to this arrangement, its description will be omitted.

[51] FIG. 10 is a layout diagram for showing arrangement of the active diffusion areas of FIG. 9 and gate layer patterns formed thereon.

[52] The arrangement of the diffusion area patterns and the gate layer formed thereon shown in FIG. 8 is similar to the arrangement of the diffusion area patterns and the gate layer formed thereon shown in FIG. 10 except for a fact that the diffusion area patterns of the first and second image signal conversion circuits RD1 and RD2 are separated from the diffusion area patterns of the extension between corresponding photodiodes as described above. Therefore, detailed description of FIG. 10 will be omitted.

[53] FIG. 11 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 3.

[54] Referring to FIG. 11, the first transmission transistor M1 is implemented on an upper right corner of the first photodiode PD1, and the second transmission transistor M2 is implemented on a lower left corner of the second photodiode PD2. The first reset transistor M3, the first conversion transistor M4, and the first selection transistor M5 are implanted on the diffusion area pattern of the first image signal conversion circuit RD1 in this order from the left side to the right side. Electric signals corresponding to image signals detected from the first and second photodiodes PD1 and PD2 are output from the right-side diffusion area of the first selection transistor M5.

[55] The third transmission transistor M11 is implemented on the upper right corner of the third photodiode PD3, and the fourth transmission transistor M12 is implemented on the lower left corner of the fourth photodiode PD4. The second reset transistor M13, the second conversion transistor M14, and the second selection transistor M15 are implemented on the diffusion area pattern of the second image signal conversion circuit RD2 in this order from the right side to the left side. Electric signals corresponding to image signals detected from the third and fourth photodiodes PD3 and PD4 are output from the left-side diffusion area of the second selection transistor M15.

[56] FIG. 12 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 5.

[57] FIG. 13 is a layout diagram illustrating a 4T-2S step & repeat unit cell implemented on the active diffusion area patterns of FIG. 7.

[58] The layout diagrams shown in FIGS. 12 and 13 would be readily understood by those

skilled in the art by referring to the description of FIG. 7, and thus, their description will be omitted.

[59] As recognized from the layout diagrams shown in FIGS. 11 and 13, the image signal conversion circuit is implemented between the lines of the photodiodes in the 4T-2S step & repeat unit cell according to the present invention in order to improve an aperture ratio.

[60] As described above, according to the present invention, a single step & repeat unit cell is defined by combining four image sensor unit cells, and the layout pattern of the defined unit cell is optimized.

[61] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the appended claims.

Claims

[1] A 4T-2S step & repeat unit cell comprising:
a first photodiode diffusion area pattern;
a second photodiode diffusion area pattern formed in a diagonal direction from the first photodiode diffusion area pattern;
a third photodiode diffusion area pattern formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern
a fourth photodiode diffusion area pattern formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern;
a first image signal conversion circuit diffusion area pattern formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern; and
a second image signal conversion circuit diffusion area pattern formed above the third photodiode diffusion area pattern beside the fourth photodiode diffusion area pattern,
wherein at least a corner of the first photodiode diffusion area pattern, at least a corner of the second photodiode diffusion area pattern, and an end of the first image signal conversion circuit diffusion area pattern are connected to one another by extension, and at least a corner of the third photodiode diffusion area pattern, at least a corner of the fourth photodiode diffusion area pattern, and an end of the second image signal conversion circuit diffusion area pattern are connected to one another by extension.

[2] A 4T-2S step & repeat unit cell comprising:
a first photodiode diffusion area pattern;
a second photodiode diffusion area pattern formed in a diagonal direction from the first photodiode diffusion area pattern;
a third photodiode diffusion area pattern formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern;
a fourth photodiode diffusion area pattern formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern;
a first image signal conversion circuit diffusion area pattern formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern; and
a second image signal conversion circuit diffusion area pattern formed above the third photodiode diffusion area pattern beside the fourth photodiode diffusion

area pattern,

wherein at least a corner of the first photodiode diffusion area pattern and at least a corner of the second photodiode diffusion area pattern are connected to each other by extension, and at least a corner of the third photodiode diffusion area pattern and at least a corner of the fourth photodiode diffusion area pattern are connected to each other by extension.

[3] The 4T-2S step & repeat unit cell according to claim 2, wherein a common diffusion area pattern for connecting at least the corner of the first photodiode diffusion area pattern and at least the corner of the second photodiode diffusion area pattern to each other by extension is connected to the first image signal conversion circuit diffusion area pattern through a metal line, and a common diffusion area pattern for connecting at least the corner of the third photodiode diffusion area pattern to at least the corner of the fourth photodiode diffusion area pattern by extension is connected to the second image signal conversion circuit diffusion area pattern through a metal line.

[4] A 4T-2S step & repeat unit cell comprising:

a first photodiode diffusion area pattern;

a second photodiode diffusion area pattern formed in a diagonal direction from the first photodiode diffusion area pattern;

a third photodiode diffusion area pattern formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern;

a fourth photodiode diffusion area pattern formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern;

a first image signal conversion circuit diffusion area pattern formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern; and

a second image signal conversion circuit diffusion area pattern formed above the third photodiode diffusion area pattern beside the fourth photodiode diffusion area pattern,

wherein a first transmission transistor is implemented near at least the corner of the first photodiode diffusion area pattern, and a second transmission transistor is implemented near at least the corner of the second photodiode diffusion area pattern on a common diffusion area pattern for connecting at least the corner of the first photodiode diffusion area pattern and at least the corner of the second photodiode diffusion area pattern to each other by extension, and

wherein a third transmission transistor is implemented near at least the corner of the third photodiode diffusion area pattern, and a fourth transmission transistor is

implemented near at least the corner of the fourth photodiode diffusion area pattern on a common diffusion area pattern for connecting at least the corner of the third photodiode diffusion area pattern and at least the corner of the fourth photodiode diffusion area pattern to each other by extension.

[5] A 4T-2S step & repeat unit cell comprising:
a first photodiode diffusion area pattern;
a second photodiode diffusion area pattern formed in a diagonal direction from the first photodiode diffusion area pattern;
a third photodiode diffusion area pattern formed above the first photodiode diffusion area pattern beside the second photodiode diffusion area pattern;
a fourth photodiode diffusion area pattern formed in a diagonal direction from the third photodiode diffusion area pattern above the second photodiode diffusion area pattern;
a first image signal conversion circuit diffusion area pattern formed beside the first photodiode diffusion area pattern below the second photodiode diffusion area pattern; and
a second image signal conversion circuit diffusion area pattern formed beside the third photodiode diffusion area pattern below the fourth photodiode diffusion area pattern above the second photodiode diffusion area pattern.

[6] The 4T-2S step & repeat unit cell according to claim 5, wherein at least a corner of the first photodiode diffusion area pattern, at least a corner of the second photodiode diffusion area pattern, and an end of the first image signal conversion circuit diffusion area pattern are connected to one another by extension, and at least a corner of the third photodiode diffusion area pattern, at least a corner of the fourth photodiode diffusion area pattern, and an end of the second image signal conversion circuit diffusion area pattern are connected to one another by extension.

[7] The 4T-2S step & repeat unit cell according to claim 5, wherein at least a corner of the first photodiode diffusion area pattern and at least a corner of the second photodiode diffusion area pattern are connected to each other by extension, and at least a corner of the third photodiode diffusion area pattern and at least a corner of the fourth photodiode diffusion area pattern are connected to each other by extension.

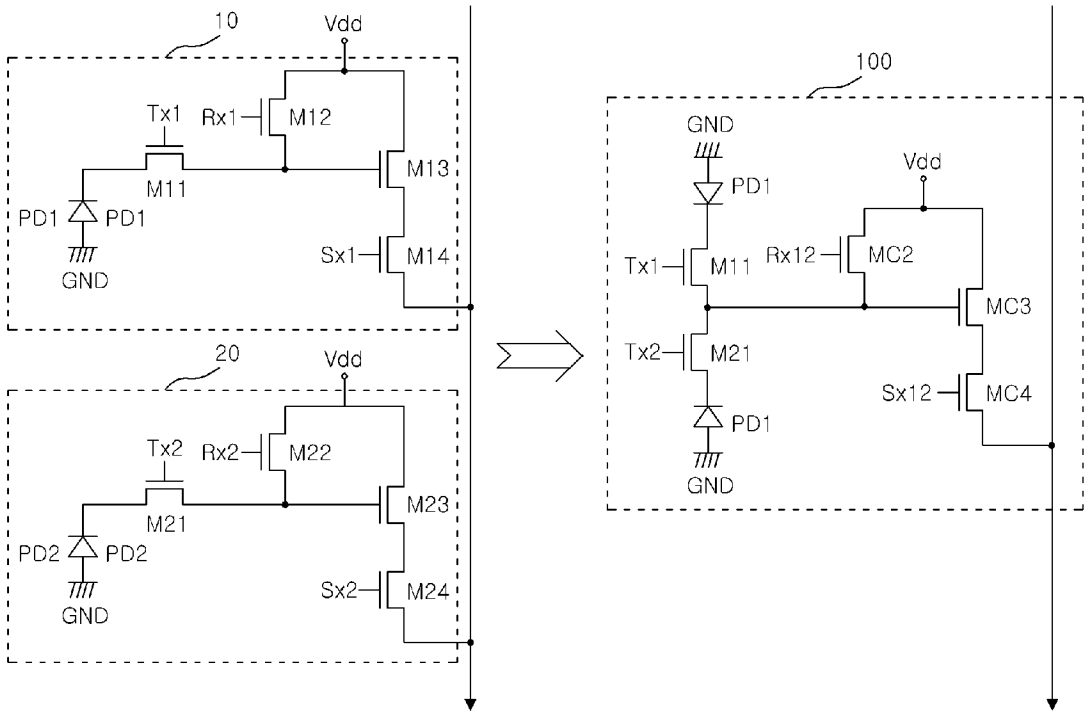
[8] The 4T-2S step & repeat unit cell according to claim 7, wherein a common diffusion area pattern for connecting at least the corner of the first photodiode diffusion area pattern and at least the corner of the second photodiode diffusion area pattern to each other by extension is connected to the first image signal conversion circuit diffusion area pattern through a metal line, and a common

diffusion area pattern for connecting at least the corner of the third photodiode diffusion area pattern and at least the corner of the fourth photodiode diffusion area pattern to each other by extension is connected to the second image signal conversion circuit diffusion area pattern through a metal line.

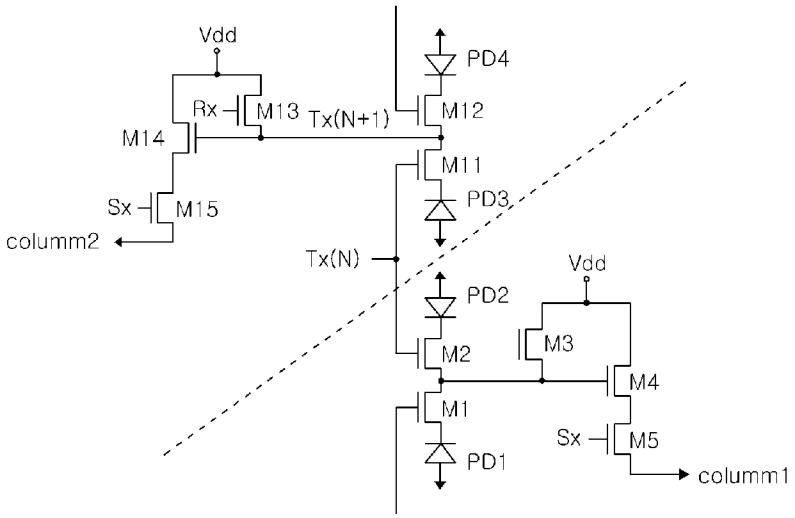
[9] The 4T-2S step & repeat unit cell according to claim 5, wherein a first transmission transistor is implemented near at least the corner of the first photodiode diffusion area pattern, and a second transmission transistor is implemented near at least the corner of the second photodiode diffusion area pattern on a common diffusion area pattern for connecting at least the corner of the first photodiode diffusion area pattern and at least the corner of the second photodiode diffusion area pattern to each other by extension, and
wherein a third transmission transistor is implemented near at least the corner of the third photodiode diffusion area pattern, and a fourth transmission transistor is implemented near at least the corner of the fourth photodiode diffusion area pattern on a common diffusion area pattern for connecting at least the corner of the third photodiode diffusion area pattern and at least the corner of the fourth photodiode diffusion area pattern to each other by extension.

[10] The 4T-2S step & repeat unit cell according to claim 5, wherein a first reset transistor, a first conversion transistor, and a first selection transistor are implemented on the first image signal conversion circuit diffusion area pattern, and a second reset transistor, a second conversion transistor, and a second selection transistor are implemented on the second image signal conversion circuit diffusion area pattern.

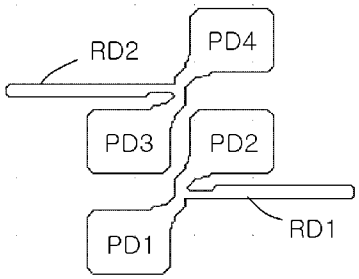
[Fig. 1]



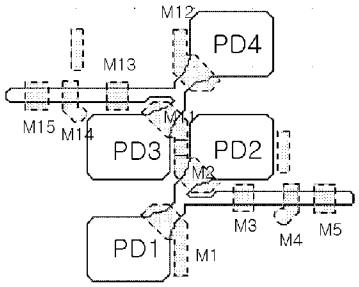
[Fig. 2]



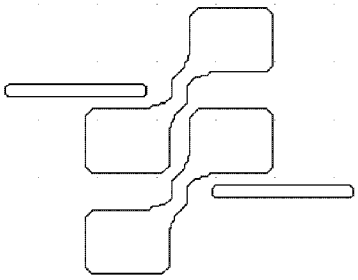
[Fig. 3]



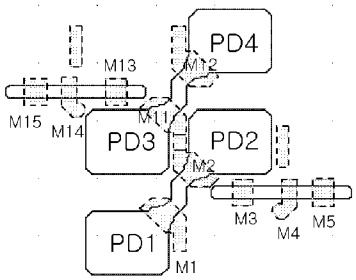
[Fig. 4]



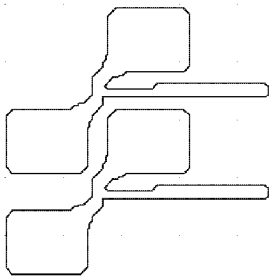
[Fig. 5]



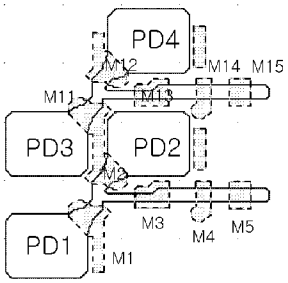
[Fig. 6]



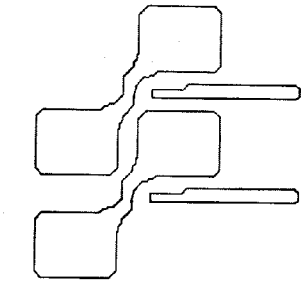
[Fig. 7]



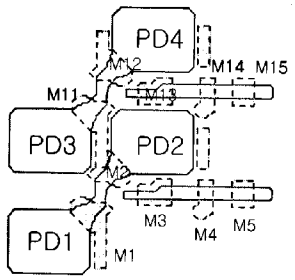
[Fig. 8]



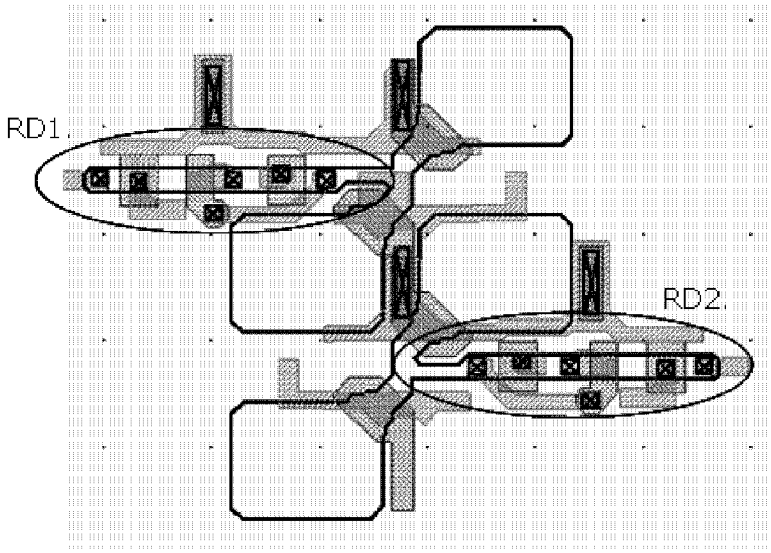
[Fig. 9]



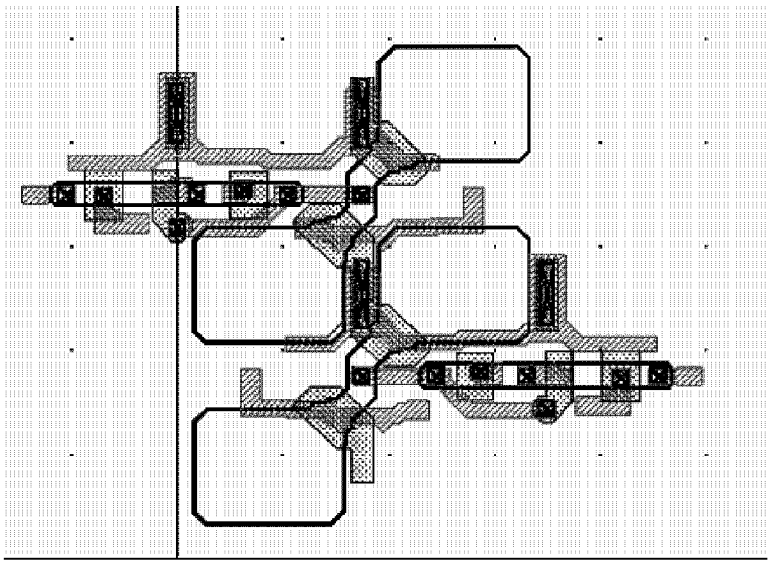
[Fig. 10]



[Fig. 11]



[Fig. 12]



[Fig. 13]