(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 August 2009 (27.08.2009)

PCT

(10) International Publication Number
WO 2009/105146 A1

(51) International Patent Classification:
H01Q 1/38 (2006.01)

(21) International Application Number:
PCT/US2008/088516

(22) International Filing Date:
30 December 2008 (30.12.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/034,023 20 February 2008 (20.02.2008) US

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; Mew Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **FLOYD, Brian** [US/US]; 4 Tanya Lane, Mahopac, NY 10541 (US). **LIU, Duixian** [US/US]; 32 Moorland Drive, Scarsdale, NY 10583 (US).

(74) Agents: **MASON, Kevin, M.** et al.; Ryan, Mason & Lewis, LLP, 1300 Post Road-suite 205, Fairfield, CA 06824 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

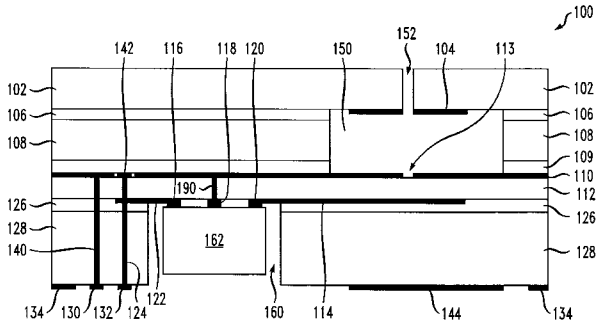
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: RADIO FREQUENCY (RF) INTEGRATED CIRCUIT (IC) PACKAGES WITH INTEGRATED APERTURE-COUPLED PATCH ANTENNA(S)

FIG. 1



(57) **Abstract**: A radio-frequency integrated circuit chip package with at least one integrated aperture-coupled patch antenna includes at least one generally planar patch and at least one generally planar ground plane spaced inwardly from the generally planar patch and substantially parallel thereto. The ground plane is formed with at least one coupling aperture slot therein. The slot is substantially opposed to the patch. Also included are at least one feed line spaced inwardly from the ground plane and substantially parallel thereto, at least one radio frequency chip spaced inwardly from the feed line and coupled to the feed line and the ground plane, and a first substrate layer spaced inwardly from the feed line. The first substrate layer is formed with a chip-receiving cavity. The chip is located in the chip-receiving cavity.

WO 2009/105146 A1

RADIO FREQUENCY (RF) INTEGRATED CIRCUIT (IC) PACKAGES WITH INTEGRATED APERTURE-COUPLED PATCH ANTENNA(S)

Field of the Invention

The present invention generally relates to communications circuitry, and, more particularly, to radio frequency (RF) integrated circuit (IC) packages.

Background of the Invention

In a wireless network, the connectivity and communication between devices is achieved through antennas attached to receivers or transmitters, in order to radiate the desired signals to or from other elements of the network. In radio communication systems, such as millimeter-wave radios, discrete components are usually assembled with low integration levels. These systems are often assembled using expensive and bulky waveguides and package-level or board-level microstrip structures to interconnect semiconductors and their required transmitter- or receiver-antennas. With recent progress in semiconductor technology and packaging engineering, the dimensions of these radio communication systems have become smaller. For applications such as wireless universal serial bus (USB), the operating distance is limited to about a meter; and a single antenna with about 7 dBi at 60 GHz will provide the necessary antenna gain. For distances as long as 10 meters (such as wireless video) or longer (such as radar), in point-to-point applications, antenna gains as high as 30 dBi, depending on the application, are required. However, high gain antennas for wireless video applications have very narrow beam widths, so pointing the antenna is very difficult for consumers. Therefore, a radiation pattern steerable array (also a phased array) is necessary. Phased arrays are also widely used in military radars. However, packaging RF chips with integrated antennas or phased arrays is extremely difficult and very expensive due to the expensive components and extensive labor involved.

Summary of the Invention

Principles of the present invention provide techniques for implementing RF IC packages with integrated aperture-coupled patch antennas.

In an exemplary embodiment, according to one aspect of the invention, a radio-frequency integrated circuit chip package with at least one integrated aperture-coupled patch antenna includes at least one generally planar patch and at least one generally planar ground plane spaced inwardly from the generally planar patch and substantially parallel thereto. The ground plane is formed with at least one coupling aperture slot therein. The slot is substantially opposed to the patch. Also included are at least one feed line spaced inwardly from the ground plane and substantially parallel thereto, at least one radio frequency chip spaced inwardly from the feed line and coupled to the feed line and the ground plane, and a first substrate layer spaced inwardly from the feed line. The first substrate layer is formed with a chip-receiving cavity. The chip is located in the chip-receiving cavity.

One or more embodiments of the invention are suitable for automatic processes and reduce the number of components previously involved with packaging antennas.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 shows an exemplary embodiment of a package, in cross section, according to an aspect of the invention;

FIG. 2 shows an exemplary embodiment of another package, in cross section, according to another aspect of the invention;

FIG. 3 shows an exemplary embodiment of yet another package, in cross section, according to yet another aspect of the invention;

FIG. 4 is a bottom view of an exemplary package with no reflector or an embedded reflector;

FIG. 5 is a bottom view of an exemplary package with a visible reflector; and

FIG. 6 is a bottom view of an exemplary planar phased array embodiment.

Detailed Description of Preferred Embodiments

One or more embodiments of the invention provide an apparatus and method for low cost packages with integrated antennas and phased arrays operating in the millimeter wave (mmWave) range. An exemplary inventive package with integrated antennas is based on a multilayer printed circuit board (PCB). The package contains multiple cavities for implementing high performance antenna(s) or antenna arrays and housing mmWave radio frequency (RF) integrated circuit chips. One or more embodiments of the invention also provide techniques to overcome the difficulties in making internal cavities and to avoid the need to employ wire bond technology at mmWave frequencies. Embodiments of the inventive packaging technology are consistent with the PCB manufacturing process and can be used for packages with an integrated antenna or antenna array.

Instances of the invention thus provide low cost packaging with integrated antennas or planar phased arrays; in particular, chip packaging with integrated antennas or planar phased array designs for mmWave frequencies and above.

Typical chip packages with integrated antennas have three major parts: (i) an RF chip, (ii) one or more antennas, and (iii) a package carrier (and in some instances, a package lid or cover, or an encapsulant to protect the package). One or more embodiments of the invention provide a package that has high performance antennas, an interface for flip-chipping an RF chip and an interface for flip-chipping the package to a printed circuit mother board.

FIG. 1 shows a cross-sectional view of an exemplary package 100, according to an aspect of the invention. Note that section lining is omitted for clarity. The package has seven total layers, including substrate and bounding layers. For mmWave applications, especially for frequencies above 60 GHz, bounding film and/or layer thickness has to be considered in the design process. Given the teachings herein, a person having ordinary skill in the antenna and packaging arts will know how to take the thickness into account and how to employ high precision PCB fabrication techniques to make embodiments of the invention. The package 100 also has a number of metal layers. In particular, there is an outermost substrate 102. Immediately inward therefrom is a metal layer used for the patch(es) 104 of the patch antenna(s). Inward of the substrate 102 and patch antenna 104 (only a single antenna is depicted in FIG. 1, but more can be

provided as discussed below) are a bound film layer 106, another substrate layer 108, and another bound film layer 109. Another metal layer, inward of bound film 109, is used for the ground plane 110 of the patch antenna. Slot(s) 113 on the ground plane are used for the apertures of the aperture-coupled patch antennas. The ground plane 110 also separates the radiating elements (patches) 104 from the feed line(s) and the RF chip(s), discussed below.

Another substrate 112 is inward from ground plane 110. Another metal layer is inward from substrate 112 and is used to implement the antenna feed line(s) 114, pads 116, 118, 120 for RF chip connections (preferably a flip-chip/C4 ("controlled collapse chip connection") type of connection), and interconnection(s) 122 (as appropriate) to one or more vias, such as via 124, in a further bound film layer 126 inward of the metal layer forming feed line 114, and a further substrate 128 inward of bound film 126. A still further metal layer provides all the pads for signal, control, power supply, and ground connections to the mother PCB (the mother PCB is omitted from the figure for clarity). Pads may include ground pad 130 interconnected with ground plane 110 through ground via 140, as well as one or more of signal, power, and control pads exemplified by pad 132 connected to interconnection 122 and antipad 142 by via 124. The vias may be, for example, plated through holes. Package pads 134 may also be provided. Depending on the patch antenna design, an optional reflector 144 can also be implemented on the same metal layer as the pads 130, 132, 134. In some instances, as discussed below, the reflector 144 is embedded.

To implement the flip-chip approach, the chip 162 preferably has a plurality of solder dots connected directly to the chip connection pads 116, 118, 120.

To enhance the patch antenna bandwidth, patches may be air suspended or supported with a foam material with a dielectric constant close to one at low frequency applications. However, at mmWave frequencies, especially for package applications, air suspended or foam supported patches are not realistic. Thus, in one or more embodiments of the invention, an air cavity 150 can be implemented in the packages. To avoid issues from hot gases during the PCB manufacturing process, vent hole(s) 152 can be employed. These holes can be designed such that they have little effect on the antenna performance. For example, hole 152 can be located near the middle of the cavity 150 or close to the

edge of the cavity 150, and can be made relatively small, consistent with adequate venting. The vent holes can be on the top (outermost part of) the cavity 150 as shown in FIG. 1 or on the side of the cavity as discussed below, depending on the manufacturing process used.

The ground plane 110 is also used for making ground connections through vias (e.g., via 140) and signal, power, and control connections through vias and antipads (e.g., via 124 with antipad 142, illustrative of a via with antipad that could be used for signal, power, or control functionality). Antipads are beneficial from a manufacturing standpoint, and result in increased reliability, as it is difficult to achieve reliability in partial vias (i.e., vias such as via 124 that do not extend completely through a structure) without use of antipads.

An open chip-receiving cavity or socket 160 is realized in the substrate 128 and bound film 126. This socket is used to hold the RF chip 162. The chip is attached to the package through flip-chip bonding.

Note that all the mmWave components (antennas, power amplifiers, low noise amplifiers, and the like) are in the package 100. Vias 124, 140 are used to pass through DC or much lower frequency signals.

The package 100 may advantageously be attached to the mother board (not shown) through a ball grid array (BGA).

FIG. 2 shows an embodiment substantially similar to embodiment 100 except that reflector 144 is encapsulated by an additional bound layer 170 inward of reflector 144 and an additional substrate 172 inward of bound layer 170. Similar items have received the same reference number and will not be described again. Chip receiving socket 160 is also formed in substrate 172 and bound layer 170 in this embodiment.

FIG. 3 shows an embodiment substantially similar to embodiment 200 except that vent 352 runs sideways through layer 108 so as to vent cavity 150. Similar items have received the same reference number and will not be described again.

FIG. 4 presents a bottom view 400 where chip 162 is encapsulated with encapsulant 402. The chip can be partially or completely encapsulated, for example, for purposes of resisting humidity. A plurality of outer pads 404 may correspond, for example, to attachment, heat conduction, or ground pads such as pad 130, while a

plurality of inner pads 406 may correspond, for example, to signal, control, or power pads such as pad 132. In FIG. 4, there is no reflector or the reflector is embedded. FIG. 5 shows a view 500 similar to view 400 but of a package with a reflector 144, such as in FIG. 1. Similar items have received the same reference number and will not be described again.

FIG. 6 shows an exemplary package 600 with a 2x2 planar phased array layout. It is possible to have more than two antennas on each row. This basic 2x2 array can be used to form much larger arrays. In addition to first antenna patch 104 with first feed line 114, also included are second, third and fourth antenna patches 602, 604, 606 with corresponding second, third and fourth feed lines 608, 610, 612. Each feed line is connected to chip 162 as described above. Although, for purposes of illustrative convenience, the feed lines are shown ending at the patches in FIG. 6, it will be appreciated that they may overlap same when viewed in top or bottom plan views, and are spaced from the corresponding patch and coupling aperture when viewed in cross-section as shown in FIGS. 1-3.

It will thus be appreciated that aspects of the invention include a package with a socket for an RF chip, and a planar antenna. In one or more instances, the RF chip is flip-chip attached to the package. Internal cavities can be used to improve the patch bandwidth. Venting holes can be used to remove the hot gases during the PCB manufacturing process. The package can be attached to the mother PCB through a BGA. The package can implement a planar phased array.

In view of the discussion of FIGS. 1-6, it will be appreciated that, in general terms, an aperture-coupled patch antenna package, according to an aspect of the invention, can include at least one generally planar patch, such as patch 104. Also included is at least one generally planar ground plane, such as plane 110, spaced inwardly from the generally planar patch 104 and substantially parallel thereto. The ground plane is formed with at least one coupling aperture slot, such as slot 113, therein. The slot 113 is substantially opposed to the patch 104. At least one feed line, such as line 114, is spaced inwardly from the ground plane 110 and is substantially parallel thereto. At least one radio frequency chip, such as chip 162, is spaced inwardly from the feed line 114 and is coupled to the feed line 114 and the ground plane 110. Also included is a first

substrate layer, such as that formed by bound film 126 and substrate 128, spaced inwardly from the feed line 114. The first substrate layer is formed with a chip-receiving cavity, such as cavity 160. The chip 162 is located in the chip-receiving cavity 160.

Given the description herein, a person skilled in the PCB and antenna arts can make embodiments of the invention. Non-limiting examples of materials that may be used include thermoset plastic/ceramic/woven glass or similar laminates such as the Rogers RO4000® series of materials (and other compatible materials) available from Rogers Corporation of Rogers, Connecticut USA, as well as copper for metal layers, possibly gold-plated on pads or other exposed areas.

It will be appreciated that advantageously, embodiments of the invention, such as 100, 200, and 300, provide a complete package and not a mere patch antenna separate from the chip and other packaging.

Note that vias such as 124, 140 may be formed, for example, using plated through holes.

Embodiments of the invention may also include a second substrate layer, such as that formed by substrate 108 and bound films 106, 109, interposed in a region between the ground plane 110 and a plane defined by the patch 104. The patch 104 may be advantageously formed in a first metal layer and the ground plane 110 may be advantageously formed in a second metal layer.

In one or more embodiments, a third substrate layer, such as that formed by substrate 112, is interposed in a region between the ground plane 110 and the feed line 114. The feed line 114 may be advantageously formed in a third metal layer. Further, one or more packages in accordance with embodiments of the invention may include at least one via, such as via 190, formed in the third substrate layer 112 and coupled to the ground plane 110. A plurality of chip connection pads, such as pads 116, 118, 120, can be formed in the third metal layer. At least one of the chip connection pads, such as 118, can be coupled to the at least one via 190 in the third substrate layer. The chip connection pads couple the chip to the feed line 114 (pad 120), the via 190 (pad 118) and the via 124 (pad 116).

One or more embodiments of the invention may include one or more signals pads, one or more control pads, and one or more power supply pads, all of which are

exemplified by pad 132, as well as one or more ground pads, such as 130. The signal, control, power supply and ground pads are advantageously formed in a fourth metal layer. As noted, package pads 134 can optionally be provided.

Also included in one or more embodiments is at least one ground via, such as 140, coupling the ground plane 110 and the ground pad 130. The at least one ground via 140 passes through the first and third substrate layers (e.g., substrate 112, bound film 126, and substrate 128), in a region not intersecting the feed line 114. One or more embodiments include at least one each of power, signal, and control antipads, such as antipad 142, formed substantially coplanar with the ground plane 110. At least one signal via couples the signal antipad and the signal pad, and passes through the first and third substrate layers. Similarly, at least one power via couples the power antipad and the power pad, and passes through the first and third substrate layers. Furthermore, at least one control via couples the control antipad and the control pad, and passes through the first and third substrate layers. As noted, pad 132, via 124, and antipad 142 are illustrative of pad, via, and antipad elements that may be provided for power, signal, and control functionality.

As also noted, in some instances, a reflector, such as 144, is spaced inwardly from the third substrate layer and is generally opposed to the coupling aperture slot 113. The reflector can be located on an inner surface of the first substrate layer (e.g., inmost surface of substrate 128). The reflector can be exposed, as in FIG. 1, or embedded, as in FIGS. 2 and 3, in which case the package can include a fourth substrate layer, such as that formed by bound film 170 and substrate 172, spaced inwardly from the reflector 144. The reflector can thus be embedded between the first and fourth substrate layers.

Advantageously, the second substrate layer, such as that formed by films 106, 109 and substrate 108, is formed with an air cavity, such as cavity 150, therein. Air cavity 150 is located between the patch 104 and the coupling aperture slot 113 in the ground plane 110. Preferably, the air cavity is formed in communication with a vent, such as vent 152 or 352. In the latter case, as in FIG. 3, the vent 352 is formed in the first substrate layer; in particular, in substrate 108. In the former case, vent 152 is formed in an additional substrate layer, such as that formed by substrate 102, spaced outwardly from the patch 104. The patch is formed on the additional substrate layer 102, and the vent is formed in the additional substrate layer 102.

As noted with regard to FIG. 6, in one or more embodiments of the invention, one or more planar phased arrays are implemented. Thus, in general terms, the above-discussed patch 104 may be designated as a first patch, and the above-discussed feed line 114 is a first feed line. The ground plane can be formed with one or more additional coupling aperture slots, like slot 113. The package can include one or more additional generally planar patches, such as patches 602, 604, 606, spaced outwardly from the ground plane. The additional slots can be substantially opposed to the additional patches. The package can also include one or more additional feed lines, such as lines 608, 610, 614, spaced inwardly from the ground plane and substantially parallel thereto. The at least one radio frequency chip 162 is coupled to the additional feed line(s) and the first patch and additional patch(es) are arranged to form a planar phased array. A single large ground plane with multiple slots can be employed in phased array embodiments. A phased array can include any number of patches greater than or equal to two; however, powers of two are advantageous, e.g., 2, 4, 8, 16, 32, and so on.

It will be appreciated and should be understood that the exemplary embodiments of the invention described above can be implemented in a number of different fashions. Given the teachings of the invention provided herein, one of ordinary skill in the related art will be able to contemplate other implementations of the invention.

Although illustrative embodiments of the present invention have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be made by one skilled in the art without departing from the scope of spirit of the invention.

Claims

What is claimed is:

1. A radio-frequency integrated circuit chip package with at least one integrated aperture-coupled patch antenna, said package comprising:

at least one generally planar patch;

at least one generally planar ground plane spaced inwardly from said generally planar patch and substantially parallel thereto, said ground plane being formed with at least one coupling aperture slot therein, said slot being substantially opposed to said patch;

at least one feed line spaced inwardly from said ground plane and substantially parallel thereto;

at least one radio frequency chip spaced inwardly from said feed line and coupled to said feed line and said ground plane; and

a first substrate layer spaced inwardly from said feed line, said first substrate layer being formed with a chip-receiving cavity, said chip being located in said chip-receiving cavity.

2. The package of Claim 1, further comprising a second substrate layer interposed in a region between said ground plane and a plane defined by said patch, wherein said patch is formed in a first metal layer and said ground plane is formed in a second metal layer.

3. The package of Claim 2, further comprising a third substrate layer interposed in a region between said ground plane and said feed line, wherein said feed line is formed in a third metal layer.

4. The package of Claim 3, further comprising:

at least one via formed in said third substrate layer and coupled to said ground plane; and

a plurality of chip connection pads formed in said third metal layer, at least one of said chip connection pads being coupled to said at least one via in said third substrate

layer, said chip connection pads coupling said chip to said feed line and said at least one via in said third substrate layer.

5. The package of Claim 4, further comprising:

at least one signal pad;

at least one control pad;

at least one power supply pad; and

at least one ground pad;

wherein said signal, control, power supply and ground pads are formed in a fourth metal layer.

6. The package of Claim 5, further comprising:

at least one ground via coupling said ground plane and said ground pad, said at least one ground via passing through said first and third substrate layers, in a region not intersecting said feed line;

at least power, signal, and control antipads formed substantially coplanar with said ground plane;

at least one signal via coupling said signal antipad and said signal pad, said at least one signal via passing through said first and third substrate layers;

at least one power via coupling said power antipad and said power pad, said at least one power via passing through said first and third substrate layers; and

at least one control via coupling said control antipad and said control pad, said at least one control via passing through said first and third substrate layers.

7. The package of Claim 3, further comprising a reflector spaced inwardly from said third substrate layer and generally opposed to said coupling aperture slot.

8. The package of Claim 7, wherein said reflector is located on an inner surface of said first substrate layer.

9. The package of Claim 8, further comprising a fourth substrate layer spaced inwardly from said reflector, said reflector being embedded between said first and fourth substrate layers.

10. The package of Claim 7, wherein said second substrate layer is formed with an air cavity therein, said air cavity being located between said patch and said coupling aperture slot in said ground plane.

11. The package of Claim 10, wherein said air cavity is formed in communication with a vent.

12 The package of Claim 11, wherein said vent is formed in said first substrate layer.

13. The package of Claim 11, further comprising an additional substrate layer spaced outwardly from said patch, said patch being formed on said additional substrate layer, said vent being formed in said additional substrate layer.

14. The package of Claim 3, wherein said second substrate layer is formed with an air cavity therein, said air cavity being located between said patch and said coupling aperture slot in said ground plane.

15. The package of Claim 1, wherein:

said at least one patch is a first patch;

said at least one feed line is a first feed line; and

said ground plane is formed with at least a second coupling aperture slot;

said package further comprising:

at least a second generally planar patch spaced outwardly from said ground plane, said second slot being substantially opposed to said second patch; and

at least a second feed line spaced inwardly from said ground plane and substantially parallel thereto;

wherein said at least one radio frequency chip is coupled to said second feed line and wherein said first and second patches are arranged to form a planar phased array.

FIG. 1

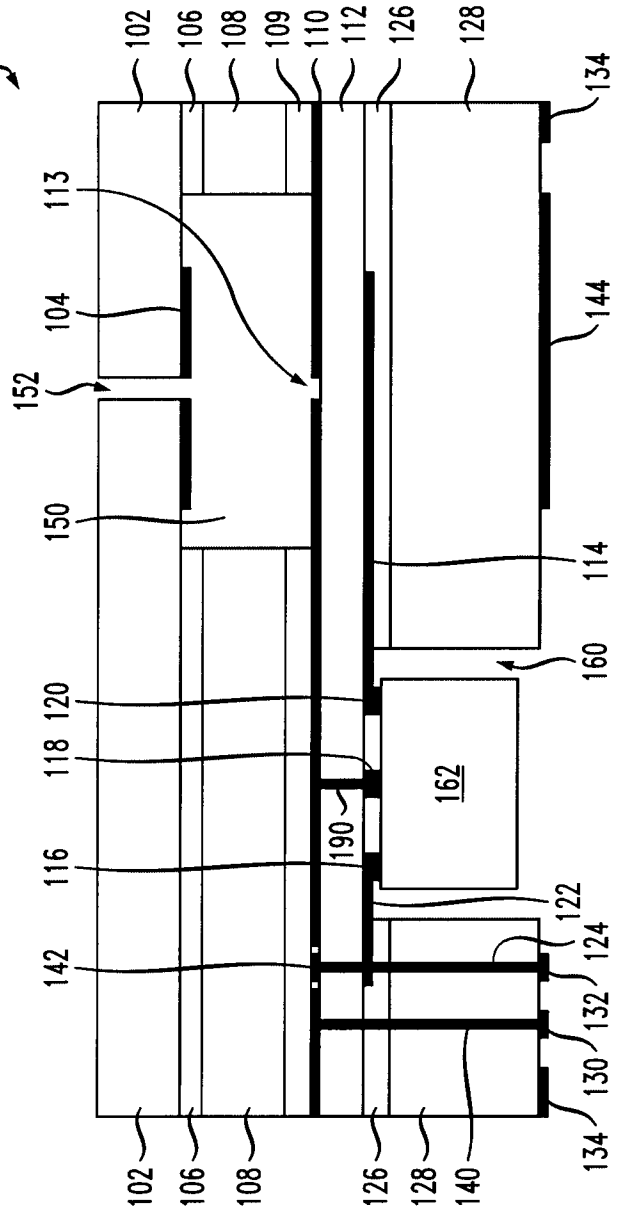

100
102
106
108
109
110
112
126
128
134
113
104
144
152
150
114
160
120
118
162
190
116
122
142
124
132
130
134
102
106
108
126
128
140

FIG. 2

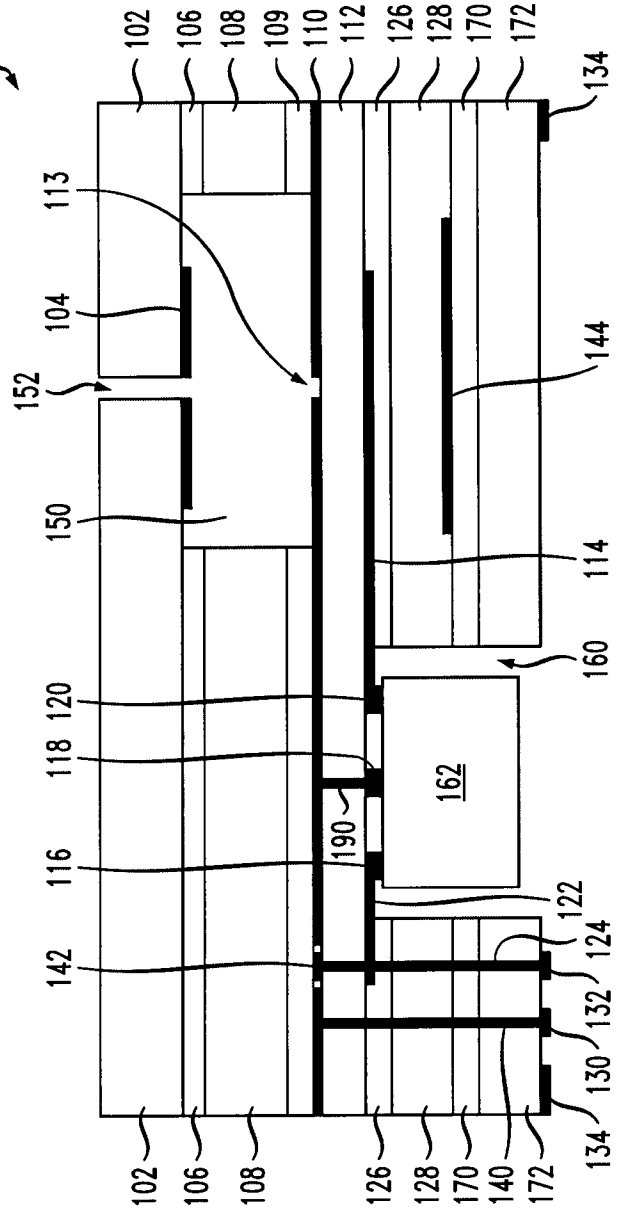
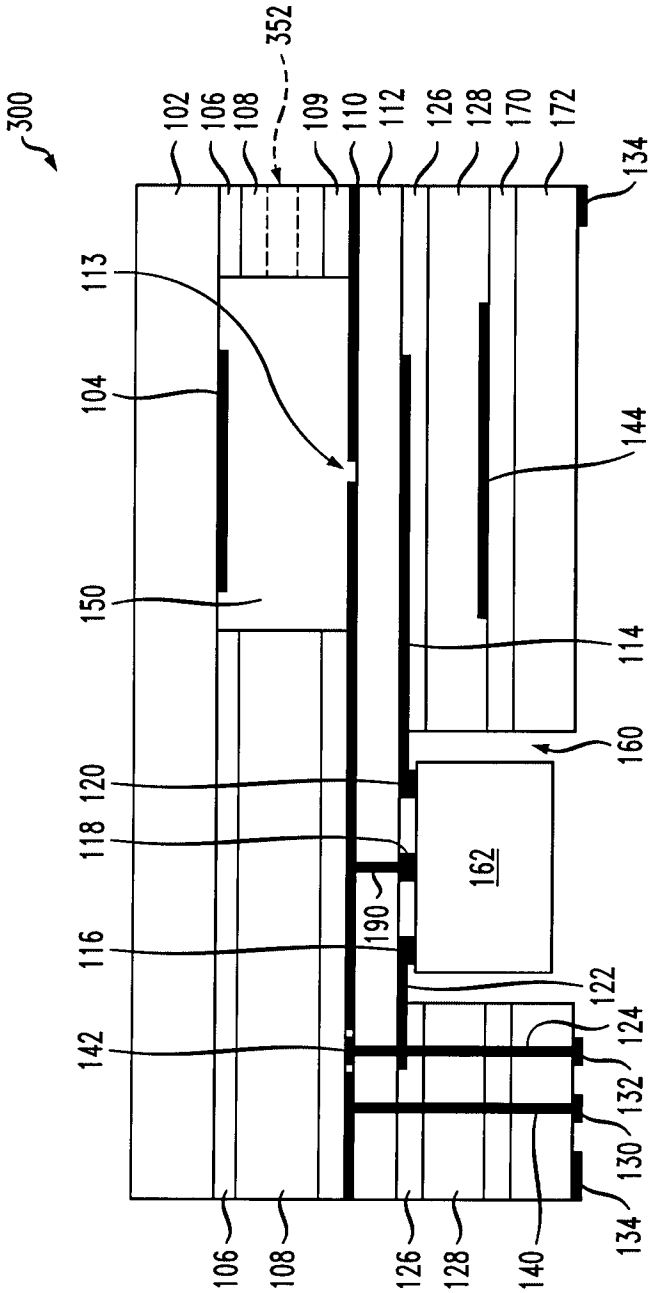

200
102
106
108
109
110
112
126
128
170
172
134
113
104
152
144
150
114
160
120
118
162
190
116
122
142
124
132
130
134
102
106
108
126
128
170
140
172

FIG. 3


300
352
102
106
108
109
110
112
126
128
170
172
134
113
104
144
150
114
160
120
118
162
190
116
122
124
142
132
130
134
106
108
126
128
140

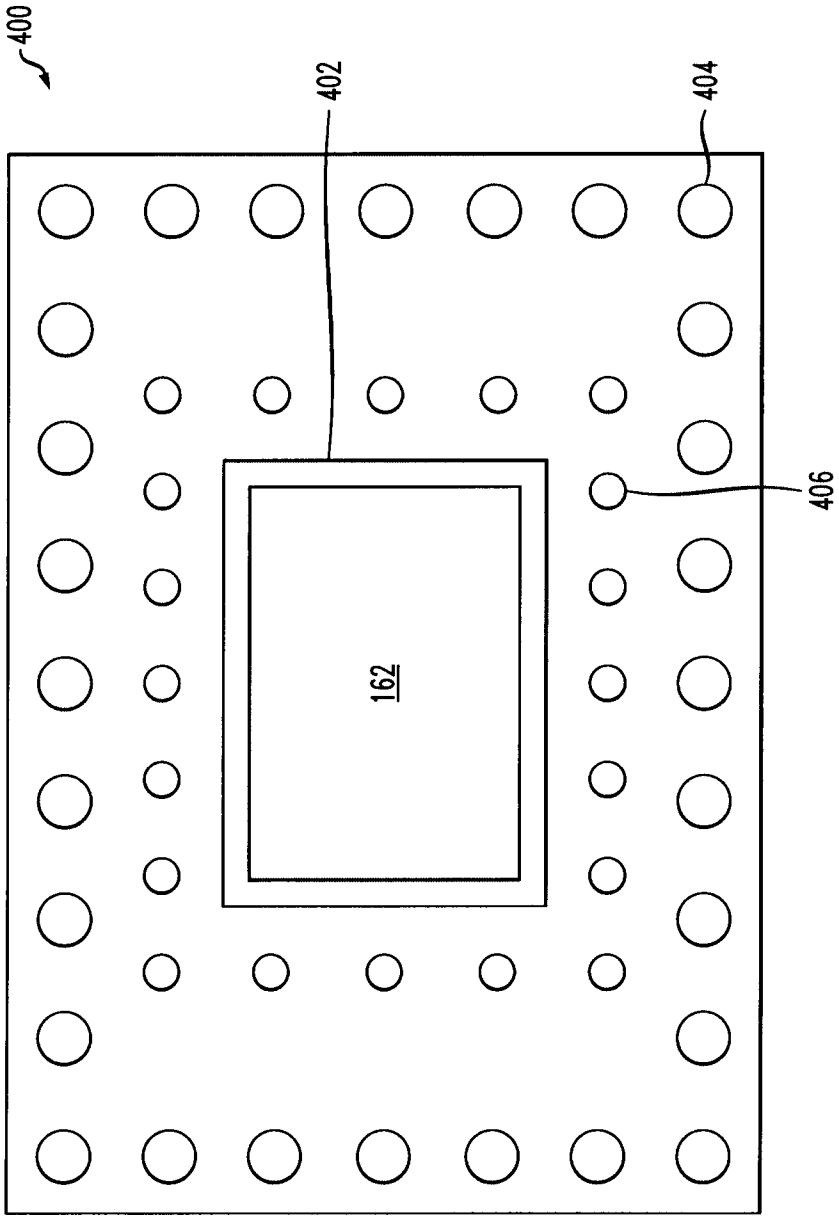


FIG. 4

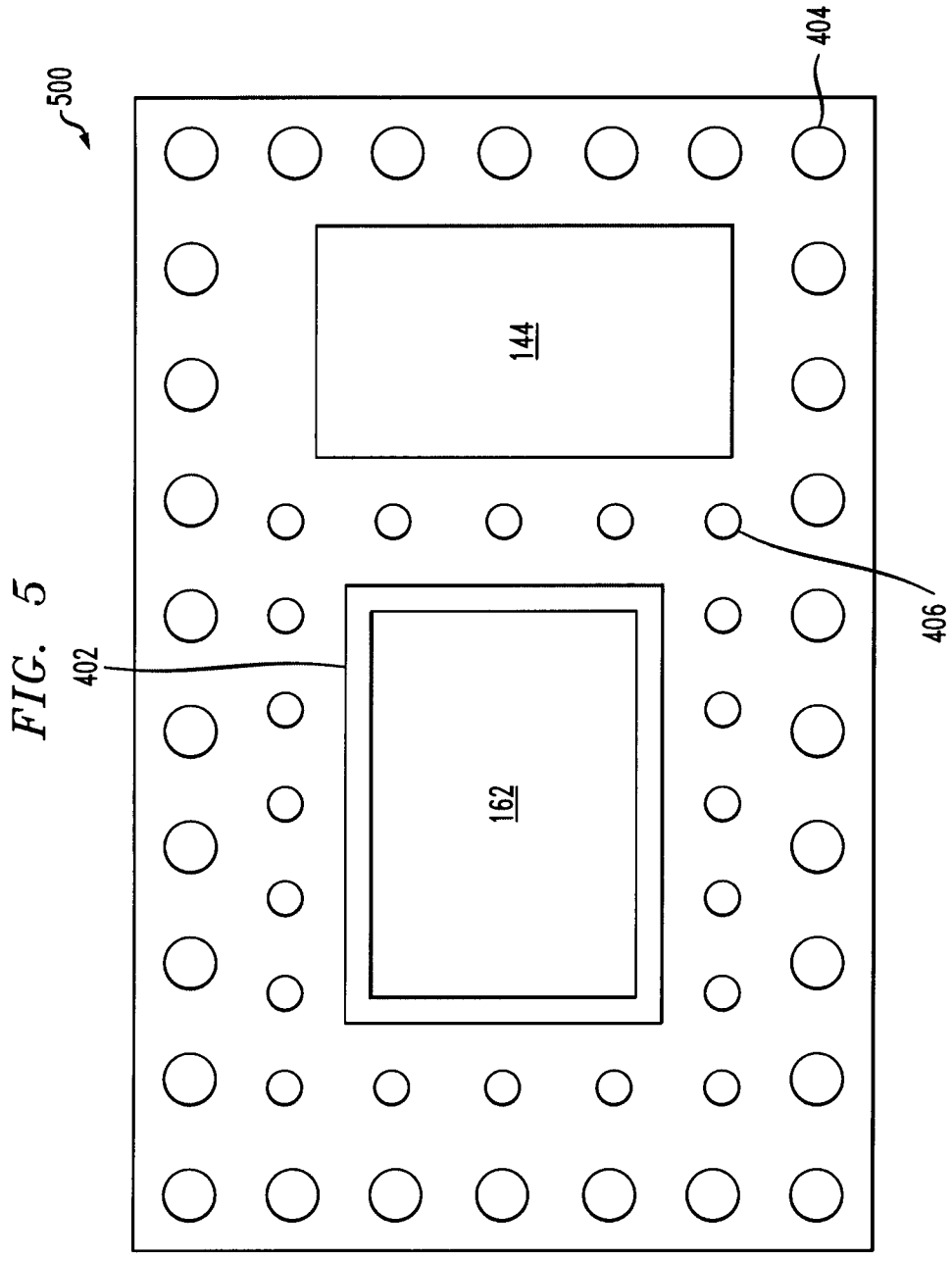
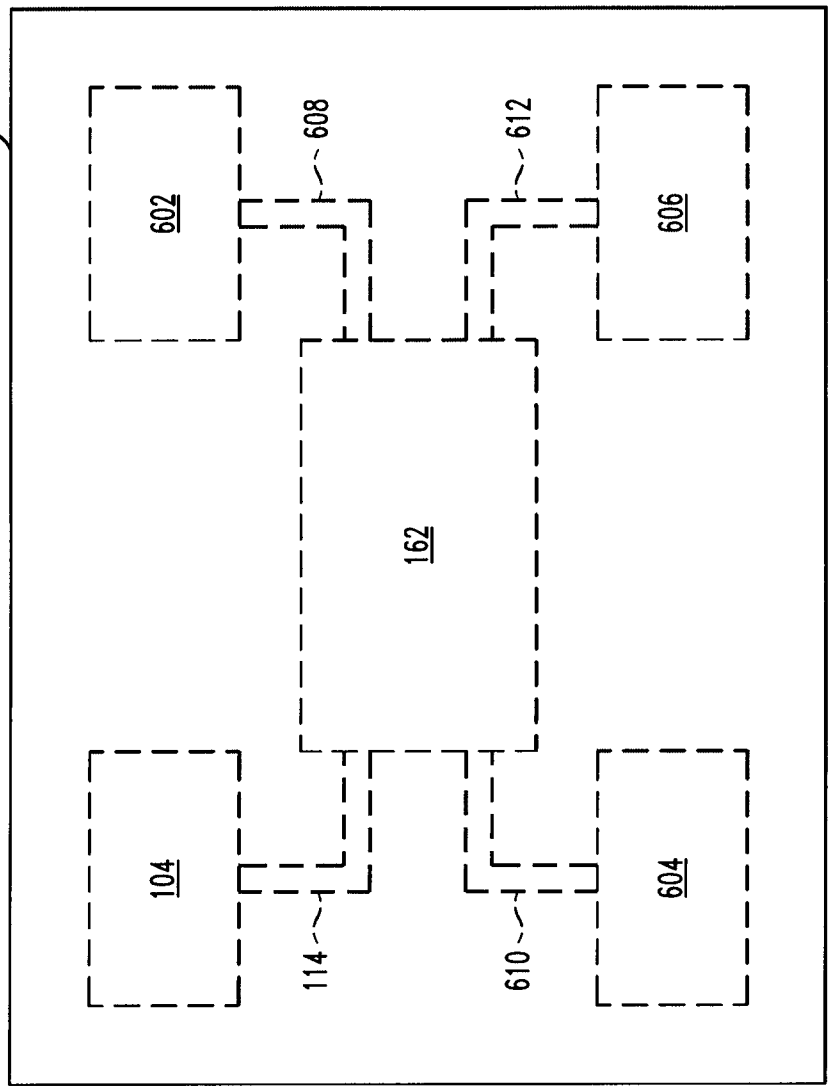


FIG. 5

FIG. 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/88516

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01Q 1/38 (2009.01)
USPC - 343/700MS
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 343/700MS

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC - 343/700, 789; 438/64; 327/524

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Dialog Classic (Chinese Pat Abstr; Derwent Index, EPFT, French Pat, Jap Abstr, USPFT, WIPO/PCT PFT); Google Scholar; Terms searched: ANTIPAD, CHIP, CONTROL, CONTROLLER, FEED LINE, FEED LINE, FREQUENCY, GROUND, PAD, PATCH, PLANAR, PLANE, POWER, RADIO, REFLECTOR, SIGNAL, VIA, WIRELESS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007/0126641 A1 (Saily) 07 June 2007 (07.06.2007); entire document, especially: fig. 5, reference numbers 502, 504, 506, 508, 514; para [0004]-[0005], [0008], [0032], [0046], [0051], [0055]-[0056]	1-15
Y	US 2006/0094155 A1 (Leibenguth et al.) 04 May 2006 (04.05.2006); entire document, especially: para [0005], [0007], [0027], [0034], [0038] and [0040]	1-15
Y	US 2006/0193093 A1 (Bertin et al.) 31 August 2006 (31.08.2006); entire document, especially: para [0042], [0126] and [0128]	5-6
A	US 7,030,706 B2 (Yao) 18 April 2006 (18.04.2006; entire document	1-15

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 February 2009 (05.02.2009)	19 FEB 2009
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774