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(54) **Title:** MEMORY DEVICE WITH ANALOG MEASUREMENT MODE FEATURES

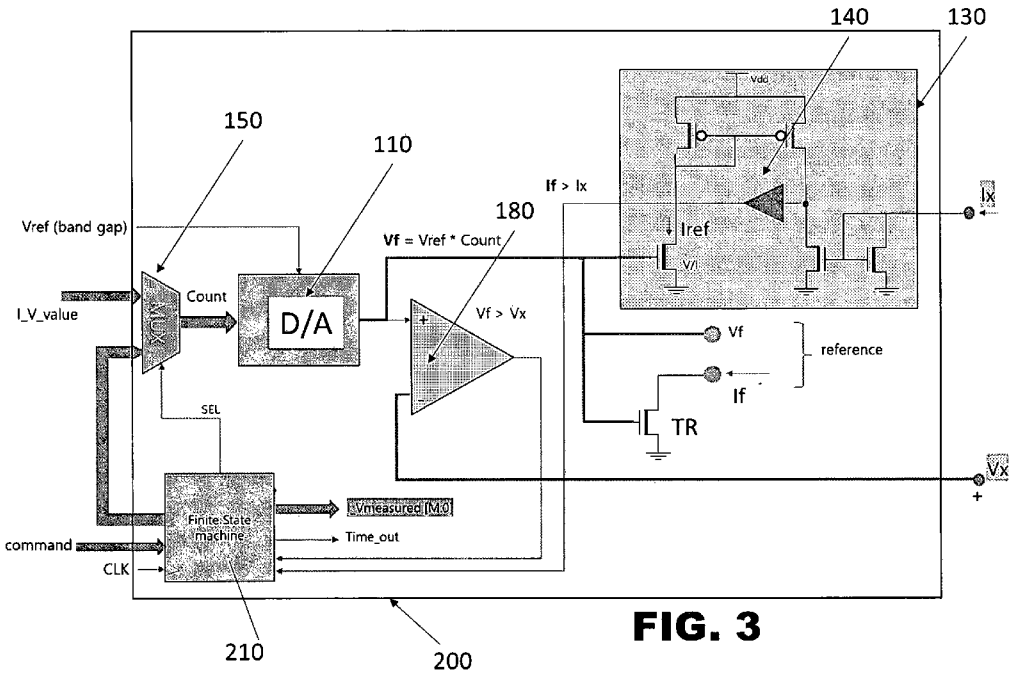


FIG. 3

(57) **Abstract:** The present disclosure relates to apparatuses and methods for memory management and more particularly to a memory device structured with internal analogic measurement mode features. The memory is provided with means for detecting a correct generation of voltage and/or current reference values in the memory device including at least a memory array and a memory controller. The method provides for a JTAG interface in the memory controller and an analogic measurement block in said memory device driven by said JTAG interface.

[Continued on next page]

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MEMORY DEVICE WITH ANALOG MEASUREMENT MODE FEATURES

DESCRIPTION

TECHNICAL FIELD

[001] The present disclosure relates in general to apparatuses and methods for memory management and more particularly to a memory device structured with internal analogic measurement mode features. The memory device is a non-volatile memory component that is coupled to a host device or to a System-on-Chip.

[002] BACKGROUND

[003] Non-volatile Flash memories are today one of the fundamental building blocks in modern electronic systems, including the SoC devices for automotive applications, in particular for Real Time Operating Systems (RTOS). Their performance in terms of speed, consumption, alterability, nonvolatility and the increasing importance of system reconfigurability have pushed up to now for flash memory integration in System-on-Chip (SoC) devices.

[004] However, with the current technologies the embedded memory portion is becoming the largest circuit portion in a SoC and it is not appropriate to increase their size to more than 128Mbit since it is very difficult to manage the whole embedded memory structure when the lithography node is below 28nm.

[005] In many applications it would be highly desirable to enlarge the size of the memory portion but it would be necessary to provide a new manner of coupling the SoC and the embedded or associated memory component. Moreover, it would be necessary to provide a more efficient manner to exchange signals and measured values between the memory portion and the controller of the SoC.

[006] In this respect a further need would be that of providing non-volatile memory devices including features for performing various measurements of the flash memory array. However, the measurement mode of a flash array can contain reserved operation that only the supplier of the component would like to use.

[007] A JTAG protocol teaches already how to implement hardware and algorithms to perform proper memory measuring. However, conventional JTAG is relatively slow for memory devices having a large size.

[008] Moreover, it would be highly desirable to provide internal analogic measurement mode features ensuring that only the right authority can access to specific measurement modes and/or to the update of the internal Flash array controller. The present disclosure is focused on the solution of the above-mentioned needs.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] – Figure 1 is a schematic view of a known digital low voltage detector for memory components realized according to a prior art solution;

[010] Figure 1A shows a first and a second diagram reporting a measurement of voltage value Vx affected by noise and more regular and stable value, respectively;

[011] Figure 2A shows a schematic view of a memory device associated to a host device or a System-on-Chip according to embodiments of the present disclosure;

[012] Figure 2B shows a schematic view of a hardware block incorporated into the memory device of the present disclosure to provide internal analogic measurement mode features;

[013] Figure 3 is a schematic view of a first embodiment of the hardware block of Figure 2B and according to the present disclosure;

[014] Figure 4 is a diagram showing a measurement of a voltage value Vx obtained with the block of Figure 3;

[015] Figure 5 is a schematic view of an alternative embodiment of the hardware block of Figure 2B according to the present disclosure;

[016] Figure 6 is a diagram showing a measurement of a current value Ix obtained with the block of Figure 5;

[017] Figure 7 shows a block diagram of a method according to the present disclosure.

DETAILED DESCRIPTION

[018] In the following detailed description, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration, specific embodiments. In the drawings, like numerals describe substantially similar components throughout the several views. Other embodiments may be disclosed and structural, logical, and electrical changes may be made without departing from the scope of the present disclosure. The following detailed description is, therefore, not to be taken in a limiting sense.

[019] Memory devices are frequently provided as internal, semiconductor, integrated circuits and/or external removable devices in computers or other electronic devices. There are many different types of memory, including volatile and non-volatile memory. Volatile memory, including random-access memory (RAM), static random access memory (SRAM), dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM), among others, may require a source of applied power to maintain its data. Non-volatile memory, by contrast, can retain its stored data even when not externally powered.

[020] Non-volatile memory is available in a wide variety of technologies, including flash memory (e.g., NAND and NOR), Read Only Memory (ROM), Electrically Erasable Programmable ROM (EEPROM), Erasable Programmable ROM (EPROM), and resistance variable memory such as phase change random access memory (PCRAM), self-selecting chalcogenide-based memories, resistive random access memory (RRAM), 3D XPoint memory (3DXP) and magneto-resistive random access memory (MRAM), among others.

[021] Memory devices can include large arrays of memory cells for storing data, frequently organized into rows and columns. Individual memory cells and/or ranges of memory cells can be addressed by their row and column. When a memory array is addressed, there may be one or more layers of address

translation, to e.g., translate between a logical address utilized by a host device and a physical address corresponding to a location in the memory array.

[022] For the regular operation of the memory array it is necessary to provide to the memory measured voltage and current values for managing the reading, writing and erasing phases of the memory cells. Moreover, it would be highly desirable to provide internal analogic measurement mode features ensuring that only the right authority can access to specific measurement modes and/or to the update of the internal Flash array controller.

[023] For a better understanding of the present disclosure, let's consider for instance a flash memory device coupled to a host device or associated to a SoC and including some circuit blocks shared with the SoC, for instance the read logic to implement the fetch/prefetch scheme and-or the branch prediction.

[024] Some of these circuit blocks need to receive signals reporting voltage and/or current values detected in the memory component for correctly driving the reading, programming or erasing phases of the memory array More specifically, these circuit blocks need to have the power supply and signals advising that the power supply is correct. For instance, the signal can be a result of a comparison between a BandGap reference voltage, with proper voltage scale, and the external supply. This signal information is driven to the memory internal controller to execute correctly the required operation following a firmware. Similar consideration may be done with respect to a reference current.

[025] The required voltage and/or current value are detected by specific circuit portions that operates as voltage or current detectors.

[026] A Flash memory device is very sensitive to the power supply when it programs and erases the memory array in particular for data retention issues and for the reliability. The Flash array must be a very high reliable device able also to inform the SoC that something wrong is happening with the power supply. This task is assigned to a controller of the flash array (not shown) that is incorporated into the memory component.

[027] Unfortunately, known standard voltage or current detectors are noise sensitive.

[028] The current/voltage under measurement cannot be stable during the measurement time frame. Therefore, the measurement could be not accurate.

[029] In some embodiments it is provided a voltage or current detector to be used in a memory component coupled to a host device or embedded/ associated to a System-on-Chip having a low sensitivity to a possible noise disturbing the measurement.

[030] In some cases the detector disclosed herewith provides just the value of the detected measurement protecting the manner in which the detector has obtained such a measurement, thus protecting the memory portion from possible hacker attack or reverse engineering in order to get some technological parameters.

[031] A further feature of the detector of the present disclosure is given by the capability of generating reference voltage or currents according to the operating needs of the memory portion wherein the detector has been incorporated.

[032] Figure 1 shows a schematic example of a prior art solution for detecting a low voltage value in a memory portion, for instance a memory portion embedded in a complex System-on-Chip.

[033] The detector shown in Figure 1 is based on a Schmitt trigger comparator 100 receiving on one input the output of a digital to analogic or analog (D/A) converter 110.

[034] This D/A converter 110 is coupled to a stable reference voltage potential Vrif generated for instance by an analogic bandgap generator with a proper configuration, i.e. a proper conversion factor, (not shown in the figures) and is driven by a digital input configuration signal Config.

[035] According to the value of the digital input configuration signal the D/A converter 110 provides a modulated output value.

[036] A sample and hold block 120 receives as input a voltage value Vx to be measured and applies its output to the other non-inverting input of the Schmitt trigger 110.

[037] The Schmitt trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier. It is an active circuit which converts an analog input signal to a digital output signal. The circuit is considered a trigger because the output retains its value until the input changes sufficiently to trigger a change. In the non-inverting configuration, when the input is higher than a chosen threshold, the output is high. When the input is below a different (lower) chosen threshold the output is low, and when the input is between the two levels the output retains its value.

[038] The output obtained from the Schmitt trigger is the voltage value Vx > Vrif * Config.

[039] This structure however is very sensitive to supply variations because of its intrinsic Schmidt trigger configuration.

[040] For example, Figure 1A shows a first diagram reporting the variations of the input voltage Vx because of the noise disturbing the measurement and a second diagram reporting a stable voltage value Vx that remains within a small range represented by a higher voltage value Vh and a lower voltage value Vl.

[041] It would be desirable to obtain a stable measurement of the voltage value Vx as shown by the second diagram and the detector of the present disclosure is structured to obtain such a result.

[042] Moreover, Flash array measuring needs some measurement modes that involves:

- reference current generation;
- reference voltage generation.

[043] According to embodiments of the present disclosure an internal analogic measurement mode structure is implemented in a single analogic block 200 managed using the JTAG interface.

[044] The analogic block 200 is substantially a hardware block incorporated into a circuit portion of a non-volatile memory device 1.

[045] The memory device 1 is shown in Figure 2A and includes an array 6 of Flash memory cells and a circuitry located around the memory array. The memory array 6 includes a non-volatile memory portion, NAND Flash or NOR Flash.

[046] Such a memory device 1 is an independent structure but it is a component strictly associated to a host device 10 or to a System-on-Chip. More particularly, the memory device 1 is associated and linked to the SoC structure 10 partially overlapping such a structure while the corresponding semiconductor area of the SoC structure has been used for other logic circuits. The coupling between the SoC structure and the memory component is obtained by interconnecting a plurality of respective pads or pin terminals that are faced one toward the other (not shown).

[047] The pads of the memory component have been realized on a surface of the memory component, in practice on the top of the array. More specifically, the pads are arranged over the array so that, when the memory component 1 is reversed or flipped, its pads are faced to corresponding pads of the host or SoC structure in a circuit layout that keeps the alignment of the pads with a technology similar to Flip-Chip. Other coupling techniques may be used.

[048] The Flash memory component 1 includes at least: an I/O circuit 5, a micro-sequencer 3, an array of memory cells 6, voltage and current reference generators 7, charge pumps 2 and decoding circuitry 8, sense amplifiers 9 and corresponding latches, a command user interface, for instance a CUI block 4; some of all of the circuitry may be located at the array periphery or under the array, depending on the manufacturing technology.

[049] The micro-sequencer 3 is substantially a memory controller that is coupled to the memory array 6. Such a controller can be a microcontroller, special purpose

logic circuitry such as a Filed programmable Gate Array (FPGA) or an Application Specific Integrated Circuit (ASIC) or other suitable processor.

[050] The memory component 1 also comprises a JTAG logic, for instance a JTAG interface adopted for the measurement and/or the test of the memory component 1 and allowing the re-use of measurement tooling.

[051] Figure 2B shows a schematic view of a hardware block incorporated into the memory device of the present disclosure to provide internal analogic measurement mode features. In one embodiment of the present disclosure the analogic block 200 is managed by using the JTAG interface.

[052] More particularly, the control signals are T_Reg bits contained in a special instruction register of the JTAG interface.

[053] According to the IEEE1149 and IEEE1532 standards a JTAG interface of the memory component 1 may be completed by additional registers that may be used as shift data registers for allowing the interaction with the core of the host device 10 for instance in the writing and/or reading phases of the memory component.

[054] However, depending on the command loaded in the IR, different registers can be combined. In this respect, the present disclosure suggests adopting a special register T_Reg including instructions to perform the analogic measurement of the analogic components of the memory device 1.

[055] Furthermore, according to an embodiment of the present disclosure, micro sequencer or controller 3 comprises an interface with a plurality of measurement or test registers (in the following globally indicated as T_reg), each register being associated with a specific address (known as T_reg_addr), for testing the functionality of the memory component to which the controller is associated, or generally for interfacing the memory component with a testing machine and/or an external core.

[056] The measurement mode architecture of the memory component is therefore based on these registers, which, under certain circumstances, can be written/read by the SoC controller via JTAG interface, by the test machine via JTAG interface, and by the flash array controller 3 via internal buses.

[057] The test registers T_reg contain the instructions (e.g. parameters such as currents/voltages) for the measurement and/or test of the memory component.

[058] In particular, test registers are organized in several banks each containing N registers (N=8, 16, etc..) and being associated with a specific address TL_addr. Each bank is also apt to drive one or more macro function (Analog or Digital).

[059] The measurement and/or test of the memory component is therefore managed by a protocol based on a JTAG interface using the instructions of the test registers T_reg. As previously observed, the measurement and/or test can be controlled by the SoC core or controller or by an external test machine. In any case, both the approaches are based on a Built-In Self-Test (BIST) executed by the internal flash array controller 3 of the present disclosure. This approach also maintains secret the internal algorithm with sensitive technological parameters (such as timing voltages and the like).

[060] Not all the test registers T_reg can be accessed by an external user, and a filtering block (not shown) in the controller 3 is configured to disable the access to some test registers T_reg based on a RUA signal generated by the processing unit. In other words, in some embodiments access to a subset of a plurality of test registers is limited.

[061] In this embodiment, the filtering block is configured in such a way that, when the RUA signal is generated by the processing unit; some reserved registers are not addressable by masking the specific address of such register, and the output of said filtering block yields only the first allowed register T_reg.

[062] The test registers T_reg that are not addressable are written by the controller 3 in a configuration register.

[063] One embodiment of the present disclosure relates to a memory device with analog measurement mode features including:

- at least a memory component with a memory array;
- a memory controller coupled to the memory component;
- a JTAG interface in said memory controller;
- voltage and current reference generators;
- an analogic measurement mode block driven by said JTAG interface.

[064] The memory device of the present disclosure further comprises a plurality of test registers in said JTAG interface, each register being associated with a specific address for testing the functionality of the memory component to which the controller is associated.

[065] The analogic measurement mode block 200 shown in Figure 2B includes also the voltage and current reference generators of the memory device.

[066] This block 200 receives as inputs a fixed reference voltage value, for instance a Vref (band gap). A further input is represented by the I_V_Value that indicates the value of the current If or voltage Vf to be generated.

[067] The schematic arrow indicating plural command signals represent a series of instructions received by the block 200 for providing various measurements, for instance: Measure Vx, Measure Ix, or for generating voltage or current values, for instance: Generate Vf, Generate If, or for other instructions.

[068] The values Vx or Ix are analogic voltage and current values to be measured, while Vf and If are programmable reference values.

[069] A clock input CLK serves as a clock an internal FSM disclosed later.

[070] It must be noted that command, IV_Values are coming from the T_reg register (not shown) and the control signals are T_Reg bits.

[071] Giving now a closer look to the internal structure of the analogic block 200 we can make reference to the example of Figure 3 wherein the block 200 embraces a certain number of circuit elements disclosed hereinafter.

[072] Figure 3 is a schematic view of a first embodiment of the hardware block of Figure 2B and according to the present disclosure. In this Figure the depicted current-to-voltage converter is not used during voltage measurement or generation.

[073] The block 200 includes a low voltage detector comprising:

- a comparator 180 receiving on a voltage input a voltage value to be detected;
- a digital to analog converter 110 coupled to a reference voltage potential and having an output connected to other input of said comparator;
- a Finite State Machine 210 receiving the output of said comparator and producing digital outputs for the inputs of said memory controller.

[074] The D/A converter 110 is coupled to a stable reference voltage potential Vref generated for instance by an analogic bandgap generator and receives a digital input signal Count.

[075] The reference voltage Vref (band gap) is to be considered as an external voltage value. A normal value for a bandgap reference could be about 1.2 Volt even if this value is just indicative. A different stable voltage generator may be used to provide Vref.

[076] The output of the D/A converter 110 is an analogic value Vf = Vref * Count and is applied to the non-inverting input (+) of the comparator 180.

[077] The comparator 180 has a second inverting (-) input receiving the voltage value Vx to be measured. The example reported herewith should be considered as a schematic indication that the inverting input of the comparator 180 is connected to a node point or to a terminal of the memory portion or component wherein a

voltage potential Vx is applied and such a potential must be measured with great precision obtaining a value not affected by noise.

[078] This basic structure of the comparator 180 and converter 110 has been further improved by the association of a Finite State Machine (FSM) 210.

[079] The Finite State Machine 210 is a complex logic portion capable to execute algorithms. In the subsequent part of the present disclosure we will provide an example of an algorithm executed by the Finite State Machine 210.

[080] This Finite State Machine 210 operates according to a clock signal CLK of the memory component and received on one input. The FSM receives also as a further input a Command signal issued by the internal memory controller to execute properly the operation that the internal firmware can require depending on the access phase to the memory array. As an alternative, the command signal may arrive from a host device coupled to the memory component or issued by a controller of the System-on-Chip hosting the embedded memory component

[081] A multiplexer 150 is provided between the Finite State Machine 210 and the digital input of the D/A converter 110. A selection signal SEL is produced by the Finite State Machine 210 to drive the multiplexer 150 and select the proper path for the input signal to the output of the multiplexer.

[082] The output of the multiplexer 150 is a Count digital input for the D/A converter 110.

[083] This multiplexer 150 receives as a first input a logic value corresponding to a voltage or a current measurement and on a second input the output of the Finite State Machine 210.

[084] The output value of the comparator 180 is applied as a feedback input to the Finite State Machine 210. This output value Vf is outputted when it is greater than a voltage value Vx to be measured.

[085] In other words, the output value Vf of the comparator 180 is triggered when the voltage value Vf is greater than the voltage value Vx to be measured. A current-

to-voltage converter 130 is depicted also in Figure 3, however it is not used during voltage detection and measurement nor during reference voltage generation. Converter 130 and its functionality will be described below with reference to current detection and measurement and reference current generation.

[086] Moreover, if the measurement is performed for a time interval of a certain duration it is possible to obtain an average value Vx that is less and less affected by possible noise.

[087] In this respect, the Finite State Machine 210 is settable with a programmable Time_out value that represents the max duration of the time interval for performing the measurement of the voltage value Vx.

[088] Just to give an example of a possible algorithm that the Finite State Machine 210 may execute to measure a voltage value Vx, we are reporting hereinafter a list of instructions and parameters that have been adopted for reaching the required measurement.

N = max measures attempt

Wait (**T0**) u-second (Vx is hopefully a stable value)

Step 1: N++;

The FSM looking for the **counter** value that provides **Vf>Vx**

Count_H ← **counter**

Count_L ← **counter - 1**

Set a Timer Δ**T** = **T1**
do {

// Is Vx stable? Is it out of ΔV?

if ((Vrif * Count_H) <Vx **||** (Vrif * Count_L) > Vx)

wait (**T2**) **go to** step 1

} **while ((elapsed time** < ΔT **) | | k>N)**

If (k<=N) I_Vmeasured [M:0] = [Vrif (Count_H)-Vrif (Count_L)]/2

Else Time_out ← 1

[089] It should be noted that the Finite State Machine 210 finds the value in a sequential manner or, as an alternative, in a dichotomic way or with any other method that can speed up the finding of the final value.

[090] As shown in the diagram of Figure 4, during the time interval ΔT the detected voltage value Vx remains substantially stable within an upper limit Vrif * Count_H and a lower limit Vrif * Count-L. The window delimited by the upper and lower voltage limits of the time interval ΔT is programmable by the user of the memory component.

[091] Moreover, the FSM 210 is always capable to detect the possible presence of noise since the detected voltage value Vx must remain within the upper and lower limits above reported and when the detected value is outside the expected range, like for instance in the portion of the diagram indicated by the number 190, the measurement is repeated automatically.

[092] Figure 4 is a diagram showing a measure of a voltage value Vx obtained with the block of Figure 3. As shown in the diagram of Figure 4, during the time interval ΔT the detected voltage value Ix remains substantially stable within an upper limit Vrif * Count_H and a lower limit Vrif * Count-L. The window delimited by the upper and lower voltage limits of the time interval ΔT is programmable by the user of the memory component.

[093] Moreover, the FSM is always capable to detect the possible presence of noise since the detected voltage value Vx must remain within the upper and lower limits above reported and when the detected value is outside the expected range, like for instance in the portion of the diagram indicated by the number 190, the measurement is repeated automatically.

[094] The numeric value N represents the maximum number of attempts that the detector should perform for obtaining the required measured value Vx. The other time T0, T1 and T2 are time parameters measured from a common origin

[095] The reported parameters N, T0, T1, T2 are all programmable in the sense that their value may be set according to the quality and reliability of the measurement to be performed. Even the time interval ΔT is a parameter that may be programmed.

[096] Just to give an indication of a value assignable to ΔT it may be set in few tens of milliseconds.

[097] Now, the detector of the present disclosure may be used for measuring also a current value, for instance a current value Ix.

[098] Figure 5 is a schematic view of an alternative embodiment of the hardware block of Figure 2B according to the present disclosure and more specifically for current measurements. Several elements in figure 5 are the same as those of figure 3 described above; however, some of them (such as voltage comparator 180) are not used during operation as current detection and measurement and reference current generation as better explained below. The basic portion of the detector disclosed herewith is structured in a similar fashion as the detector described with reference to Figure 3; however, instead of voltage comparator 180 a converter 130 from current to voltage is used.

[099] The structure of this converter 130 is based on a current mirror including a differential cell 140 comprising PMOS and NMOS transistors.

[0100] One input of the current mirror is the current value Ix to be measured. In this respect, we must intend that current input terminal of the converter 130 corresponds to a node point or to a terminal of the memory portion or component wherein a current value Ix is flowing and such a current value must be measured with great precision obtaining a value not affected by noise. In other words, the current to voltage converter has an input node on a first leg coupled

to a node of a circuit in the memory component, the circuit configured to drain the current Ix.

[0101] For completeness sake it should be noted that the differential cell 140 of the current mirror includes a first leg associated to the input current value Ix and a second leg associated to the output of the D/A converter 110.

[0102] More particularly, the output of the D/A converter 110 is applied to a gate of an NMOS transistor of the second current mirror leg draining a reference current If. The voltage value Vf at the output of the D/A converter is proportional to the reference voltage Vref (band gap) and is further applied to the gate terminal of a buffer transistor TR having conducting terminal linked between the reference current If node and a ground potential reference. Transistor TR further mirrors the current Iref in the second leg of the current-to-voltage converter 130, making it possibly available at its drain node.

[0103] The output of the voltage or current detector of the present disclosure is represented by a digital output of the FSM wherein a digital value I_Vmeasured [M:0] is presented to the outside world, for instance the SoC controller.

[0104] As previously disclosed with reference to the voltage detector, the Finite State Machine 210 receives as input an output value If outputted by the converter 130 and is capable to issue digital values for the input of the D/A converter 110.

[0105] Similarly, to the previous schematic example of Figure 3, the multiplexer 150 receives as input the signal output of the FSM 210 and as a further input a digital current/voltage value I_V_value.

[0106] Similarly, to the example of the voltage detector, it is proposed herewith an algorithm that the Finite State Machine 210 may execute to measure a current value Ix. The algorithm includes a list of instructions and parameters that have been adopted for reaching the required measurement.

N = max measures attempt

Wait (**T0**) u-second (Ix is hopefully a stable value)

Step 3: N++;

The FSM looking for the **counter** value that provides **If>Ix**

Count_H ← **counter**

Count_L ← **counter - 1**

Set a Timer Δ**T = T1**
do {

// Is Ix stable? Is it out of IV?

if ((Vrif * Count_H * **α**) <Ix **| |** (Vrif * Count_L * **α**) > Ix)

wait (**T2**) **go to** step 3

} **while ((elapsed time** < Δ**T) | | k>N)**

If (k<=N) I_Vmeasured [M:0] = **α** * [Vrif (Count_H)-Vrif (Count_L)]/2

Else Time_out ← 1

[0107] As previously disclosed, the numeric value N represents the maximum number of attempts that the detector should perform for obtaining the required measured value Ix. The other time T0, T1 and T2 are time parameters measured from a common origin.

[0108] The reported parameters N, T0, T1, T2 are all programmable in the sense that their value may be set according to the quality and reliability of the measure to be performed. Even the time interval ΔT is a parameter that may be programmed.

[0109] Figure 6 is a diagram showing a measurement of a current value Ix obtained with the block of Figure 5. As shown in the diagram of Figure 6, during the time interval ΔT the detected current value Ix remains substantially stable within an upper limit given for instance by Irif*Count_H* α = Vrif*Count_H and a lower limit given by Irif*Count_L* α = Vrif*Count_L. The figure reports a scale factor α (alpha) to allow the proper comparison; α is a conversion factor from voltage to current (e.g., such that Vrif*Count_L*α corresponds to Irif*Count_L and Vrif*Count_H*α corresponds to Irif*Count_H). The window delimited by the upper and lower current limits of the time interval ΔT is programmable by the user of the memory component.

[0110] Moreover, the FSM is always capable to detect the possible presence of noise since the detected current value Ix must remain within the upper and lower limits above reported and when the detected value is outside the expected range, like for instance in the portion of the diagram indicated by the number 290, the measurement is repeated automatically.

[0111] One embodiment of the present disclosure relates to a method to operate a memory device including at least a memory array and a memory controller, the method comprising:

- driving by the memory controller an analogic measurement block through a JTAG interface,
- generating voltage and/or current reference values based on the driving, and;
- detecting that the generated voltage and/or current is correct.

[0112] Figure 7 shows a block diagram of a method 700 according to the present disclosure.

[0113] According to method 700 a memory device including at least a memory array and a memory controller may be operated.

[0114] Method 700 comprises, at block 710 driving by the memory controller an analogic measurement block through a JTAG interface. The driving may be carried out according to the embodiments described above with reference to figures 1 to 6. For example, commands may be issued to Finite State Machine 210 by the JTAG interface in controller 3.

[0115] Method 700 comprises, at block 720, generating voltage and/or current reference values based on the driving. The generating voltage and/or current may be implemented by Current/Voltage generation and measurement block 200 described in Figure 2B and in more details 3 and 5, for example.

[0116] Method 700 further comprises, at block 730, detecting that the generated voltage and/or current is correct. Generated voltage or current detection may be implemented by the circuits described in figures 3 and 5, in some embodiments.

[0117] Method 700 may further comprise generating instructions by at least a test register of said JTAG interface for said analogic measurement block. In some embodiments, method 700 may also comprise limiting access to a subset of a plurality of test registers, as described above. In some embodiments, method 700 comprises applying to an input of a comparator a voltage value Vx to be detected and/or applying to an input of a current to voltage converter a current value Ix to be detected. Method 700 may also comprise feeding the comparator output and the current to voltage converter output to corresponding inputs of a Finite State Machine and applying digital outputs of said Finite State Machine to a digital to analog converter coupled to a reference voltage potential and having an output connected to another input of said comparator for detecting an average voltage value or an average current value in a time interval

[0118] One of the advantage of the method of the present disclosure is given by the presence of a on board mechanism for measuring voltage values V and current values I related to the flash array without exposing the cells terminal to any contact from an external component, for instance a host device or a SoC to whom the memory is associated. This feature has the great advantage to permit

to protect some technological secret not directly measurable from outside the memory component thus rendering the memory device more robust against attacks directed to detect process parameter hacking direct measurement on flash cells.

[0119] In the previous description numerous specific details are discussed to provide a thorough and enabling description for embodiments of the present technology.

[0120] However, one skilled in the relevant art will recognize that the disclosure can be practiced without one or more of the specific details. In other instances, well-known structures or operations often associated with memory devices are not shown, or are not described in detail, to avoid obscuring other aspects of the technology. For example, several functional components of memory devices and/or memory systems that are well-known to those skilled in the art are not discussed in detail below (e.g., circuit components such as multiplexers and decoders, data structures such as address registers and data registers, etc.).

[0121] In general, it should be understood that various other devices, systems, and methods in addition to those specific embodiments disclosed herein may be within the scope of the present technology.

CLAIMS

1. A memory device with analog measurement mode features including:

- at least a memory component with a memory array;
- a memory controller coupled to the memory component;
- a JTAG interface in said memory controller;
- voltage and current reference generators;
- an analogic measurement block driven by said JTAG interface.

2. The memory device of claim 1 comprising a plurality of test registers in said JTAG interface, each register being associated with a specific address for testing the functionality of the memory component to which the controller is associated.

3. The memory device of claim 1 wherein said JTAG interface includes at least a test register configured to generate instructions for said analogic measurement block.

4. The memory device of claim 1 wherein said voltage and current reference generators are incorporated into said analogic measurement block.

5. The memory device of claim 1 comprising a voltage detector including:

- a comparator configured to receive on a voltage input a voltage value Vx to be detected;
- a digital to analog converter coupled to a reference voltage potential and having an output connected to other input of said comparator;
- a Finite State Machine receiving the output of said comparator and configured to produce digital outputs for the inputs of said memory controller.

6. The memory device of claim 5 further comprising a multiplexer between the digital outputs of the Finite State Machine and the inputs of the digital to analog converter.

7. The memory device of claim 6 wherein said Finite State Machine is configured to issue a selection signal for enabling said multiplexer.

8. The memory device of claim 5 wherein the voltage input of the comparator is an inverting input of the comparator.

9. The memory device of claim 5 further comprising a current to voltage converter configured to receive as input a current value Ix to be detected and having an output connected to said Finite State Machine.

10. The memory device of claim 9 wherein said current to voltage converter includes a current mirror.

11. An apparatus including a host device coupled to a memory component with analog measurement mode features including:

- at least a memory array in said memory component;
- a memory controller coupled to the memory component;
- a JTAG interface in said memory controller;
- voltage and current reference generators;
- an analogic measurement block driven by said JTAG interface.

12. The apparatus of claim 11 comprising a plurality of test registers in said JTAG interface, each register being associated with a specific address for testing the functionality of the memory component to which the controller is associated.

13. The apparatus of claim 11 wherein said JTAG interface includes at least a test register configured to generate instructions for said analogic measurement block.

14. The apparatus of claim 11 wherein said voltage and current reference generators are incorporated into said analogic measurement block.

15. The apparatus of claim 11 wherein said analogic measurement block includes a current detector comprising:

- a current to voltage converter configured to receive as input a current value Ix to be detected and having an output connected to a Finite State Machine;
- a Finite State Machine configured to produce digital outputs for the inputs of said memory controller;
- a digital to analog converter coupled to a reference voltage potential and having an output connected to a transistor of the current to voltage converter.

16. The apparatus of claim 15 further comprising a multiplexer between the digital outputs of the Finite State Machine and the transistor of the current to voltage converter.

17. The apparatus of claim 16 wherein said Finite State Machine is configured to issue a selection signal for enabling said multiplexer.

18. The apparatus of claim 15 wherein the operation of said Finite State Machine is scheduled by a clock signal of the memory component.

19. The apparatus of claim 15 wherein the current to voltage converter has an input node on a first leg coupled to a node of a circuit in the memory component, the circuit in the memory component configured to drain the current Ix.

20. The apparatus of claim 15 further comprising a voltage comparator receiving as input a voltage Vx and having an output connected to said finite state machine.

21. A method to operate a memory device including at least a memory array and a memory controller, the method comprising:

- driving by the memory controller an analogic measurement block through a JTAG interface,

- generating voltage and/or current reference values based on the driving, and;

- detecting that the generated voltage and/or current is correct.

22. The method of claim 21 further comprising generating instructions by at least a test register of said JTAG interface for said analogic measurement block.

23. The method of claim 21 further comprising limiting access to a subset of a plurality of test registers.

24. The method of claim 21 comprising:

- applying to an input of a comparator a voltage value Vx to be detected;

- applying to an input of a current to voltage converter a current value Ix to be detected;

- feeding the comparator output and the current to voltage converter output to corresponding inputs of a Finite State Machine;

- applying digital outputs of said Finite State Machine to a digital to analog converter coupled to a reference voltage potential and having an output connected to another input of said comparator for detecting an average voltage value or an average current value in a time interval.

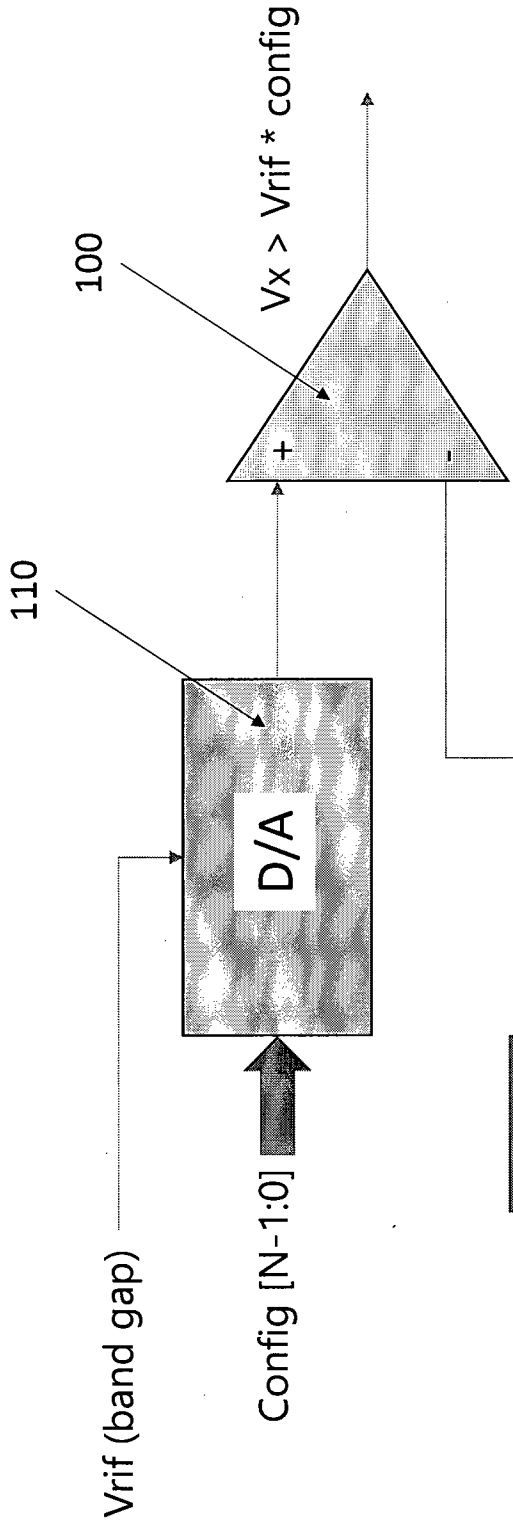


FIG. 1 – PRIOR ART

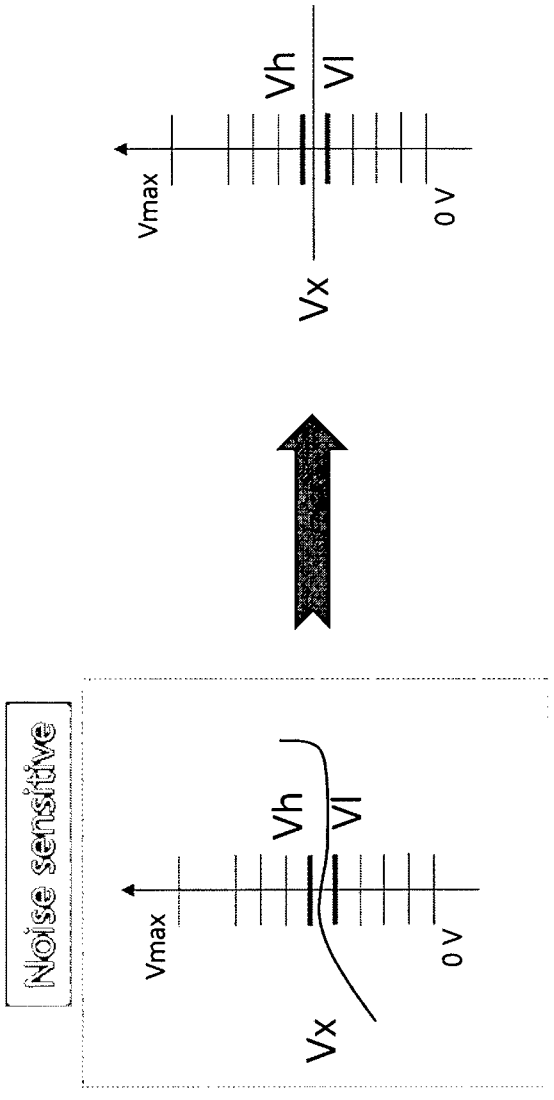


FIG. 1A

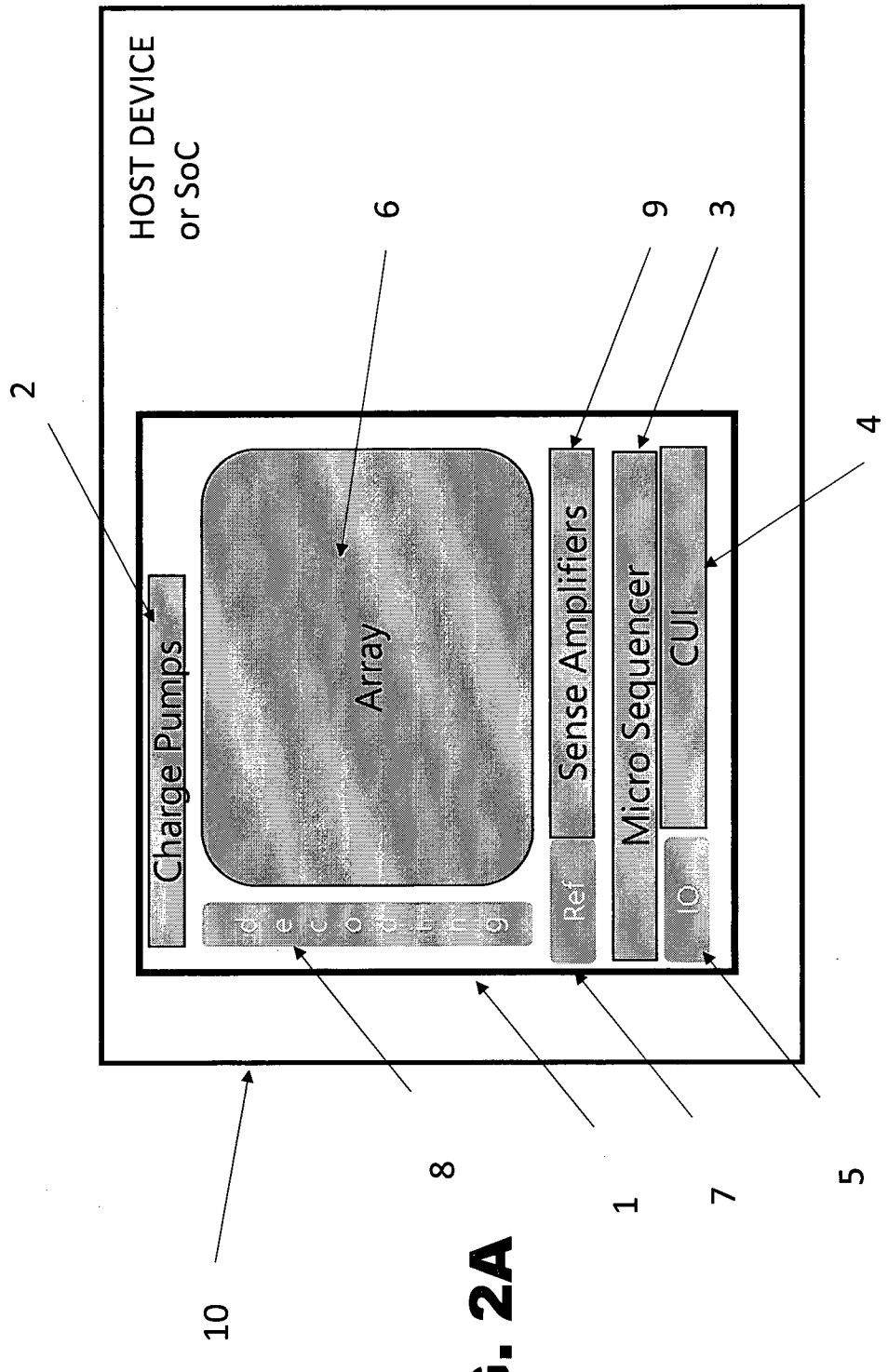

HOST DEVICE
or SoC
Charge Pumps
Array
Decoding
Sense Amplifiers
Ref
Micro Sequencer
CUI
IO
2
6
9
3
4
10
8
1
7
5

FIG. 2A

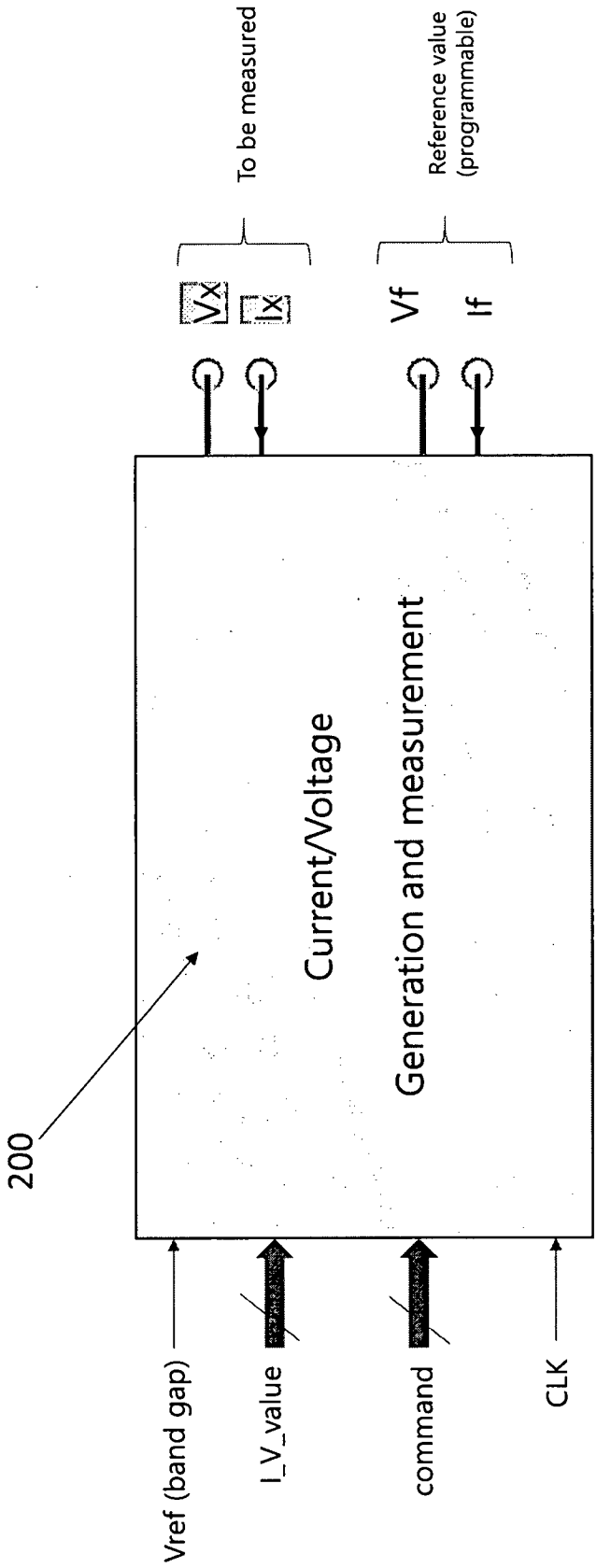

To be measured
Reference value (programmable)
Vx
Ix
Vf
If
200
Current/Voltage
Generation and measurement
Vref (band gap)
I_V_value
command
CLK

FIG. 2B

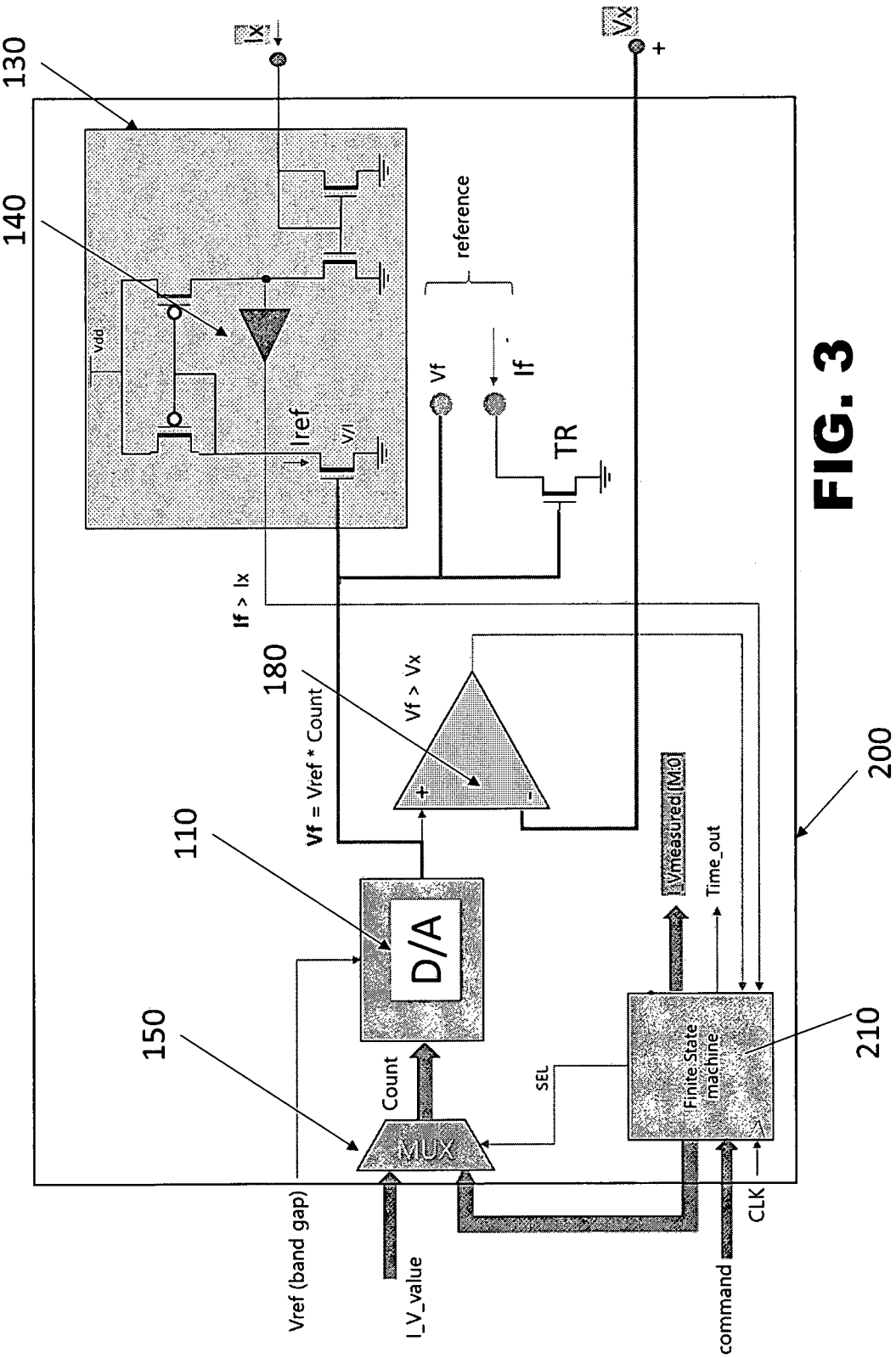

130
140
Ix
Vx
+
reference
Vf
If
TR
Vdd
Iref
Vfl
If > Ix
180
Vf = Vref * Count
Vf > Vx
+
-
110
D/A
200
Vmeasured [M:0]
Time_out
150
Count
SEL
MUX
Finite State machine
210
Vref (band gap)
I_V_value
command
CLK

FIG. 3

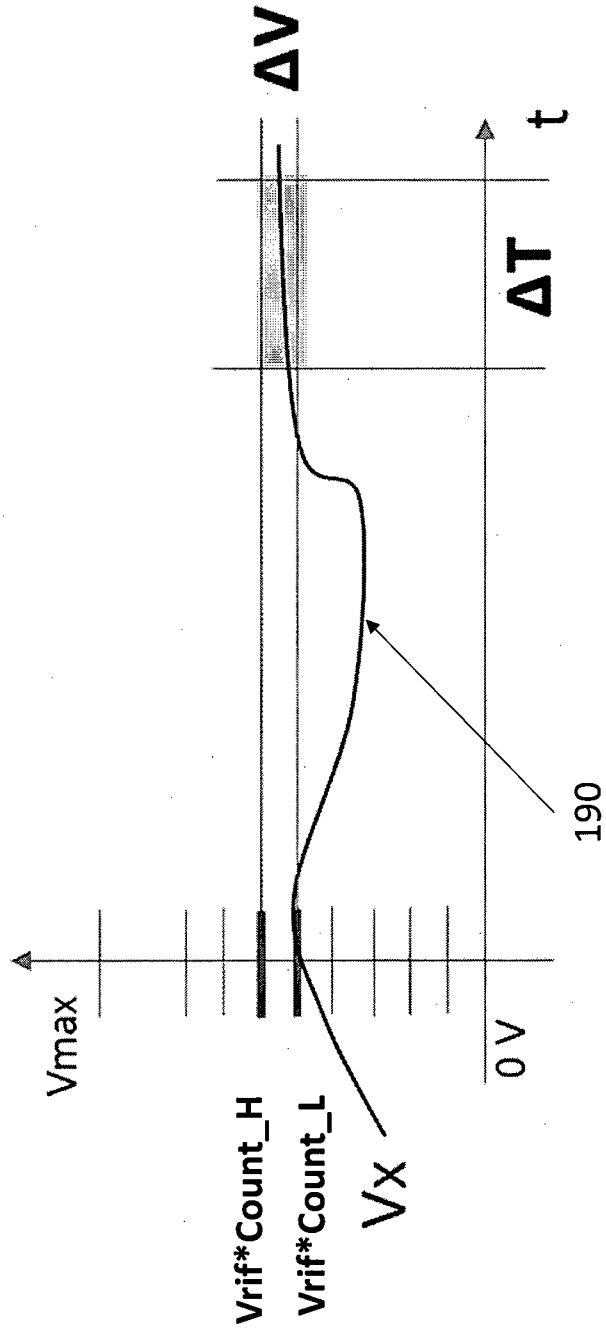


FIG. 4

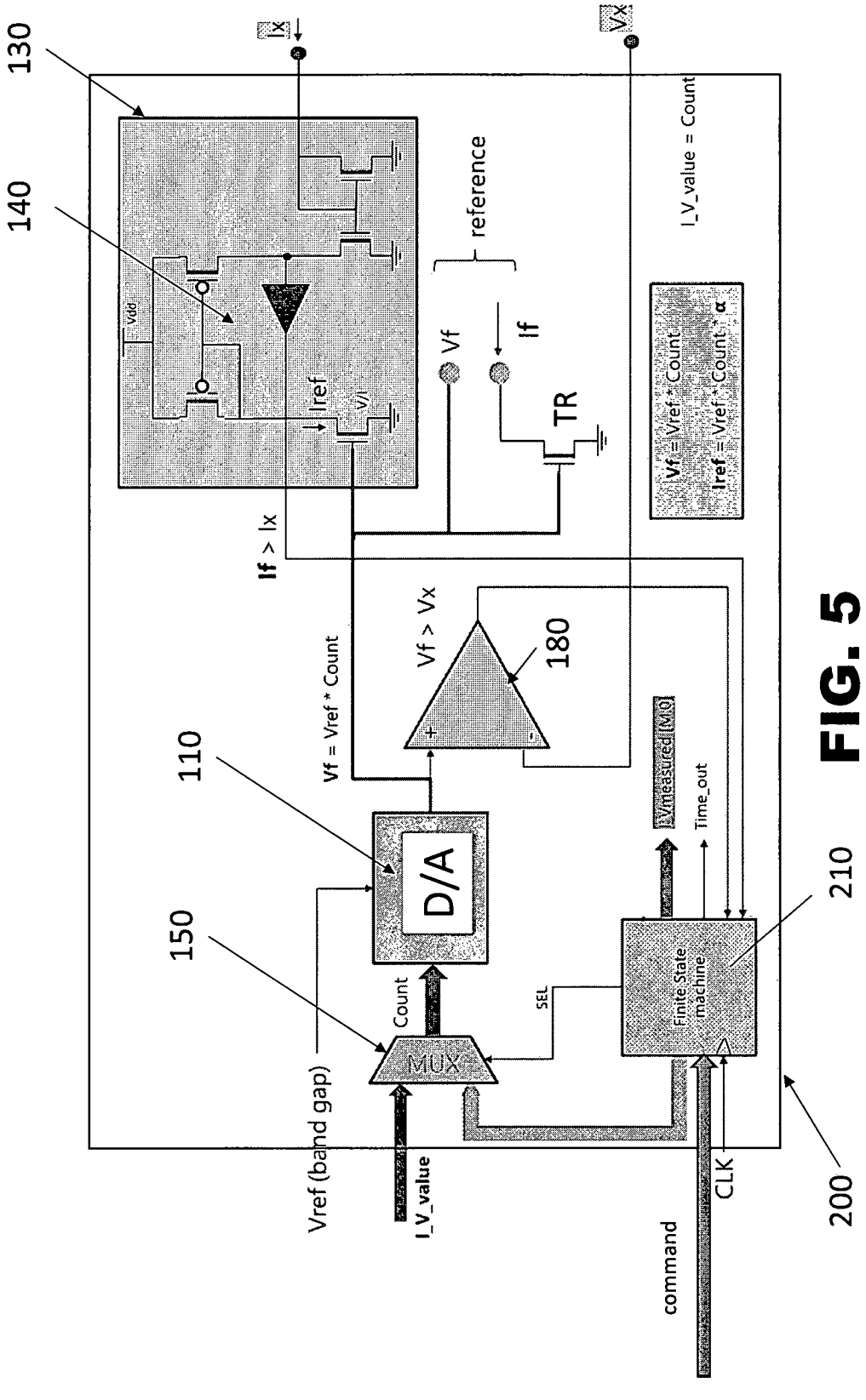

130
140
Ix
Vx
reference
I_V_value = Count
Vdd
Iref
Vf
If
TR
Vf = Vref * Count
Iref = Vref * Count * α
If > Ix
Vf > Vx
180
Vf = Vref * Count
110
D/A
Vmeasured (Mi0)
Time_out
150
Count
SEL
MUX
Finite State machine
210
Vref (band gap)
I_V_value
command
CLK
200

FIG. 5

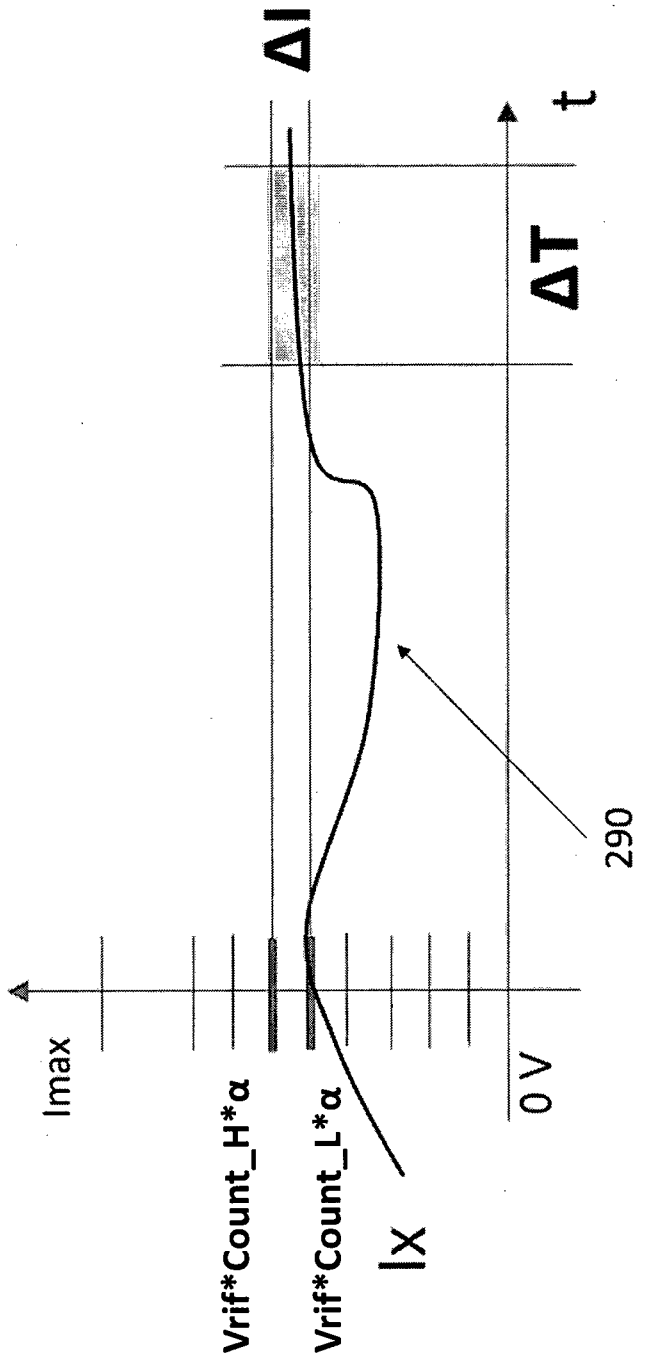


FIG. 6

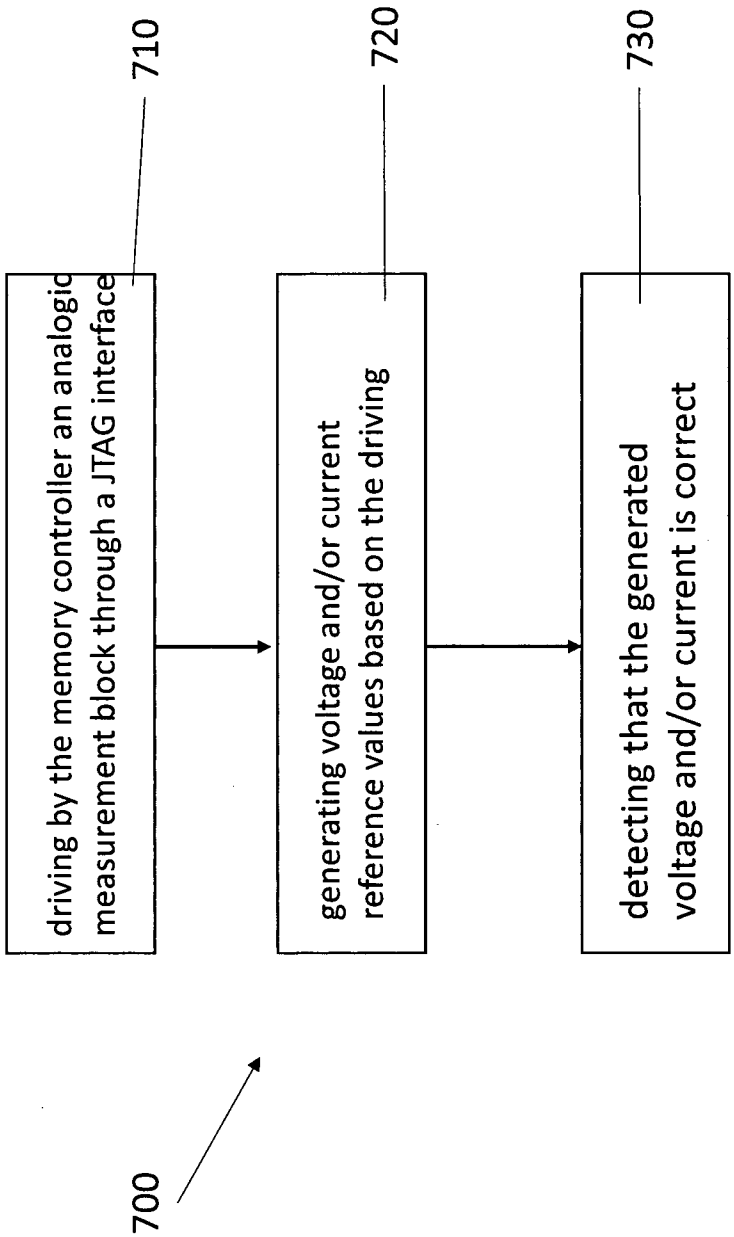

700
710
driving by the memory controller an analogic measurement block through a JTAG interface
720
generating voltage and/or current reference values based on the driving
730
detecting that the generated voltage and/or current is correct

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2019/000479

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C29/56 G11C5/14 G11C29/02 G11C29/50
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2005/242980 A1 (COLLINS ANTHONY J [IE] ET AL) 3 November 2005 (2005-11-03) paragraph [0232] - paragraph [0234]; figures 1,3A,3B,10,12,15B -----	1,4,11, 14,21 5,15 6-10, 16-20,24
Y	US 2009/157340 A1 (GOPALAN ANAND [US] ET AL) 18 June 2009 (2009-06-18) paragraph [0033] - paragraph [0041]; figures 3,4 -----	5,15
A	US 2012/229169 A1 (NGUYEN ANDY [US] ET AL) 13 September 2012 (2012-09-13) paragraph [0020] - paragraph [0059]; figures 2,3 -----	1,4,5, 11,14, 15,21,24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 January 2020	01/04/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wolff, Norbert

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2019/000479

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 2, 3, 12, 13, 22
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1, 4-11, 14-21, 24

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 4-11, 14-21, 24

   Generation of analog measurement values
   ---

2. claim: 23

   Access limitation to test registers

Continuation of Box II.2

Claims Nos.: 2, 3, 12, 13, 22

The subject-matter of dependent claims 2, 3, 12, 13, 22 lacks clarity to that extend, that their technical features can not be understood and substantial assumption would be required to guess what is likely meant.
Dependent claim 2 reads:
"The memory device of claim 1 comprising a plurality of test registers in said JTAG interface, each register being associated with a specific address for testing the functionality of the memory component to which the controller is associated."
Dependent claim 3 reads:
"The memory device of claim 1 wherein said JTAG interface includes at least a test register configured to generate instructions for said analogic measurement block."
The person skilled in the technical field of semiconductor memories identifies a register as a location to store data, wherein the particular location is identified by its associated address. The feature of a "register ... for testing the functionality" appears obscure and the examiner does not guess which particular technical feature is meant. This feature is understood from the description as those registers which store instructions for conducting the test (see par.[0054], [0057], [0117]). However, as merely being a storage location a register does not provide any additional functionality for performing the claimed functionality test.
The description also describes, as defined in dependent claim 3, that the test registers "generate" instructions, which also appears not understandable, since registers merely store data, but do not generate them. The subject-matter of claims 2 and 3 is therefore too broad, unspecific and not usable to identify their features as the first invention whereon a search may focus.
It is noted that the subject-matter of dependent claims 2 and 3 is substantially different from the subject-matter of other dependent claims, i.e. dependent claims 5 - 10, such that it may not be considered as subject-matter of the searched first invention.
The subject-matter of dependent claims 12, 13, and 22 corresponds to the subject-matter of dependent claims 2 and 3 and was therefore correspondingly not searched.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase

before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-IV, 7.2), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2019/000479

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005242980 A1	03-11-2005	NONE	
US 2009157340 A1	18-06-2009	NONE	
US 2012229169 A1	13-09-2012	CN 102027382 A	20-04-2011
		US 2009261862 A1	22-10-2009
		US 2011204924 A1	25-08-2011
		US 2012229169 A1	13-09-2012
		WO 2009129273 A2	22-10-2009