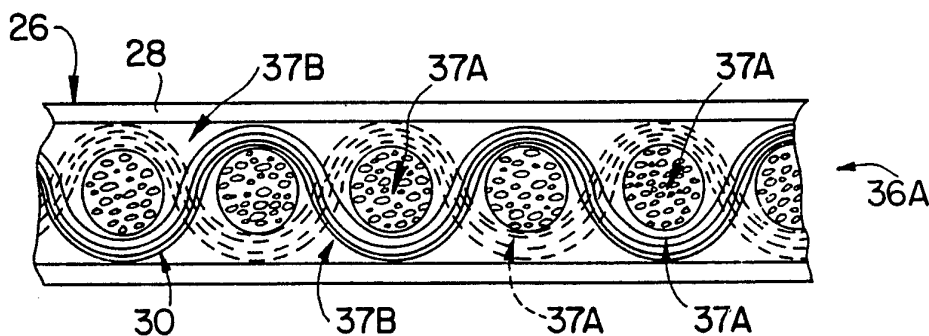




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁵ : B32B 3/00, 7/00	A1	(11) International Publication Number: WO 94/02310 (43) International Publication Date: 3 February 1994 (03.02.94)
<p>(21) International Application Number: PCT/US92/05957</p> <p>(22) International Filing Date: 16 July 1992 (16.07.92)</p> <p>(71) Applicant: ZYCON CORPORATION [US/US]; 445 El Camino Real, Santa Clara, CA 95050 (US).</p> <p>(72) Inventors: HOWARD, James, R. ; 138 Forest Hill Drive, Los Gatos, CA 95030 (US). LUCAS, Gregory, L. ; 7680 Crestmont Avenue, Newark, CA 94560 (US).</p> <p>(74) Agents: DVORAK, George, F. et al.; 53 West Jackson Boulevard, Suite 1616, Chicago, IL 60604 (US).</p> <p>(81) Designated States: AT, AU, BB, BG, BR, CA, CH, CS, DE, DK, ES, FI, GB, HU, JP, KP, KR, LK, LU, MG, MN, MW, NL, NO, PL, RO, RU, SD, SE, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, SN, TD, TG).</p>	<p>Published <i>With international search report.</i></p>	

(54) Title: PRINTED CIRCUIT BOARD WITH INTERNAL CAPACITOR



(57) Abstract

A printed circuit board (PCB) has an internal capacitor (26) with at least two conductive foils (28, 30) and one intermediate dielectric sheet (36A), the dielectric sheet including spacer material (37A) extending therethrough for uniformly maintaining its thickness and dielectric material (37B) developing a uniform dielectric constant therein, the spacer material and dielectric material maintaining the uniform thickness and uniform dielectric constant of the internal capacitor during final lamination of formation of the PCB. The internal capacitor may depend upon borrowed capacitance with the total effective capacitance of the internal capacitor being less than the combined capacitive requirements of devices coupled with the internal capacitor. In one embodiment, at least a portion of the internal capacitor is formed simultaneously with final formation of the PCB by an in situ method. In another embodiment, the internal capacitor is formed with multiple capacitor elements, at least one conductive foils in the internal capacitor forming a portion of two different capacitor elements, the number of dielectric sheets in the internal capacitor equaling the number of capacitor elements, the number of conductive foils in the internal capacitor equaling the number of capacitor elements plus one.

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PRINTED CIRCUIT BOARD WITH INTERNAL CAPACITOR

Field of the Invention

5 The present invention relates to a capacitive printed circuit board (PCB) with an internal capacitor providing a bypass capacitive function for devices mounted or formed on the PCB.

Background of the Invention

10 Printed circuit boards (PCBs) are commonly formed with internal power and ground planes which are connected with surface devices such as integrated circuits mounted on the PCBs. In the operation of the PCBs, it is commonly necessary to compensate for voltage fluctuations arising between the power and ground planes in the PCBs, particularly when sensitive devices such as integrated circuits are mounted on the board and connected with the power and ground planes for operation.

15 Voltage fluctuations of the type referred to above are commonly caused by the integrated circuits switching on and off, the fluctuations resulting in "noise" which is undesirable and/or unacceptable in many applications.

20 A preferred solution to this problem has been the provision of capacitors connected directly with the integrated circuits and/or with the power and ground planes in the vicinity of selected integrated circuits. Initially, surface capacitors were formed with the surface devices or separately mounted upon the surface of the PCB and connected with the respective devices or integrated circuits, *etc.*, either by surface traces or by through-hole connections, for example.

25 Surface capacitors of this type were generally effective to reduce or minimize undesirable voltage fluctuations for the devices. However, surface or bypass capacitors have not always been effective in all applications. For example, the capacitors may tend to affect "response" of the integrated circuits or other devices because the capacitors have not only a capacitive value but an inductive value as well. In this regard, it is well known that inductance arises because of currents passing

through conductors such as the traces or connectors coupling the capacitors with the devices or power and ground planes.

Furthermore, the integrated circuits or other devices are a primary source of radiated energy creating noise from voltage fluctuations in the PCBs.

5 Different characteristics are commonly observed for such devices operating at different speeds or frequencies. Accordingly, the PCBs and device arrays as well as associated capacitors must commonly be designed to assure necessary noise suppression at both high and low speed operation.

10 The design of PCBs and device arrays as discussed above are well known to those skilled in the art of printed circuit board design. For purposes of the present invention, it is sufficient to realize that the use of surface mounted capacitors which are individually connected with the integrated circuits or devices substantially increase the complexity and cost of manufacture for the PCBs as well as undesirably affecting their reliability.

15 In order to overcome these limitations or for other reasons, a number of capacitive PCBs have been provided in the prior art. Initially, U.S. Patent 4,775,573 issued October 4, 1988 to Turek disclosed a multilayer printed circuit board having conductive and dielectric layers deposited on a surface of the board in order to form a bypass capacitor for devices mounted on the board.

20 More recently, U.S. Patent 5,010,641 issued April 30, 1991 to Sisler disclosed a method of making a multilayer printed circuit board with a fully cured dielectric material positioned between power and ground plane layers therein.

25 Still further, U.S. Patent 5,079,069 issued January 7, 1992 to Howard, *et al.* and assigned to Zycon Corporation, the assignee of the present invention, disclosed a capacitive printed circuit board including a capacitor laminate therein to provide a bypass capacitive function for devices mounted for formed on the PCB.

30 The printed circuit board variations disclosed above were suitable for their intended purposes. However, there has been found to remain a need for further improvements in order to both enhance operation of devices on the PCBs as well as to improve, simplify and/or reduce costs of the PCBs themselves.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a capacitive PCB with an internal capacitor as a bypass capacitor element suitable for coupling with devices mounted or formed on the PCB.

5 More specifically, it is an object of the invention to provide such a capacitive PCB with an internal capacitor including at least two conductive foils and one intermediate dielectric sheet, the dielectric sheet including spacer material extending throughout the dielectric sheet for uniformly maintaining its thickness and dielectric material developing a uniform dielectric constant therein, the spacer material
10 and dielectric material in combination maintaining both the uniform thickness and uniform dielectric constant of the internal capacitor during and following formation of the PCB.

Preferably, the spacer material is intimately and uniformly intermixed with the dielectric material in order to maintain the uniform thickness and uniform
15 dielectric constant of the dielectric sheet.

The internal capacitor may be formed with a total capacitive capability equal to the combined capacitive values for devices coupled therewith or, alternatively, with a substantially reduced capacitive value whereby the devices are required to
20 operate on a principle of borrowed capacitance.

It is a further related object of the invention to form all or a portion of the internal capacitor by an *in situ* method simultaneously with final formation of the PCB, the final formation of the PCB preferably being carried out by means of a final lamination step.

It is a still further related object of the invention to form the internal
25 capacitor with multiple capacitor elements, at least one conductive foil in the internal capacitor forming a portion of two capacitor elements, the number of dielectric sheets in the internal capacitor equalling the number of capacitor elements therein and the number of conductive foils in the internal capacitor equalling the number of capacitor elements therein plus one.

Additional objects and advantages of the invention are made apparent in the following specification having reference to the accompanying drawings.

Brief Description of the Drawings

5 FIGURE 1 is a plan view of a capacitive printed circuit board (PCB) constructed according to the present invention.

 FIGURE 2 is an enlarged fragmentary view of a portion of the printed circuit board showing a device such as an integrated circuit mounted on the board and connected with other devices and a power source in the board by through-hole connections.

10 FIGURE 3 is a view similar to FIGURE 2 while illustrating a surface mounted device arranged upon the board and connected with other devices or components and a power source in the board by surface traces or paths.

 FIGURE 4 is a schematic sectional view of a printed circuit board illustrating connections or traces for coupling a representative surface device on the board to power and ground planes formed by an internal bypass capacitive subassembly arranged within the PCB and constructed according to the present invention.

 FIGURE 5 is an enlarged, fragmentary view in cross-section of a dielectric sheet forming a portion of the internal capacitor of the present invention.

20 FIGURE 6 is a generally schematic cross-sectional representation of an internal bypass capacitive subassembly constructed according to the invention to emphasize the compound capacitor structure thereof.

 FIGURE 7 is an exploded cross-sectional view of components in the internal bypass capacitive subassembly to illustrate a preferred method of manufacture.

25 FIGURE 8 is similar to FIGURE 6 while representing yet a further manufacturing step for the same internal bypass capacitive subassembly.

 FIGURE 9 illustrates an exploded assembly of components suitable for forming a capacitive PCB according to the *in situ* method of the present invention.

30 FIGURES 10A, 10B, 10C and 10D illustrate an *in situ* process according to the present invention for also forming a capacitive PCB and

simultaneously forming a bypass capacitive element internally therein by the final lamination step for the PCB.

FIGURES 11 and 12 illustrate additional embodiments of the method of the present invention for *in situ* formation of compound bypass capacitive subassemblies within a capacitive PCB according to the present invention.

(NOTE: The above drawings correspond to drawings in either File 399P or File 402P except for FIGURE 5. FIGURE 5 corresponds to the added disclosure of the application and is intended to illustrate both the fiberglass as a spacer means and the surrounding dielectric material forming the dielectric sheet. Please let me know if you have any suggestions for additional features in FIGURE 5 to further enhance the additional disclosure in this application.)

Description of the Preferred Embodiments

An internal bypass capacitive subassembly for use in a capacitive printed circuit board is described in greater detail below. It is particularly important to note that the internal bypass capacitor subassembly is designed to facilitate and simplify manufacture, preferably by lamination of the internal bypass capacitor subassembly as a unitary component. The conductive foils and dielectric sheets employed within the internal bypass capacitive subassembly are formed from existing state of the art materials. However, it is emphasized that the internal bypass capacitive subassembly may also be constructed by other techniques besides lamination and may also take advantage of improvements in either the conductive foils or dielectric material used in the dielectric sheets.

It is also important to understand that substantial amounts of capacitance may be required for devices on the PCB. In this regard, the above noted Zycon patent initially disclosed the concept of borrowed or shared capacitance. According to the concept of borrowed or shared capacitance, the internal bypass capacitive subassembly is capable of satisfying capacitive requirements for surface devices even though the total capacitance requirements for the devices are greater than the capacitance of the internal bypass capacitive subassembly. As originally set forth in the above patent, such operation is possible based on intermittent operation of the

devices so that actual capacitance requirements for the devices at any given time are only a fraction of the cumulative capacitive requirements for all of the devices.

Even though the present invention contemplates the use of such a concept of borrowed or shared capacitance, it is also important to understand that the internal bypass capacitive subassembly of the invention may in fact be capable of simultaneously satisfying the cumulative capacitive requirements for all of the devices. Such a possibility exists initially because of the compound capacitor construction of the internal bypass capacitive subassembly, provided in one embodiment of the present invention. Because of the construction for the capacitive subassembly as described in greater detail below, it is possible to provide a substantial number of capacitor elements within the capacitive subassembly, each of the capacitor elements extending substantially throughout the surface area of the board. In this manner, it is accordingly possible to substantially increase the available capacitance provided in a capacitive PCB by the internal bypass capacitive subassembly of the invention.

Secondly, it is also possible to substantially increase the total capacitance of the capacitive subassembly by using dielectric materials of substantially increased dielectric constant. Dielectric materials of greatly increased dielectric constant are believed possible. Accordingly, the present invention contemplates not only a capacitive PCB based on the concept of borrowed or shared capacitance as noted above but also a capacitive PCB wherein the total capacitance is approximately equal to or even in excess of total capacitive requirements for devices mounted on the PCB.

In addition to further facilitating manufacture of the capacitive printed circuit board with even greater economy and even more greatly enhanced reliability, the present invention has also been found to permit improved response of large numbers of devices provided with capacitance by the compound bypass capacitive subassembly, similarly as the capacitive printed circuit boards in the above noted Zycon patent.

The compound capacitor of the invention is also similar to the capacitor laminate of the above noted Zycon patent in permitting precise voltage regulation and

noise reduction over broad device frequency ranges and particularly achieving similar voltage regulation and noise reduction at lower frequencies, for example, up to about 40 MHz, by tuning wherein limited numbers of surface capacitors are interconnected with the compound capacitor as described for the capacitor laminate in the above noted Zycon patent.

Referring initially to FIGURE 1, a capacitive PCB constructed according to the present invention is generally indicated at 10. The printed circuit board 10 is of generally conventional construction except for the provision of an internal capacitor laminate as described in greater detail below. Accordingly, external features of the capacitive printed circuit board 10 are only briefly noted, the architecture and design considerations for the printed circuit board otherwise being generally of a type well known to those skilled in the art.

For purposes of the present invention, it is sufficient to understand that the capacitive PCB 10 is of a type including large numbers of devices 12 arranged upon its surfaces. In accordance with well known printed circuit board technology, the devices or components may be arranged upon one or both sides of the board and may include both active devices such as integrated circuits, transistors, *etc.* Such active devices may even include components such as vacuum tubes or the like. The devices 12 may also include passive devices such as capacitors, resistors, inductors, *etc.*

In the design of PCBs such as that illustrated at 10, it is common practice to employ a power source described and illustrated in greater detail below which is embodied by power and ground planes or conductors formed as laminates in the printed circuit board itself. A variety of configurations are provided for mounting the devices upon the PCB and for interconnecting them both with the power source and each other. Although such design considerations are generally outside the scope of the present invention, two such configurations are described below with reference to FIGURES 2 and 3.

Referring to FIGURE 2, an active device such as integrated circuit is indicated at 14 with a passive device, specifically a capacitor being generally indicated

at 16. These devices, particularly the active device or integrated circuit 14, are representative of large numbers of devices arranged upon the printed circuit board as generally indicated in FIGURE 1. In a configuration of the type illustrated in FIGURE 2, the devices are interconnected to power and ground planes within the printed circuit board and to other devices by through-hole connectors or pins generally indicated at 18. In FIGURE 2, two such connectors or pins 18 are illustrated for the capacitor 16 while the integrated circuit 14 is of a 16-pin design including 16 through-hole connectors or pins 18 as illustrated. Additional traces may be provided as generally indicated at 20 for facilitating interconnection of the various devices upon the printed circuit board.

Another configuration for a printed circuit board is indicated by the fragmentary representation of FIGURE 3 which similarly illustrates an active device such as an integrated circuit being generally indicated at 14' and illustrated in phantom since it is mounted on the opposite or top surface of the circuit board from the bottom surface illustrated in FIGURE 3. A passive device or capacitor 16' is also illustrated in FIGURE 3 preferably mounted on the bottom surface 22 of the printed circuit board. In the surface mounted configuration of FIGURE 3, both the active device 14' and the capacitor 16' are mounted upon surface traces or pads 24. In accordance with well known techniques in the printed circuit board technology, the pads 24 facilitate surface mounting of the devices while providing for interconnection of the devices with each other and with a power source such as the internal power and ground planes referred to above by both surface traces and through-hole connectors or pins where necessary.

With reference to both FIGURES 2 and 3, the present invention particularly contemplates the use of an internal capacitive layer in the form of the capacitor laminate of the present invention in order to replace large numbers of surface capacitors. Accordingly, although most of the surface capacitors are replaced in the printed circuit board 10 by the capacitor laminate of the invention, a limited number of surface capacitors may still be desirable as illustrated in FIGURES 2 and 3, at least for the purpose of achieving low frequency tuning as discussed in greater detail below.

FIGURE 4 is a sectional view of the capacitive PCB 10 of FIGURE 1 and illustrates a compound bypass capacitor or capacitive subassembly 26 constructed according to the present invention and forming an internal capacitive device within or on the printed circuit board 10. The compound bypass capacitor 26 includes
5 conductive foils 28, 30, 32 and 34, preferably formed from copper, with dielectric sheets 36 arranged between each adjacent pairs of the foils. Preferably, the conductive foils 28, 30, 32 and 34 form power and ground planes for the printed circuit board. Such a configuration, specifically in terms of the power and ground planes, is well known in the art and no further discussion in that regard is believed necessary. More
10 specifically, the foils 28 and 32 are power planes and the foils 30 and 34 are ground planes.

A surface mounted device 14', corresponding to the integrated circuit of FIGURE 2, is mounted on the surface of the board in FIGURE 4 and is interconnected with the conductive foil by respective power and ground leads 38 and 40. The power
15 lead 38 is connected with the conductive foils 28 and 32 while a hole (not shown) is formed at corresponding portions in the other conductive foils 30 and 34. Similarly, the ground lead 40 passes through holes in the conductive foils 28 and 32 while being electrically coupled with the conductive foils 30 and 34. In this manner, the surface device 14' is properly connected with both the power and ground planes. Signal
20 traces such as that indicated at 42 are also provided for interconnecting the devices or for making other connections within the PCB as necessary.

Referring now to FIGURE 5, the present invention essentially contemplates formation of each dielectric sheet to include both spacer material 37A and dielectric material 37B. In FIGURE 5, one of the dielectric sheets from FIGURE
25 4 is illustrated, preferably the upper dielectric sheet indicated at 36A. However, it is to be understood that all other dielectric sheets employed in both embodiments of the invention have a similar configuration and method of construction.

More specifically, the spacer material indicated at 37A is preferably finely divided fiberglass of a type conventionally employed in prepreg layers of
30 conventional printed circuit boards. As illustrated in FIGURE 5, the strands of

fiberglass 37A are arranged uniformly and multi-directionally throughout the dielectric sheet in order to provide a generally incompressible component in the dielectric sheet. Incompressibility of the dielectric sheet is especially important during lamination operations, including the final lamination step for the PCB. During such lamination steps, substantial heat and pressure are of course applied to the PCB and it is the function of the spacer material 37A to maintain uniform spacing for the dielectric sheet both during formation of the PCB and thereafter.

At the same time, the spacer material 37A is intimately and uniformly intermixed with the dielectric material 37B. The dielectric material 37B may, for example, be a mixture of epoxy and other materials, preferably selected for having a relatively high dielectric constant. Such materials are well known to those skilled in the art and include — (NOTE: Please add a listing of suitable dielectric materials).

Furthermore, the dielectric material 37B may be in either a cured or uncured stage. It is well known to those skilled in the art of printed circuit boards that such materials can be initially uncured prior to their inclusion in a lamination operation. During the application of heat and pressure in the lamination process, the material becomes cured and, at the same time, is intimately bonded to adjacent layers of material. In the present case, the dielectric sheet 36A, upon being cured, is intimately bonded to the conductive foils 28 and 30.

In any event, the intimately and uniformly intermixed spacer material 37A and dielectric material 37B form a novel function in the present invention of maintaining the essential uniform thickness of the dielectric sheets (because of the spacer material 37A) while at the same time also maintaining a uniform dielectric constant for the dielectric sheet (because of the relatively high dielectric constant for the dielectric material 37B).

In this regard, it is to be understood that other combinations of spacer material and dielectric material could be employed in the present invention in the place of the fiberglass described as a preferred spacer material and the combination of epoxy and dielectric described for the dielectric material 37B. Rather, it is to be understood as essential according to the present invention that each dielectric sheet

include a spacer material for maintaining uniform thickness and a dielectric material suitable for maintaining a uniform dielectric constant at a suitable level according to the present invention.

5 Referring now to FIGURE 6, one embodiment of the invention includes the compound capacitor subassembly which is illustrated in greater detail with the three dielectric sheets of the compound capacitor subassembly being indicated respectively at 36A, 36B and 36C. The compound capacitor subassembly of FIGURE 6 novelly includes both of the interior conductive foils 30 and 32 in two different capacitor elements. In this regard, each capacitor element includes one of the dielectric sheets 36A, 36B and 36C. The first capacitor element includes the dielectric sheet 36A together with the power and ground planes 28 and 30. The second capacitor element includes the dielectric sheet 36B and the ground and power planes 30 and 32. The third capacitor element includes the dielectric sheet 36C and the power and ground planes 32 and 34.

15 It may be seen from the above description that the compound bypass capacitive subassembly 26 of FIGURE 6 includes a total of three capacitor elements. At the same time, the capacitive subassembly 26 includes three dielectric sheets equal to the number of capacitor elements in the capacitive subassembly. The capacitive subassembly also includes four conductive foils or a total number of conductive foils equal to the number of capacitor elements plus one.

20 The above summary illustrates a particularly important feature of the invention in that the capacitive subassembly employs compound use of one or more conductive foils, each in two different capacitor elements. This initially reduces the cost of the capacitive subassembly since the conductive foils represent the most expensive portion thereof. At the same time, the compound construction of the capacitive subassembly permits a particularly compact configuration for the capacitive subassembly 26 which also greatly facilitates its manufacture.

25 Through the construction of the compound bypass capacitive subassembly 26 as described above, it is thus possible to greatly increase the total

capacitance for the PCB 10 or 10' merely by increasing the number of capacitor elements.

It may also be seen from the above summary that the invention contemplates a capacitive subassembly with at least three conductive foils and dielectric sheets arranged between each adjacent pair of foils. More preferably, the
5 capacitive subassembly 26 of the present invention includes four or even more conductive foils as illustrated in FIGURE 6 with three or more dielectric sheets arranged respectively between adjacent pairs of the foils in the preferred configuration as illustrated.

10 Referring again to FIGURE 4, it may be seen that the odd conductive foils and the even conductive foils, numbered from either side of the capacitive subassembly 26, are respectively power and ground planes which are separately interconnected, for example by the traces 34 and 36 as illustrated in FIGURE 4.

The compound capacitor 26 is designed to provide necessary
15 capacitance for all or a substantial number of devices mounted upon the surface of the PCB 10 or 10'. These devices may be interconnected with the power and ground planes either by separate through-hole pins or by surface traces of the type illustrated respectively in FIGURES 2 and 3.

20 Preferably, because of the very substantial capacitance for the combined devices, the compound capacitor 26 is contemplated to operate on the concept of borrowed capacitance as discussed above wherein the total capacitance of the compound capacitor 26 is less than the total required capacitance for all of the devices on the PCB 10 or 10'. However, as noted above, the compound capacitor 26 is effective for supplying capacitance to all of the devices based on the concept of
25 random operation for the devices. In other words, the combined capacitor elements within the capacitive subassembly 26 provide sufficient capacitance in order to permit operation of each individual device with sufficient capacitance for its proper operation.

Although the capacitive subassembly 26 is adapted for operation based upon the concept of borrowed capacitance, the total capacitance of the compound
30 capacitor 26 may be substantially increased. Initially, it is of course possible to

include larger numbers of capacitor elements within the compound capacitive subassembly 26. In addition, higher capacitive values per unit area for each capacitor element in the subassembly 26 may also be substantially increased, for example, by use of much higher dielectric constant materials in the dielectric sheets 36.

5 In any event, although the compound capacitive subassembly 26 is contemplated for operation on the basis of borrowed capacitance, the present invention also contemplates the possibility that the compound capacitive subassembly 26 may also have a greatly increased total capacitance either approaching or even equalling the total capacitive requirements for all of the devices on the PCB 10 or 10'.

10 As was also discussed above, each of the conductive foils is formed with a sufficient mass of copper per unit area in order to achieve structural rigidity or self-support and also preferably to permit sufficient electron flow or current flow in accordance with the concept of borrowed capacitance. More specifically, it is contemplated that each of the conductive foils is formed with at least about 0.5 ounces
15 of copper per square foot, that mass corresponding generally to a thickness of about 0.5 mils, more specifically about 0.6-0.7 mils. The thickness of the conductive sheets may be increased, for example, in order to meet larger voltage or current carrying capacities for the power and ground planes in a particular application. Preferably, each of the conductive sheets includes about 1-2 ounces of copper per square foot,
20 those masses corresponding to thicknesses for the individual sheets in the range of about 1.2-2.4 mils. More preferably, the conductive foils are formed with about one ounce of copper per square foot or having a thickness in the range of about 1.2-1.4 mils to achieve optimum performance of the capacitor laminate 26. That amount of copper in each of the conductive foils is also selected as a minimum for achieving
25 good structural rigidity within the conductive sheets 28 and 30 alone prior to their lamination into the compound capacitive subassembly 26.

30 The composition and thickness of the dielectric sheets 36 are selected to achieve necessary capacitance, again in accordance with the concept of borrowed capacitance, and also to achieve structural rigidity for the dielectric sheets 36, both prior to and after inclusion within the compound capacitive subassembly.

The present invention preferably contemplates the use of dielectric material having a dielectric constant of at least about 4. A range of dielectric materials widely available in the present state-of-the-art having dielectric constants in the range of about 4-5. Furthermore, it is possible to formulate dielectric compositions, for example, from ceramic filled epoxies, with dielectric constants ranging up toward 10 for example. Thus, the present invention preferably contemplates use of a material with a dielectric constant of at least about 4, more preferably within a range of about 4-5 and most preferably about 4.7, at least for the specific composition contemplated in the preferred embodiment. However, much higher capacitances are also contemplated, as discussed above.

A preferred dielectric constant can be achieved by combinations of a woven component and a resin component combined together to form the necessary combination of dielectric constant and structural rigidity. The woven component may include polymers such as polytetrafluoroethylene (available under the trade names TEFLON and GORETEX) and epoxies. However, the woven components are preferably formed from glass which may be of a quartz variety but is preferably silica, the glass being formed in threads which are then woven together to form sheets filled or impregnated with a selected resin. The resins are commonly selected for fire retardant characteristics and may include materials such as cyanate esters, polyimides, kapton materials and other known dielectric materials. However, the resin is preferably an epoxy, again in order to take advantage of the existing state-of-the-art regarding use of such resins in PCB manufacture.

A dielectric sheet formed from a single woven layer of glass and about 70.0% by weight resin has the preferred dielectric constant of 4.7 as noted above while also exhibiting good structural rigidity at a thickness of about 1.5 mils.

The thickness of the dielectric sheet in the present invention is selected not only to achieve the desired capacitance but also to assure electrical integrity, particularly the prevention of shorts developing between the conductive foils in the compound capacitor 26. Common practice contemplates treatment of the surfaces of the conductive sheets adjacent the dielectric sheet in order to enhance adhesion within

the compound capacitor 26. Such adhesion is necessary not only for structural integrity but also to assure proper electrical performance. Typically adjacent surfaces of the conductive foils are treated by deposition in zinc or zinc and copper (a brass alloy), usually by plating, in order to form roughened surfaces in a manner well known to those skilled in the PCB art. These roughened surfaces provide "tooth" to enhance mechanical bonding to the dielectric material in the sheets 36.

Another aspect of the invention is noted with respect to characteristics of the conductive foils, 28, 30, 32 and 34. In accordance with standard practice, each of the conductive foils commonly has a matte or tooth side and a barrel or smooth side. Surface variations of the tooth side of the conductive foils is substantially greater than for the opposite smooth side. Such conductive foils are commercially supplied by a number of sources including Gould Electronics and Texas Instruments. Conductive foils formed from copper are available from Gould under the trade name "JTC" FOIL as described in Gould Bulletin 88401 published by Gould, Inc., Eastlake, Ohio in March 1989. Other foils available from Gould include those available under the trade names LOW PROFILE "JTC" FOIL and "TC/TC" DOUBLE TREATED COPPER FOIL and described respectively in Bulletin 88406 and Bulletin 88405, both published in March 1989 by Gould, Inc.

In the capacitor subassembly 26 of the present invention, the greater surface differential on the rough side of the foil is generally excessive for preferred dimensions of dielectric as noted above. This is a consideration in the present invention since, for the two internal conductive foils 30 and 32, both surfaces of those foils are employed in different capacitor elements. In order to assure "capacitive integrity", that is, absence of shorts, *etc.*, the present invention contemplates a number of different approaches for overcoming this problem.

Initially, the thickness of the dielectric sheet 36 may be increased adjacent the rough sides of the conductive foils in order to assure adequate spacing between all surface portions of opposing conductive foils. Alternatively, the surface variations on the rough side of the foil may be reduced, for example by further calendaring or scrubbing. Generally, a calendaring operation as contemplated for

compacting ductile material of the foil in order to reduce surface variations on the rough side thereof. In a scrubbing or abrading operation, some of the conductive foil material would be removed on the rough side again for the purpose of reducing surface variations thereon. The use of a scrubbing or abrading technique might require
5 a somewhat thicker conductive foil if excessive amounts of material are to be removed.

Yet another approach in this regard is to coat the rough side of the conductive foil, for example with oxide, again for the purpose of reducing surface variations. In this regard, both surfaces of the conductive foils are preferably surface
10 treated in a generally conventional manner in order to assure adhesion to adjacent layers, in the case of the present invention, the dielectric material 36.

In any event, the problem of different surface variations on opposite sides of the conductive foil can be minimized and/or eliminated by one or more of the above techniques.

15 The method of operation for the capacitive PCB 10 or 10' as described above is believed clearly apparent from the preceding description. The following is a description of a preferred method for forming the compound bypass capacitive subassembly 26 with reference to FIGURES 7 and 8.

Referring initially to FIGURE 6, capacitor laminates 40 and 42 may
20 initially be formed by conventional laminating steps, the capacitor laminate 40 including the power plane 28', the ground plane 30' and the dielectric sheet 36A'. The other capacitor laminate 42 may similarly be formed including the power plane 32' and the ground plane 34' together with the dielectric sheet 36C' arranged therebetween.

25 Following curing in a conventional manner of the capacitor laminates 40 and 42, the internal conductive foils 30' and 32' are etched as illustrated in FIGURE 7 for desired purposes including formation of through-holes necessary for permitting passage of traces such as those indicated at 34, 36 and 38 in FIGURE 4.

30 Thereafter, an uncured sheet 36B' of dielectric material is placed between the etched foils 30' and 32'. Thereafter, the combination of the capacitor

laminates 40 and 42 with the uncured dielectric sheet 36B' is laminated and cured, again in a conventional manner to form the completed compound bypass capacitive laminate 26' as also illustrated in FIGURE 8. As further illustrated in FIGURE 8, the conductive foils 28' and 34' may be etched following complete lamination of the compound bypass capacitive subassembly 26' prior to lamination of the entire capacitive subassembly 26' into a PCB such as indicated at 10 or 10' in the other figures.

Accordingly, there have been described above a variety of embodiments for a compound bypass capacitive subassembly or internal capacitor and capacitive PCB constructed and manufactured according to the present invention.

Yet another embodiment of the invention is described below with reference to FIGURES 9-12 which illustrate an *in situ* process according to the present invention for forming a capacitive PCB and simultaneously forming an internal bypass capacitor within the PCB. Referring now to FIGURE 9, an exploded assembly of components is generally indicated at 44 for forming a capacitive PCB such as those indicated at 10 and 10' in FIGURES 1-4 according to the *in situ* method of the present invention. Accordingly, the assembly 44 includes dielectric foils 28' and 30' arranged on opposite sides of a dielectric sheet 32' to form a capacitor element 26'. In the assembly of FIGURE 9, it is important to note that the dielectric layer or sheet 32' is uncured or in a so-called "B" stage according to conventional PCB terminology. Additional PCB layers such as those indicated at 40' and 42' are arranged on opposite sides of the conductive foils 28' and 30'. Preferably, the layers 40' and 42' are respectively laminated to the dielectric foils 28' and 30' so that the conductive foils can be etched prior to their arrangement within the assembly 44. Even more preferably, the conductive foils 28 and 30' form power and ground planes for the PCB 10'. In accordance with conventional PCB practice, portions of the conductive foils or power and ground planes 28' and 30' are etched away or removed. This allows for formation of through-holes in the PCB for receiving leads such as those indicated at 34, 36 and 38 in FIGURE 4.

Additional conductive foils layers 46 and 48 may be laminated to exterior surfaces of the layers 40' and 42'. With the layers 40' and 42' being formed from dielectric material, they are of course converted to a fully cured or so-called "C" stage during lamination to the conductive foils 28' and 30' as well as the outer foils 46 and 48.

With the components of the assembly 44 arranged as illustrated in FIGURE 9, they are subjected to heat and pressure in a conventional final lamination step well known to those skilled in the printed circuit board art to form a PCB such as that indicated at 10 or 10' in FIGURES 1-4 with simultaneous *in situ* formation or lamination of the capacitor element 26' including the conductive foils 28' and 30' as well as the dielectric sheet 32'. During the final lamination step, the dielectric sheet 32' is laminated to both of the conductive foils 28' and 30' while also being converted to a fully cured or "C" stage condition generally similar to the other layers 40' and 42'.

The method of the present invention is described in somewhat greater detail below in FIGURES 10A-10B. Referring initially to FIGURE 10A, an initial lamination product 50 is obtained or formed including the fully cured dielectric sheet 40' with conductive foils 28' and 46' laminated or bonded on opposite sides thereof.

Referring also to FIGURE 10B, with the conductive foil 28' forming for example a power plane for a PCB, the conductive foil 28' is then etched as indicated in FIGURE 10B for reasons discussed in greater detail above.

Referring now to FIGURE 10C, another lamination product 52 is formed in a similar manner as the lamination product 50. The lamination product 52 includes the other PCB layer 42' and the conductive foils 30' and 48'. The conductive foil 30' also preferably forms a ground plane for a resulting PCB and is similarly etched as the conductive foil 28' in FIGURE 10B.

Continuing with reference to FIGURE 10C, the uncured dielectric sheet 32' is then arranged between the lamination products 50 and 52 so that it is adjacent both the conductive foils or power and ground planes 28' and 30'.

With the lamination products 50 and 52 arranged on opposite sides of the uncured dielectric sheet 32' as illustrated in FIGURE 10C, they are then subjected to heat and pressure in a conventional final lamination step as described above for forming the PCB with simultaneous *in situ* formation of the capacitor element 26' from the dielectric sheet 32' and the conductive foils 28' and 30'. Here again, the final lamination step results in conversion of the uncured dielectric sheet 32' to a fully cured or "C" stage condition as described above. The final lamination step described above with reference to FIGURE 10C results in formation of a finished capacitive PCB 10' as illustrated in FIGURE 10D.

The preceding method described particularly with reference to FIGURES 9 and 10A-10D can also be carried out with additional capacitor elements formed within the PCB during the final lamination step similar to the capacitor element 26'. Such an arrangement is not illustrated in the drawings but simply includes one or more additional capacitor elements such as that indicated at 26 or 26' similarly formed during final lamination of the PCB and preferably spaced apart by additional PCB layers (not shown).

The method of the present invention also contemplates formation of the capacitor elements as compound bypass capacitor subassemblies formed according to the method of the present invention as described below with reference to FIGURES 11 and 12.

Referring initially to FIGURE 11, an exploded assembly 54 includes lamination product 50' and 52' similar to the lamination products 50 and 52 of FIGURES 10A-10D. An additional lamination product 56 is centrally arranged within the assembly 54 between the lamination products 50' and 52'. The lamination product 56 includes a fully cured dielectric sheet 58 laminated to conductive foils 60 and 62.

With the assembly as described above, the conductive foils 28' and 62 are preferably power planes for a PCB resulting from the assembly of FIGURE 11 with the conductive foils 30' and 60 being ground planes for the PCB. All of the conductive foils 28', 30', 60 and 62 may be etched if desired after they are laminated respectively onto their supporting dielectric sheets.

Thereafter, uncured dielectric sheets 64 and 66 are arranged respectively between the conductive foils 28', 60 and 30', 62. The components of the assembly 54 are then subjected to heat and pressure, again in a conventional manner for a final lamination step to result in formation of the PCB and simultaneous *in situ* formation of a compound bypass capacitive subassembly 64. The subassembly 64 includes three capacitive elements formed respectively by the conductive foils 28' and 60 together with the dielectric sheet 64, the conductive foils 60 and 62 together with the dielectric sheet 58 and the conductive foils 30' and 62 together with the dielectric sheet 66. The dielectric sheet 64 and 66 are of course converted to a fully cured or "C" stage condition during the final lamination step. Within the subassembly 64, it may also be seen that certain of the conductive foils, particularly those indicated at 60 and 62 are included in multiple capacitor elements to achieve greater efficiency and an increased capacitance for the resulting PCB.

Referring now to FIGURE 12, another exploded assembly of components is generally indicated at 68 for forming a capacitive PCB. The assembly 68 includes lamination products 50', 52' and 56' similar to the lamination products of FIGURE 11. In addition, the assembly 68 includes another lamination product 70 formed from conductive foils 72 and 74 laminated to a dielectric sheet 76.

Uncured sheets of dielectric material respectively indicated at 78, 80 and 82 are then respectively arranged between adjacent pairs of conductive foils 28', 60'; 62', 72 and 30', 74. The components of the assembly 68 are then similarly subjected to heat and pressure in a conventional final lamination step for forming a resulting PCB with simultaneous *in situ* formation of a compound bypass capacitive subassembly 84 including five capacitor elements formed respectively by adjacent conductive foils and intervening dielectric sheets.

In the method according to the present invention described above with reference to FIGURES 11 and 12, it may be seen that alternate capacitor elements are formed by lamination or the conversion of uncured dielectric sheets to a fully cured condition while the other capacitor elements are laminated together prior to the final lamination step described above. In this regard, it is essential to the present invention

that at least one of the capacitor elements be formed by conversion of an uncured sheet of dielectric to a fully cured condition as described above.

5 It is noted again that the capacitive PCBs described above with reference to the figures are designed to provide necessary capacitance for all or a substantial number of devices mounted thereupon. The devices may be interconnected with the power and ground planes either by separate through-hole pins or by surface traces of the type illustrated respectively in FIGURES 2 and 3. With the compound bypass capacitive subassemblies illustrated in FIGURES 11 and 12, the power and ground planes are respectively interconnected in order to assure parallel operation of
10 the capacitor elements in each subassembly.

Because of the very substantial capacitance required for the combined devices, the capacitive PCBs of the present invention are preferably contemplated for operation based on the concept of borrowed capacitance as discussed above wherein the total capacitance of the capacitor elements in any of the capacitive PCBs is less
15 than the total required capacitance for all of its devices. However, as noted above, the invention contemplates that any of the capacitive PCBs may be provided with sufficient capacitance equal to or greater than the cumulative capacitance requirements of the devices. This would of course permit simultaneous operation of all of the devices on the PCB. As noted above, higher capacitive values may be obtained either
20 by an increased number of capacitor elements in the PCB and/or by the use of higher dielectric constant materials in the capacitor elements.

As was also noted above, the conductive foils in the capacitive PCBs are preferably formed with a sufficient mass of copper or conductive material per unit area in order to achieve structural rigidity or self-support and also preferably to permit
25 sufficient electron flow or current flow in accordance with the concept of borrowed capacitance. More specifically, it is contemplated that each of the conductive foils be formed with at least about 0.5 ounces of copper per square foot, that mass corresponding generally to a thickness of about 0.5 mils, more specifically about 0.6-0.7 mils. The thickness of the conductive sheets may be increased, for example,
30 in order to meet larger voltage or current carrying capacities for the power and ground

planes in a particular application. Preferably, each of the conductive sheets includes about 1-2 ounces of copper per square foot, those masses corresponding to thicknesses for the individual sheets in the range of about 1.2-2.4 mils. More preferably, the conductive foils are formed with about one ounce of copper per square foot or having a thickness in the range of about 1.2-1.4 mils to achieve optimum performance of the capacitor laminates. That amount of copper in each of the conductive foils is also selected as a minimum for achieving good structural rigidity within the conductive sheets alone prior to their lamination into the capacitor elements.

The composition and thickness of the dielectric sheets are selected to achieve necessary capacitance, again in accordance with the concept of borrowed capacitance, and also to achieve structural rigidity for the dielectric sheets both prior to and after inclusion within the compound capacitive subassembly.

The present invention preferably contemplates the use of dielectric material having a dielectric constant of at least about 4. A range of dielectric materials widely available in the present state-of-the-art having dielectric constants in the range of about 4-5. Furthermore, it is possible to formulate dielectric compositions, for example, from ceramic filled epoxies, with dielectric constants ranging up toward 10 for example. Thus, the present invention preferably contemplates use of a material with a dielectric constant of at least about 4, more preferably within a range of about 4-5 and most preferably about 4.7, at least for the specific composition contemplated in the preferred embodiment. However, much higher capacitances are also contemplated, as discussed above.

A preferred dielectric constant can be achieved by combinations of a woven component and a resin component combined together to form the necessary combination of dielectric constant and structural rigidity. The woven component may include polymers such as polytetrafluoroethylene (available under the trade names TEFLON and GORETEX) and epoxies. However, the woven components are preferably formed from glass which may be of a quartz variety but is preferably silica, the glass being formed in threads which are then woven together to form sheets filled or impregnated with a selected resin. The resins are commonly selected for fire

retardant characteristics and may include materials such as cyanate esters, polyimides, kapton materials and other known dielectric materials. However, the resin is preferably an epoxy, again in order to take advantage of the existing state-of-the-art regarding use of such resins in PCB manufacture.

5 A dielectric sheet formed from a single woven layer of glass and about 70.0% by weight resin has the preferred dielectric constant of 4.7 as noted above while also exhibiting good structural rigidity at a thickness of about 1.5 mils.

10 The thickness of the dielectric material in the present invention is selected not only to achieve the desired capacitance but also to assure electrical integrity, particularly the prevention of shorts developing between the conductive foils in the capacitor elements. Common practice contemplates treatment of the surfaces of the conductive sheets adjacent the dielectric sheet in order to enhance adhesion within the capacitor elements. Such adhesion is necessary not only for structural integrity but also to assure proper electrical performance. Typically adjacent surfaces of the
15 conductive foils are treated by deposition in zinc or zinc and copper (a brass alloy), usually by plating, in order to form roughened surfaces in a manner well known to those skilled in the PCB art. These roughened surfaces provide "tooth" to enhance mechanical bonding to the dielectric material.

20 Another aspect of the invention is noted with respect to characteristics of the conductive foils. In accordance with standard practice, each of the conductive foils commonly has a matte or tooth side and a barrel or smooth side. Surface variations of the tooth side of the conductive foils is substantially greater than for the opposite smooth side. Such conductive foils are commercially supplied by a number of sources including Gould Electronics and Texas Instruments. Conductive foils
25 formed from copper are available from Gould under the trade name "JTC" FOIL as described in Gould Bulletin 88401 published by Gould, Inc., Eastlake, Ohio in March 1989. Other foils available from Gould include those available under the trade names LOW PROFILE "JTC" FOIL and "TC/TC" DOUBLE TREATED COPPER FOIL and described respectively in Bulletin 88406 and Bulletin 88405, both published in March
30 1989 by Gould, Inc.

In the capacitor elements of the present invention, the greater surface differential for the rough side of the foil is generally excessive for preferred dimensions of dielectric as noted above. This is a consideration in the present invention since, for certain of the conductive foils, both surfaces of those foils are employed in different capacitor elements. In order to assure "capacitive integrity", that is, absence of shorts, *etc.*, the present invention contemplates a number of different approaches for overcoming this problem.

Initially, the thickness of the dielectric sheets may be increased adjacent the rough sides of the conductive foils in order to assure adequate spacing between all surface portions of opposing conductive foils. Alternatively, the surface variations for the rough side of the foil may be reduced, for example by further calendaring or scrubbing. Generally, a calendaring operation as contemplated for compacting ductile material of the foil in order to reduce surface variations on the rough side thereof. In a scrubbing or abrading operation, some of the conductive foil material would be removed on the rough side again for the purpose of reducing surface variations thereon. The use of a scrubbing or abrading technique might require a somewhat thicker conductive foil if excessive amounts of material are to be removed.

Yet another approach in this regard is to coat the rough side of the conductive foil, for example with oxide, again for the purpose of reducing surface variations. In this regard, it is also noted that both surfaces of the conductive foils are preferably surface treated in a generally conventional manner in order to assure adhesion to adjacent layers, in the case of the present invention, the dielectric sheets.

In any event, the problem of different surface variations on opposite sides of the conductive foil can be minimized and/or eliminated by one or more of the above techniques.

Accordingly, there have been described above a variety of methods for *in situ* formation of capacitive elements within PCBs during a final lamination step.

Modifications and variations in addition to those described above for the various embodiments of the invention will be apparent to those skilled in the art.

Accordingly, the scope of the present invention is defined only by the following appended claims which are also set forth as further examples of the invention.

WHAT IS CLAIMED IS:

1. A printed circuit board (PCB) having an internal capacitor to provide capacitance for a plurality of devices to be mounted or formed on the PCB, the internal capacitor comprising two conductive foils and one intermediate dielectric sheet, the conductive foils and dielectric sheet each having dimensions similar to those of the PCB for forming layers therein, the dielectric sheet including spacer material extending throughout the dielectric sheet for uniformly maintaining its thickness and dielectric material developing a uniform dielectric constant therein, the PCB being subjected to a final lamination step with the spacer material and dielectric material of the dielectric sheet maintaining the uniform thickness and uniform dielectric constant of the internal capacitor in the PCB.
2. The PCB of Claim 1 wherein the spacer material is intimately and uniformly intermixed with the dielectric material in order to maintain the uniform thickness and uniform dielectric constant of the dielectric sheet during and following the final lamination step forming the PCB.
3. The PCB of Claim 2 wherein the spacer material is finely divided fiberglass arranged uniformly and multi-directionally throughout the dielectric sheet.
4. The PCB of Claim 2 wherein the dielectric sheet has a uniform thickness of at least about 0.5 mils.
5. The PCB of Claim 2 wherein the dielectric sheet has selected values of thickness and dielectric constant for providing each individual device with a capacitive value by a portion of the internal capacitor to which the individual device is proportional and by borrowed capacitance from other portions of the internal capacitor to which other devices are proportional, the capacitive function of the internal capacitor being dependent upon random firing or operation of the devices, the conductive foils having minimum conductivity to permit adequate current flow necessary to provide each individual device with sufficient borrowed capacitance for its proper operation.

6. The PCB of Claim 2 formed by an *in situ* method wherein the dielectric sheet is initially uncured, the conductive foils being arranged as layers adjacent both sides of the uncured dielectric sheet and between other PCB layers, the conductive foils being laminated to the dielectric sheet and the dielectric sheet cured in the final lamination step for simultaneously forming the PCB and the internal capacitor.

7. The PCB of Claim 6 wherein the conductive foils are bonded to adjacent PCB layers and portions of the conductive foils are etched away prior to their arrangement within the PCB.

8. The PCB of Claim 7 wherein the adjacent PCB layers are also dielectric sheets and further comprising additional conductive foils in the internal capacitor so that compound capacitive elements are respectively formed by the dielectric sheets with at least one of the conductive foils being included in two adjacent capacitive elements.

9. The PCB of Claim 2 wherein the internal capacitor includes at least three conductive foils with a dielectric sheet having a predetermined dielectric constant arranged respectively between each adjacent pair of conductive foils to form multiple capacitor elements, first and third conductive foils numbered from one side of the internal capacitor being connected together, whereby at least one conductive foil is a portion of two capacitor elements, and means for connecting the conductive foils of the multiple capacitor elements with the surface devices.

10. The PCB of Claim 9 further comprising at least four conductive foils with a dielectric sheet having a predetermined dielectric constant arranged respectively between each adjacent pair of conductive foils to form multiple capacitor elements, the odd and even conductive foils numbered from one side of the internal capacitor being respectively connected together, the number of dielectric sheets in the internal capacitor equalling the number of capacitor elements therein and the number of conductive foils in the internal capacitor equalling the number of capacitor elements therein plus one.

11. The PCB of Claim 10 wherein the internal capacitor or a portion thereof is formed as a unitary component prior to its arrangement within the PCB.

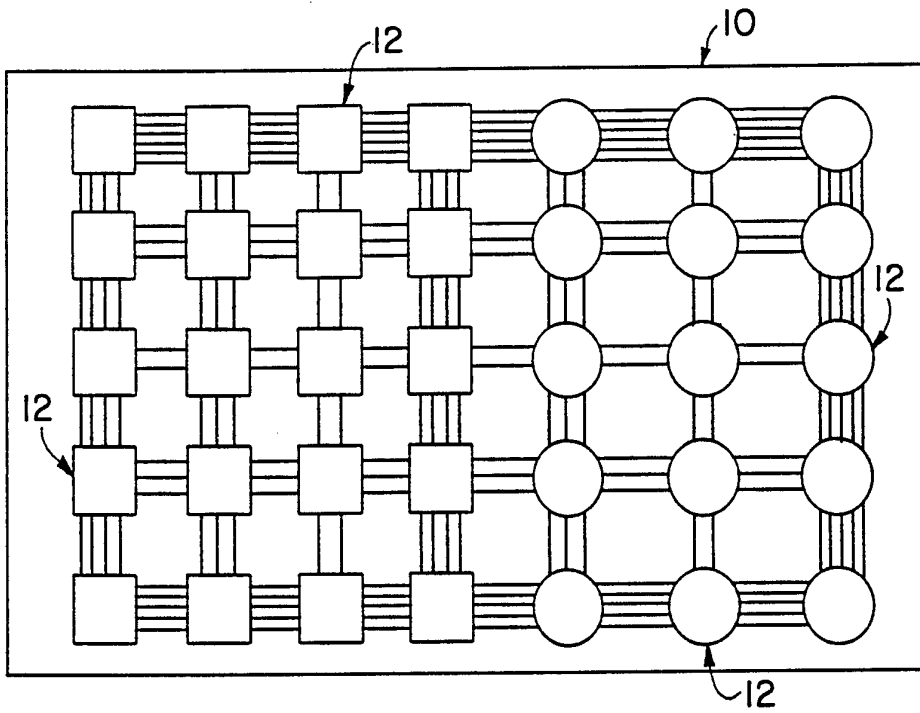


FIG. 1

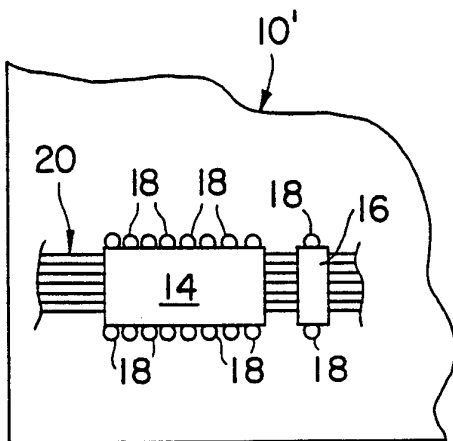


FIG. 2

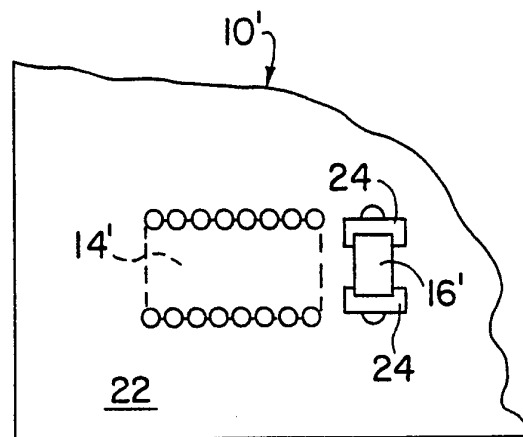


FIG. 3

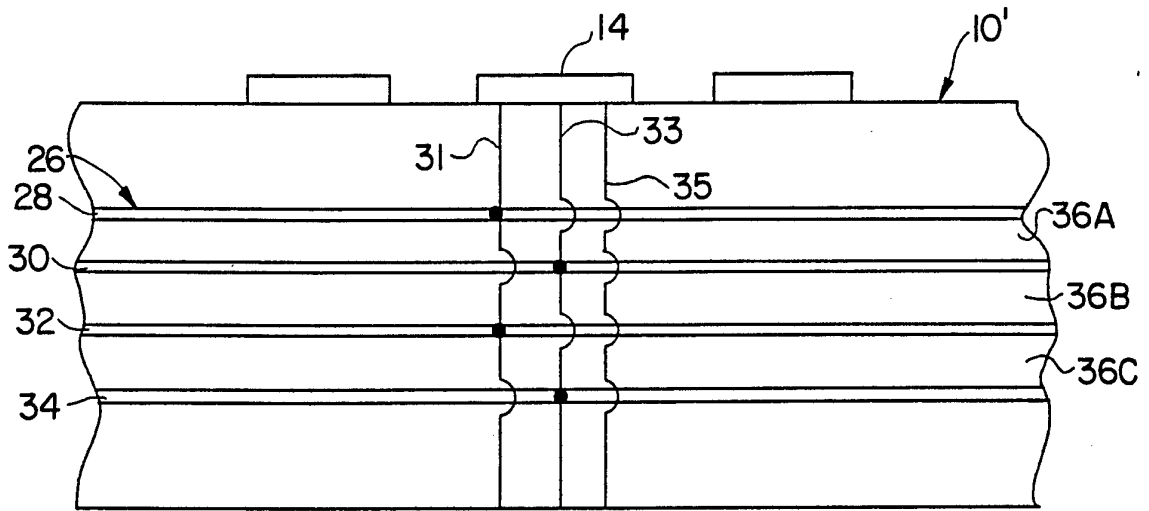


FIG. 4

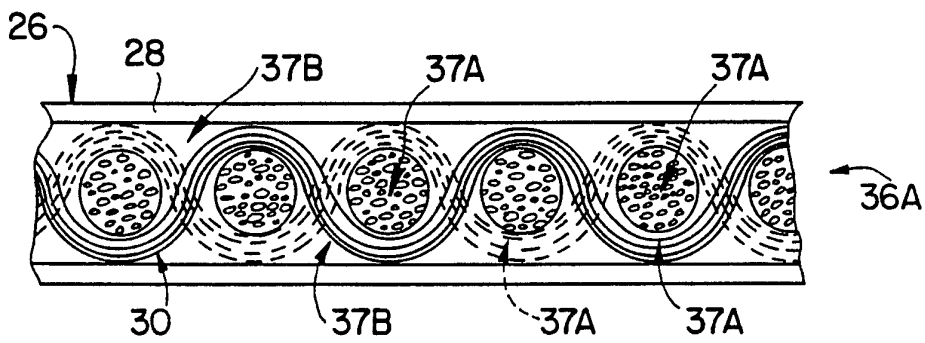


FIG. 5

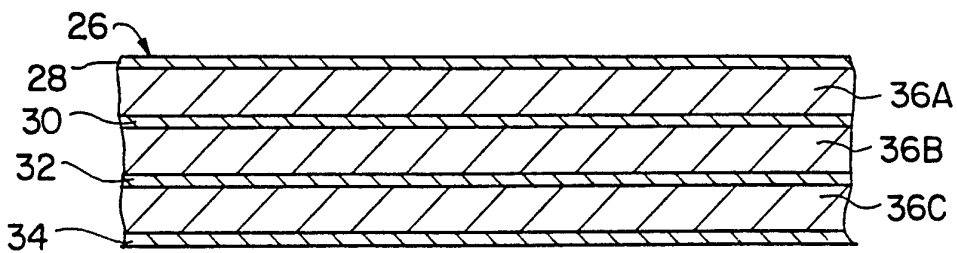


FIG. 6

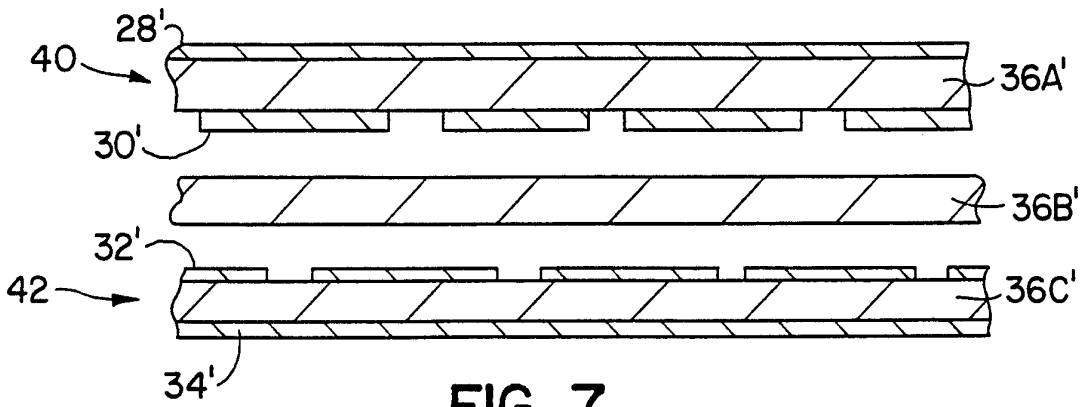


FIG. 7

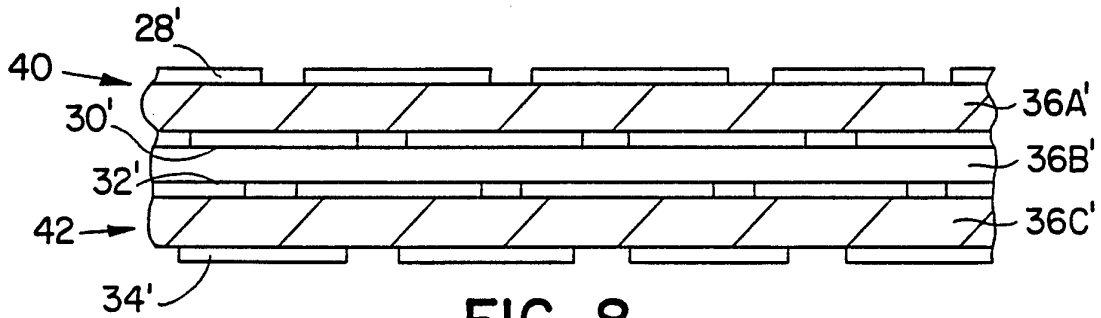


FIG. 8

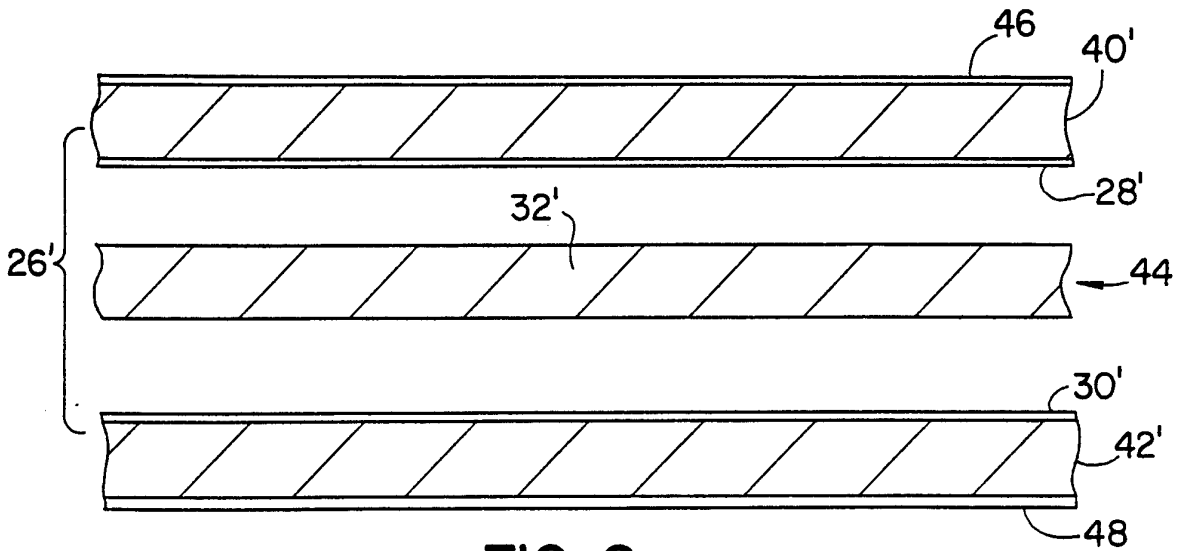


FIG. 9

SUBSTITUTE SHEET

FIG. IOA

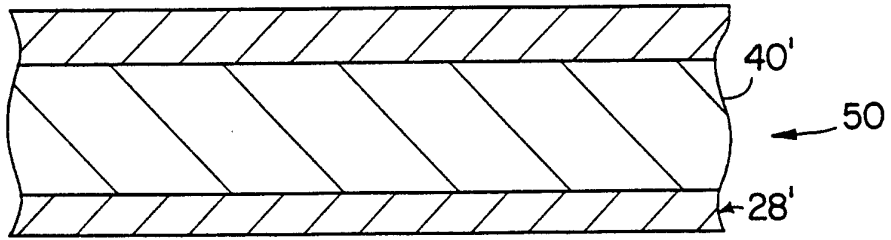


FIG. IOB

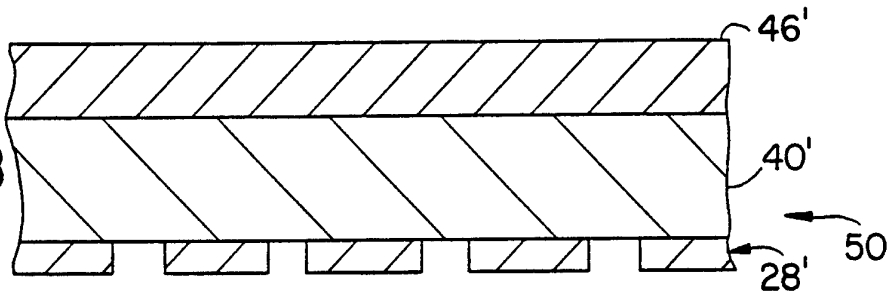


FIG. IOC

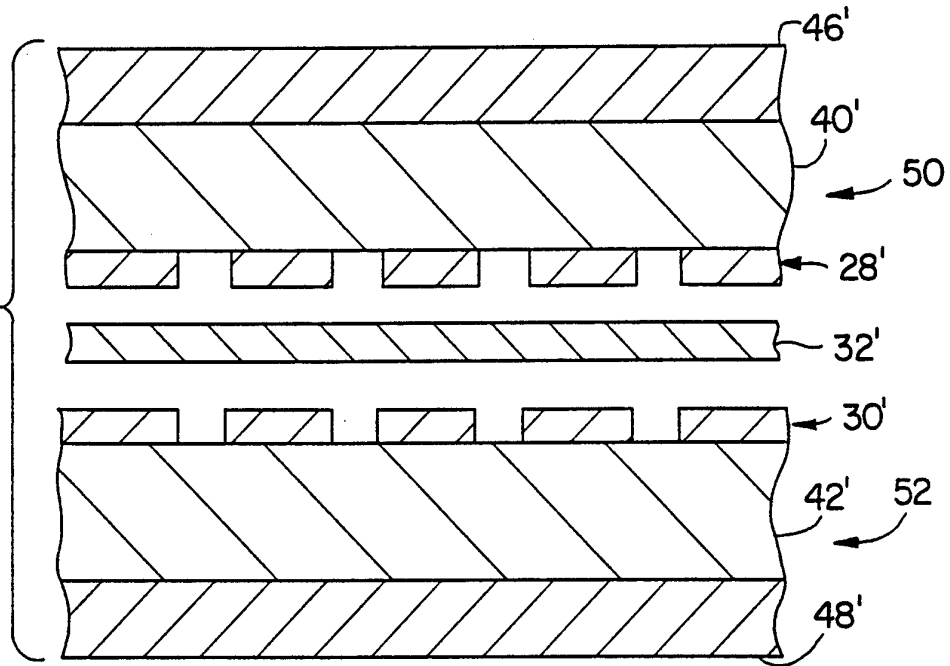
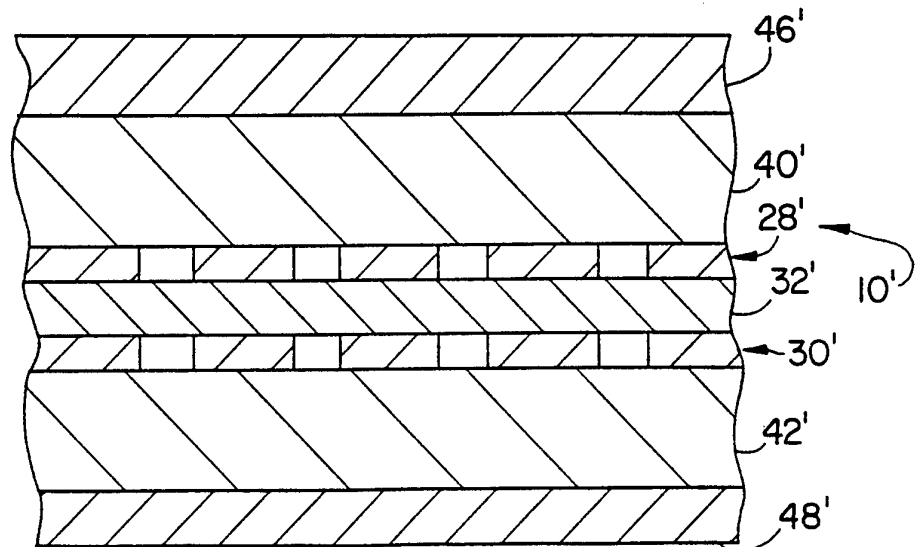


FIG. IOD



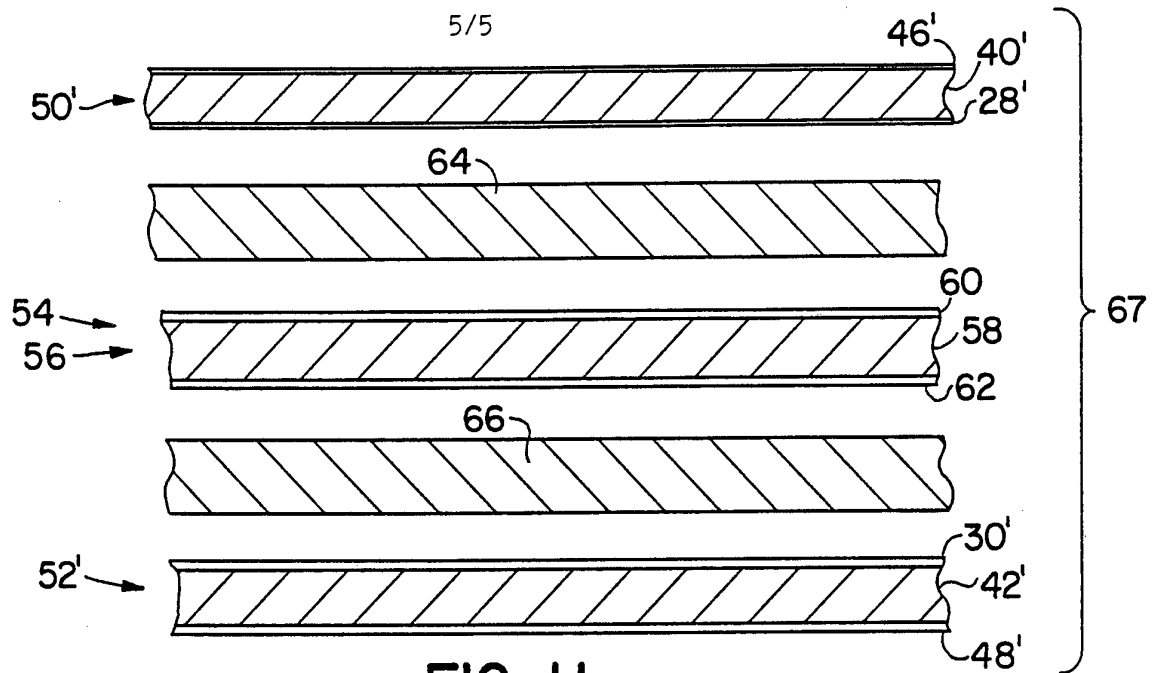


FIG. 11

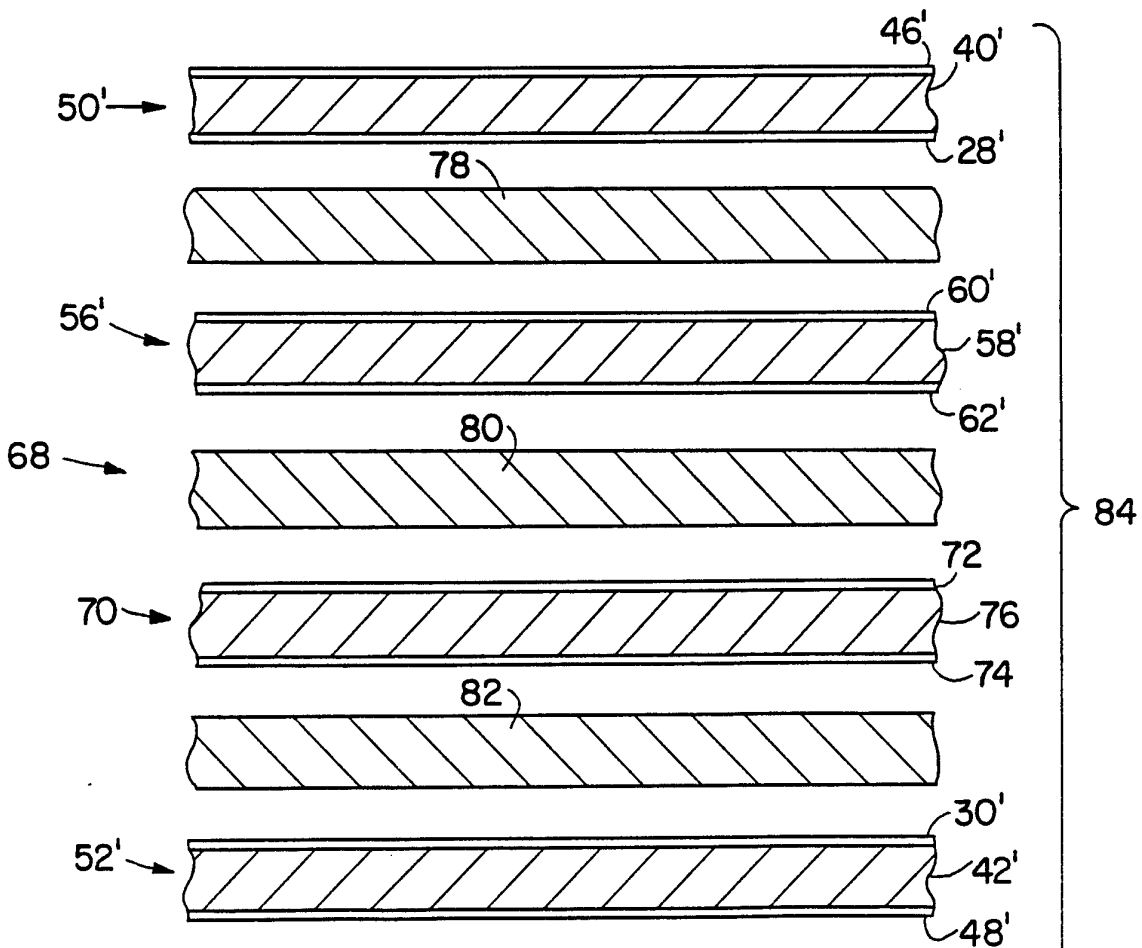


FIG. 12
SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05957

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : Please See Extra Sheet.
US CL : 428/209

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 428/209, 457, 901

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,079,069 (HOWARD ET AL) 07 JANUARY 1992 See entire document.	1-11
E, Y	US, A, 5,162,977 (PAURUS ET AL) 10 NOVEMBER 1992 See entire document.	1-11
Y	US, A, 5,010,641 (SISLER) 30 APRIL 1991 See entire document.	1-11
A	US, A, 4,781,969 (KOBAYASHI ET AL) C1 NOVEMBER 1988. See entire document.	1-11
Y	US, A, 4,775,573 (TUREK) 04 OCTOBER 1988 See abstract, column 4, lines 18-66, column 5, lines 19-46 and column 7, lines 21-65.	1-11

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be part of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	* & * document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

07 DECEMBER 1992

Date of mailing of the international search report

12 JAN 1993

Name and mailing address of the ISA/
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

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J.M. GRAY

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Telephone No. (703) 308-2351

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05957

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,006,397 (DURAND) 09 APRIL 1991 See column 4, line 11 through 7, line 59.	1-11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05957

A. CLASSIFICATION OF SUBJECT MATTER:

IPC (5):

B32B 3/00, 7/00