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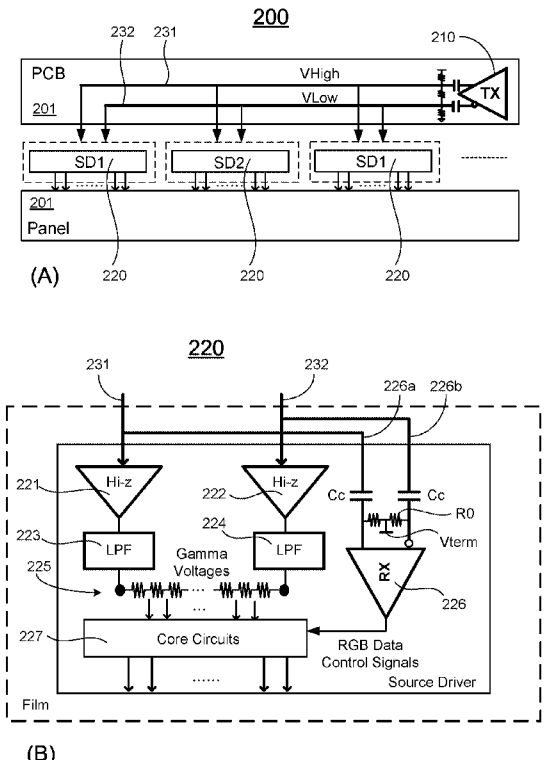



Fig.2

(57) Abstract: In one aspect of the invention, a driving circuit has a PCB, a transmitter disposed on the PCB for providing an input signal, first and second transmission lines disposed on the PCB and electrically coupled to the transmitter for transmitting the input signal, and a plurality of source drivers formed in a COF architecture disposed between the PCB and the display panel. The input signal is an encoded signal including first and second Gamma reference voltages control signals, and image data. The first and second Gamma reference voltages are transmitted by the PLC technology through the first and second transmission lines, respectively. The driving circuit is implemented with differential transmission of the Gamma voltages, the image data and the control signals.

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# DRIVING CIRCUIT AND DISPLAY DEVICE OF USING SAME

## Technical Field

The disclosure relates generally to a display device, and more particularly to a driving circuit that utilizes the power line communication (PLC) technology in the Gamma voltage transmission paths to transmit the Gamma voltages, image data and control signals, and a display device of using the same.

## Background of the Invention

A common architecture of a source driver for a display device is a chip-on-glass (COG) architecture or a chip-on-film (COF) architecture. The former applies a flip chip bonding technology to directly dispose source driver integrated circuits (IC) onto a glass substrate, while the latter applies the flip chip bonding technology to directly dispose source driver IC and active components onto a flexible printed circuit board/film (PCB), which is in turn connected to a substrate.

Compared to the COF architecture, wires of the COG architecture are disposed on the glass substrate, which reduces the assembly area in the PCB. The COG architecture thus has a cost-effective advantage and is usually implemented in small size display panels. However, signals can easily be reflected in the transmission channels in the COG architecture, thereby causing poor signal quality. In addition, re-working may cause damages to the display panel. Further, the IC may be deformed at a high temperature.

For the COF architecture, signal reflections during the signal transmission are relatively small, and further, the transmitted signals have better quality. In addition, display panel damages due to bonding defects can be avoided. The COF architecture is more suited for large-size, high-resolution displays. However, because a great number of wires needs being laid on the PCB, a relatively large assembly area is required in the PCB. The wires and/or film of the COF architecture may also generate signal noises and causes heating problems.

Therefore, a heretofore unaddressed need exists in the art to address the aforementioned deficiencies and inadequacies.

## Summary of the Invention

In one aspect, the invention relates to a driving circuit for driving a display device having a display panel. In one embodiment, the driving circuit has a printed circuit board (PCB), a transmitter disposed on the PCB for providing an input signal comprising first and second

Gamma reference voltages, VHigh and VLow, control signals, and image data, first and second transmission lines disposed on the PCB and electrically coupled to the transmitter for transmitting the input signal, wherein the first and second Gamma reference voltages are transmitted through the first and second transmission lines, respectively, and a plurality of source drivers formed in a chip-on-film (COF) architecture between the PCB and the display panel.

Each source driver comprises first and second Hi-z components electrically coupled to the first and second transmission lines, respectively, for preventing voltage drops of the input signal, first and second low pass filters electrically coupled to the first and second Hi-z components, respectively, for removing high frequency components of the input signal and outputting the first and second Gamma reference voltages, a plurality of resistors electrically coupled in series between the first and second low pass filters, for generating a plurality of Gamma voltages, a receiver having first and second inputs electrically coupled to the first and second transmission lines, respectively, for removing DC components of the input signal and outputting the image data and the control signals, and core circuits electrically coupled to the plurality of resistors and the receiver for generating gray-scale voltages responsive to the image data for driving corresponding data lines of the display panel.

In one embodiment, the first and second Gamma reference voltages are transmitted by the power-line communication technology to the first and second transmission lines.

In one embodiment, the image data and the control signals are transmitted through a high pass filter of the transmitter to the first and second transmission lines.

In one embodiment, each source driver further comprises a pair of capacitors, each capacitor electrically coupled between a respective transmission line and a respective input of the receiver, for removing DC component of the input signal and passing AC component of the input signal, a terminal supply voltage, Vterm, and one or more resistors electrically coupled between the terminal supply voltage Vterm and the first and second inputs of the receiver, for setting a voltage on receiver side of the pair of capacitors.

In one embodiment, each source driver further comprises a pre-charging circuit configured such that when the most significant bit (MSB) of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, pre-charging to the data lines starts for a pre-charge period.

In one embodiment, power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

In one embodiment, the voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

$$(½)*VHigh < VH1 < VHigh, \text{ and}$$

$$VLigh < VL1 < (½)*VHigh.$$

In one embodiment, VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

In one embodiment, the pre-charging period is substantially coincident with a high-z time of the control signal STB.

In one embodiment, when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

In another aspect, the invention relates to a driving circuit for driving a display device having a display panel. In one embodiment, the driving circuit includes a PCB, a transmitter disposed on the PCB for providing an input signal comprising a first Gamma reference voltage and control signals, first and second transmission lines disposed on the PCB and electrically coupled to the transmitter for transmitting the input signal, wherein the first Gamma reference voltage is transmitted through the first transmission line, and wherein the second transmission line is electrically coupled to ground, and a plurality of source drivers formed in a COF architecture between the PCB and the display panel.

Each source driver has first and second Hi-z components electrically coupled to the first and second transmission lines, respectively, for preventing voltage drops of the input signal, and outputting the first and second Gamma reference voltages, a plurality of resistors electrically coupled in series between the first and second low pass filters, for generating a plurality of Gamma voltages, a comparator having first and second inputs electrically coupled to the first transmission line and a reference voltage Vref, respectively, for outputting the control signals, and core circuits electrically coupled between the plurality of resistors and the comparator for generating gray-scale voltages for driving corresponding data lines of the display panel.

In one embodiment, the first and second Gamma reference voltages are transmitted by the power-line communication technology to the first and second transmission lines.

In one embodiment, the reference voltage Vref is provided externally.

In one embodiment, each source driver further comprises a pre-charging circuit configured such that when the MSB of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, pre-charging to the data lines starts for a pre-charge period.

In one embodiment, power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

In one embodiment, the voltages VH1 and VL1 are designed to respectively satisfy the

relationships of:

$$(½)*VHigh < VH1 < VHigh, \text{ and}$$

$$VLigh < VL1 < (½)*VHigh.$$

In one embodiment, VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

In one embodiment, the pre-charging period is substantially coincident with a high-z time of the control signal STB.

In one embodiment, when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

In another aspect, the invention relates to a method for driving a display device having a plurality of source drivers formed in a COF architecture. In one embodiment, the method includes the steps of generating first and second reference Gamma voltages of high-potential and low-potential supply, VHigh and VLow, wherein VHigh and VLow are corresponding to a highest gray-scale voltage and a lowest gray-scale supply voltage, respectively, transmitting the Gamma voltages, image data and control signals through first and second transmission lines by the power-line communication technology to the plurality of source drivers, maintaining the potential levels of the Gamma voltages by operational-amplifiers (OP) embedded in each source driver so as to prevent Gamma voltage drops, selecting Gamma voltages provided by a plurality of resistors connected in series between a highest gray-scale voltage and a lowest gray-scale supply voltage, removing Gamma amp offset voltages by Gamma switches of each source driver, pre-charging the data lines by the half-voltage technique so as to prevent thermal noises generated by the COF source drivers, and generating gray-scale voltages for channel outputs from core circuits of each source driver to a display panel of the display device.

In one embodiment, the step of selecting Gamma voltages is performed with a plurality of Gamma voltage selectors.

In one embodiment, when the MSB of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, the pre-charging to the data lines starts for a pre-charge period.

In one embodiment, the pre-charging period is substantially coincident with a high-z time of the control signal STB.

In one embodiment, when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

In one embodiment, power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

In one embodiment, the voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

$$(½)*VHigh < VH1 < VHigh, \text{ and}$$

$$VLigh < VL1 < (½)*VHigh.$$

In one embodiment, VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

These and other aspects of the present invention will become apparent from the following description of the preferred embodiment taken in conjunction with the following drawings, although variations and modifications therein may be effected without departing from the spirit and scope of the novel concepts of the disclosure.

**Brief Description of the Drawings**

The accompanying drawings illustrate one or more embodiments of the invention and together with the written description, serve to explain the principles of the invention. Wherever possible, the same reference numbers are used throughout the drawings to refer to the same or like elements of an embodiment, and wherein:

FIG. 1 shows schematically a TX and RX architecture utilizing the power line communication (PLC) technology to transmit image (RGB) data, Gamma voltages and control signals according to one embodiment of the present invention;

FIG. 2 shows schematically a COF architecture of a driving circuit for a display device that utilizes the PLC technology to transmit RGB data, Gamma voltages and control signals according to one embodiment of the present invention, (A) the driving circuit, and (B) a source driver;

FIG. 3 shows schematically the driving circuit as shown in FIG. 1;

FIG. 4 shows signals at nodes (a), (b), (c) and (d) of the driving circuit of FIG. 3;

FIG. 5 shows schematically a COF architecture of a driving circuit for a display device that utilizes the PLC technology to transmit RGB data, Gamma voltages and control signals, according to another embodiment of the present invention, (A) the driving circuit, and (B) a source driver, (C) a comparator, and (D) a waveform of the control signal;

FIG. 6 shows schematically waveforms of input signals and output signals of the driving circuit shown in FIG. 5;

FIG. 7 shows schematically a driving circuit having a pre-charging function according to another embodiment of the present invention;

FIG. 8 shows schematically waveforms of pre-charging signals according to another

embodiment of the present invention;

FIG. 9 shows schematically waveforms of pre-charging signals according to another embodiment of the present invention;

FIG. 10 shows schematically a flowchart of a method for driving a display device according to another embodiment of the present invention; and

FIG. 11 shows schematically display panel architecture according to another embodiment of the present invention.

**Detailed Description of the Invention**

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

The terms used in this specification generally have their ordinary meanings in the art, within the context of the invention, and in the specific context where each term is used. Certain terms that are used to describe the invention are discussed below, or elsewhere in the specification, to provide additional guidance to the practitioner regarding the description of the invention. For convenience, certain terms may be highlighted, for example using italics and/or quotation marks. The use of highlighting has no influence on the scope and meaning of a term; the scope and meaning of a term is the same, in the same context, whether or not it is highlighted. It will be appreciated that same thing can be said in more than one way. Consequently, alternative language and synonyms may be used for any one or more of the terms discussed herein, nor is any special significance to be placed upon whether or not a term is elaborated or discussed herein. Synonyms for certain terms are provided. A recital of one or more synonyms does not exclude the use of other synonyms. The use of examples anywhere in this specification including examples of any terms discussed herein is illustrative only, and in no way limits the scope and meaning of the invention or of any exemplified term. Likewise, the invention is not limited to various embodiments given in this specification.

It will be understood that when an element is referred to as being “on” another element, it can be directly on the other element or intervening elements may be present therebetween. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising", or "includes" and/or "including" or "has" and/or "having" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top", may be used herein to describe one element's relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in one of the figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompasses both an orientation of "lower" and "upper", depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

As used herein, "around", "about", "substantially" or "approximately" shall generally mean within 20 percent, preferably within 10 percent, and more preferably within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term

"around", "about", "substantially" or "approximately" can be inferred if not expressly stated.

The description will be made as to the embodiments of the present invention in conjunction with the accompanying drawings in FIGS. 1-11. In accordance with the purposes of this invention, as embodied and broadly described herein, this invention, in one aspect, relates to a driving circuit that utilizes the power line communication (PLC) technology in the Gamma voltage transmission lines (paths) to transmit the Gamma voltages, image (RGB) data and control signals, and a display device of using the same. More specifically, the image data and the control signals are encoded by differential or single-end transmission methods, to the Gamma voltages. The encoded image data and control signals and the Gamma voltages are transmitted through the Gamma voltage transmission lines (paths). Accordingly, the wires needed for the signal transmission on the PCB are reduced, and thus, the size of the PCB can be reduced.

Referring to FIG. 1, TX and RX architecture 100 of a driving circuit of a display device, which utilizes the PLC technology to transmit image (RGB) data, Gamma voltages and control signals, is shown schematically according to one embodiment of the present invention. The TX and RX architecture 100 includes a transmitter 110, a receiver 120 and transmission lines (paths) 130 electrically connected between the transmitter 110 and the receiver 120. The transmission lines 130 are corresponding to the Gamma voltage (power) transmission paths. According to the invention, the RGB (image) data, the control signals and the Gamma voltages are encoded at the transmitter 110 by either a differential transmission method or a single-end transmission method. The encoded RGB (image) data, control signals and Gamma voltages are transmitted through the transmission lines 130 by the PLC technology. At the receiver 120, the received encoded signal of the RGB data, the control signals and the Gamma voltages through the transmission lines 130 is decoded, which are then output to a display panel of the display device.

Referring to FIG. 2, a COF architecture 200 (FIG. 2A) of a driving circuit for a display panel and a source driver 210 (FIG. 2B) utilized in the COF architecture 200 of the driving circuit are shown schematically according to one embodiment of the present invention.

The driving circuit 200 has a printed circuit board (PCB) 201, a transmitter 210 disposed on the PCB 201 for providing an input signal, first and second transmission lines 231 and 231 disposed on the PCB 201 and electrically coupled to the transmitter 210 for transmitting the input signal, and a plurality of source drivers 220 formed in a COF architecture disposed between the PCB 201 and the display panel 202. The input signal is an encoded signal including first and second Gamma reference voltages, VHigh and VLow, control signals, and image data. The driving circuit 200 is implemented with differential transmission of the Gamma voltages, the image data and the control signals. The first and second Gamma reference voltages VHigh

and VLow are transmitted by the PLC technology through the first and second transmission lines 231 and 232, respectively. In one embodiment, the image data and the control signals are transmitted through a high pass filter (not shown) of the transmitter 210 to the first and second transmission lines 231 and 232.

As shown in FIG. 2B, each source driver 220 comprises first and second Hi-z components 221 and 222 electrically coupled to the first and second transmission lines 231 and 232, respectively, first and second low pass filters 223 and 224 electrically coupled to the first and second Hi-z components 221 and 222, respectively, a plurality of resistors 225 electrically coupled in series between the first and second low pass filters 223 and 224, a receiver 226 having first and second inputs 226a and 226b electrically coupled to the first and second transmission lines 231 and 232, respectively, and core circuits 227 electrically coupled to the plurality of resistors 225 and the receiver 226.

The Gamma reference voltages VHigh and VLow are transmitted to each source driver 220 through embedded first and second Hi-z components 221 and 222 that are adapted for preventing voltage drops of the input signal because of the length difference between the Gamma voltage transmission paths, so as to prevent Mura phenomena from occurring. Generally, the transmission paths are designed as short as possible. The first and second low pass filters 223 and 224 are adapted for removing high frequency components of the input signal so as to provide the first and second reference voltages for the Gamma voltages. For example, in one embodiment, for a 200Hz and 16V input signal, after passing the LPF, the output is about 15.8V, while for a 200kHz and 16V input signal, after passing the LPF, the output is about 126mV. The high frequency signals are filtered out significantly. The plurality of resistors 225 is adapted for generating a plurality of Gamma voltages. The receiver 226 is adapted for removing DC components of the input signal and outputting the image data and the control signals. The core circuits 227 are adapted for generating gray-scale voltages responsive to the image data for driving corresponding data lines of the display panel 202.

In addition, each source driver 220 may further include a pair of capacitors, Cc, each capacitor Cc electrically coupled between a respective transmission line 231 (232) and a respective input 226a (226b) of the receiver 226, for removing DC component of the input signal and passing AC component of the input signal, a terminal supply voltage, Vterm, and one or more resistors, R0, electrically coupled between the terminal supply voltage Vterm and the first and second inputs 226a and 226b of the receiver 226, for setting a voltage on receiver side of the pair of capacitors Cc. The capacitor Cc coupled before RX removes the DC component of the signal, while the AC voltage swing is passed on. The resistor R0 to the terminal voltage Vterm coupled before RX represents the biasing structure used to set the voltage on the receiver

side of the ac-coupling capacitor Cc. The coupling capacitors Cc prevent DC current from flowing from the termination voltage Vterm through CML driver. The common-mode voltage can be adjusted by the termination voltage Vterm.

FIG. 3 shows schematically the driving circuit as shown in FIG. 1. FIG. 4 shows signal outputs at nodes (a), (b), (c) and (d) of the driving circuit of FIG. 3. Clearly, the signal output at the node (c) is corresponding to the RGB data and the control signal, while the signal output at the node (d) is the DC Gamma reference voltage.

Referring to FIG. 5, a driving circuit 500 for driving a display device having a display panel is schematically shown according to another embodiment of the invention. The driving circuit 500 includes a PCB 501, a transmitter 510 disposed on the PCB 501 for providing an input signal first and second transmission lines 531 and 532 disposed on the PCB 501 and electrically coupled to the transmitter 510 for transmitting the input signal, and a plurality of source drivers 520 formed in a COF architecture between the PCB 501 and the display panel 502. In one embodiment of the invention, the first Gamma reference voltage VHigh and control signals are encoded in the transmitter 510. The first Gamma reference voltage VHigh is transmitted through the first transmission line 531. In addition, the second transmission line 532 is electrically coupled to ground. Thus, the second Gamma reference voltage VLow is a ground voltage, or zero. The driving circuit 500 is corresponding to a single-end control signal transmission.

As shown in FIG. 5B, each source driver 520 has first and second Hi-z components 521 and 522 electrically coupled to the first and second transmission lines 531 and 532, respectively, for preventing voltage drops of the input signal, and outputting the first and second Gamma reference voltages, a plurality of resistors 525 electrically coupled in series between the first and second low pass filters 521 and 522, for generating a plurality of Gamma voltages, a comparator 526 having first and second inputs 526a and 526b electrically coupled to the first transmission line 531 and a reference voltage Vref, respectively, for outputting the control signals, and core circuits 527 electrically coupled between the plurality of resistors 525 and the comparator for generating gray-scale voltages for driving corresponding data lines of the display panel. The first and second Hi-z components 521 and 522 may be embedded in the driver IC and are adapted for preventing the Gamma reference voltage drops. FIGS. 5C and 5D show schematically a circuit diagram of the comparator 526 and the waveform of its output signal, respectively. In this exemplary embodiment, one reference voltage Vref provided externally or internally is required, which is employed as a reference for the comparator 526. In operation, the comparator 526 decodes the control signal from the encoded Gamma reference voltages and the control signal, and then transmits the decoded control signal to the core circuit 527.

FIG. 6 shows schematically waveforms of input signals such as image data, Gamma reference voltages, control signal (STB) and channel output signals of the driving circuit shown in FIG. 5.

In addition, according to the invention, the driving circuit 700 also has an MSB pre-charging function/circuit 750, as shown in FIG. 7 In one embodiment, the MSB pre-charging circuit 750 is configured such that when the MSB of the image data applied to a data line (e.g., $C_{2n+2}$) and the MSB of the image data applied to the immediately prior data line (e.g., $C_{2n+1}$) change from one state to another state (i.e., from "0" to "1", or from "1" to "0"), pre-charging to the data lines starts for a pre-charge period, T. The pre-charging period T is substantially coincident with a high-z time of the control signal STB.

Power of the pre-charging is supplied by internal sources of voltages, VH1 and VL1, which are provided by the Gamma resistor-string 725 of the source driver 720. The voltage sources VH1 and VL1 are designed to respectively satisfy the relationships of:

$$(½)*VHigh < VH1 < VHigh, \text{ and}$$

$$VLigh < VL1 < (½)*VHigh.$$

Preferably, VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

In one embodiment, when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal ST, which are controlled by switches 751 and 752 of the pre-charging circuit 750, as shown in FIG. 7. The polarity of a channel output is generally controlled by a group of switches 760.

FIGS. 8 and 9 show the waveforms of the pre-charging signals. As the MSB inverted, then do pre-charging on STB falling N-clk width, and then out data waveform. As the MSB doesn't inverted, then enlarge STB pulse with N-clk width (by PCE setting), and output data waveform at STB falling.

According to the invention, voltage levels of channel outputs of the source drivers are pre-charged to voltages VH1 and VL1, by using a pre-charging mechanism and two power sources VH1 and VL1 provided by an internal resistor-string for dividing Gamma voltages, thereby, reducing the power consumption and operation temperature of the source driver IC, which solves the problem of heating conduction of the film due to the high temperature of the film in the COF architecture.

Table 1 lists experimental results of temperatures (°C) of the COF drivers with or without pre-charging for H-stripe, sub-checker and one-dot patterns. It is clearly shown that with the pre-charging, the temperature can be reduced from 39.7 °C to 42.5 °C for the pre-charging

period of 1.47 μs, and from 20.2 °C to 24.7 °C for the pre-charging period of 0.47 μs.

Table 1: Temperatures (°C) of pre-charging effect.

| Pattern | | H-stripe | Sub-checker | One-dot |
|---|---|---|---|---|
| | | MSB state charges | | |
| Pre-charging period 1.47 μs | No pre-charging | 145.8 | 133 | 137.1 |
| | Pre-charging | 103.6 | 93.3 | 94.6 |
| | Temperature decrease | 42.2 | 39.7 | 42.5 |
| Pre-charging period 0.47 μs | No pre-charging | 132.5 | 122 | 122.6 |
| | Pre-charging | 112.3 | 97.3 | 100.2 |
| | Temperature decrease | 20.2 | 24.7 | 22.4 |

Referring to FIG. 10, a method 1000 for driving a display device having a plurality of source drivers formed in a COF architecture is shown according to one embodiment of the invention. The method 1000 includes the following steps:

At step 1010, first and second reference Gamma voltages VHigh and VLow of high-potential and low-potential supply are generated or provided from an external power source. The first and second reference Gamma voltages VHigh and VLow are corresponding to a highest gray-scale voltage and a lowest gray-scale supply voltage, respectively.

At step 1020, the Gamma voltages, image data and control signals are transmitted through first and second transmission lines by the power-line communication technology to the plurality of source drivers.

At step 1030, the potential levels of the Gamma voltages are maintained by operational-amplifiers (OP) embedded in each source driver so as to prevent Gamma voltage drops.

At step 1040, Gamma voltages provided by a plurality of resistors connected in series between a highest gray-scale voltage and a lowest gray-scale supply voltage are selected. In one embodiment, the selecting of the Gamma voltages is performed with a plurality of Gamma voltage selectors.

At step 1050, Gamma amp offset voltages are removed by Gamma switches of each source driver.

At step 1060, pre-charging the data lines by the half-voltage technique so as to prevent thermal noises generated by the COF source drivers. The power of the pre-charging is supplied by internal sources of voltages, VH1 and VL1, which are provided by the Gamma resistor-string. The voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

$$(½)*VHigh < VH1 < VHigh, \text{ and}$$

$$VLigh < VL1 < (½)*VHigh.$$

Preferably, VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

In one embodiment, when the MSB of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, the pre-charging to the data lines starts for a pre-charge period. The pre-charging period is substantially coincident with a high-z time of the control signal STB.

Additionally, when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

At step 1070, gray-scale voltages are generated for channel outputs from core circuits of each source driver to a display panel of the display device.

Referring to FIG. 11, display panel architecture 1100 is shown schematically according to another embodiment of the present invention. The display panel architecture 1100 includes a PCB 1101, first and second transmission lines 1104 and 1105 disposed on the PCB 1101 for transmitting the input signal including two Gamma reference voltages, RGB data and control signals, a COF architecture 1103 of source drivers disposed between the PCB 1101 and the display panel 1102. The source drivers include Gamma correct circuit 1110 that has embedded Gamma OPs 1130 electrically coupled to the first and second transmission lines 1104 and 1105 for preventing the Gamma voltage drops, Gamma switches 1120 for cancelling Gamma AMP offset voltages. The source drivers also include source driver circuit 1140 electrically coupled to the Gamma correcting circuit 1110 responsively for generating gray-scale voltages to drive the data lines of the display panel 1102.

Briefly, the invention, among other things, recites a driving circuit for driving a display device, which utilizes the PLC technology in the Gamma voltage transmission lines (paths) to transmit the Gamma voltages, image (RGB) data and control signals. The image data and the control signals are encoded by differential or single-end transmission methods, to the Gamma voltages. The encoded image data and control signals and the Gamma voltages are transmitted through the Gamma voltage transmission lines (paths). Accordingly, the wires needed for the signal transmission on the PCB are reduced, and thus, the size of the PCB can be reduced. In addition, according to the invention, voltage levels of channel outputs of the source drivers are pre-charged to voltages VH1 and VL1, by using a pre-charging mechanism and two power sources VH1 and VL1 provided by an internal resistor-string for dividing Gamma voltages, thereby, reducing the power consumption and operation temperature of the source driver IC, which solves the problem of heating conduction of the film due to the high temperature of the

film in the COF architecture.

The foregoing description of the exemplary embodiments of the invention has been presented only for the purposes of illustration and description and is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching.

The embodiments were chosen and described in order to explain the principles of the invention and their practical application so as to activate others skilled in the art to utilize the invention and various embodiments and with various modifications as are suited to the particular use contemplated. Alternative embodiments will become apparent to those skilled in the art to which the present invention pertains without departing from its spirit and scope. Accordingly, the scope of the present invention is defined by the appended claims rather than the foregoing description and the exemplary embodiments described therein.

**What is claimed is:**

1. A driving circuit for driving a display device having a display panel, comprising:

(a) a printed circuit board (PCB);

(b) a transmitter disposed on the PCB for providing an input signal comprising first and second Gamma reference voltages, VHigh and VLow;

(c) first and second transmission lines disposed on the PCB and electrically coupled to the transmitter for transmitting the input signal, wherein the first and second Gamma reference voltages are transmitted through the first and second transmission lines, respectively; and

(d) a plurality of source drivers formed in a chip-on-film (COF) architecture between the PCB and the display panel, wherein each source driver comprises:

first and second Hi-z components electrically coupled to the first and second transmission lines, respectively, for preventing voltage drops of the input signal.

2. The driving circuit of claim 1, wherein the input signal further comprises control signals, and image data.

3. The driving circuit of claim 2, wherein the image data and the control signals are transmitted through a high pass filter of the transmitter to the first and second transmission lines.

4. The driving circuit of claim 2, wherein each source driver further comprises:

first and second low pass filters electrically coupled to the first and second Hi-z components, respectively, for removing high frequency components of the input signal and outputting the first and second Gamma reference voltages;

a plurality of resistors electrically coupled in series between the first and second low pass filters, for generating a plurality of Gamma voltages;

a receiver having first and second inputs electrically coupled to the first and second transmission lines, respectively, for removing DC components of the input signal and outputting the image data and the control signals; and

core circuits electrically coupled to the plurality of resistors and the receiver for generating gray-scale voltages responsive to the image data for driving corresponding data lines of the display panel.

5. The driving circuit of claim 4, wherein each source driver further comprises:

(a) a pair of capacitors, each capacitor electrically coupled between a respective transmission line and a respective input of the receiver, for removing DC component of the input signal and passing AC component of the input signal;

(b) a terminal supply voltage; and

(c) one or more resistors electrically coupled between the terminal supply voltage and the

first and second inputs of the receiver, for setting a voltage on receiver side of the pair of capacitors.

6. The driving circuit of claim 5, wherein each source driver further comprises a pre-charging circuit configured such that when the most significant bit (MSB) of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, pre-charging to the data lines starts for a pre-charge period.

7. The driving circuit of claim 6, wherein power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

8. The driving circuit of claim 7, wherein the voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

(½)*VHigh < VH1 < VHigh, and

VLigh < VL1 < (½)*VHigh.

9. The driving circuit of claim 8, wherein VH1 = (¾)*VHigh and VL1 = (¼)*VHigh.

10. The driving circuit of claim 6, wherein the pre-charging period is substantially coincident with a high-z time of the control signal STB.

11. The driving circuit of claim 10, wherein when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

12. A driving circuit for driving a display device having a display panel, comprising:

(a) a printed circuit board (PCB);

(b) a transmitter disposed on the PCB for providing an input signal comprising a first Gamma reference voltage;

(c) first and second transmission lines disposed on the PCB and electrically coupled to the transmitter for transmitting the input signal; wherein the first Gamma reference voltage is transmitted through the first transmission line; and

(d) a plurality of source drivers formed in a chip-on-film (COF) architecture between the PCB and the display panel, wherein each source driver comprises:

first and second Hi-z components electrically coupled to the first and second transmission lines, respectively, for preventing voltage drops of the input signal, and outputting the first and second Gamma reference voltages.

13. The driving circuit of claim 12, wherein the input signal further comprises control signals.

14. The driving circuit of claim 12, wherein the second transmission line is electrically

coupled to ground.

15. The driving circuit of claim 14, wherein the first and second Gamma reference voltages are transmitted by the power-line communication technology to the first and second transmission lines.

16. The driving circuit of claim 13, wherein each source driver further comprises:

a plurality of resistors electrically coupled in series between the first and second low pass filters, for generating a plurality of Gamma voltages;

a comparator having first and second inputs electrically coupled to the first transmission line and a reference voltage, respectively, for outputting the control signals; and

core circuits electrically coupled between the plurality of resistors and the comparator for generating gray-scale voltages for driving corresponding data lines of the display panel.

17. The driving circuit of claim 16, wherein each source driver further comprises a pre-charging circuit configured such that when the most significant bit (MSB) of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, pre-charging to the data lines starts for a pre-charge period.

18. The driving circuit of claim 17, wherein power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

19. The driving circuit of claim 18, wherein the voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

$(\frac{1}{2})*VHigh < VH1 < VHigh$, and

$VLigh < VL1 < (\frac{1}{2})*VHigh$.

20. The driving circuit of claim 18, wherein $VH1 = (\frac{3}{4})*VHigh$ and $VL1 = (\frac{1}{4})*VHigh$.

21. The driving circuit of claim 16, wherein the pre-charging period is substantially coincident with a high-z time of the control signal STB.

22. The driving circuit of claim 21, wherein when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

23. A method for driving a display device having a plurality of source drivers formed in a chip-on-film (COF) architecture, comprising the steps of:

(a) generating first and second reference Gamma voltages of high-potential and low-potential supply, VHigh and VLow, wherein VHigh and VLow are corresponding to a highest gray-scale voltage and a lowest gray-scale supply voltage, respectively;

(b) transmitting the Gamma voltages through first and second transmission lines by the

power-line communication technology to the plurality of source drivers;

(c) maintaining the potential levels of the Gamma voltages by operational-amplifiers (OP) embedded in each source driver so as to prevent Gamma voltage drops;

(d) selecting Gamma voltages provided by a plurality of resistors connected in series between a highest gray-scale voltage and a lowest gray-scale supply voltage; and

(e) removing Gamma amp offset voltages by Gamma switches of each source driver.

24. The method of claim 23, further comprising transmitting image data and control signals through first and second transmission lines by the power-line communication technology to the plurality of source drivers.

25. The method of claim 24, further comprising:

(a) pre-charging the data lines by the half-voltage technique so as to prevent thermal noises generated by the COF source drivers; and

(b) generating gray-scale voltages for channel outputs from core circuits of each source driver to a display panel of the display device.

26. The method of claim 23, wherein the step of selecting Gamma voltages is performed with a plurality of Gamma voltage selectors.

27. The method of claim 23, wherein when the most significant bit (MSB) of the image data applied to a data line and the MSB of the image data applied to the immediately prior data line change from one state to another state, the pre-charging to the data lines starts for a pre-charge period.

28. The method of claim 27, wherein the pre-charging period is substantially coincident with a high-z time of the control signal STB.

29. The method of claim 28, wherein when a channel output to a data line has a positive polarity, the data line is pre-charged with VH1 in the high-z time of the control signal STB, and when a channel output to a data line has a negative polarity, the data line is pre-charged with VL1 in the high-z time of the control signal STB.

30. The method of claim 29, wherein power of the pre-charging is supplied by internal voltages, VH1 and VL1, provided by the plurality of resistors.

31. The method of claim 30, wherein the voltages VH1 and VL1 are designed to respectively satisfy the relationships of:

$(\frac{1}{2})*VHigh < VH1 < VHigh$, and

$VLigh < VL1 < (\frac{1}{2})*VHigh$.

32. The method of claim 31, wherein $VH1 = (\frac{3}{4})*VHigh$ and $VL1 = (\frac{1}{4})*VHigh$.

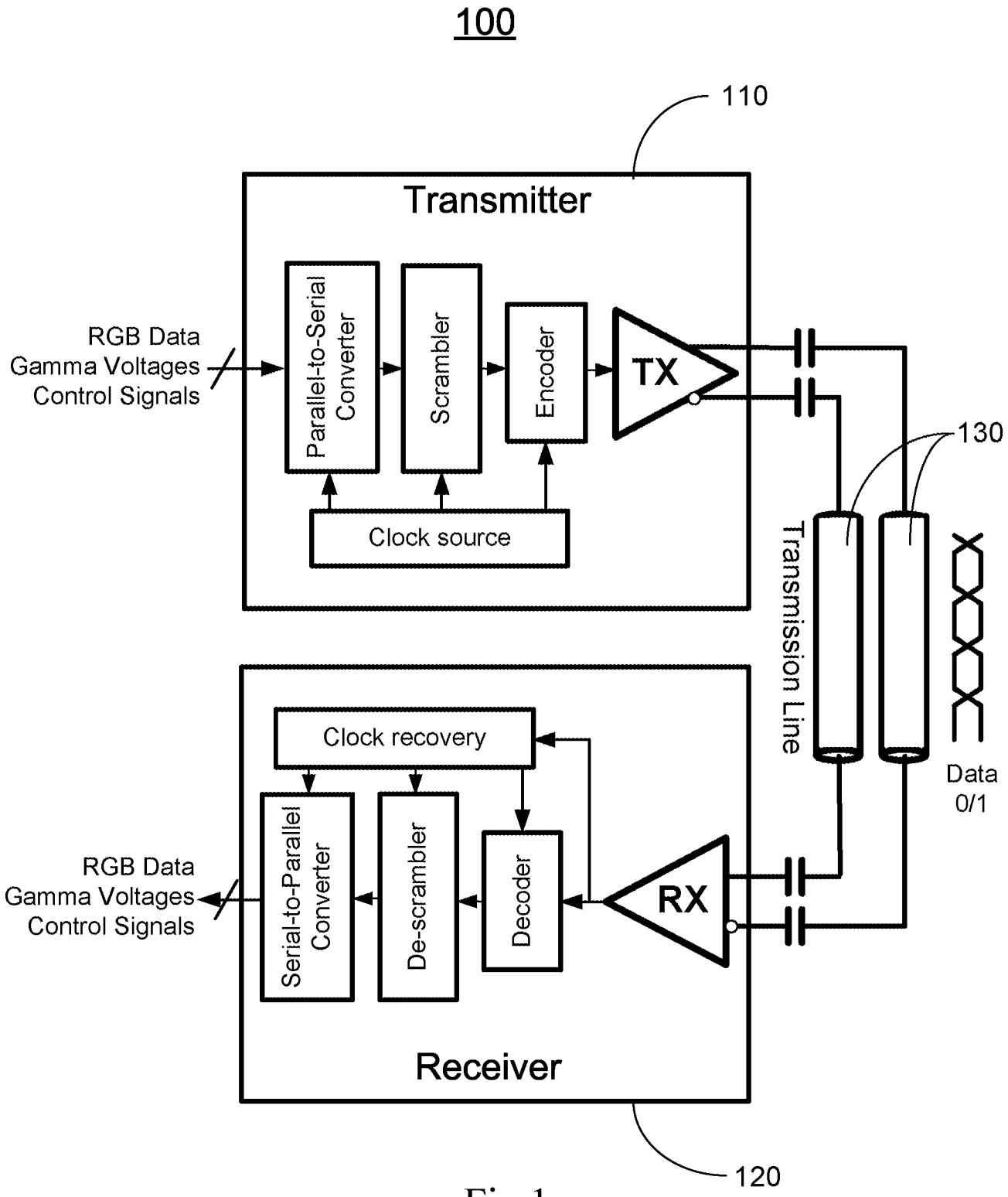
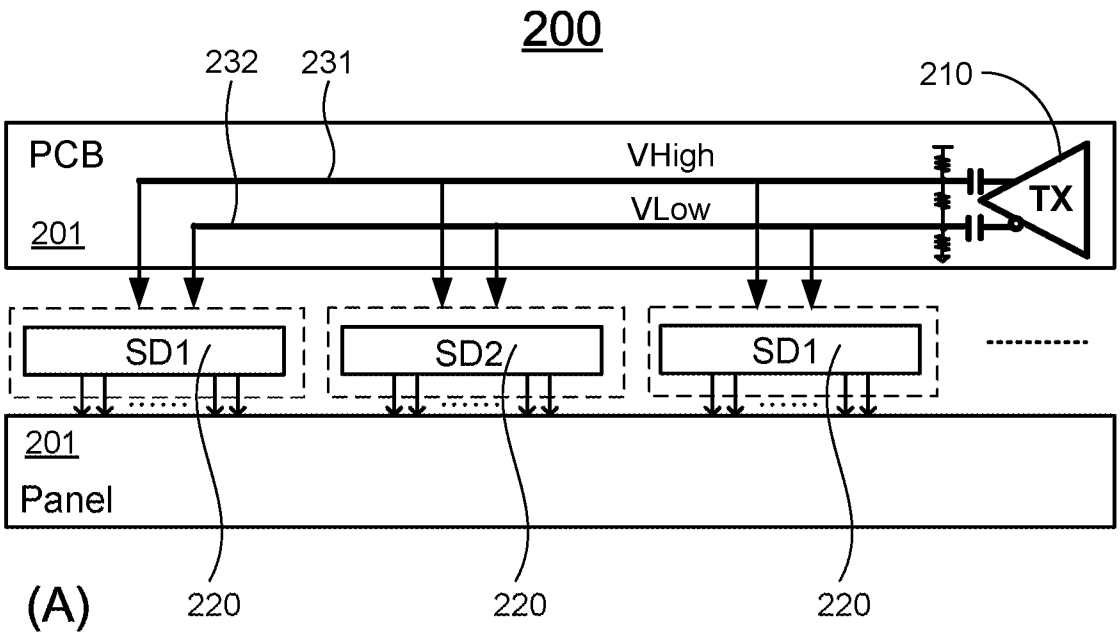

100
110
Transmitter
RGB Data
Gamma Voltages
Control Signals
Parallel-to-Serial Converter
Scrambler
Encoder
TX
Clock source
130
Transmission Line
Data
0/1
Clock recovery
Serial-to-Parallel Converter
De-scrambler
Decoder
RX
RGB Data
Gamma Voltages
Control Signals
Receiver
120

Fig.1


200
232
231
210
PCB
VHigh
VLow
TX
201
SD1
SD2
SD1
201
Panel
(A)
220
220
220

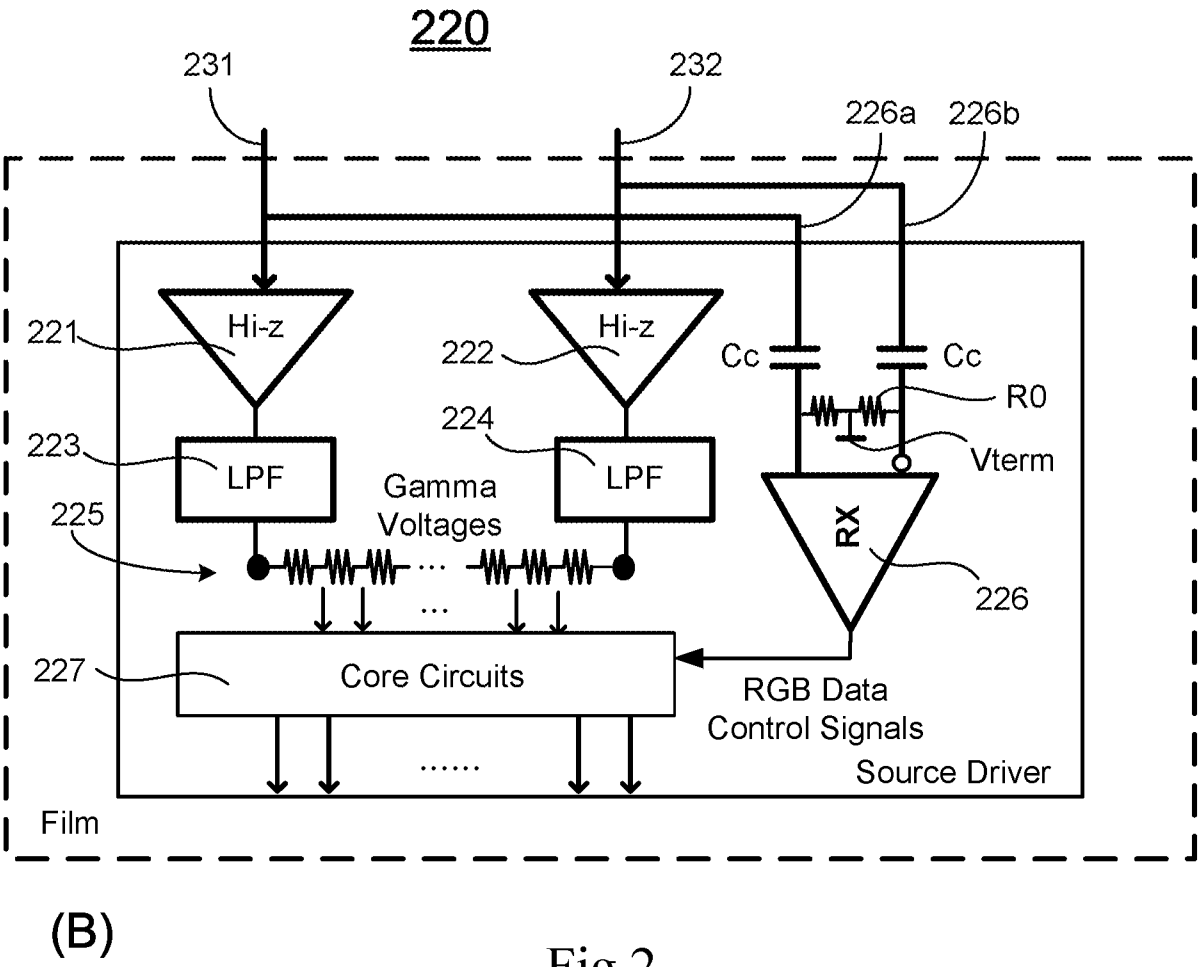

220
231
232
226a
226b
221
Hi-z
222
Hi-z
Cc
Cc
R0
224
223
LPF
LPF
Vterm
Gamma
Voltages
225
RX
226
227
Core Circuits
RGB Data
Control Signals
Source Driver
Film
(B)

Fig.2

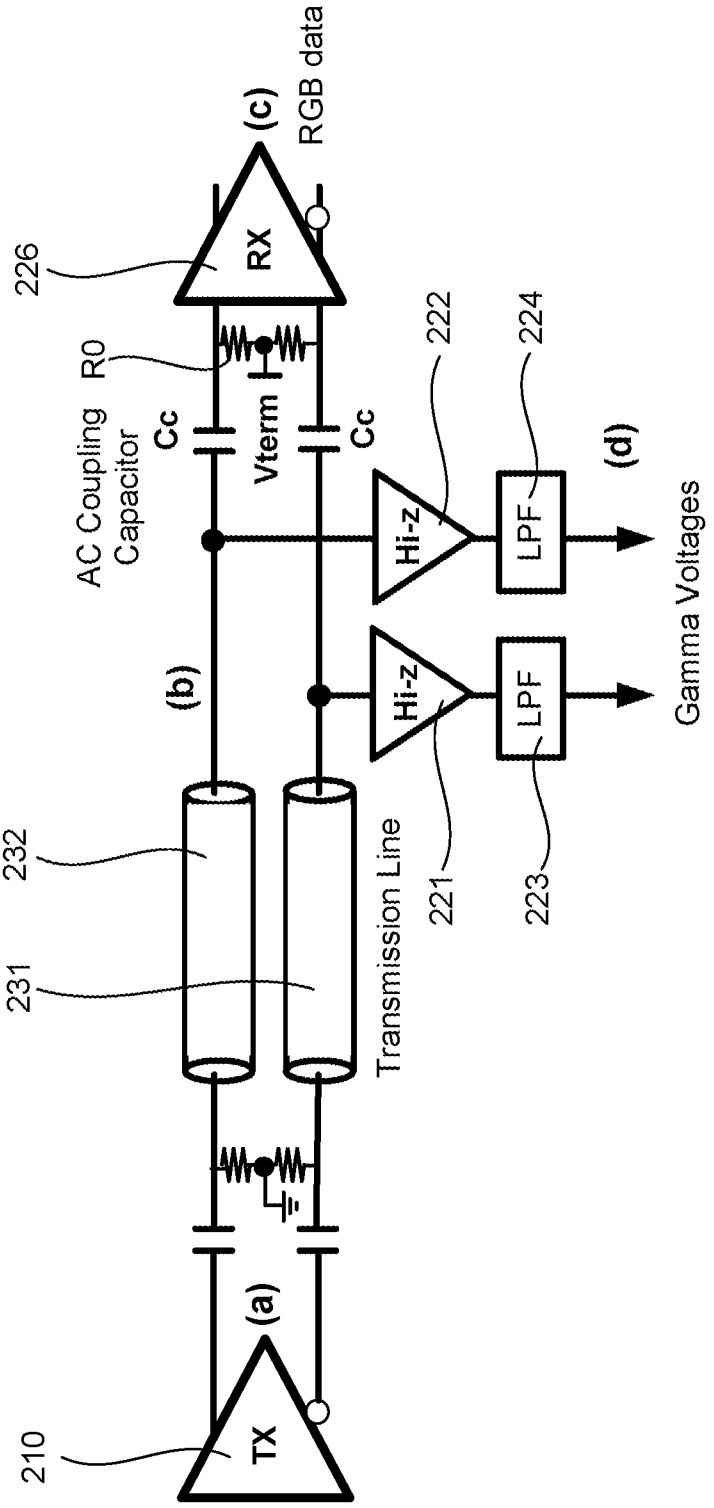

RGB data
(c)
RX
226
R0
Vterm
Cc
Cc
AC Coupling Capacitor
222
224
Hi-z
LPF
(d)
Gamma Voltages
(b)
Hi-z
LPF
232
231
Transmission Line
221
223
(a)
TX
210

Fig.3

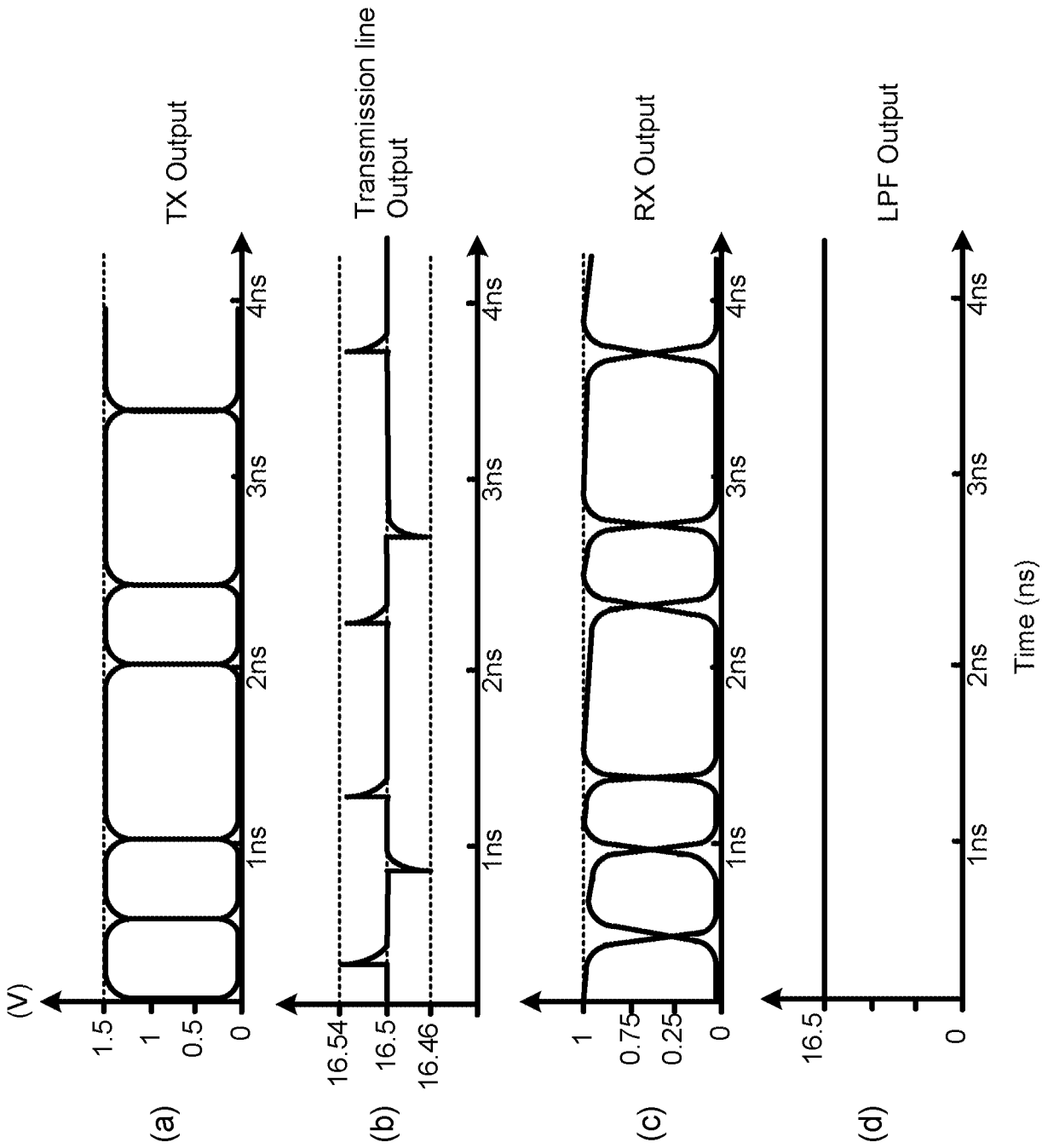

TX Output
Transmission line Output
RX Output
LPF Output
(V)
1.5
1
0.5
0
16.54
16.5
16.46
0.75
0.25
(a)
(b)
(c)
(d)
1ns
2ns
3ns
4ns
Time (ns)

Fig.4

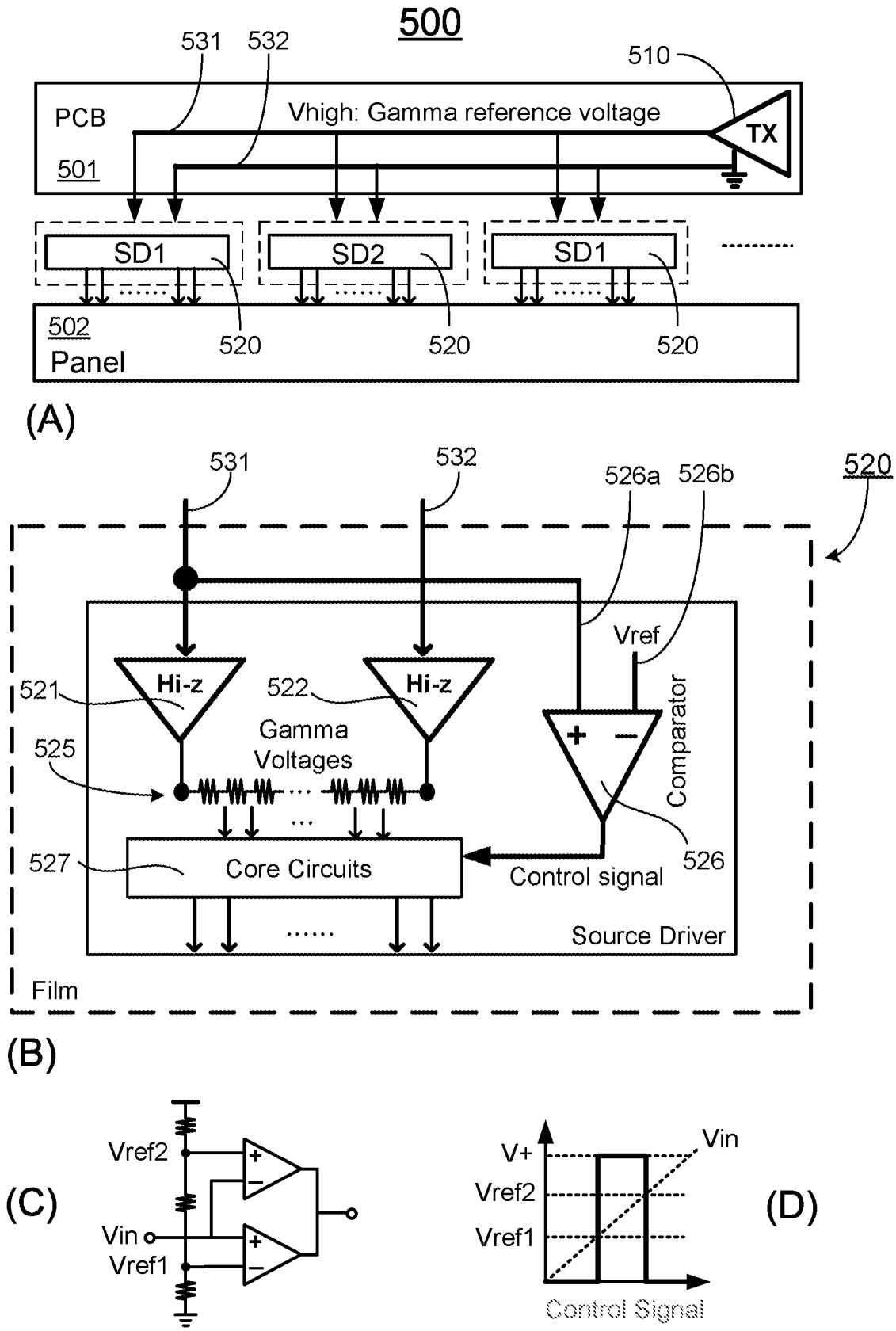

500
531
532
510
PCB
501
Vhigh: Gamma reference voltage
TX
SD1
SD2
SD1
502
Panel
520
520
520
(A)
531
532
526a
526b
520
Vref
521
Hi-z
522
Hi-z
Gamma
Voltages
525
Comparator
527
Core Circuits
Control signal
526
Source Driver
Film
(B)
(C)
Vref2
Vin
Vref1
V+
Vref2
Vref1
Vin
Control Signal
(D)

Fig.5

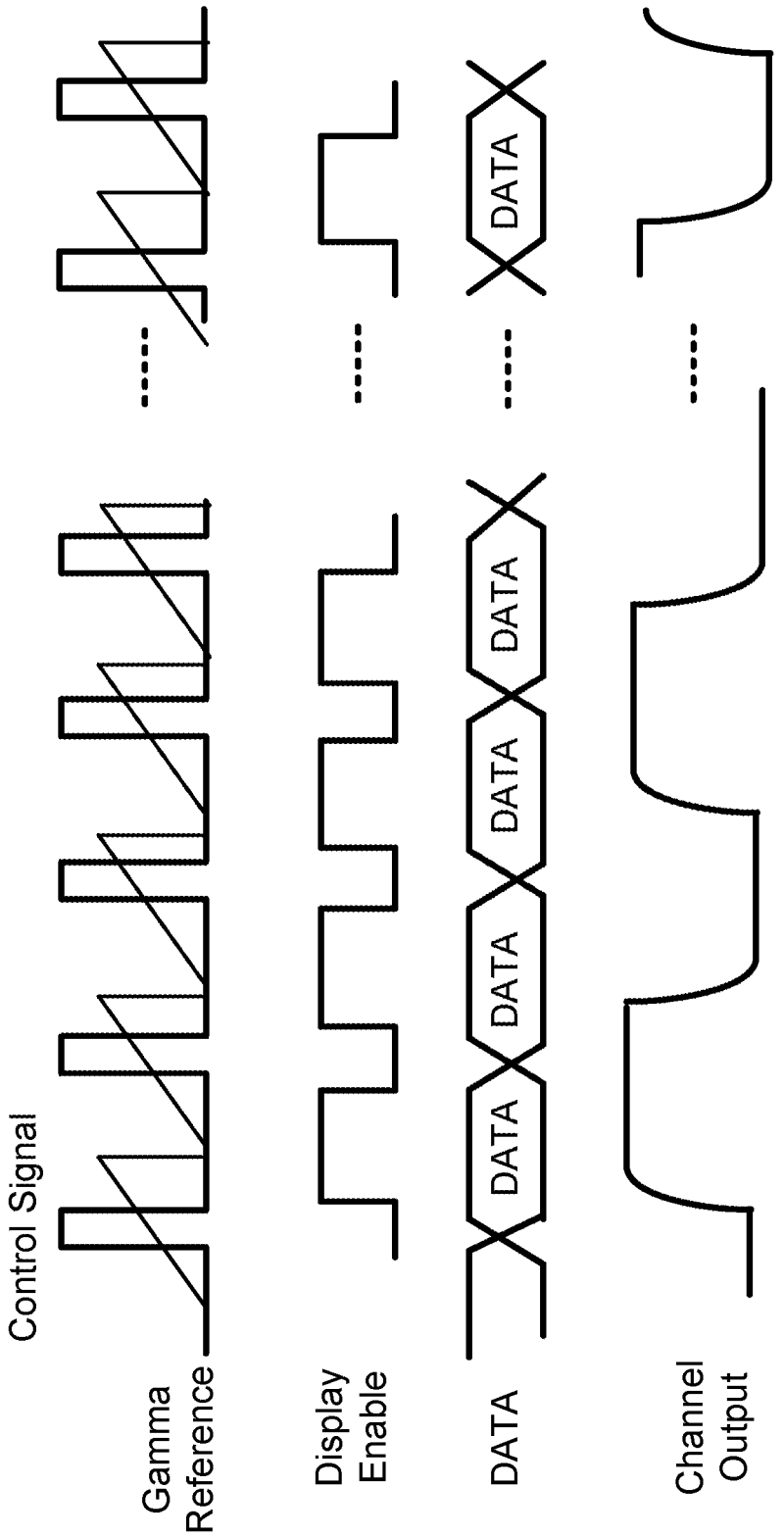

Control Signal
Gamma Reference
Display Enable
DATA
DATA
DATA
DATA
DATA
Channel Output

Fig.6

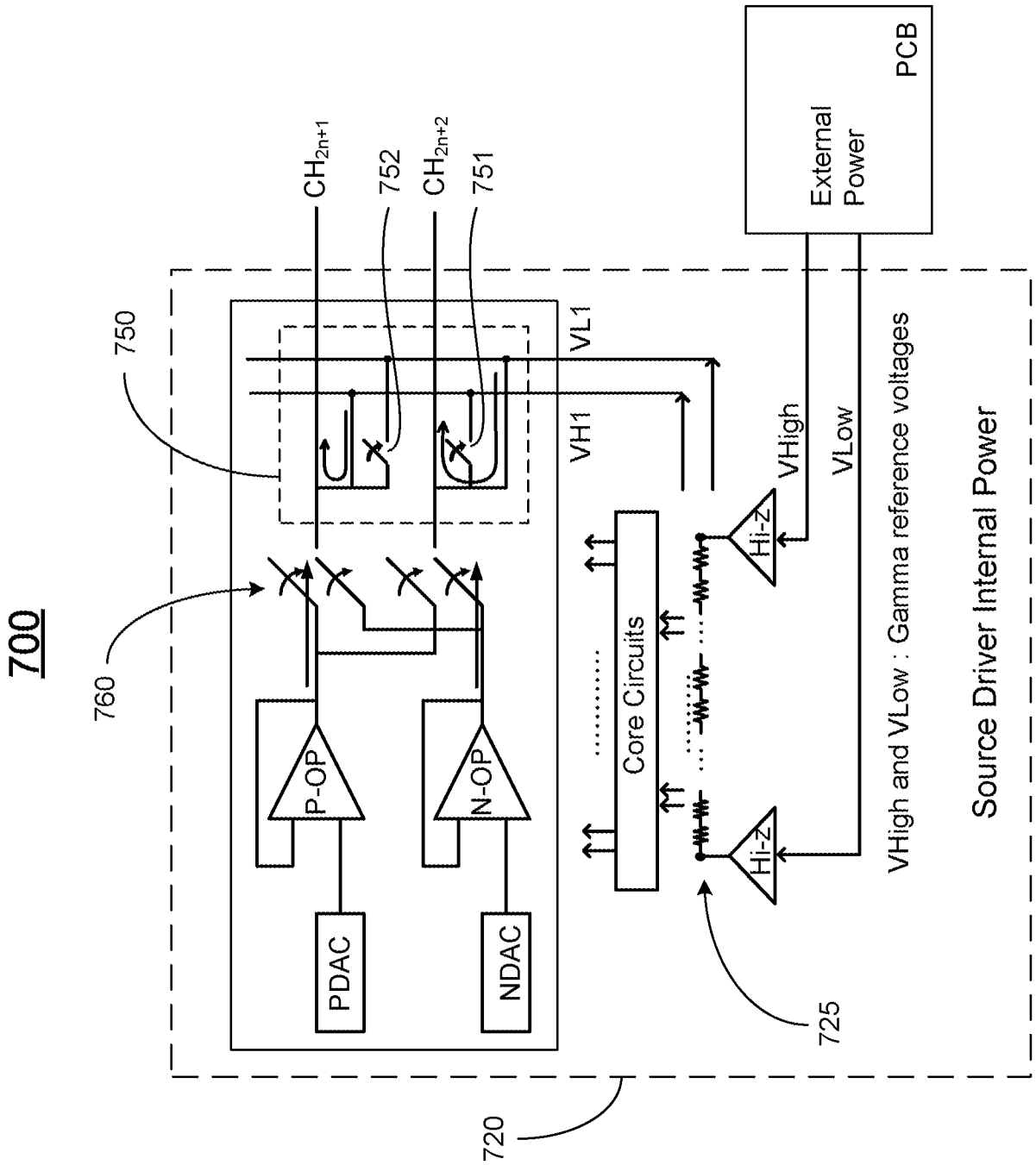

700
760
750
$CH_{2n+1}$
752
$CH_{2n+2}$
751
VL1
VH1
P-OP
N-OP
PDAC
NDAC
Core Circuits
Hi-z
Hi-z
VHigh
VLow
External Power
PCB
VHigh and VLow : Gamma reference voltages
Source Driver Internal Power
725
720

Fig.7

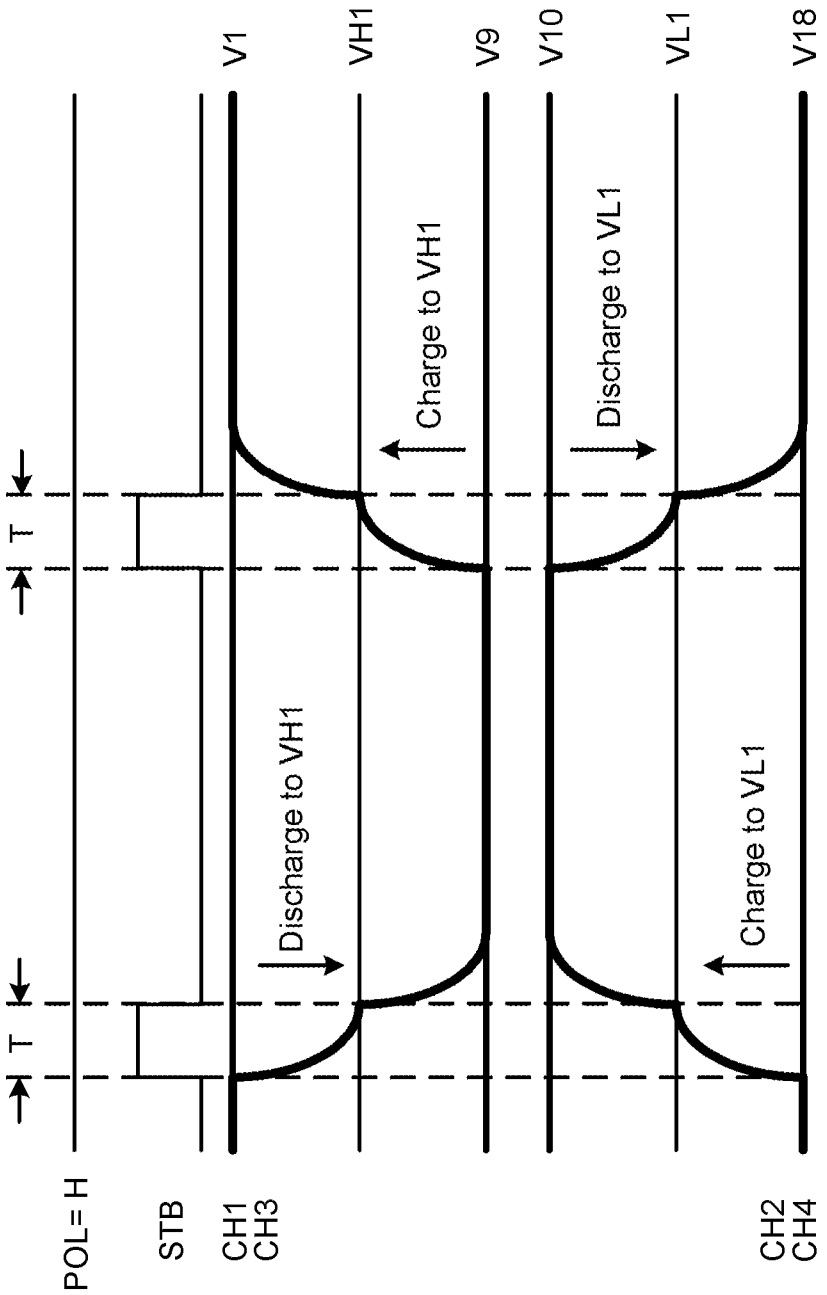

V1
VH1
V9
V10
VL1
V18
T
T
Discharge to VH1
Charge to VH1
Discharge to VL1
Charge to VL1
POL= H
STB
CH1
CH3
CH2
CH4

Fig.8

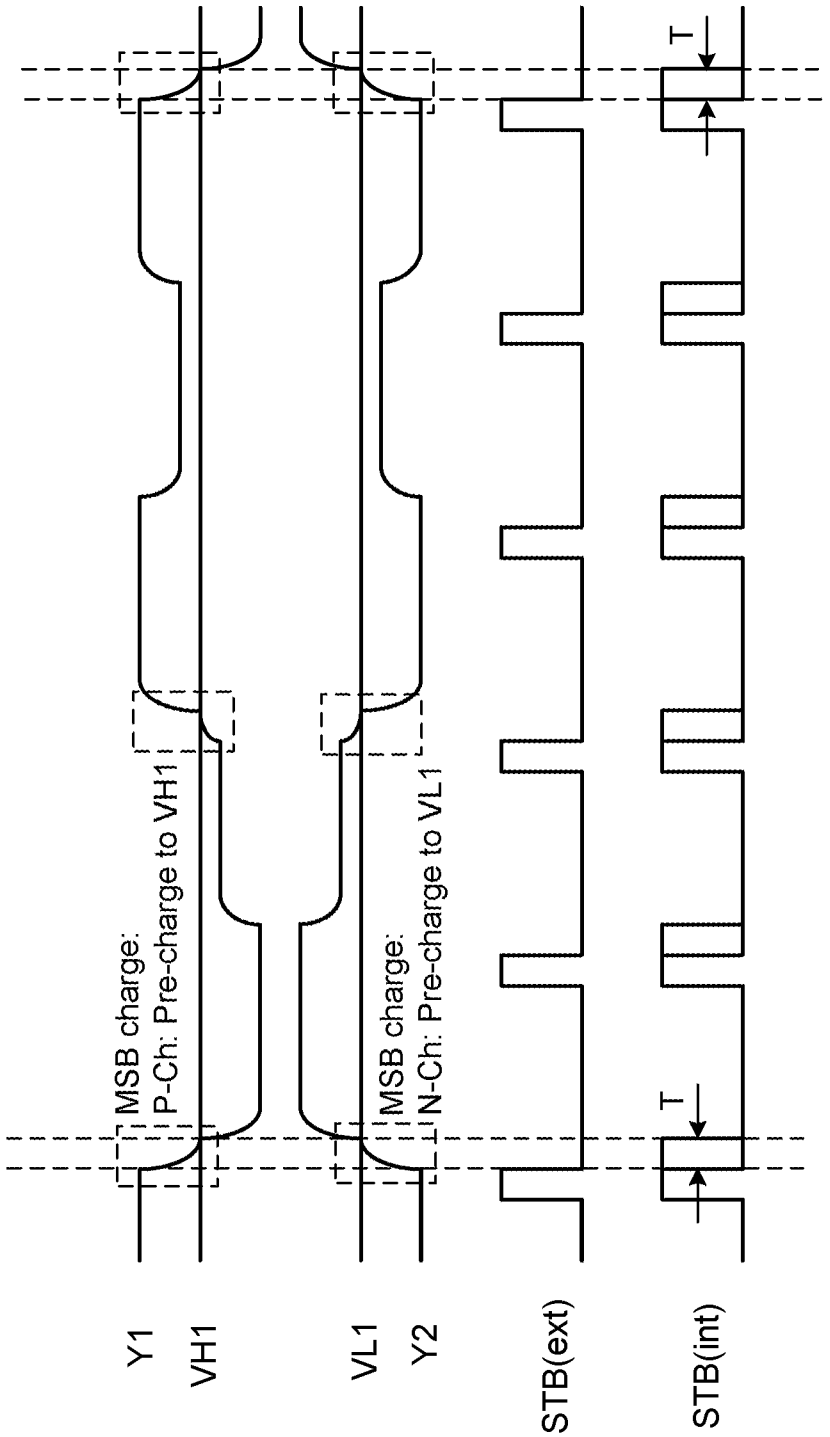

Y1
VH1
VL1
Y2
STB(ext)
STB(int)
MSB charge:
P-Ch: Pre-charge to VH1
MSB charge:
N-Ch: Pre-charge to VL1
T
T

Fig.9

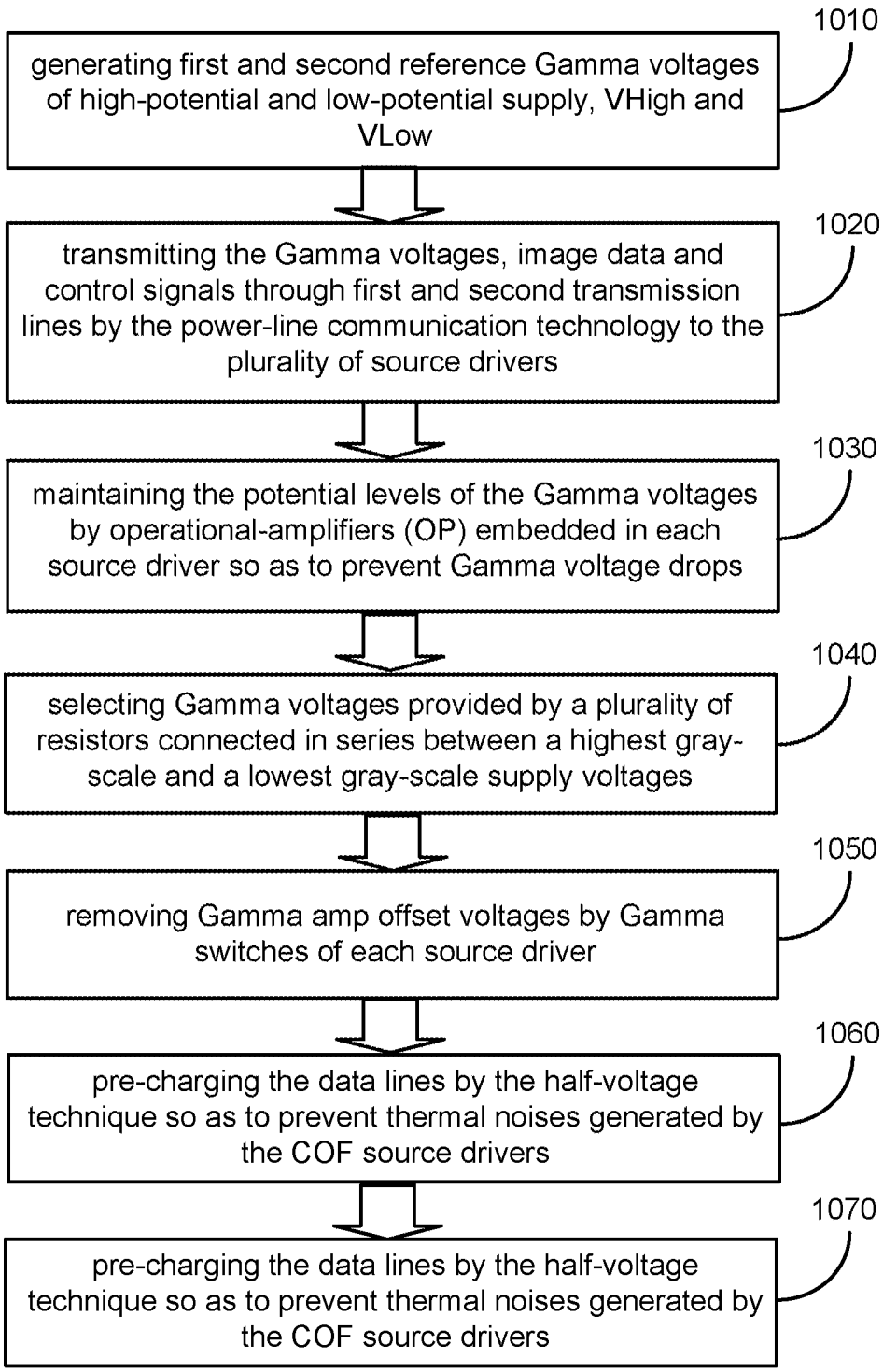

1010
generating first and second reference Gamma voltages of high-potential and low-potential supply, VHigh and VLow
1020
transmitting the Gamma voltages, image data and control signals through first and second transmission lines by the power-line communication technology to the plurality of source drivers
1030
maintaining the potential levels of the Gamma voltages by operational-amplifiers (OP) embedded in each source driver so as to prevent Gamma voltage drops
1040
selecting Gamma voltages provided by a plurality of resistors connected in series between a highest gray-scale and a lowest gray-scale supply voltages
1050
removing Gamma amp offset voltages by Gamma switches of each source driver
1060
pre-charging the data lines by the half-voltage technique so as to prevent thermal noises generated by the COF source drivers
1070
pre-charging the data lines by the half-voltage technique so as to prevent thermal noises generated by the COF source drivers

Fig.10

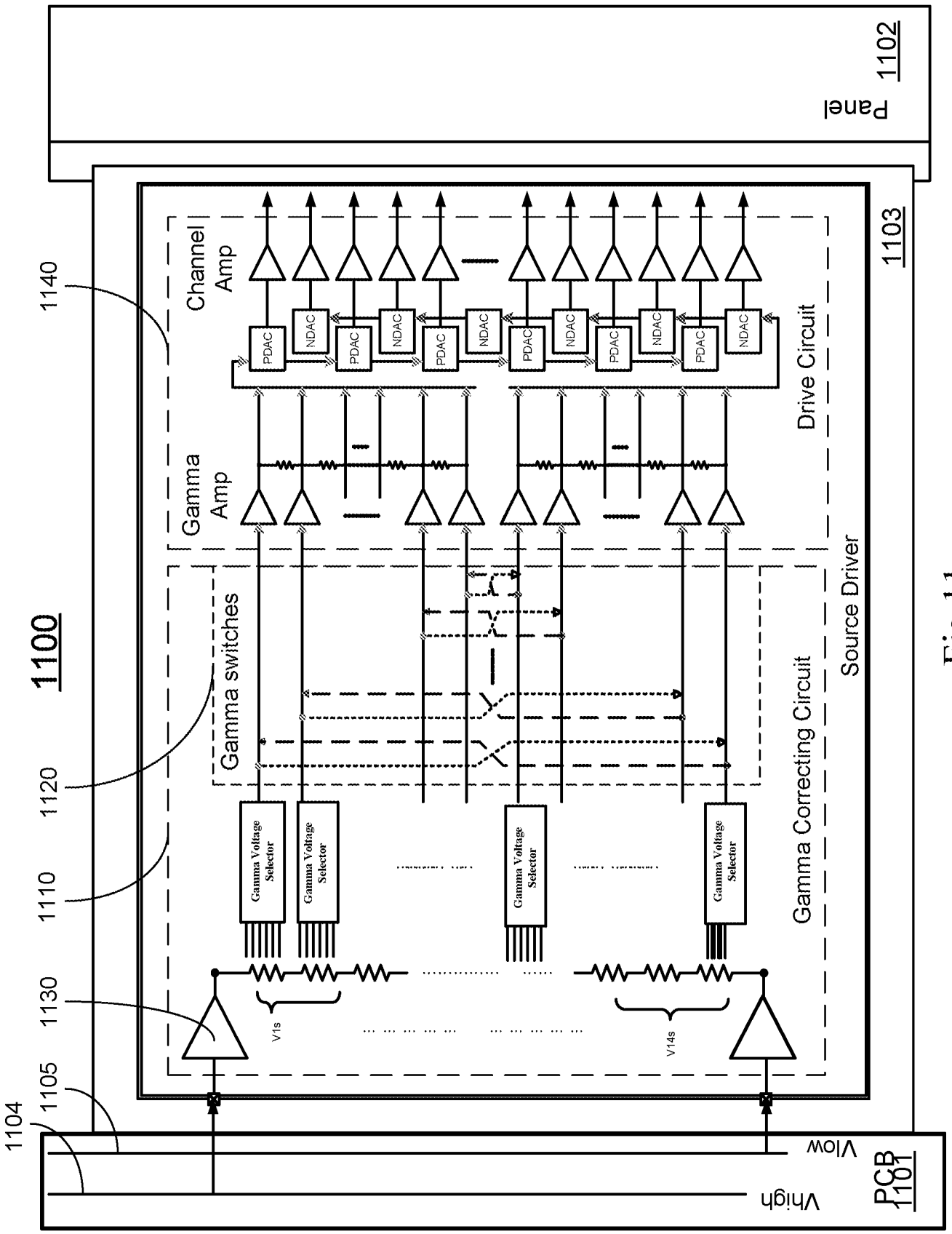

Panel
1102
1103
1100
1140
1120
1110
1130
1105
1104
Channel Amp
PDAC
NDAC
Drive Circuit
Gamma Amp
Gamma switches
Gamma Voltage Selector
Gamma Correcting Circuit
Source Driver
V1s
V14s
Vlow
Vhigh
PCB
1101

Fig.11

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/086035

**A. CLASSIFICATION OF SUBJECT MATTER**

G09G 3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, WPI, EPODOC: driver, display, LCD, PCB, Gamma, reference, COF, film, Hi-z, drop, voltage, transmission, line, source, gray, OP

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
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| A | | 4-11, 16-32 |
| A | US 2011012822 A1 (PARK Mangyu, et al.) 20 January 2011 (20.01.2011) the whole document | 1-32 |
| A | CN 101144919 A (SAMSUNG ELECTRONICS CO., LTD.) 19 March 2008 (19.03.2008) the whole document | 1-32 |

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 11 January 2014 (11.01.2014) | **20 Feb. 2014 (20.02.2014)** |
| Name and mailing address of the ISA/CN<br>The State Intellectual Property Office, the P.R.China<br>6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088<br>Facsimile No. 86-10-62019451 | Authorized officer<br>XIE,Xingchu<br>Telephone No. (86-10)62413405 |

Form PCT/ISA /210 (second sheet) (July 2009)

# INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2013/086035

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