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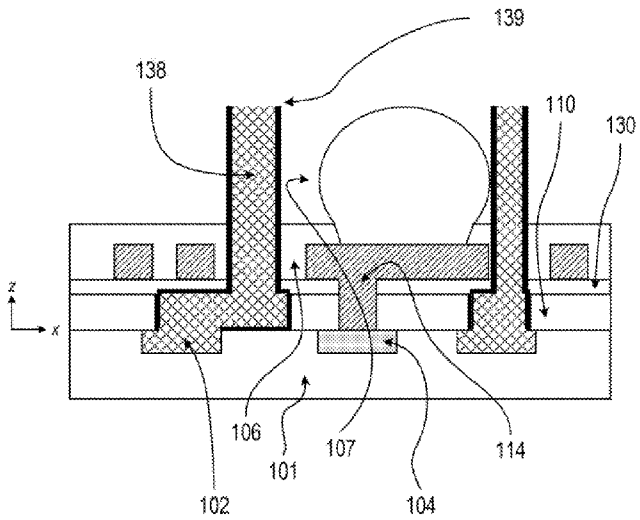

100

FIG. 1

(57) Abstract: Disclosed is a package comprising a substrate having a patterned surface with an optical contact area, an optical redistribution layer (oRDL) feature, and a build-up material extending over the patterned surface of the substrate and around portions of the oRDL features. In some embodiments, the package comprises a liner sheathing the oRDL features. In some embodiments, the oRDL feature extends through openings in an outer surface of the build-up material and forms posts extending outward from the outer surface. In some embodiments, the package comprises an electrical redistribution layer (eRDL) feature, at least some portion of which overlap at least some portion of the oRDL feature. In some embodiments, the package comprises an optical fiber coupled to the oRDL features.

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INTEGRATED CIRCUIT PACKAGES INCLUDING AN OPTICAL REDISTRIBUTION LAYER

CLAIM FOR PRIORITY

[001] This application claims priority to U.S. Patent Application Serial No. 15/089,524, filed on April 2, 2016 and titled "INTEGRATED CIRCUIT PACKAGES INCLUDING AN OPTICAL REDISTRIBUTION LAYER", which is incorporated by reference in its entirety.

BACKGROUND

[002] Packaging of an IC chip or die often entails, in part, fabrication of electrically-isolated interconnect features through formation of patterned layers of metal and patterned layers of electrically-insulating or dielectric material (which may be referred to as build-up, or build-up material). The interconnect features may provide pathways for electrically-conductive pads on the chip to connect electrically to an external interface of the package containing the fabricated IC chip. The interconnect features may also break-out the points of electrical connection from being over or above some areas of the IC chip (e.g., the pads, which may be located in central regions or densely packed regions of the IC chip) to positions scaled for the electrical interface of the package. The interconnect features may accordingly be referred to as electrical Redistribution Layer (eRDL) features.

BRIEF DESCRIPTION OF THE DRAWINGS

[003] The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements. In the figures:

[004] **FIG. 1** illustrates a cross-sectional view of a packaged component comprising an optical Redistribution Layer feature, in accordance with some embodiments;

[005] **FIGS. 2A, 2B, 2C, 2D, 2E, 2F, 2G, 2H, 2I, 2J, 2K, 2L, and 2M**illustrate cross-sectional views of a packaged component comprising an optical RDL feature as a method of

fabricating the packaged component is performed, and illustrate flow diagrams for a method of fabricating a packaged component comprising an optical RDL feature, in accordance with some embodiments;

[006] **FIG. 3** illustrates a cross-sectional view of a packaged component comprising an optical RDL feature, in accordance with some embodiments;

[007] **FIG. 4** illustrates a cross-sectional view of a packaged component comprising an optical RDL feature both electrically coupled and optically coupled to a printed circuit board (PCB) component, in accordance with some embodiments;

[008] **FIGS. 5 and 6** illustrate cross-sectional views of packages integrating packaged components with optical RDL features, and illustrate plan views of the packages, in accordance with some embodiments;

[009] **FIG. 7** illustrates a mobile computing platform and a data server machine employing a package including an optical RDL feature, in accordance with some embodiments; and

[010] **FIG. 8** is a functional block diagram of an electronic computing device, in accordance with some embodiments.

DETAILED DESCRIPTION

[011] One or more embodiments are described with reference to the enclosed figures. While specific configurations and arrangements are depicted and discussed in detail, it should be understood that this is done for illustrative purposes only. Persons skilled in the relevant art will recognize that other configurations and arrangements are possible without departing from the spirit and scope of the description. It will be apparent to those skilled in the relevant art that techniques and/or arrangements described herein may be employed in a variety of other systems and applications other than what is described in detail herein.

[012] Reference is made in the following detailed description to the accompanying drawings, which form a part hereof and illustrate exemplary embodiments. Further, it is to be understood that other embodiments may be utilized and structural and/or logical changes may be made without departing from the scope of claimed subject matter. It should also be noted that directions and references, for example, up, down, top, bottom, and so on, may be used merely to facilitate the description of features in the drawings and are not intended to restrict the application of claimed subject matter. Terms such as “upper” and “lower” “above” and “below”

may be understood by reference to illustrated X-Z coordinates, and terms such as "adjacent" may be understood by reference to X,Y coordinates or to non-Z coordinates. Therefore, the following detailed description is not to be taken in a limiting sense and the scope of claimed subject matter is defined solely by the appended claims and their equivalents.

[013] In the following description, numerous details are set forth. However, it will be apparent to one skilled in the art that the various embodiments discussed herein may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the embodiments. Reference throughout this specification to "an embodiment" or "one embodiment" means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrase "in an embodiment" or "in one embodiment" in various places throughout this specification are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[014] As used in the description and the appended claims, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items.

[015] As used in throughout this description, and in the claims, a list of items joined by the term "at least one of" or "one or more of" can mean any combination of the listed terms. For example, the phrase "at least one of A, B or C" can mean A; B; C; A and B; A and C; B and C; or A, B and C.

[016] The terms "coupled" and "connected," along with their derivatives, may be used herein to describe functional or structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical, optical, or electrical contact with each other. "Coupled" may be used to indicate that two or more elements are in either direct or indirect (with other intervening elements between

them) physical, optical, electrical, or electromagnetic contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause-and-effect relationship).

[017] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one component or material with respect to other components or materials where such physical relationships are noteworthy. For example, in the context of materials, one material disposed over or under another material may be directly in contact with the other material and/or with one or more intervening materials. Similarly, one material disposed between two materials may be directly in contact with the two materials and/or with one or more intervening materials. In contrast, a first material "on" a second material is in direct contact with that second material. Similar distinctions are to be made in the context of component assemblies.

[018] Described herein are packaged components including optical Redistribution Layer features. Some fabrication recipes may be directed in part toward the creation of IC chips that have optical features within and/or over a substrate. Optical features may include optical devices such as optical converters, light-emitting diodes (LEDs), laser diodes, photovoltaic cells, optical amplifiers, optical detectors, optical modulators, and/or parts of such devices.

[019] In some embodiments discussed below, a chip packaging process creates optically-transmissive interconnect features by forming layers of an optically transmissive material and layers of a build-up material (which may include a dielectric material). The optically-transmissive interconnect features provide pathways for optical features created on the IC chip to optically couple to optically-transmissive inputs and/or outputs on an external optical interface of a package containing the IC chip. The package-level optically-transmissive interconnect features also break-out optical I/O at the chip-level to locations on the package that are better suited for the external optical interface of a board or other host to which the package is mounted. Accordingly, such interconnect features may be referred to as optical Redistribution Layer (oRDL) features.

[020] Package processing to create oRDL features may advantageously provide reduced complexity, reduced cost, increased ease, and/or increased flexibility of manufacturing optical components, and may advantageously facilitate the incorporation of optical components within a package. In addition, package processing described herein to create oRDL features may advantageously integrate the oRDL features with eRDL features of a chip package. In turn, such

integrated package redistribution layers may provide reduced complexity, reduced cost, increased ease, and/or increased flexibility of integrating electronic components with optical components.

[021] **FIG. 1** illustrates a cross-sectional view of a portion of a packaged component 100 comprising an oRDL feature 138, in accordance with some embodiments. Packaged component 100 comprises an IC chip 101. IC chip 101 includes an optical component, such as, but not limited to, a photo diode operable to receive over an optical band or laser diode operable to transmit over an optical band. At least a portion of IC chip 101 has a semiconductor lattice structure suitable for semiconductor devices, such as but not limited to transistors. In various embodiments, substrate 101 may include a group IV semiconductor material such as silicon. In some embodiments, substrate 101 may include a composite group III / group V semiconductor material, such as gallium arsenide.

[022] Substrate 101 has one or more optical contact areas 102, which comprise an optically-transmissive or optically sensitive material. Optical contact areas 102 may be optically coupled to one or more optical devices, which may accept optical input signals (e.g., incident light) through optical contact areas 102 and which may in turn be operable to respond to the optical signals by converting and/or propagating them. Such optical devices may include, for example, optical converters, optical diodes, optical amplifiers, optical detectors, optical modulators, photovoltaic cells, and/or parts of such devices. Optical contact areas 102 may also be operable to emit optical signals by generating and/or propagating them. Such optical devices may include, for example, light-emitting diodes and laser diodes.

[023] In various embodiments, one or more of optical contact areas 102 may be optically coupled to parts of optical devices within substrate 101. Optical contact areas 102 may accordingly be operable to accept incident optical signals (e.g., incident light) and guide or otherwise deliver the optical signals to parts of optical devices, or to guide or otherwise deliver optical signals from parts of optical devices.

[024] Substrate 101 additionally has one or more electrical contact areas 104, which comprise an electrically-conductive material. Electrical contact areas 104 may be electrically coupled with one or more electronic devices, which may accept electrical signals (e.g., electric currents) through electrical contact areas 104 and which may in turn be operable to respond to the electrical signals by processing and/or propagating them, or which may deliver electrical

signals through electrical contact areas 104. Such electronic devices may include transistors, diodes, and thyristors, and/or parts of such devices. Some embodiments of packaged component 100 may not have electrical contact areas 104.

[025] In various embodiments, one or more of electrical contact areas 104 may be electrically coupled to parts of electrical devices within substrate 101. Electrical contact areas 104 may accordingly be operable to accept electrical signals (e.g., electric currents) and propagate the electrical signals to parts of electrical devices, or to guide or otherwise deliver electrical signals from parts of electrical devices. Some electrical contact areas 104 may be electrically-conductive pads for electrically coupling electrical devices of substrate 101 to structures outside substrate 101.

[026] Optical contact areas 102 and electrical contact areas 104 are positioned on a patterned side or region of substrate 101, such as front or back sides of substrate 101. Optical contact areas 102 and electrical contact areas 104 accordingly form parts of front or back surfaces of substrate 101, which is a patterned surface of substrate 101.

[027] Packaged component 100 comprises one or more dielectric build-up layers positioned over and/or on portions of the patterned surface of substrate 101. The various build-up layers comprise a dielectric material. For example, some of the build-up, such as lower build-up layer 110 and upper build-up layer 130, may comprise an organic material, an epoxy thermoset, or a thermoplastic material. Solder-mask 106 disposed over the build-up may also be formed of a similar polymer material that is likewise deposited and cured or applied as a dry film.

[028] The package build-up has a layered structure, with various layers of build-up positioned on top of each other. For example, the one or more build-up layers comprise a lower build-up layer 110 positioned over and/or on portions of substrate 101. Lower build-up layer 110 is accordingly in direct contact with various portions of the patterned surface of substrate 101, including portions of optical contact areas 102 and portions of electrical contact areas 104. The build-up also comprises an upper build-up layer 130 positioned over and/or on portions of lower build-up layer 110. Upper build-up layer 130 is accordingly in direct contact with various portions of lower build-up layer 110. Solder mask 106 is positioned over and/or on portions of upper build-up layer 130. Although only a few build-up layers are depicted in **FIG. 1**, a build-up material in packaged component 100 may include any number of build-up layers.

[029] Packaged component 100 also comprises one or more oRDL features 138, which extend from optical contact areas 102 to an exterior of packaged component 100. As depicted in **FIG. 1**, for example, each oRDL feature 138 has a first terminus that is optically coupled with optical contact areas 102. In some embodiments, the first terminus may be in direct contact with optical contact areas 102. As depicted, each oRDL feature 138 also has a second terminus positioned at, or extending through, openings or apertures in an outer surface of the various build-up layers (e.g., openings in an outer surface of solder mask 106). Between the first terminus and the second terminus, each oRDL feature 138 extends through the various build-up layers, and the various build-up layers accordingly extend around portions of oRDL features 138.

[030] oRDL features 138 comprise an optically-transmissive material (e.g., a material that transmits electromagnetic radiation in a given optical band). In some embodiments, oRDL features 138 include a substantially transparent material for a desired range of wavelengths over which optical devices on substrate 101 are operable. In some embodiments, the optically-transmissive material may be an epoxy material. In some embodiments, the optically-transmissive material is polymethyl methacrylate (PMMA).

[031] Packaged component 100 comprises one or more liners 139 sheathing, coating, or encasing one or more surfaces of oRDL features 138. Liners 139 are to contain optical energy within oRDL features 138. Liners 139 may be optically reflective. In various embodiments, liners 139 may be in direct contact with oRDL features 138. Liners 139 of some embodiments comprise an electrically-conductive material (e.g., a metal) and/or a material having a refractive index below that of a refractive index of a material of oRDL features 138, to provide a sufficient refractive index contrast for internal reflection. For some embodiments, liners 139 ~~may~~ comprise one or more of aluminum, copper, or titanium. In some embodiments, liners 139 comprise a metal nitride, such as, but not limited to, titanium nitride. Liners 139 may advantageously reduce optical signal loss into the build-up layers surrounding oRDL features 138.

[032] For other embodiments of packaged component 100, however, one or more oRDL features 138 may not include liners 139. For such embodiments, material properties of the package build-up (e.g., lower build-up layer 110, upper build-up layer 130, and/or solder mask 106) may advantageously reduce optical signal loss, such as by providing beneficial

optical reflectivity, for example as a result of index contrast with the material employed in oRDL features 138. In some such embodiments, the package build-up may comprise a material substantially non-transmissive to the optical wavelength transmitted by oRDL features 138.

[033] Liners 139 sheathe or otherwise cover substantially all surfaces of oRDL features 138. In some embodiments however, liner 139 is present on sidewalls of oRDL features 138 but is absent from one or more surfaces that are to couple light vertically (e.g., z-dimension). The absence of liners 139 in select regions enables oRDL features 138 to directly contact optical contact areas 102. Liners 139 may also be absent from surfaces of the package that are to optically couple with a component external to packaged component 100. In other embodiments, liners 139 may merely partially sheathe or otherwise cover oRDL features 138. For example, liners 139 may sheathe portions of oRDL features 139 not surrounded by various build-up layers. Other portions of oRDL features not sheathed by liners 139 may be in contact with, for example, reflective surfaces of the build-up layers (as discussed above).

[034] In embodiments that include the creation of eRDL features, packaged component 100 also comprises one or more eRDL features 114 and one or more solder connections 107. Before packaged component 100 is integrated with a host, solder connections 107 may have a substantially spherical shape. After packaged component 100 is mounted to a host, solder connections 107 may no longer have a substantially spherical shape (potentially as a result of a reflow process), and may take a more cylindrical or even hourglass-like shape. Embodiments of packaged component 100 that do not include electrical contact areas 104 may also lack eRDL features 114 and solder connections 107.

[035] One or more of eRDL features 114 extend from electrical contact areas 104 to solder connections 107. As depicted in **FIG. 1**, each eRDL feature 114 has a first terminus that is coupled with an electrical contact area 104, which is an electrically-conductive pad formed on substrate 101. In various embodiments, the first terminus may be in direct contact with electrical contact areas 104. eRDL features 114 also have a second terminus positioned proximal to openings or apertures in one or more of the build-up layers, such a ball grid array (BGA) pad surrounded by solder mask 106. Solder connections 107 are disposed within and/or adjacent to the openings or apertures in solder mask 106. The second terminus of each eRDL feature 114 is coupled to a solder connection 107. Between the first terminus and the second terminus, eRDL features 114 extend through the various build-up layers, and the various build-up layers

accordingly extend around portions of eRDL features 114.

[036] eRDL features 114 may comprise any electrically-conductive material, such as a metal. Solder connections 107 are accordingly electrically coupled to electrical contact areas 104, through eRDL features 114.

[037] Solder connections 107 extend outward a first distance from an outer surface of the build-up material. Similarly, oRDL features 138 extend vertically (e.g., z-dimension) beyond the outer surface of the package build-up to form optically transmissive posts extending outward a second distance from the outer surface. In some embodiments, the second distance may be substantially equal to the first distance.

[038] The optically transmissive posts extending outward from the outer surface have a longitudinal length (e.g., z-dimension) oriented substantially normal to a patterned surface of substrate 101, as well as a transverse width (e.g., x-dimension) oriented substantially parallel to substrate 101. In some embodiments, a ratio of the longitudinal length to the transverse width is greater than 2. In some embodiments, that ratio is greater than 3, and may even be greater than 5.

[039] In some embodiments, the longitudinal length of optically transmissive posts 138 is substantially equal to a solder ball diameter and/or z-height of a solder joint. A subsequent integration process may be advantageously facilitated by oRDL features 138 extending to a same z-height as eRDL features 114. For such embodiments, both oRDL features 138 and eRDL features 114 may interface with substantially co-planar features of a host external to packaged component 100.

[040] In various embodiments, packaged component 100 may comprise one or more regions in which oRDL features 138 and eRDL features 114 physically overlap. Portions of oRDL features may be positioned above, over, and/or on portions of eRDL features 114, and may accordingly overlap portions of eRDL features 114. Similarly, portions of eRDL features 114 may be positioned above, over, and/or on portions of oRDL features 138, and may accordingly overlap portions of oRDL features 138. In some such embodiments, a portion of a build-up may be positioned between overlapping portions of oRDL features 138 and portions of eRDL features 114. In other embodiments, portions of eRDL features 114 that overlap portions of oRDL features 138 may be in direct contact with those portions of oRDL features 138. For embodiments that include liner 139, portions of eRDL features 114 that overlap portions of

oRDL features 138 may be in direct contact with liner 139 covering those portions of oRDL features 138.

[041] The material and/or structural properties of oRDL features 138 and eRDL features 114 may advantageously permit them to be located in proximity to each other without either feature disruptively interfering with the functionality of the other. Portions of the two types of features may accordingly overlap each other, or may otherwise be in close proximity with each other (e.g., adjacent within a same build-up layer), without the operation of either type of RDL feature being inherently interfered with or disrupted. As a result, fabrication processes to create oRDL features may be integrated with fabrication processes to create eRDL features. In turn, such integrated fabrication processes may advantageously provide reduced complexity, reduced cost, increased ease, and/or increased flexibility of manufacturing components that integrate electronic devices with optical devices.

[042] As discussed above, packaged component 100 comprises substrate 101, optical contact areas 102, various build-up layers such as lower build-up layer 110, upper build-up layer 130, and oRDL features 138. Packaged component 100 also comprises liners 139, electrical contact areas 104, solder mask 106, and eRDL features 114, although these features may be absent in some embodiments of packaged component 100. Since these features may be monolithically formed, as discussed in detail immediately below, packaged component 100 is accordingly a monolithic packaged component.

[043] **FIGS. 2A, 2B, 2C, 2D, 2E, 2F, 2G, 2H, 2I, 2J, 2K, 2L, and 2M** illustrate cross-sectional views of a packaged component comprising an oRDL feature as a method of fabricating the packaged component is performed, and illustrate flow diagrams of a method of fabricating a packaged component comprising an oRDL feature, in accordance with some embodiments.

[044] A method 250 may be undertaken to fabricate a packaged component 200. As depicted in **FIG. 2A**, in some embodiments, method 250 comprises receiving a workpiece at operation 252 and depositing and patterning a build-up layer at operation 254. In the illustrative embodiment, an IC chip 201 having a patterned surface with one or more optical areas 202 is received at operation 252. For the depicted embodiment, which includes the creation of eRDL features, the patterned surface of IC chip 201 also has one or more electrical areas 204. The IC chip may comprise a semiconductor lattice suitable for use in a semiconductor device

fabrication process, and may include a material such as silicon or gallium arsenide.

[045] At operation 254, a first build-up layer 210 is deposited over IC chip 201 and optical contact areas 202. First build-up layer 210 is then patterned to at least partially expose IC chip 201 and optical contact areas 202. For the depicted embodiment, which includes the creation of eRDL features, first build-up layer 210 is also deposited over electrical contact areas 204, and is also patterned to at least partially expose electrical contact areas 204. First build-up layer 210 may comprise a dielectric material, such as an organic material, an epoxy thermoset, or a thermoplastic material. Any thin film or dry film, or spin-and-cure deposition process known in the art may be employed at operation 254.

[046] For the embodiment depicted in **FIG. 2B**, which includes the creation of liners around oRDL features, a liner layer 211 is deposited over first build-up layer 210 at operation 256. Liner layer 211 may also be deposited over any exposed portions of IC chip 201, and over any exposed optical contact areas 202. For the depicted embodiment, which includes the creation of eRDL features, liner layer 211 is also deposited over any exposed electrical contact areas 204. Any deposition process known in the art may be employed at operation 256. For example, a metal may be deposited by physical vapor deposition (PVD).

[047] For the embodiment depicted in **FIG. 2C**, which includes the creation of liners around oRDL features, one or more apertures 241 is formed through liner layer 211 at operation 258. Apertures 241 may be formed, for example, by laser drilling or a suitable etching process. Apertures 241 are formed through portions of liner layer 211 above optical contact areas 202. The formation of apertures 241 accordingly exposes portions of optical contact areas 202.

[048] Liner layer 211 may comprise a conductive material and/or a material having a refractive index below that of a refractive index of a material that will be subsequently deposited as the oRDL. In some embodiments, liner layer 211 is a metal. In some such embodiments, liner layer 211 may comprise one or more of aluminum, copper, or titanium. In some embodiments, liner layer 211 may comprise a metal nitride, such as, but not limited to, titanium nitride.

[049] As is further depicted in **FIG. 2C**, method 250 continues at operation 260 where an oRDL 212 is deposited over build-up layer 210, any exposed portions of IC chip 201, and any exposed optical contact areas 202. oRDL 212 is subsequently hardened. For the depicted embodiment, which includes the creation of liners around oRDL features, oRDL 212 is

deposited over liner layer 211, and over any exposed portions of optical contact areas 202 through apertures 241.

[050] oRDL 212 comprises an optically transmissive material. In some embodiments, oRDL 212 includes an epoxy material. In various embodiments, oRDL 212 comprises PMMA.

[051] In some embodiments represented by **FIG. 2D**, oRDL 212 is polished back (e.g., by chemical mechanical planarization), and overburden of oRDL 212 thereby removed. The polishing exposes first build-up layer 210 and a pattern of various portions of oRDL 212 in-between portions of the exposed first build-up layer 210 (e.g., x-dimensionally). The polishing may also planarize oRDL 212 with a top surface of the exposed build-up layer 210.

[052] For the depicted embodiment, which includes the creation of liners around oRDL features, the polishing also removes portions of liner layer 211 above build-up layer 210 to expose build-up layer 210. In such embodiments, portions of liner layer 211 are left between IC chip 201 and portions of oRDL 212 that may be positioned above IC chip 201. In addition, portions of liner layer 211 are left between build-up layer 210 and the various portions of oRDL 212 in-between portions of the exposed build-up layer 210.

[053] For some embodiments, as depicted in **FIG. 2E**, which include the creation of eRDL features, one or more apertures 242 may be formed completely through portions of build-up layer 210 to expose portions of electrical contact areas 204. Apertures 244 may be formed, for example, by laser drilling or a suitable etching process. For the depicted embodiment, which includes the creation of liners around oRDL features, another liner layer 221 is deposited on build-up layer 210, on oRDL 212, and on any exposed portions of electrical contact areas 204. Liner layer 221 may be any of the materials provided above for liner layer 211, for example.

[054] For some embodiments, as depicted in **FIG. 2F**, which include the creation of liners around oRDL features, at operation 268 another build-up layer 220 is deposited over liner layer 221. Build-up layer 220 may be any of the materials provided above for build-up layer 210. Build-up layer 220 is then patterned, leaving exposed portions of liner layer 221. Exposed portions of liner layer 221 are then removed at operation 270, leaving portions of liner layer 221 between oRDL 212 and build-up layer 220. With reference to **FIG. 2G**, in removing 272, second build-up layer 220 may be thinned or completely removed, leaving exposed portions of build-up layer 210 and portions of liner layer 221 above oRDL 212. For the depicted embodiment, which includes the creation of eRDL features, the removal of build-up layer 220

additionally leaves exposed portions of electrical contact areas 204.

[055] In some embodiments represented by **FIG. 2G**, another build-up layer 230 is deposited over build-up layer 210 and oRDL 212. For the depicted embodiment, which includes the creation of liners around oRDL features, build-up layer 230 is also disposed over portions of liner layer 221 above oRDL 212.

[056] For the depicted embodiment, which includes the creation of eRDL features, build-up layer 230 is also deposited over exposed portions of electrical contact areas 204. For such embodiments, at operation 276 a plurality of apertures 243 is then formed through portions of build-up layer 230 over electrical contact areas 204. Apertures 243 may be formed, for example, by laser drilling or a suitable etching process.

[057] With reference to **FIG. 2H**, at operation 278 an eRDL 214 is deposited over build-up layer 230, and over exposed portions of electrical contact areas 204 through apertures 243. eRDL 214 is then patterned to form various features, such as one or more electrically-conductive pads, and one or more eRDL features extending between electrical contact areas 204 and the electrically-conductive pads.

[058] With reference to **FIG. 2I**, at operation 280, a solder mask 206 is deposited over eRDL 214 and over build-up layer 230. One or more apertures 244 are formed to extend completely through solder mask 206 and expose portions of the electrically-conductive pads of eRDL 214. Any known solder mask patterning process may be employed at operation 280. At operation 284, one or more solder connections 207 are positioned within apertures 244 and above the exposed portions of the electrically-conductive pads. A solder reflow then electrically couples solder connections 207 to the exposed electrically-conductive pads of eRDL 214.

[059] In some embodiments, as further illustrated in **FIG. 2J**, a resist layer 208 is deposited over build-up layer 230. Resist layer 208 is then patterned to expose portions of build-up layer 230. Resist layer 208 may be a light sensitive polymer, or a hardmask which may be removable by reactive ion etching. Subsequently, at operation 288 a plurality of apertures 245 are formed through build-up layer 230.

[060] For the depicted embodiment, which includes the creation of eRDL features, resist layer 208 is also deposited over eRDL 214, solder mask 206, and solder connections 207, and resist layer 208 is patterned to expose portions of solder mask 206. Subsequently, at operation 288, apertures 245 are additionally etched into solder mask 206.

[061] For the depicted embodiment, which includes the creation of liners around oRDL features, at operation 288 another liner layer 231 is deposited on exposed portions of oRDL 212, and also on sidewalls of apertures 245, which comprise portions of resist layer 208 and third build-up layer 230. The aperture sidewalls also include portions of solder mask 206 for the depicted embodiment that includes the formation of eRDL features). At operation 290, a plurality of apertures 246 are formed completely through portions of liner layer 230, thereby exposing portions of oRDL 212. Apertures 246 may be formed using methods similar to those used to form the apertures through liner layer 211.

[062] **FIG. 2K** depicts operation 292 where an oRDL 222 is deposited over resist layer 208 and exposed portions of oRDL 212. For the depicted embodiment, which includes the creation of liners around oRDL features, oRDL 222 is also deposited over liner layer 231, and is deposited through apertures 246 over exposed portions of oRDL 212. oRDL 222 is subsequently hardened. oRDL 222 may comprise a material similar to, or the same as, oRDL 212.

[063] As depicted in **FIG. 2L**, at operation 250 oRDL 222 is polished back, and overburden of oRDL 222 thereby removed. The polishing exposes resist layer 208. For the depicted embodiment, which includes the creation of liners around oRDL features, the polishing additionally removes portions of liner layer 231 above resist layer 208 to expose resist layer 208.

[064] The polishing accordingly forms one or more oRDL features 238 comprising portions of oRDL 212 and portions of RDL 222. For the depicted embodiment, which includes the creation of liners around oRDL features, the polishing also forms one or more liners 239 around oRDL features 238. Liners 239 comprise portions of liner layer 211, portions of liner layer 221, and portions of liner layer 231.

[065] In **FIG. 2M**, resist layer 208 is removed at operation 296 to expose build-up layer 230. For the depicted embodiment, which includes the creation of eRDL features, the removal of resist layer 208 exposes solder mask 206 and solder connections 207 which (along with eRDL features 214) are positioned above build-up layer 230. For the depicted embodiment, which includes the creation of liners around oRDL features, the removal of resist layer 208 additionally exposes portions of liners 239.

[066] Removal of resist layer 208 accordingly forms a packaged component 200

similar to packaged component 100 of **FIG. 1**. As depicted, packaged component 200 comprises an IC chip 201, one or more optical contact areas 202 coupled to one or more oRDL features 238, one or more liners 239 sheathing oRDL features 238, one or more electrical contact areas 204 coupled to one or more eRDL features 214 and coupled (through eRDL features 214) to one or more solder connections 207, and various build-up layers such as first build-up layer 210, second build-up layer 230, and solder mask 206. eRDL features 238 and solder connections 207 extend outward from an upper surface of solder mask 206 to approximately equivalent distances (although in some embodiments, eRDL features 238 and solder connections 207 may extend outward from the upper surface of solder mask 206 to different z-heights).

[067] **FIG. 3** illustrates a cross-sectional view of a packaged component comprising an oRDL feature, in accordance with some embodiments. Packaged component 300 is similar to packaged component 200. Packaged component 300 comprises an IC chip 301, one or more optical contact areas 302 coupled to one or more oRDL features 338, which are sheathed by one or more liners 339, and one or more electrical contact areas 304 coupled to one or more solder connections 307 through one or more eRDL features 314.

[068] Packaged component 300 comprises a build-up 310. While build-up 310 is similar to build-up layer 210, build-up layer 230, and solder mask 206 of packaged component 200, build-up 310 does not extend between and separate portions of oRDL features 338 from portions of eRDL features 314. Accordingly, portions of eRDL features 314 directly contact portions of liners 339 sheathing oRDL features 338 and/or, in some embodiments, portions of oRDL features 338 themselves.

[069] **FIG. 4** illustrates a cross-sectional view of a packaged component 300 comprising an oRDL feature both electrically coupled and optically coupled to a PCB component 450, in accordance with some embodiments. In **FIG. 4**, a PCB component 450 comprises one or more optical contact areas 452, such as light conducting areas, which is optically coupled to one or more optical devices disposed on PCB component 450. PCB 450 similarly comprises one or more electrical contact areas 454, which are electrically coupled to one or more electrically conducting features 464.

[070] As depicted in **FIG. 4**, packaged component 300 may be oriented to place oRDL features 238 near optical contact areas 452, and to place solder connections 307 near electrically

conducting features 464. oRDL features 238 may then be optically coupled to optical contact areas 452, and solder connections 307 may be electrically coupled to electrical contact areas 454 (e.g., by a reflow operation that may flow both the oRDL post and solder). Packaged component 300 and PCB 450 may accordingly be integrated into a package 400.

[071] **FIGS. 5 and 6** illustrate cross-sectional views of packages integrating packaged components with oRDL features, and plan views of the packages, in accordance with some embodiments. In **FIG. 5**, package 500 comprises a packaged component 501 with oRDL features and eRDL features, a bottom die 502, one or more solder connections 547, and one or more optical fibers 548. Optical fibers 548 are coupled to various optical contact areas on a top surface 550 of package 500.

[072] Packaged component 501 is an IC chip having a patterned surface and a back surface opposite the patterned surface. Similarly, bottom die 502 has a patterned surface and a back surface opposite the patterned surface. As depicted, the back surface of packaged component 501 is disposed adjacent to the back surface of bottom die 502. Solder connections 547 are disposed adjacent to the patterned surface of the bottom die

[073] The patterned surface of packaged component 501 has one or more optical contact areas and one or more electrical contact areas, and the patterned surface of bottom die 502 has one or more electrical contact areas. Package 500 comprises one or more optically-transmissive features 538, which may include oRDL features in some embodiments, and which optically couples the oRDL features of packaged component 501 to optical fibers 548. Package 500 also comprises one or more electrically conductive features 514, which may include eRDL features in some embodiments, and which electrically couples the eRDL features of packaged component 501 to the electrical contact areas of the bottom die, to solder connections 547, or to both.

[074] Packaged component 501 may comprise an optical converter, which may receive optical signals through optical fibers 548, then lead electrical signals to bottom die 502, and/or to solder connections 547.

[075] In **FIG. 6**, package 600 comprises a packaged component 601 with oRDL features and eRDL features, a bottom die 602, one or more solder connections 647, and one or more optical fibers 648. In some embodiments, optical fibers 648 are coupled at various optical contact areas to a top surface 650 of package 600. In comparison with package 500, package

600 also comprises a top die 603.

[076] Packaged component 601 is an IC chip having a patterned surface and a back surface opposite the patterned surface. Similarly, bottom die 602 has a patterned surface and a back surface opposite the patterned surface. The back surface of packaged component 601 is disposed adjacent to the back surface of bottom die 602, and solder connections 647 is disposed adjacent to the patterned surface of the bottom die. Top die 603 has one or more electrically conductive features (which includes eRDL features) protruding from an inward-facing surface, e.g., a surface facing toward the bulk of package 600.

[077] The patterned surface of packaged component 601 has one or more optical contact areas and one or more electrical contact areas, and the patterned surface of bottom die 602 has one or more electrical contact areas. Meanwhile, package 600 comprises one or more optically-transmissive features 638, which may include oRDL features in some embodiments, and which optically couple the oRDL features of packaged component 601 to optical fibers 648. Package 600 also comprises one or more electrically conductive features 614, which may include eRDL features in some embodiments, and which electrically couple the eRDL features of packaged component 601 to one or more of the electrical contact areas of the bottom die, solder connections 647, and the electrically conductive features of top die 603.

[078] Packaged component 601 may comprise an optical converter, which may receive optical signals through optical fibers 648, then lead electrical signals to one or more of bottom die 602, solder connections 647, and top die 603.

[079] **FIGS. 4 through 6** accordingly depict packaged components having oRDL features, incorporated in various ways within various packages. In various embodiments, a monolithic packaged component having one or more oRDL features (such as packaged component 200 or packaged component 300) may be incorporated in a package, along with one or more optically-transmissive fibers coupled to the oRDL features.

[080] Based upon the methods discussed herein, oRDL features may be integrated within packages in a variety of ways. oRDL features may be placed on a top side (or a front side) of a package, or on a bottom side (or a back side) of a package. In various embodiments, multiple layers of oRDL features and/or eRDL features may be integrated in an IC chip. oRDL features may be integrated in a variety of package configurations, including ball grid array BGA configurations, embedded wafer-level BGA configurations, wafer-level chip scale packaging

configurations, flip chip configurations, and panel-level fan-out package configurations. oRDL features may also be integrated in a molded interconnect substrate.

[081] **FIG. 7** illustrates a mobile computing platform and a data server machine employing a package including an oRDL feature, in accordance with some embodiments. The server machine 706 may be any commercial server, for example including any number of high-performance computing platforms disposed within a rack and networked together for electronic data processing, which in the exemplary embodiment includes a packaged monolithic SoC 750. The mobile computing platform 705 may be any portable device configured for electronic data display, for electronic data processing, for wireless electronic data transmission, or the like. For example, the mobile computing platform 705 may be any of a tablet, a smart phone, a laptop computer, etc., and may include a display screen (e.g., a capacitive, inductive, resistive, or optical touchscreen), a chip-level or package-level integrated system 710, and a battery 715.

[082] Either disposed within the integrated system 710 illustrated in the expanded view 720, or as a stand-alone packaged chip within the server machine 706, monolithic SoC 750 includes a memory block (e.g., RAM) and a processor block (e.g., a microprocessor, a multi-core microprocessor, graphics processor, or the like). The packaged chip includes an oRDL feature, for example as described elsewhere herein. The monolithic SoC 750 may be further coupled to a board, a substrate, or an interposer 760 along with one or more of a power management integrated circuit (PMIC) 730, an RF (wireless) integrated circuit (RFIC) 725 including a wideband RF (wireless) transmitter and/or receiver (TX/RX) (e.g., including a digital baseband and an analog front end module further comprises a power amplifier on a transmit path and a low noise amplifier on a receive path), and a controller 735.

[083] Functionally, PMIC 730 may perform battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to battery 715 and with an output providing a current supply to other functional modules. As further illustrated, in the exemplary embodiment, RFIC 725 has an output coupled to an antenna (not shown) to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 4G, and beyond. In alternative implementations, each of these board-level modules may be integrated onto

separate ICs or integrated into monolithic SoC 750.

[084] **FIG. 8** is a functional block diagram of an electronic computing device, in accordance with some embodiments. Computing device 800 may be found inside platform 705 or server machine 706, for example. Device 800 further includes a motherboard 802 hosting a number of components, such as, but not limited to, a processor 804 (e.g., an applications processor), which may be in a package coupled to motherboard 802 by BGA connections of differing height (volume), for example as described elsewhere herein. Processor 804 may be physically and/or electrically coupled to motherboard 802. In some examples, processor 804 includes an integrated circuit die packaged within the processor 804 and connections between the IC die and the processor 804 are further by BGA solder connections of differing heights, for example as described elsewhere herein. In general, the term "processor" or "microprocessor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be further stored in registers and/or memory.

[085] In various examples, one or more communication chips 806 may also be physically and/or electrically coupled to the motherboard 802. In further implementations, communication chips 806 may be part of processor 804. Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to motherboard 802. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, touchscreen display, touchscreen controller, battery, audio codec, video codec, power amplifier, global positioning system (GPS) device, compass, accelerometer, gyroscope, speaker, camera, and mass storage device (such as hard disk drive, solid-state drive (SSD), compact disk (CD), digital versatile disk (DVD), and so forth), or the like. Any of these other components may also be coupled to motherboard 802 by BGA solder connections of differing heights, for example as described elsewhere herein.

[086] Communication chips 806 may enable wireless communications for the transfer of data to and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a

non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. Communication chips 806 may implement any of a number of wireless standards or protocols, including but not limited to those described elsewhere herein. As discussed, computing device 800 may include a plurality of communication chips 806. For example, a first communication chip may be dedicated to shorter-range wireless communications, such as Wi-Fi and Bluetooth, and a second communication chip may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[087] While certain features set forth herein have been described with reference to various implementations, this description is not intended to be construed in a limiting sense. Hence, various modifications of the implementations described herein, as well as other implementations, which are apparent to persons skilled in the art to which the present disclosure pertains are deemed to lie within the spirit and scope of the present disclosure.

[088] The following examples pertain to particular exemplary embodiments.

[089] An example provides a package comprising: a substrate having a patterned surface with an optical contact area; an optical redistribution layer (oRDL) feature; a liner sheathing the oRDL feature; and a build-up material extending over the patterned surface of the substrate and around portions of the oRDL feature.

[090] Some embodiments provide a package, wherein the optical contact area is in direct contact with the oRDL feature. Some embodiments provide a package, wherein the oRDL feature extends from the optical contact area to an opening in an outer surface of the build-up material. Some embodiments provide a package, wherein the liner comprises one of: an electrically conductive material, and a material having a refractive index below that of a refractive index of the oRDL feature. Some embodiments provide a package, wherein the liner comprises at least one of: aluminum, a copper, titanium, and titanium material. Some embodiments provide a package, wherein the oRDL feature comprises an optically-transmissive material. Some embodiments provide a package, wherein the optically-transmissive material comprises polymethyl methacrylate. Some embodiments provide a package, wherein the oRDL feature extend through the openings in an outer surface of the build-up material and forms a post extending outward from the outer surface. Some embodiments provide a package, comprising an electrical redistribution layer (eRDL) feature, wherein the patterned surface of

the substrate has an electrical contact area, wherein the build-up material extends around portions of the eRDL feature, and wherein the eRDL feature extends from the electrical contact area to an additional opening in the build-up material.

[091] Some embodiments provide a package, comprising a solder connection disposed adjacent to the additional opening in the build-up material, the solder connection being electrically coupled to the eRDL feature. Some embodiments provide a package, wherein the oRDL feature extends through the opening in the build-up material and forms a post extending outward a first distance from an outer surface of the build-up material, and wherein the solder connection extends outward a second distance from the outer surface of the build-up material, the second distance being substantially equal to the first distance. Some embodiments provide a package, comprising a region between the patterned surface of the substrate and an outer surface of the build-up material in which the oRDL feature and the eRDL feature overlap. Some embodiments provide a package, comprising: a bottom die having a patterned surface with an electrical contact area and a back surface opposite the patterned surface; a solder connection; and an optical fiber, wherein the substrate has a back surface opposite the patterned surface; wherein the back surface of the substrate is disposed adjacent to the back surface of the bottom die; wherein the solder connection is disposed adjacent to the patterned surface of the bottom die, and is electrically coupled to the electrical contact area of the bottom die; and wherein the optical fiber is optically coupled to the oRDL feature.

[092] An example provides a system comprising a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device, the system including a package as provided above.

[093] An example provides a monolithic packaged component, comprising: a substrate having a patterned surface with one or more electrical contact areas and one or more optical contact areas; one or more electrical redistribution layer (eRDL) features; one or more optically-transmissive optical redistribution layer (oRDL) features; and a build-up layer extending over the patterned surface of the substrate, around portions of the eRDL features, and around portions of the oRDL features, wherein the build-up layer has an outer surface with one or more first apertures and one or more second apertures; wherein the eRDL features extend from the electrical contact areas to the first apertures; wherein the oRDL features extend from the optical contact areas to the second apertures; and wherein the oRDL features comprise an optically

transmissive material.

[094] Some embodiments provide a monolithic package component, comprising one or more regions between the patterned surface of the substrate and the outer surface of the build-up layer in which the eRDL features and the oRDL features overlap. Some embodiments provide a monolithic package component, wherein the oRDL features are sheathed along their lengths with reflective liners. Some embodiments provide a monolithic package component, wherein the liners comprise a metal material. Some embodiments provide a monolithic package component, wherein the liners are in direct contact with the oRDL features. Some embodiments provide a monolithic package component, wherein the metal material comprises at least one of: aluminum, copper, titanium, and titanium nitride.

[095] Some embodiments provide a monolithic package component, wherein the oRDL features extend through the second apertures and form posts extending outward from the outer surface of the build-up layer. Some embodiments provide a monolithic package component, comprising one or more solder connections disposed adjacent to the first apertures, wherein the solder connections are electrically coupled to the eRDL features. Some embodiments provide a monolithic package component, wherein the posts extend outward a first distance from the outer surface of the build-up layer, and wherein the solder connections extend outward a second distance from the outer surface of the build-up layer, the second distance being substantially equal to the first distance. Some embodiments provide a monolithic package component, wherein the oRDL features form posts extending outward from the outer surface of the build-up layer, and wherein the oRDL features are sheathed along their lengths with a reflective liner. Some embodiments provide a monolithic package component, wherein a material of the oRDL features comprises polymethyl methacrylate.

[096] An example provides a package comprising: the monolithic packaged component as provided above; and one or more optically-transmissive fibers, wherein the optical fibers are optically coupled to the oRDL feature.

[097] Some embodiments provide a package, comprising: a bottom die having a patterned surface with one or more electrical contact areas and a back surface opposite the patterned surface; and one or more solder connections, wherein the monolithic packaged component has a back surface opposite the patterned surface of the substrate; wherein the back surface of the monolithic packaged component is disposed adjacent to the back surface of the

bottom die; wherein the solder connections are disposed adjacent to the patterned surface of the bottom die; and wherein the solder connections are electrically coupled to at least one of: the electrical contact areas of the bottom die, and the eRDL features of the monolithic packaged component.

[098] Some embodiments provide a package, comprising: a top die having a patterned surface with one or more electrical contact areas; a bottom die having a patterned surface with one or more electrical contact areas and a back surface opposite the patterned surface; and one or more solder connections, wherein the monolithic packaged component has a back surface opposite the patterned surface of the substrate; wherein the back surface of the monolithic packaged component is disposed adjacent to the back surface of the bottom die; and wherein the solder connections are disposed adjacent to the patterned surface of the bottom die; and wherein the solder connections are electrically coupled to at least one of: the electrical contact areas of the bottom die, the eRDL features of the monolithic packaged component, and the electrical contact areas of the top die.

[099] Some embodiments provide a package comprising: the monolithic packaged component as provided above; and a printed circuit board (PCB) including one or more electrical contact areas and one or more optical contact areas, wherein the solder connections of the monolithic packaged component are electrically coupled to the electrical contact areas of the PCB; and the oRDL features of the monolithic packaged component are optically coupled to the optical contact areas of the PCB.

[0100] An example provides a system comprising a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device, the system including the apparatus as provided above.

[0101] An example provides a method of fabricating a packaged component, the method comprising: receiving a substrate having a patterned surface with one or more optical contact areas; depositing a build-up layer over the substrate; patterning the build-up layer to at least partially expose the optical contact areas; depositing an optical redistribution layer (oRDL) above the build-up layer and the exposed optical contact areas; and polishing the oRDL to expose the build-up layer, wherein the polished oRDL is planar with the exposed build-up layer.

[0102] Some embodiments provide a method, wherein the oRDL layer comprises polymethyl methacrylate.

[0103] Some embodiments provide a method, wherein the build-up layer is a first build-up layer, comprising: depositing a liner layer over the first build-up layer and the exposed optical contact areas; and depositing the oRDL over the liner layer, and above the first build-up layer and the exposed optical contact areas.

[0104] Some embodiments provide a method, wherein the patterned surface of the substrate has one or more electrical contact areas, comprising: forming apertures extending completely through the exposed first build-up layer to at least partially expose the electrical contact areas.

[0105] Some embodiments provide a method, wherein the liner layer is a first liner layer, comprising: depositing a second liner layer over the polished oRDL, the exposed build-up layer, and the exposed electrical contact areas; depositing a second build-up layer over the second liner layer; patterning the second build-up layer to expose portions of the second liner layer not covering the oRDL; and removing the exposed portions of the second liner layer to expose the first build-up layer and the exposed electrical contact areas.

[0106] Some embodiments provide a method, wherein a material of the first liner layer and a material of the second liner layer comprise at least one of titanium and titanium nitride.

[0107] Some embodiments provide a method, comprising: depositing a third build-up layer over the first build-up layer, the second liner layer, and the exposed electrical contact areas; forming apertures extending completely through the third build-up layer to at least partially expose the electrical contact areas; depositing an electrical redistribution layer (eRDL) over the third build-up layer and the exposed electrical contact areas; patterning the eRDL to form one or more electrically-conductive pads and one or more eRDL features extending between the electrical contact areas and the electrically-conductive pads; depositing a solder mask over the electrically-conductive pads, the eRDL features, and the third build-up layer; forming apertures extending completely through the solder mask to at least partially expose the electrically-conductive pads; positioning one or more solder connections above the exposed electrically-conductive pads; and soldering the solder connections to electrically couple them to the exposed electrically-conductive pads.

[0108] Some embodiments provide a method, wherein the oRDL is a first oRDL, comprising: depositing a resist layer over the solder mask and the solder connections; patterning the resist layer to expose portions of the solder mask above the first oRDL; forming apertures

extending completely through the resist layer, the solder mask, and the third build-up layer to expose portions of the second liner layer; depositing a third liner layer over the resist layer, over sidewalls of the apertures extending through the resist layer, the solder mask, and the third build-up layer, and over the exposed second liner layer; forming apertures extending completely through the third liner layer and the second liner layer to expose portions of the first oRDL; depositing a second oRDL over the solder mask and the exposed first oRDL; and polishing the second oRDL and portions of the third liner layer, wherein the polishing forms one or more oRDL features comprising portions of the first oRDL and portions of the second oRDL; and wherein the polishing forms one or more liners around the oRDL features comprising portions of the first liner layer, portions of the second liner layer, and portions of the third liner layer.

[0109] Some embodiments provide a method, comprising: removing the resist layer to expose the solder mask, the solder connections, and portions of the liners around the oRDL features.

[0110] An example provides machine readable storage media having machine executable instructions stored thereon that, when executed, cause one or more processors to perform a method as provided above.

[0111] An example provides machine readable storage media having machine executable instructions stored thereon that, when executed, cause one or more processors to perform an operation comprising: receive a substrate having a patterned surface with one or more optical contact areas; deposit a build-up layer over the substrate; pattern the build-up layer to at least partially expose the optical contact areas; deposit an optical redistribution layer (oRDL) above the build-up layer and the exposed optical contact areas; and polish the oRDL to expose the build-up layer, wherein the polished oRDL is planar with the exposed build-up layer.

[0112] Some embodiments provide a machine readable storage media, wherein the oRDL layer comprises polymethyl methacrylate.

[0113] Some embodiments provide a machine readable storage media, wherein the build-up layer is a first build-up layer, the operation comprising: deposit a liner layer over the first build-up layer and the exposed optical contact areas; and deposit the oRDL over the liner layer, and above the first build-up layer and the exposed optical contact areas.

[0114] Some embodiments provide a machine readable storage media, wherein the patterned surface of the substrate has one or more electrical contact areas, the operation

comprising: form apertures extending completely through the exposed first build-up layer to at least partially expose the electrical contact areas.

[0115] Some embodiments provide a machine readable storage media, wherein the liner layer is a first liner layer, the operation comprising: deposit a second liner layer over the polished oRDL, the exposed build-up layer, and the exposed electrical contact areas; deposit a second build-up layer over the second liner layer; pattern the second build-up layer to expose portions of the second liner layer not covering the oRDL; and remove the exposed portions of the second liner layer to expose the first build-up layer and the exposed electrical contact areas.

[0116] Some embodiments provide a machine readable storage media, wherein a material of the first liner layer and a material of the second liner layer comprise at least one of titanium and titanium nitride.

[0117] Some embodiments provide a machine readable storage media, the operation comprising: deposit a third build-up layer over the first build-up layer, the second liner layer, and the exposed electrical contact areas; form apertures extending completely through the third build-up layer to at least partially expose the electrical contact areas; deposit an electrical redistribution layer (eRDL) over the third build-up layer and the exposed electrical contact areas; pattern the eRDL to form one or more electrically-conductive pads and one or more eRDL features extending between the electrical contact areas and the electrically-conductive pads; deposit a solder mask over the electrically-conductive pads, the eRDL features, and the third build-up layer; form apertures extending completely through the solder mask to at least partially expose the electrically-conductive pads; position one or more solder connections above the exposed electrically-conductive pads; and solder the solder connections to electrically couple them to the exposed electrically-conductive pads.

[0118] Some embodiments provide a machine readable storage media, wherein the oRDL is a first oRDL, the operation comprising: deposit a resist layer over the solder mask and the solder connections; pattern the resist layer to expose portions of the solder mask above the first oRDL; form apertures extending completely through the resist layer, the solder mask, and the third build-up layer to expose portions of the second liner layer; deposit a third liner layer over the resist layer, over sidewalls of the apertures extending through the resist layer, the solder mask, and the third build-up layer, and over the exposed second liner layer; form apertures extending completely through the third liner layer and the second liner layer to expose

portions of the first oRDL; deposit a second oRDL over the solder mask and the exposed first oRDL; and polish the second oRDL and portions of the third liner layer, wherein the polishing forms one or more oRDL features comprising portions of the first oRDL and portions of the second oRDL; and wherein the polishing forms one or more liners around the oRDL features comprising portions of the first liner layer, portions of the second liner layer, and portions of the third liner layer.

[0119] Some embodiments provide a machine readable storage media, the operation comprising: remove the resist layer to expose the solder mask, the solder connections, and portions of the liners around the oRDL features.

[0120] An example provides an apparatus comprising: means for receiving a substrate having a patterned surface with one or more optical contact areas; means for depositing a build-up layer over the substrate; means for patterning the build-up layer to at least partially expose the optical contact areas; means for depositing an optical redistribution layer (oRDL) above the build-up layer and the exposed optical contact areas; and means for polishing the oRDL to expose the build-up layer, wherein the polished oRDL is planar with the exposed build-up layer.

[0121] Some embodiments provide an apparatus, wherein the oRDL layer comprises polymethyl methacrylate.

[0122] Some embodiments provide an apparatus, wherein the build-up layer is a first build-up layer, comprising: means for depositing a liner layer over the first build-up layer and the exposed optical contact areas; and means for depositing the oRDL over the liner layer, and above the first build-up layer and the exposed optical contact areas.

[0123] Some embodiments provide an apparatus, wherein the patterned surface of the substrate has one or more electrical contact areas, comprising: means for forming apertures extending completely through the exposed first build-up layer to at least partially expose the electrical contact areas.

[0124] Some embodiments provide an apparatus, wherein the liner layer is a first liner layer, comprising: means for depositing a second liner layer over the polished oRDL, the exposed build-up layer, and the exposed electrical contact areas; means for depositing a second build-up layer over the second liner layer; means for patterning the second build-up layer to expose portions of the second liner layer not covering the oRDL; and means for removing the exposed portions of the second liner layer to expose the first build-up layer and the exposed

electrical contact areas.

[0125] Some embodiments provide an apparatus, wherein a material of the first liner layer and a material of the second liner layer comprise at least one of titanium and titanium nitride.

[0126] Some embodiments provide an apparatus, comprising: means for depositing a third build-up layer over the first build-up layer, the second liner layer, and the exposed electrical contact areas; means for forming apertures extending completely through the third build-up layer to at least partially expose the electrical contact areas; means for depositing an electrical redistribution layer (eRDL) over the third build-up layer and the exposed electrical contact areas; means for patterning the eRDL to form one or more electrically-conductive pads and one or more eRDL features extending between the electrical contact areas and the electrically-conductive pads; means for depositing a solder mask over the electrically-conductive pads, the eRDL features, and the third build-up layer; means for forming apertures extending completely through the solder mask to at least partially expose the electrically-conductive pads; means for positioning one or more solder connections above the exposed electrically-conductive pads; and means for soldering the solder connections to electrically couple them to the exposed electrically-conductive pads.

[0127] Some embodiments provide an apparatus, wherein the oRDL is a first oRDL, comprising: means for depositing a resist layer over the solder mask and the solder connections; means for patterning the resist layer to expose portions of the solder mask above the first oRDL; means for forming apertures extending completely through the resist layer, the solder mask, and the third build-up layer to expose portions of the second liner layer; means for depositing a third liner layer over the resist layer, over sidewalls of the apertures extending through the resist layer, the solder mask, and the third build-up layer, and over the exposed second liner layer; means for forming apertures extending completely through the third liner layer and the second liner layer to expose portions of the first oRDL; means for depositing a second oRDL over the solder mask and the exposed first oRDL; and means for polishing the second oRDL and portions of the third liner layer, wherein the polishing forms one or more oRDL features comprising portions of the first oRDL and portions of the second oRDL; and wherein the polishing forms one or more liners around the oRDL features comprising portions of the first liner layer, portions of the second liner layer, and portions of the third liner layer.

[0128] Some embodiments provide an apparatus, comprising: means for removing the resist layer to expose the solder mask, the solder connections, and portions of the liners around the oRDL features.

[0129] It will be recognized that the principles of the disclosure are not limited to the embodiments so described, but can be practiced with modification and alteration without departing from the scope of the appended claims. For example, the above embodiments may include specific combination of features.

[0130] However, the above embodiments are not limited in this regard and, in various implementations, the above embodiments may include undertaking only a subset of such features, undertaking a different order of such features, undertaking a different combination of such features, and/or undertaking additional features than those features explicitly listed. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

1. A package comprising:

a substrate having a patterned surface with an optical contact area;

an optical redistribution layer (oRDL) feature;

a liner sheathing the oRDL feature; and

a build-up material extending over the patterned surface of the substrate and around portions of the oRDL feature.

2. The package of claim 1,

wherein the optical contact area is in direct contact with the oRDL feature; or

wherein the oRDL feature extends from the optical contact area to an opening in an outer surface of the build-up material; or

wherein the liner comprises one of: an electrically conductive material, and a material having a refractive index below that of a refractive index of the oRDL feature; or

wherein the liner comprises at least one of: aluminum, a copper, titanium, and titanium material.

3. The package of claim 1, wherein the oRDL feature comprises an optically-transmissive material.

4. The package of claim 1, wherein the oRDL feature extend through the openings in an outer surface of the build-up material and forms a post extending outward from the outer surface.

5. The package of claim 1, comprising an electrical redistribution layer (eRDL) feature, wherein the patterned surface of the substrate has an electrical contact area, wherein the build-up material extends around portions of the eRDL feature, and wherein the eRDL feature extends from the electrical contact area to an additional opening in the build-up material.

6. The package of claim 5, comprising a solder connection disposed adjacent to the additional opening in the build-up material, the solder connection being electrically coupled to the

eRDL feature.

7. The package of claim 6, wherein the oRDL feature extends through the opening in the build-up material and forms a post extending outward a first distance from an outer surface of the build-up material, and wherein the solder connection extends outward a second distance from the outer surface of the build-up material, the second distance being substantially equal to the first distance.

8. The package of claim 5, comprising a region between the patterned surface of the substrate and an outer surface of the build-up material in which the oRDL feature and the eRDL feature overlap.

9. A system comprising a memory, a processor coupled to the memory, and a wireless interface for allowing the processor to communicate with another device, the system including the package of any of claims 1 through 8.

10. A method of fabricating a packaged component, the method comprising:
receiving a substrate having a patterned surface with one or more optical contact areas;
depositing a build-up layer over the substrate;
patterning the build-up layer to at least partially expose the optical contact areas;
depositing an optical redistribution layer (oRDL) above the build-up layer and the exposed optical contact areas; and
polishing the oRDL to expose the build-up layer, wherein the polished oRDL is planar with the exposed build-up layer.

11. The method of claim 10, wherein the oRDL layer comprises polymethyl methacrylate.

12. The method of claim 10, wherein the build-up layer is a first build-up layer, comprising:
depositing a liner layer over the first build-up layer and the exposed optical contact areas; and
depositing the oRDL over the liner layer, and above the first build-up layer and the exposed optical contact areas.

13. The method of claim 12, wherein the patterned surface of the substrate has one or more electrical contact areas, comprising:

forming apertures extending completely through the exposed first build-up layer to at least partially expose the electrical contact areas.

14. The method of claim 13, wherein the liner layer is a first liner layer, comprising:

depositing a second liner layer over the polished oRDL, the exposed build-up layer, and the exposed electrical contact areas;

depositing a second build-up layer over the second liner layer;

patterning the second build-up layer to expose portions of the second liner layer not covering the oRDL; and

removing the exposed portions of the second liner layer to expose the first build-up layer and the exposed electrical contact areas.

15. The method of claim 14, wherein a material of the first liner layer and a material of the second liner layer comprise at least one of titanium and titanium nitride.

16. The method of claim 14, comprising:

depositing a third build-up layer over the first build-up layer, the second liner layer, and the exposed electrical contact areas;

forming apertures extending completely through the third build-up layer to at least partially expose the electrical contact areas;

depositing an electrical redistribution layer (eRDL) over the third build-up layer and the exposed electrical contact areas;

patterning the eRDL to form one or more electrically-conductive pads and one or more eRDL features extending between the electrical contact areas and the electrically-conductive pads;

depositing a solder mask over the electrically-conductive pads, the eRDL features, and the third build-up layer;

forming apertures extending completely through the solder mask to at least partially expose the

electrically-conductive pads;

positioning one or more solder connections above the exposed electrically-conductive pads; and

soldering the solder connections to electrically couple them to the exposed electrically-conductive pads.

17. The method of claim 16, wherein the oRDL is a first oRDL, comprising:

depositing a resist layer over the solder mask and the solder connections;

patterning the resist layer to expose portions of the solder mask above the first oRDL;

forming apertures extending completely through the resist layer, the solder mask, and the third build-up layer to expose portions of the second liner layer;

depositing a third liner layer over the resist layer, over sidewalls of the apertures extending through the resist layer, the solder mask, and the third build-up layer, and over the exposed second liner layer;

forming apertures extending completely through the third liner layer and the second liner layer to expose portions of the first oRDL;

depositing a second oRDL over the solder mask and the exposed first oRDL; and

polishing the second oRDL and portions of the third liner layer,

wherein the polishing forms one or more oRDL features comprising portions of the first oRDL and portions of the second oRDL; and

wherein the polishing forms one or more liners around the oRDL features comprising portions of the first liner layer, portions of the second liner layer, and portions of the third liner layer.

18. Machine readable storage media having machine executable instructions stored thereon that, when executed, cause one or more processors to perform a method according to any one of claims 10 through 17.

19. An apparatus comprising:

means for receiving a substrate having a patterned surface with one or more optical contact areas;

means for depositing a build-up layer over the substrate;

means for patterning the build-up layer to at least partially expose the optical contact areas;

means for depositing an optical redistribution layer (oRDL) above the build-up layer and the exposed optical contact areas; and

means for polishing the oRDL to expose the build-up layer, wherein the polished oRDL is planar with the exposed build-up layer.

20. The apparatus of claim 19, wherein the oRDL layer comprises polymethyl methacrylate.

21. The apparatus of either of claims 19 or 20, wherein the build-up layer is a first build-up layer, comprising:

means for depositing a liner layer over the first build-up layer and the exposed optical contact areas; and

means for depositing the oRDL over the liner layer, and above the first build-up layer and the exposed optical contact areas.

22. The apparatus of claim 21, wherein the patterned surface of the substrate has one or more electrical contact areas, comprising:

means for forming apertures extending completely through the exposed first build-up layer to at least partially expose the electrical contact areas.

23. The apparatus of claim 22, wherein the liner layer is a first liner layer, comprising:

means for depositing a second liner layer over the polished oRDL, the exposed build-up layer, and the exposed electrical contact areas;

means for depositing a second build-up layer over the second liner layer;

means for patterning the second build-up layer to expose portions of the second liner layer not covering the oRDL; and

means for removing the exposed portions of the second liner layer to expose the first build-up layer and the exposed electrical contact areas.

24. The apparatus of claim 23, comprising:

means for depositing a third build-up layer over the first build-up layer, the second liner layer,

and the exposed electrical contact areas;

means for forming apertures extending completely through the third build-up layer to at least partially expose the electrical contact areas;

means for depositing an electrical redistribution layer (eRDL) over the third build-up layer and the exposed electrical contact areas;

means for patterning the eRDL to form one or more electrically-conductive pads and one or more eRDL features extending between the electrical contact areas and the electrically-conductive pads;

means for depositing a solder mask over the electrically-conductive pads, the eRDL features, and the third build-up layer;

means for forming apertures extending completely through the solder mask to at least partially expose the electrically-conductive pads;

means for positioning one or more solder connections above the exposed electrically-conductive pads; and

means for soldering the solder connections to electrically couple them to the exposed electrically-conductive pads.

25. The apparatus of claim 24, wherein the oRDL is a first oRDL, comprising:

means for depositing a resist layer over the solder mask and the solder connections;

means for patterning the resist layer to expose portions of the solder mask above the first oRDL;

means for forming apertures extending completely through the resist layer, the solder mask, and the third build-up layer to expose portions of the second liner layer;

means for depositing a third liner layer over the resist layer, over sidewalls of the apertures extending through the resist layer, the solder mask, and the third build-up layer, and over the exposed second liner layer;

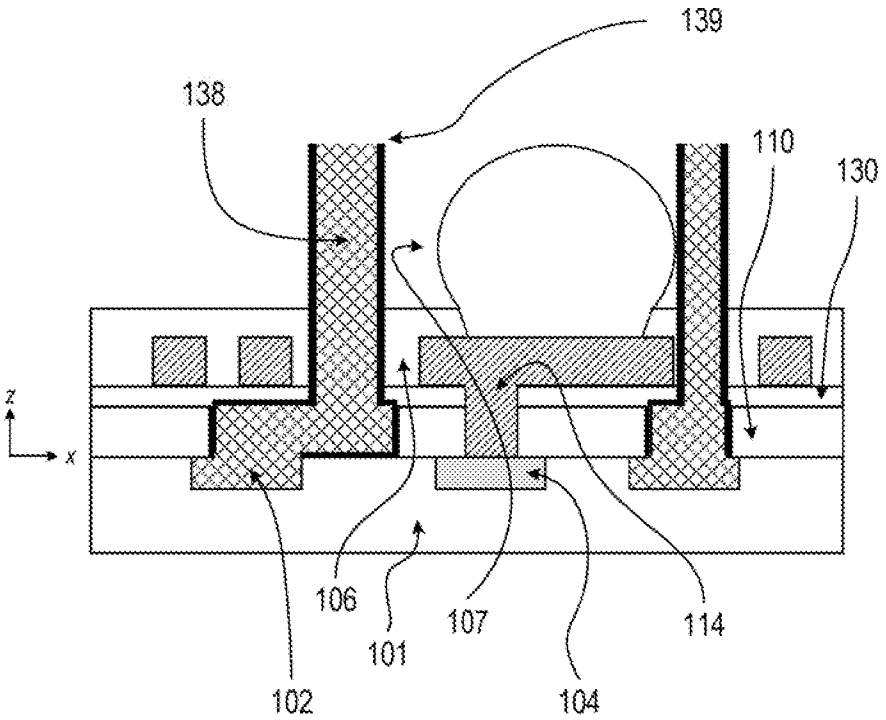
means for forming apertures extending completely through the third liner layer and the second liner layer to expose portions of the first oRDL;

means for depositing a second oRDL over the solder mask and the exposed first oRDL; and

means for polishing the second oRDL and portions of the third liner layer,

wherein the polishing forms one or more oRDL features comprising portions of the first oRDL and portions of the second oRDL; and

wherein the polishing forms one or more liners around the oRDL features comprising portions of the first liner layer, portions of the second liner layer, and portions of the third liner layer.



100

FIG. 1

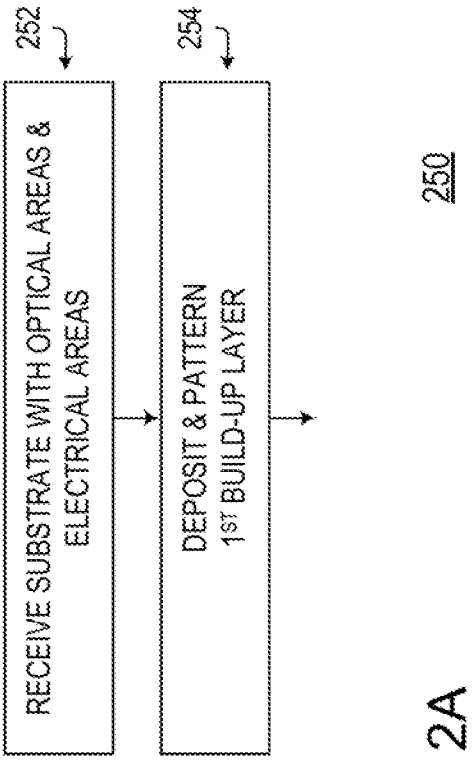
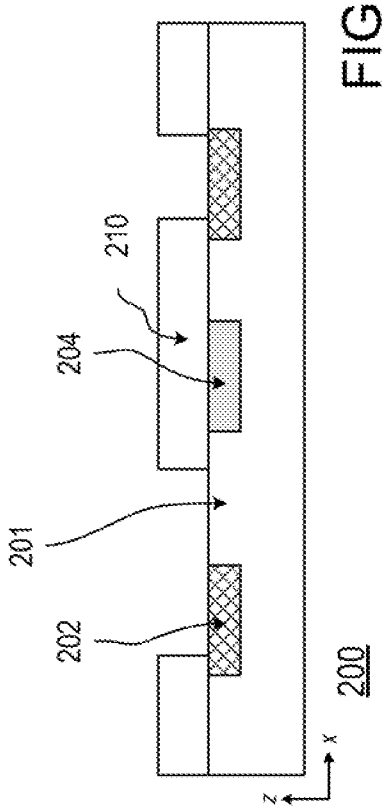

252
RECEIVE SUBSTRATE WITH OPTICAL AREAS & ELECTRICAL AREAS
254
DEPOSIT & PATTERN 1ST BUILD-UP LAYER
250

FIG. 2A


210
204
201
202
200
x
z

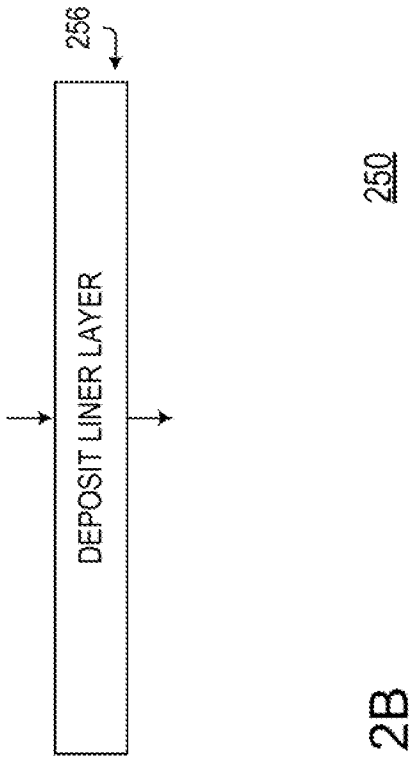
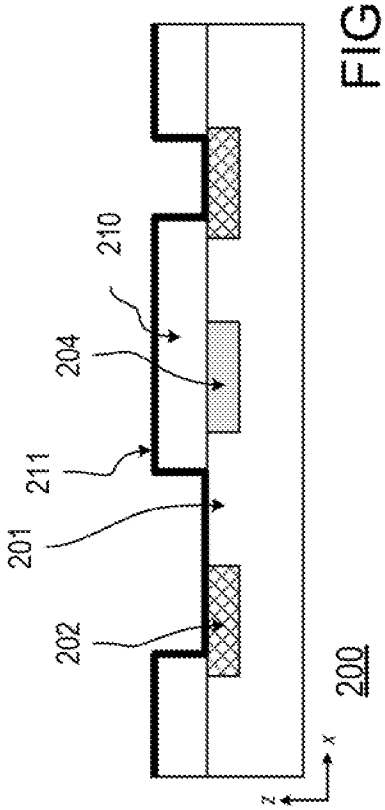

256
DEPOSIT LINER LAYER
250

FIG. 2B


210
204
211
201
202
200
x
z

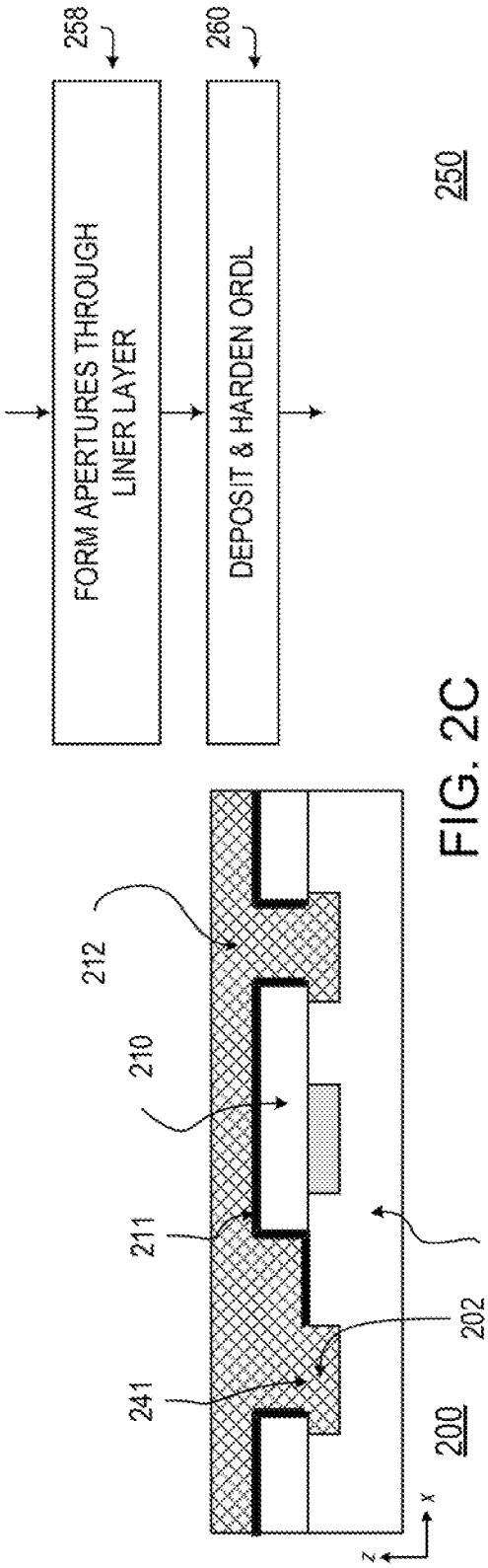

258
FORM APERTURES THROUGH LINER LAYER
260
DEPOSIT & HARDEN ORDL
250
212
210
211
241
202
201
200
z
x

FIG. 2C

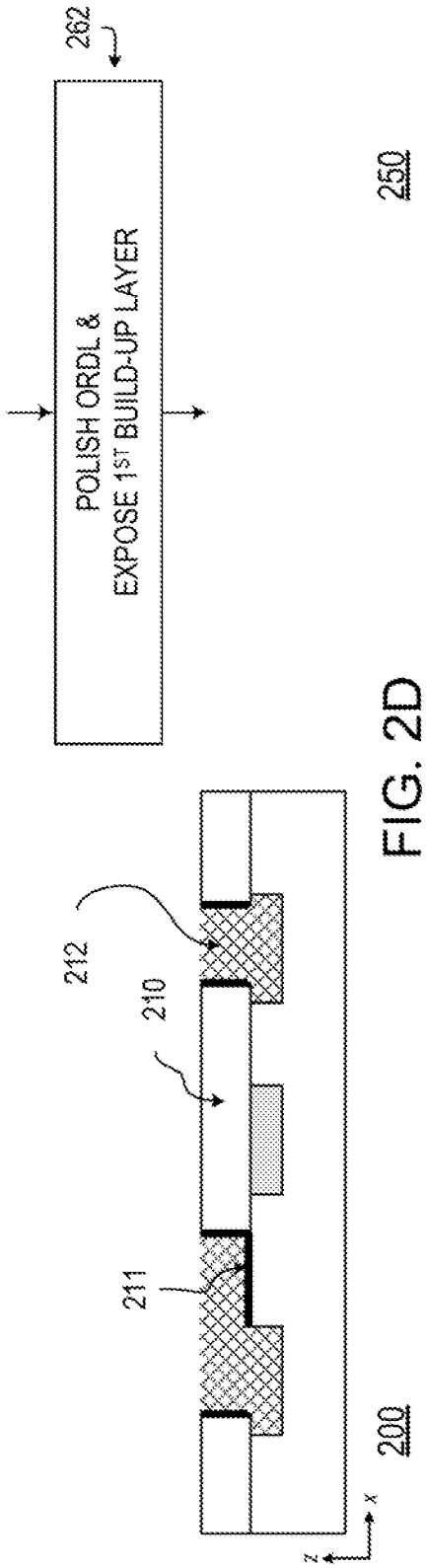

262
POLISH ORDL & EXPOSE 1ST BUILD-UP LAYER
250
212
210
211
200
z
x

FIG. 2D

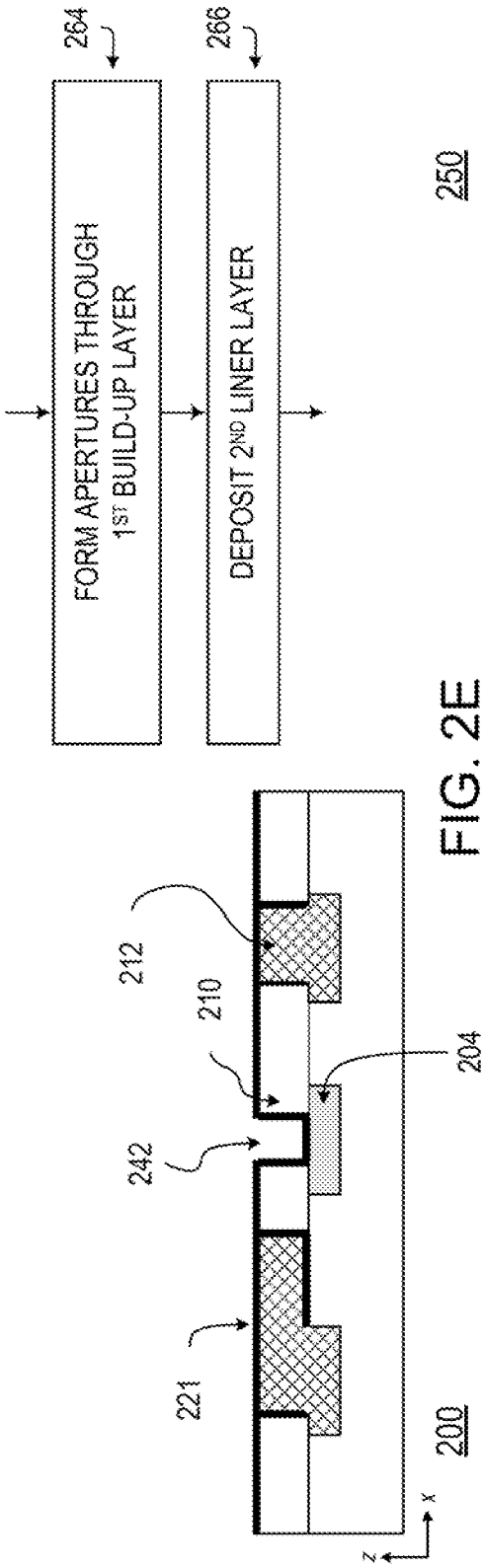

264
FORM APERTURES THROUGH 1ST BUILD-UP LAYER
266
DEPOSIT 2ND LINER LAYER
250
212
210
204
242
221
200
x
z

FIG. 2E

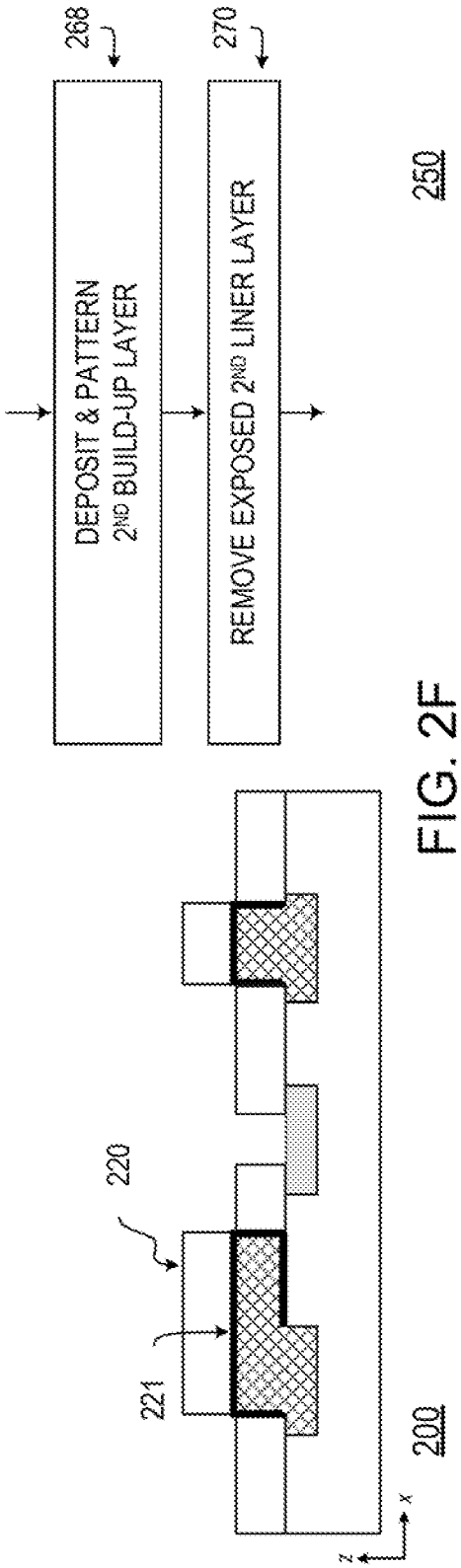

268
DEPOSIT & PATTERN 2ND BUILD-UP LAYER
270
REMOVE EXPOSED 2ND LINER LAYER
250
220
221
200
x
z

FIG. 2F

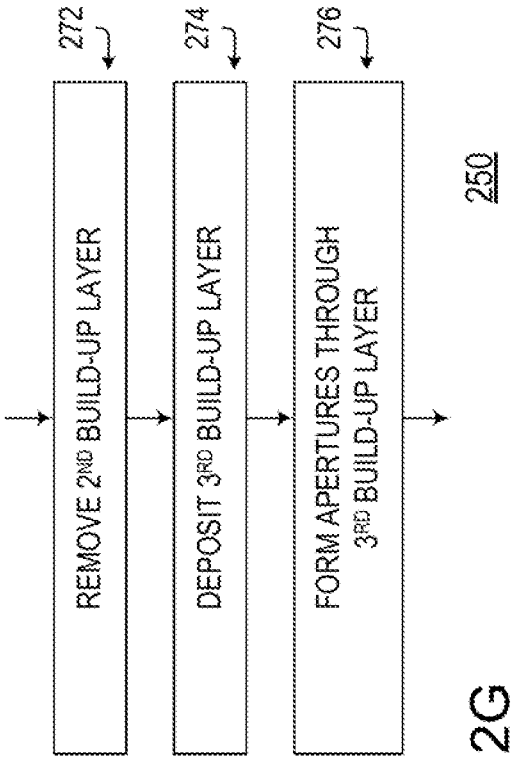
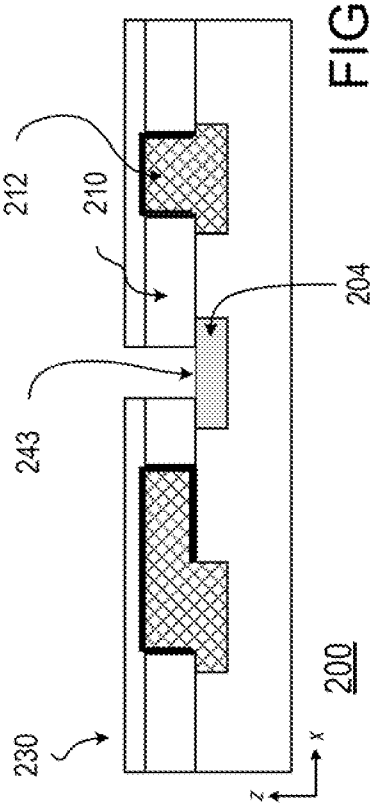

272
274
276
REMOVE 2ND BUILD-UP LAYER
DEPOSIT 3RD BUILD-UP LAYER
FORM APERTURES THROUGH 3RD BUILD-UP LAYER
250

FIG. 2G


212
210
204
243
230
200
x
z

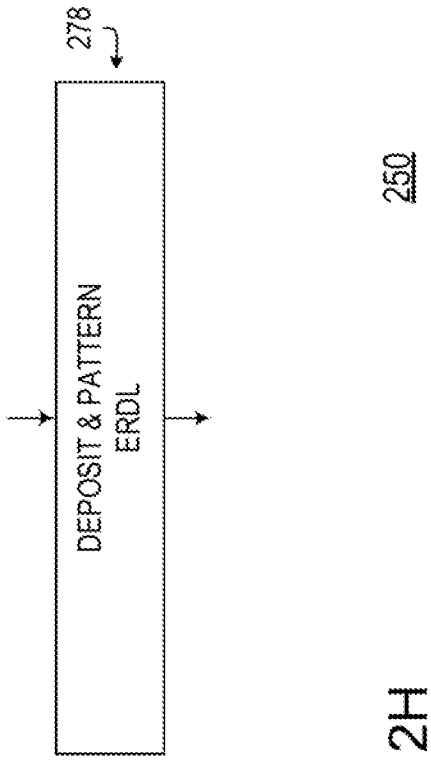
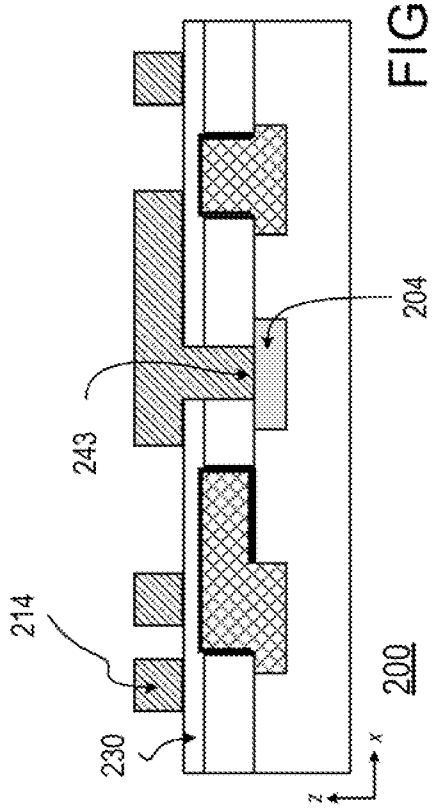

278
DEPOSIT & PATTERN ERDL
250

FIG. 2H


214
204
243
230
200
x
z

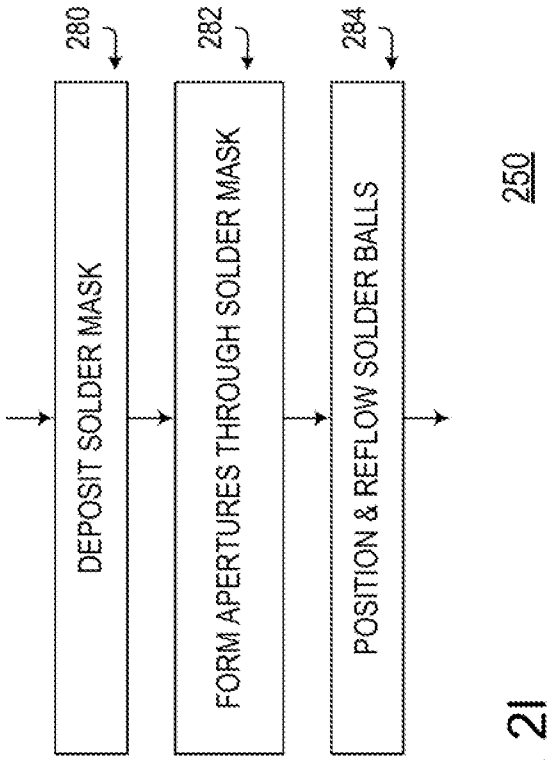
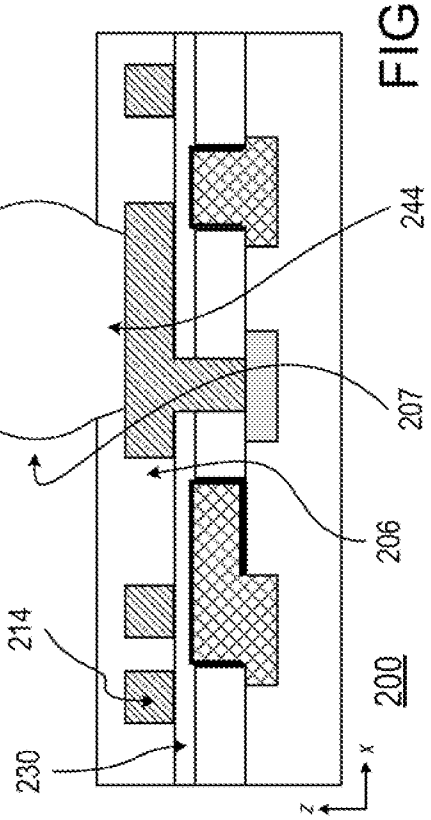

280
DEPOSIT SOLDER MASK
282
FORM APERTURES THROUGH SOLDER MASK
284
POSITION & REFLOW SOLDER BALLS
250

FIG. 2I


244
207
206
214
230
200
x
z

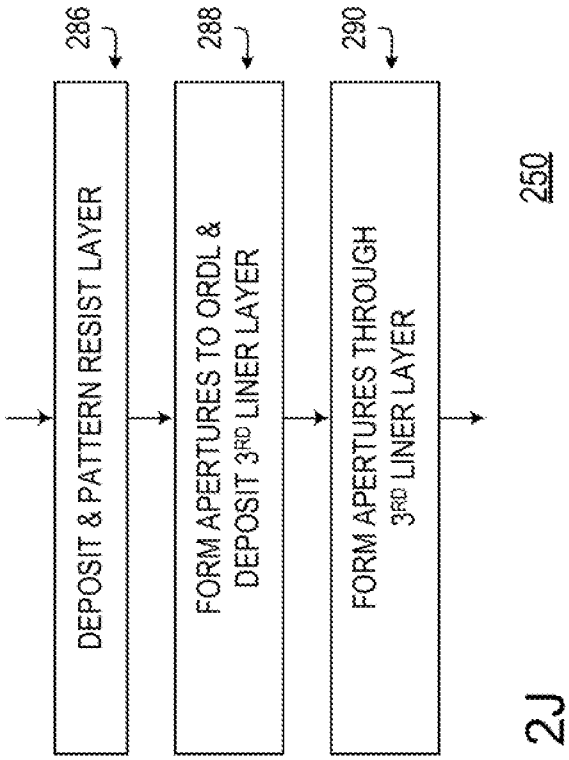
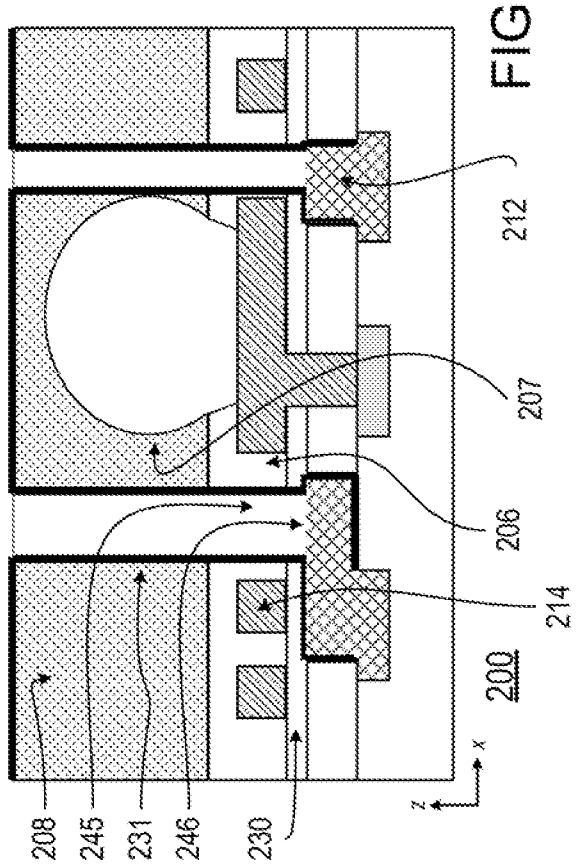

286
DEPOSIT & PATTERN RESIST LAYER
288
FORM APERTURES TO ORDL & DEPOSIT 3RD LINER LAYER
290
FORM APERTURES THROUGH 3RD LINER LAYER
250

FIG. 2J


212
207
206
214
208
245
231
246
230
200
x
z

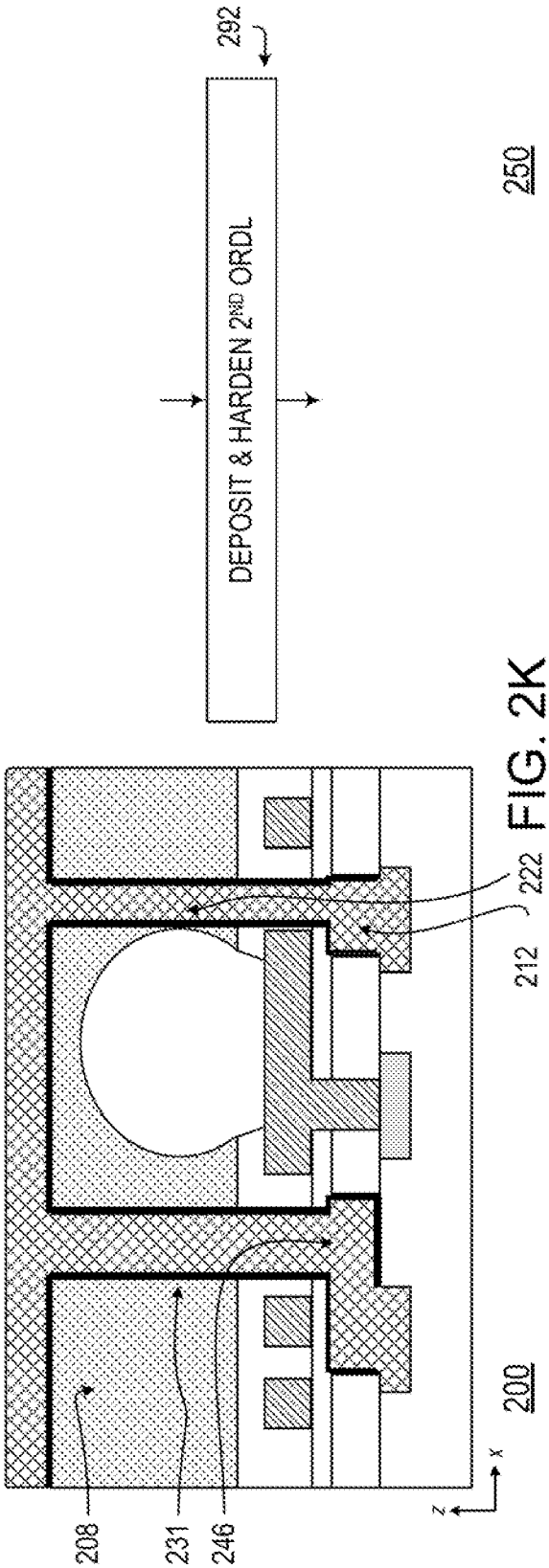

292
DEPOSIT & HARDEN 2ND ORDL
250
222
212
200
208
231
246
x
z

FIG. 2K

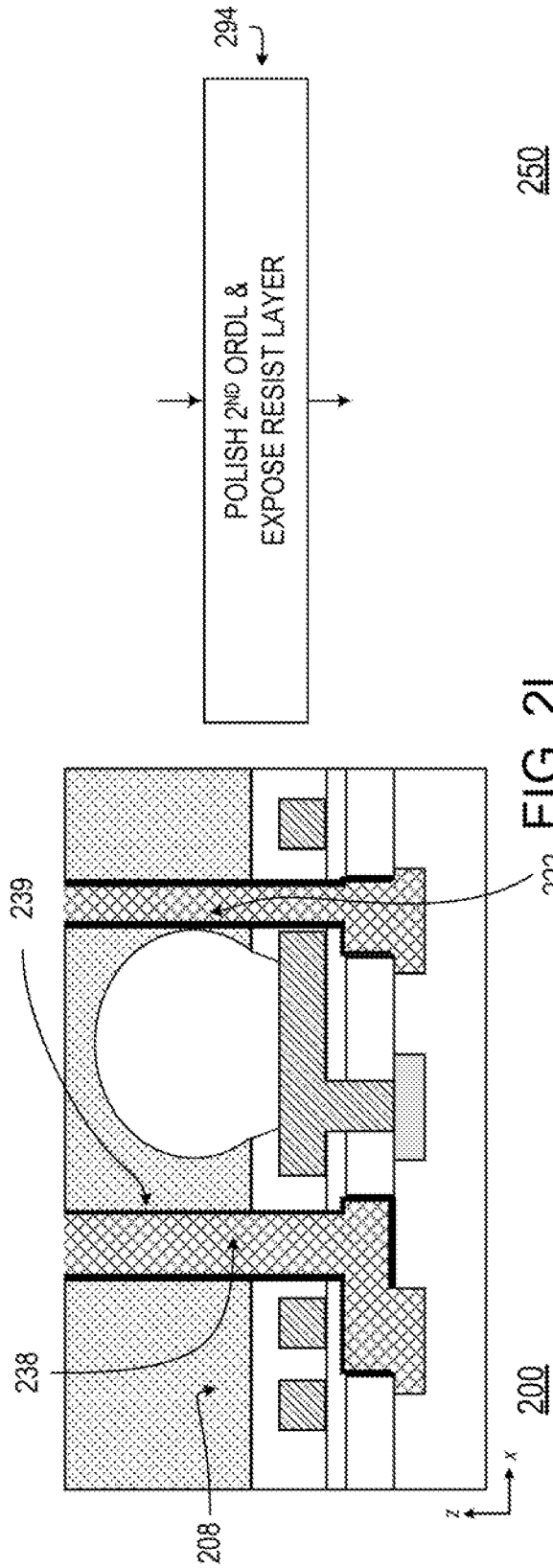

294
POLISH 2ND ORDL &
EXPOSE RESIST LAYER
250
222
239
238
200
208
x
z

FIG. 2L

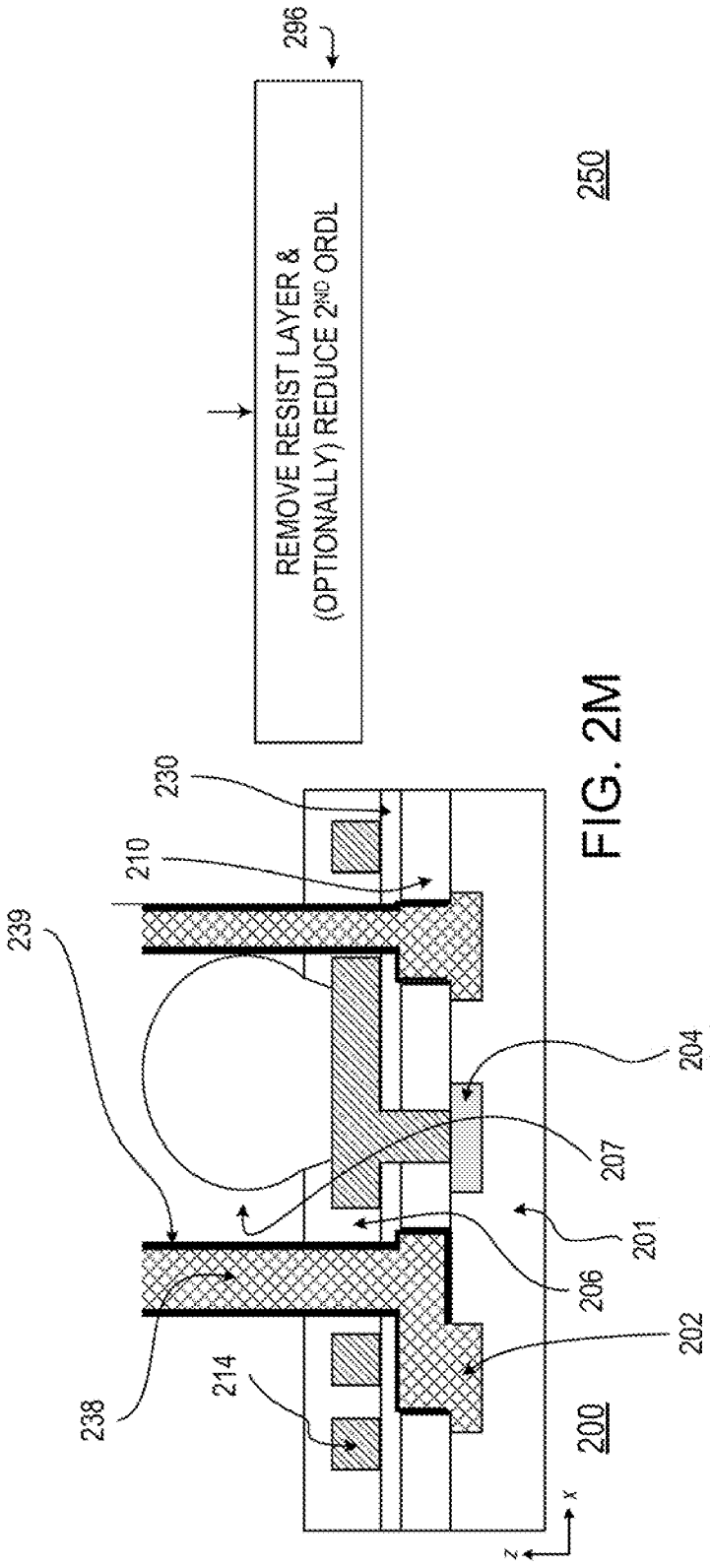
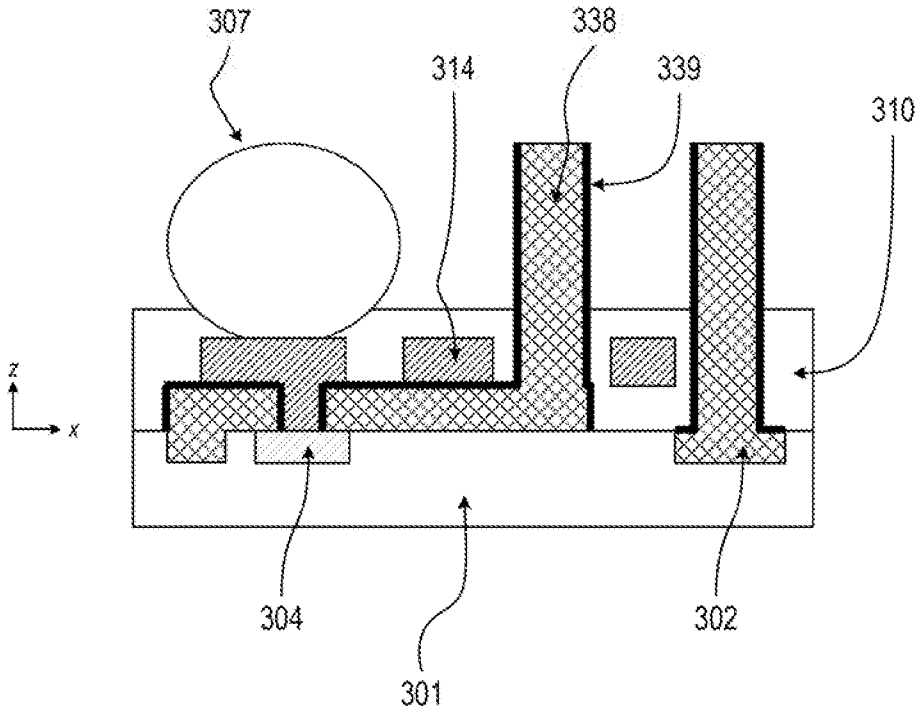

296
REMOVE RESIST LAYER &
(OPTIONALLY) REDUCE 2ND ORDL
250
230
210
239
204
207
201
206
202
214
238
200
x
z

FIG. 2M



300

FIG. 3

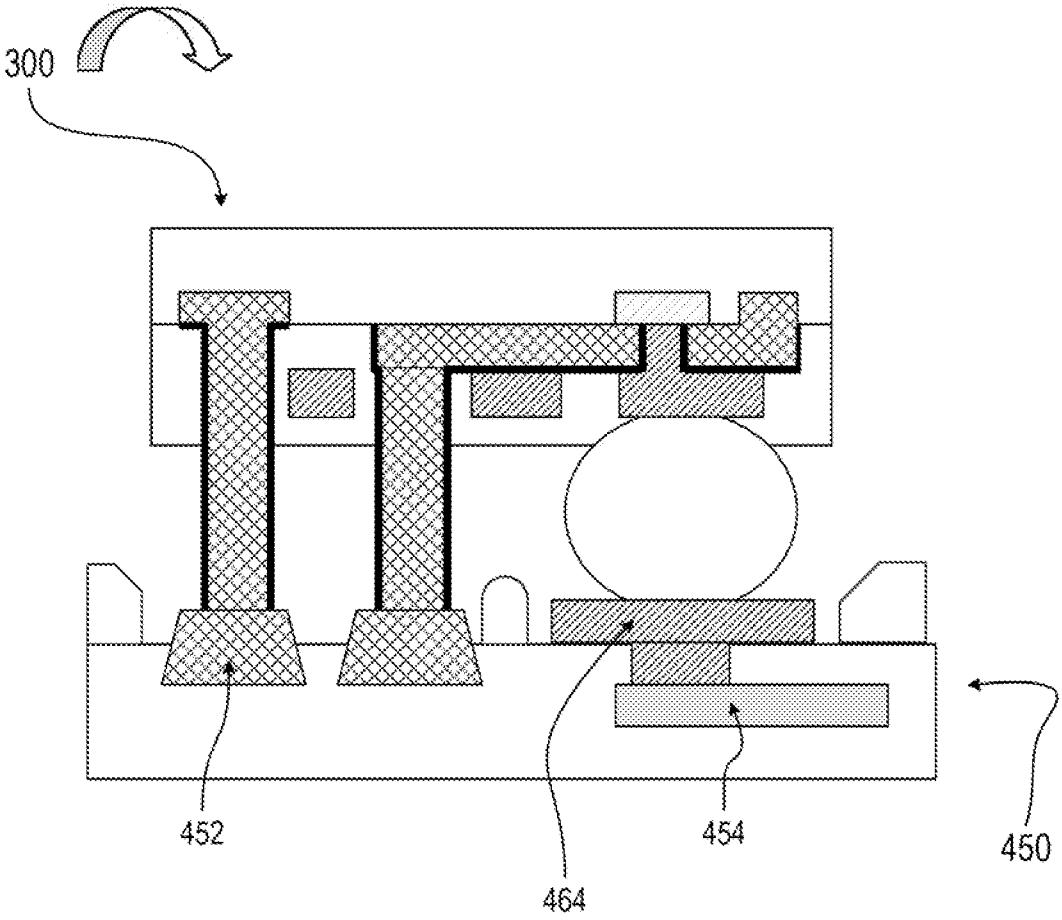


FIG. 4

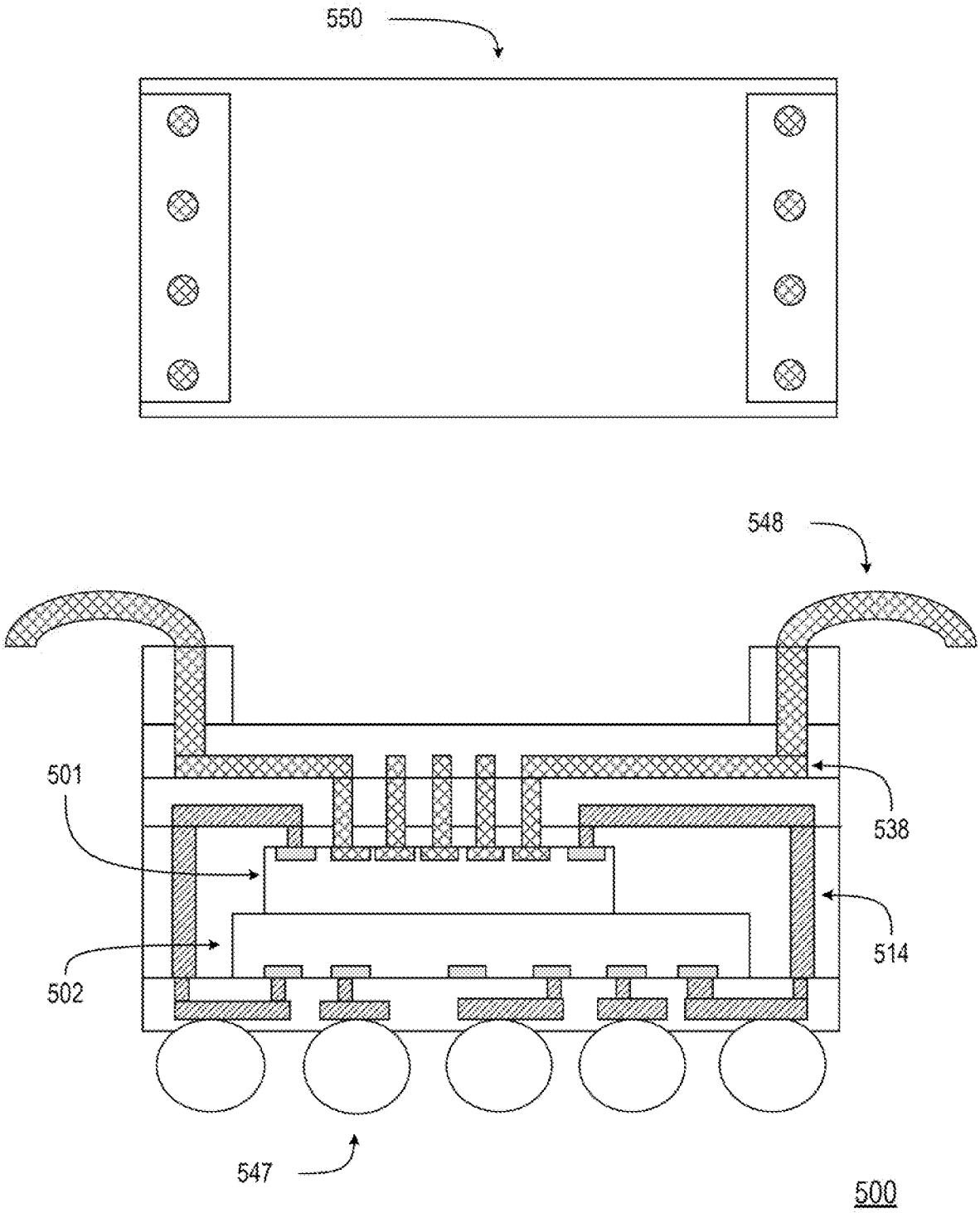


FIG. 5

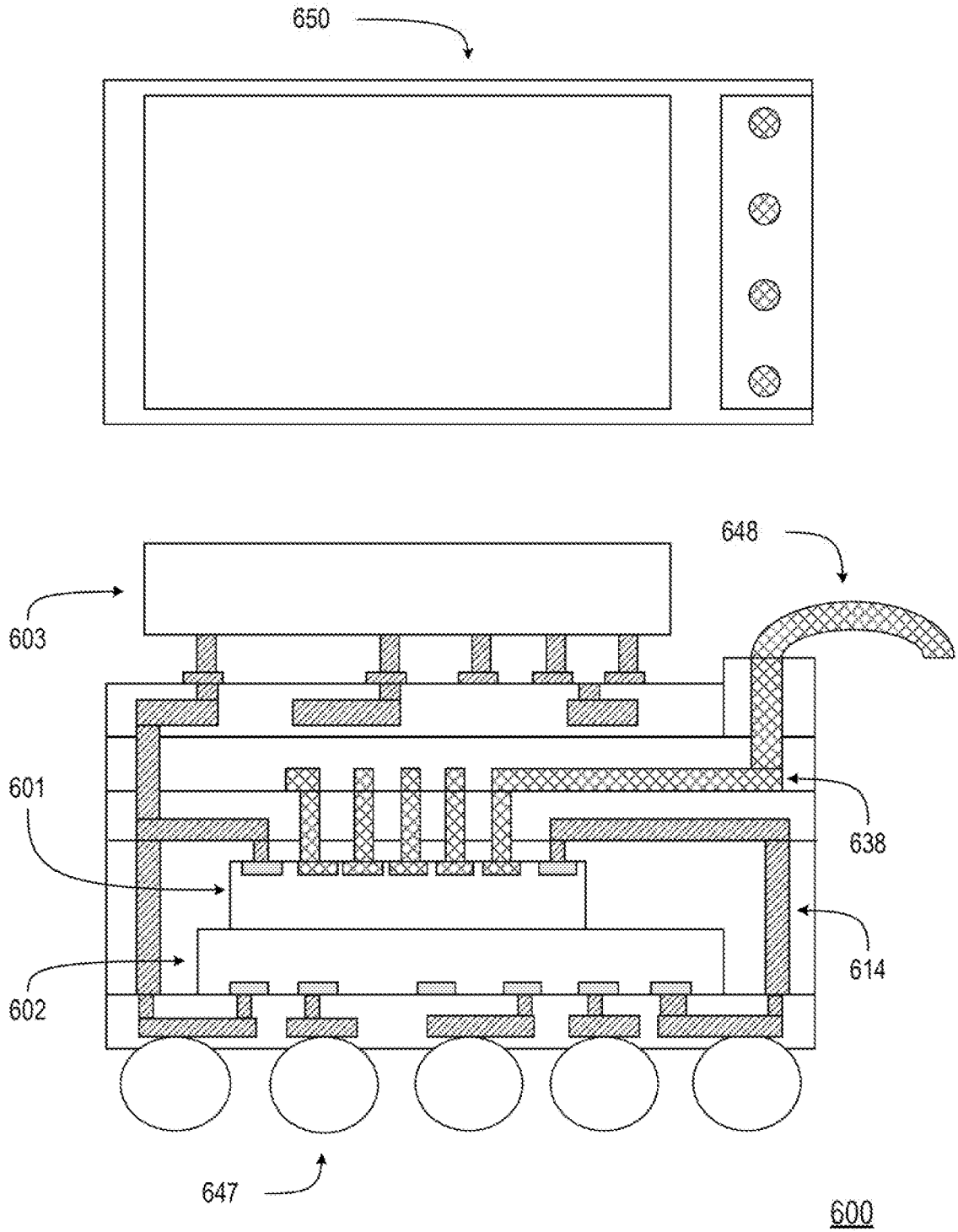


FIG. 6

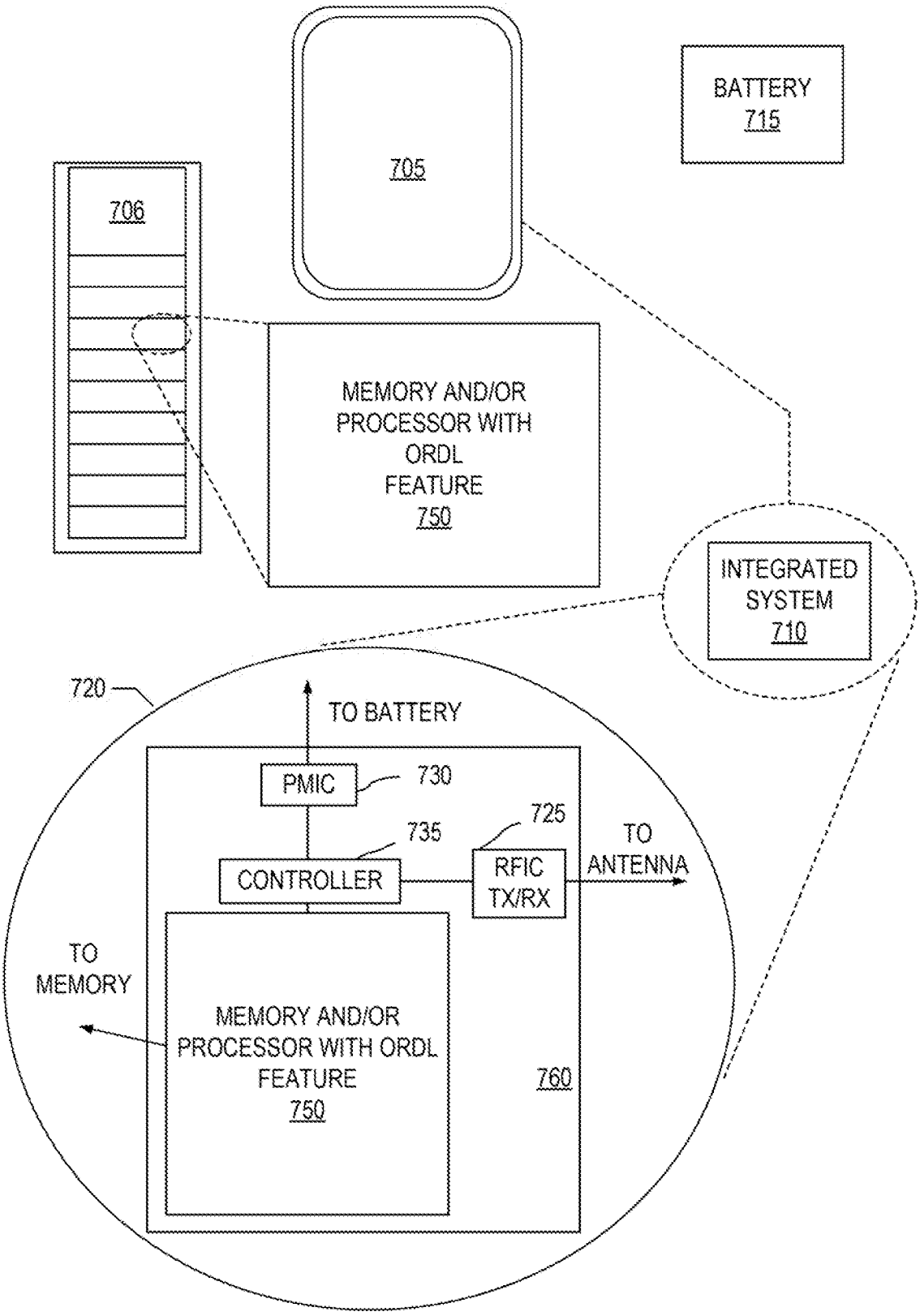

705
BATTERY
715
706
MEMORY AND/OR
PROCESSOR WITH
ORDL
FEATURE
750
INTEGRATED
SYSTEM
710
720
TO BATTERY
PMIC
730
735
725
TO
ANTENNA
CONTROLLER
RFIC
TX/RX
TO
MEMORY
MEMORY AND/OR
PROCESSOR WITH ORDL
FEATURE
750
760

FIG. 7

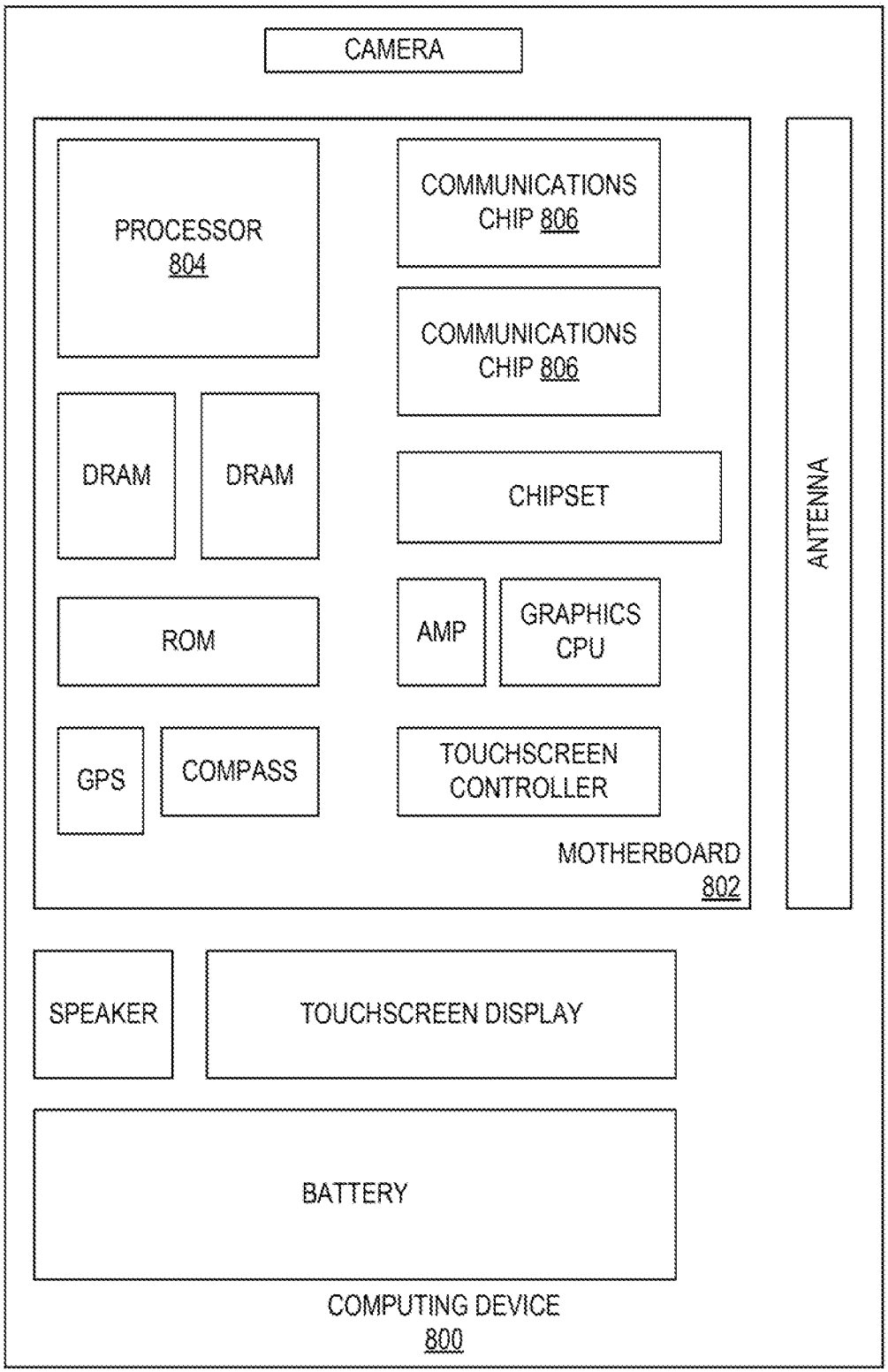

CAMERA
PROCESSOR 804
COMMUNICATIONS CHIP 806
COMMUNICATIONS CHIP 806
DRAM
DRAM
CHIPSET
ROM
AMP
GRAPHICS CPU
GPS
COMPASS
TOUCHSCREEN CONTROLLER
MOTHERBOARD 802
ANTENNA
SPEAKER
TOUCHSCREEN DISPLAY
BATTERY
COMPUTING DEVICE 800

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/020278

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/522(2006.01)i, H01L 23/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/522; H01L 21/304; H01L 31/02; H01L 25/16; H01L 23/00; H01L 23/48; H01L 23/58

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: package, optical, redistribution, layer, circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9287417 B2 (XINTEC INC.) 15 March 2016 See claims 5, 7 and figure 2.	1-25
A	US 2015-0364453 A1 (AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.) 17 December 2015 See paragraphs [0003], [0030], claims 1-5 and figure 2E.	1-25
A	US 2014-0106507 A1 (INTEL MOBILE COMMUNICATIONS GMBH) 17 April 2014 See paragraphs [0057]-[0058] and figures 7G-7H.	1-25
A	US 2009-0243045 A1 (REZA A. PAGAILA et al.) 01 October 2009 See paragraph [0060], claims 1-3 and figure 8d.	1-25
A	US 8536672 B2 (SHU-MING CHANG et al.) 17 September 2013 See claims 1-4 and figure 3.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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31 May 2017 (31.05.2017)	**31 May 2017 (31.05.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US2017/020278

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 9287417 B2	15/03/2016	CN 103943641 A	23/07/2014
		TW 201431023 A	01/08/2014
		US 2014-203387 A1	24/07/2014
US 2015-0364453 A1	17/12/2015	DE 102013220360 A1	10/04/2014
		US 2014-097536 A1	10/04/2014
		US 9177884 B2	03/11/2015
US 2014-0106507 A1	17/04/2014	US 9165841 B2	20/10/2015
US 2009-0243045 A1	01/10/2009	US 2012-034777 A1	09/02/2012
		US 8072079 B2	06/12/2011
		US 8940636 B2	27/01/2015
US 8536672 B2	17/09/2013	CN 102194781 A	21/09/2011
		CN 102194781 B	04/11/2015
		CN 105047629 A	11/11/2015
		TW 201143074 A	01/12/2011
		TW I508273 B	11/11/2015
		US 2011-227186 A1	22/09/2011