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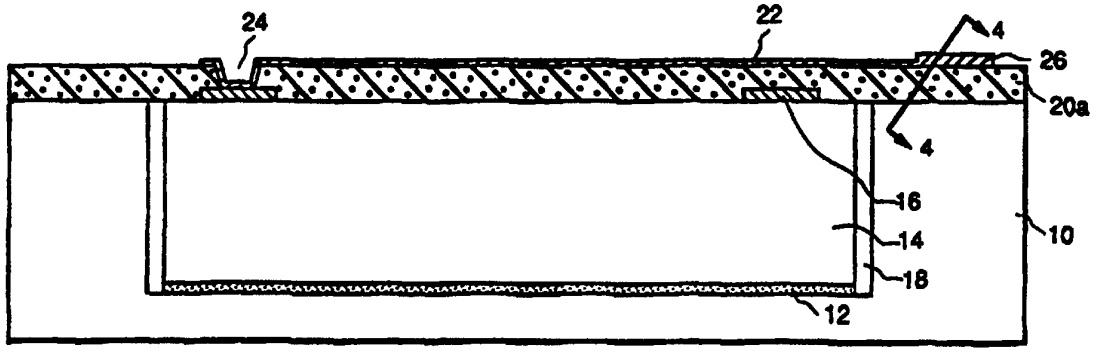

(57) Abstract

A method for processing a low dielectric constant material includes dispersing an additive material in a porous low dielectric constant layer, fabricating a desired electronic structure, and then removing the additive material from the pores of the low dielectric constant layer. The removal of the additive material from the pores can be accomplished by sublimation, evaporation, and diffusion. Applications for the low dielectric constant layer include the use as an overlay layer (20a) for interconnecting a circuit chip (14) supported by a substrate (10) and the use as printed circuit board material (110).

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PROCESSING LOW DIELECTRIC CONSTANT MATERIALS FOR HIGH SPEED ELECTRONICS

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to low dielectric constant porous materials and, more particularly, to a process for using porous layers in printed circuit boards and over electronic circuits and supporting substrates.

Description of the Related Art

Electronic circuits have inherent limitations in high frequency applications. For example, capacitive loading is increased at higher frequencies because capacitive reactance is directly proportional to frequency. In high frequency circuits capacitive loading becomes so high that a semiconductor chip cannot drive the low reactive impedance. Because these high frequency circuits have historically been power inefficient, their usefulness in airborne and satellite applications is limited.

Foam cored cable technology has been used for years in attempts to reduce capacitive loading of electronic signals. Porous polytetrafluoroethylene (PTFE) materials such as Gortex™ (Gortex is a trademark of W.L. Gore & Associates, Inc., of Newark, DE) have excellent low dielectric constant properties, but unfortunately they absorb process chemicals in their pores during MCM (multi-chip module) or PC (printed circuit) board processing that cannot be removed. Additionally, the fact that the porous material deforms during pressurized processing destroys its porous properties, and therefore the deformed material does not provide the desired consistent low dielectric constant.

In microwave circuit chip structures, certain electrical conductor paths in sensitive areas of the chip circuitry require a dielectric constant close to that of air (1) to work properly in these areas. Chip manufacturers fabricate air bridges to provide the low dielectric constant. These sensitive air bridge structures create processing challenges for both the manufacturer and the end user. Even Teflon polytetrafluoroethylene (Teflon is a trademark of E.I. DuPont de Nemours and Co.), which typically has a dielectric constant between 1.9 and 2.0, can create too much of an impedance loading effect at microwave frequencies.

The DuPont Teflon polytetrafluoroethylene line of materials has intrinsically low dielectric constants and has the necessary high temperature stability for most industrial and military uses. As described in Gore, U.S. Patent No. 3,962,153, and Gore, U.S. Patent No. 4,096,227, Gortex material is a Teflon PTFE-based material that is filled with micro-pores that create a foam-like cloth material. Porous PTFE material is generally used in clothes to simultaneously provide warmth and allow perspiration and moisture vapors to vent through its pores. Porous PTFE material is alternatively sold as a filled porous PTFE material. Filling the pores with a material such as an acrylate glue enables use of the material as a laminant film; however, this causes the resultant dielectric constant to degrade and limits the material's usefulness at high frequencies. Unfilled porous PTFE material is an excellent candidate for high frequency circuits because the dielectric constant can be significantly less than that found in other materials. However, in laminant applications and processing, the pores can collapse under pressure and/or be filled with processing materials during fabrication which cannot be easily removed.

Ceramic foam materials are discussed, for example, in "Giants in advanced ceramics," Ceramic Industry, vol. 141, 47 (August 1993), and Te-Kao Wu, "Dielectric properties measurement of substrate and support materials," Microwave and Optical Technology Letters, vol. 3, 283-286 (August 1990). These materials, however, are inflexible and not fabricated in large area sections. Because the ceramic foam materials are inflexible, they can be used as substrates but cannot be used in overlay technologies that are not perfectly flat. Because ceramic foam materials are fragile, they are typically not capable of withstanding PC board lamination processing in their intrinsic state. Furthermore, ceramic foam materials can be filled with processing materials which degrade their low dielectric constant.

Another problem common to both porous PTFE material and ceramic foam material is that if the porous/foam material is to be used in any process in which a metallization layer is applied over the material, the metal tends to extend into the pores and it is thus difficult to achieve a smooth and continuous metal surface for use in high frequency applications where skin-effect related losses are of importance.

Few intrinsically low dielectric constant materials can withstand the high temperatures in commercial and military processing. Most of the low dielectric constant materials that can withstand higher temperatures are only absorptive below the 200 nanometer wavelength region of the light spectrum, and thus it is nearly impossible to process those materials using ion argon and other CW (continuous wave) lasers.

Polymer materials in high frequency circuits are preferably laser ablatable by ultraviolet light in order to

form the via openings through which different layers of metallization are connected. Laser processing (ablation, photoresist exposure, etc.) is normally done with several passes of the laser beam with a power ranging from 0.5 to 2.0 watts, with a preferred maximum power level being about 1.5 watts. Thus, when a dielectric layer is characterized as being laser ablatable, it means that such layer can be totally removed by progressive passes of a laser beam of this power level, and when it is characterized as not being laser ablatable, it means that a layer is not completely removed by progressive passes of such a laser beam. One method of adaptive laser ablation is discussed in Eichelberger et al., U.S. Patent No. 4,835,704. Most polytetrafluoroethylene materials are not laser ablatable and generally do not easily adhere to other materials. A method of modifying the ultraviolet absorption characteristics of a polymer material with the addition of an ultraviolet absorbing dye is discussed is Cole et al., U.S. Patent No. 5,169,678.

To minimize the complexity and cost of equipment for fabricating high density interconnect structures, it is considered desirable to be able to do all laser processing at a single frequency in order that only a single laser is required. Accordingly, preferred materials are those which can be processed at a laser frequency of 351 nm. This frequency was selected in accordance with the characteristics of desirable dielectric layers such as Kapton™ polyimide (Kapton is a trademark of E.I. DuPont de Nemours and Co.) and the fact that there are commercial photoresists which can be processed at this frequency. Ultem™ polyetherimide resin (Ultem is a registered trademark of General Electric Co.) has been used as an adhesive layer in this high density interconnect structure

for bonding Kapton polyimide to the underlying structures. The Ultem polyetherimide resin is laser ablatable at 351 nm.

PC boards typically have dielectric constants ranging from 2 through 5, and nonporous ceramics can have dielectric constants as high as 9. It would be desirable to have a low dielectric constant PC board material for use in high frequency and high speed electronics.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a new material and method of manufacturing high frequency and high speed electronic circuits with low power capabilities.

Another object of this invention is to provide a method for processing low dielectric constant porous materials which does not leave process chemicals behind in the porous materials.

Another object of this invention is to provide a method for adding materials to the pores of the porous material that allow laser processing at an ultra-violet (UV) wavelength of about 350 nanometers (nm).

Another object of this invention is to provide low dielectric constant polymer and ceramic PC boards.

This invention modifies a low dielectric constant polymeric porous material, such as porous PTFE material, which has a dielectric constant of approximately 1.2-1.3, by filling the material's pores with a sublimable (or otherwise removable) material that prevents deformation and enables laser processing during high speed circuit fabrication. The term "low dielectric constant" is intended to mean a dielectric constant as close to 1 as possible and not greater than about 2. After processing, the filler material is

removed, and the original porous material is left with the intrinsically low dielectric constant. The process, which enables foam-like materials to be laminated and laser machined without the use of solvents or other chemical processing, can be used in PC boards, MCM modules, and anywhere else low dielectric constant surfaces are desired.

Porous PTFE material is approximately 70% air and is generally made by stretching PTFE to cause approximately nine billion holes per square inch to be distributed evenly throughout its volume. This porous structure is composed of mostly air and can readily be filled with a sublimable material. The resulting porous material can be used as a low dielectric constant material in the manufacture of high frequency circuits and can reduce the need for laser ablation of material situated over air bridge structures and other microwave structures and devices.

Briefly, in accordance with a preferred embodiment of the invention, a method for applying a low dielectric constant material over a substrate comprises dispersing an additive material in a low dielectric constant layer; attaching the layer to a surface of the substrate; and removing the additive material from the layer. In one embodiment the low dielectric constant layer is a porous layer comprising polytetrafluoroethylene. The step of removing the additive material from the layer comprises subliming, evaporating, and/or diffusing away the additive material. The substrate can support a circuit chip having chip pads on a connection surface. In this embodiment the step of attaching the porous layer to the surface of the substrate includes attaching the porous layer to the connection surface of the circuit chip, and further steps include forming at least one via in the porous layer extending to at least one of the chip pads and applying a

pattern of electrically conductive material over the porous layer extending into the at least one via.

In accordance with another preferred embodiment of the invention, a method for applying and ablating a low dielectric constant material over a substrate comprises attaching a low dielectric constant polymer layer to a surface of the substrate; applying mask material over the polymer layer; forming a via in the mask material extending through to the polymer layer; diffusing an additive material in a region of the polymer layer through the via in the mask material; removing the mask material; and ablating at least some of the polymer layer in the region where the additive material was diffused.

In accordance with another preferred embodiment of the invention, a method for fabricating a low dielectric constant printed circuit board comprises dispersing an additive material in a low dielectric constant layer; applying an adhesive over at least one side of the low dielectric constant layer; applying a metallization layer over the adhesive; providing a plurality of holes through the low dielectric constant layer, the adhesive, and the metallization layer; patterning the metallization layer; and removing the additive material from the low dielectric constant layer.

In accordance with another preferred embodiment of the invention, a structure comprises a substrate, a circuit chip having chip pads and supported by the substrate, a low dielectric constant porous layer situated over the substrate and circuit chip and having at least one via therein aligned with at least one of the chip pads, and a pattern of electrical conductors extending over a portion of the porous layer and into the at least one via.

In accordance with another preferred embodiment of the invention, a low dielectric constant printed circuit board comprises a low dielectric constant layer, an adhesive overlying at least one side of the low dielectric constant layer, a patterned metallization layer over the adhesive, and a plurality of holes through the low dielectric constant layer, the adhesive, and the metallization layer. In one embodiment, the low dielectric constant layer comprises a ceramic material.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings, where like numerals represent like components, in which:

FIGs. 1-5 are views showing steps in a process for applying a low dielectric constant porous layer over a selected surface;

FIGs. 6-9 are views showing steps in another process for applying a low dielectric constant porous layer over a selected surface;

FIGs. 10-11 are views showing steps in a process for applying multiple low dielectric constant porous layers;

FIGs. 12-16 are views showing steps in a process for enabling laser ablation of low dielectric constant porous material; and

FIGs. 17-19 are views showing steps in a process for forming a low dielectric constant printed circuit board.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

FIGs. 1-5 are views showing steps in a process for applying a low dielectric constant porous material over a selected surface. In the view of **FIG. 1**, a semiconductor chip 14, which for example may comprise a GaAs (gallium arsenide) chip having chip pads 16, is attached with an adhesive 12 in a chip well 18 of a milled substrate 10. The substrate may comprise any suitable structural material such as, for example, aluminum nitride or beryllium oxide. Adhesive 12 may comprise a material such as Ultem polyetherimide resin or silicone epoxy which can withstand high temperature processing.

As shown in **FIG. 2**, a low dielectric constant porous layer 20 is applied over the surfaces of substrate 10 and chip 14. In one embodiment the porous layer comprises a porous PTFE material having its pores filled with an additive material. In one example, the pores have diameters ranging approximately from 0.01 to 5 μm.

Although the porous material is preferably a polymer material, other materials such as ceramics and metals can also be used. Expanded PTFE is a useful porous layer because it does not dissolve in most of the fabricating chemicals. Other examples of potentially useful porous material include polyethylene and polystyrene, for example.

The selected additive material must be capable of withstanding high processing temperatures and capable of removal after processing by any appropriate process, such as heat or a combination of heat and applied vacuum.

For example, the additive material may comprise materials such as low melting temperature waxes,

anthraquinone (as well as derivatives of anthraquinone such as alizarin), and other sublimable organic solids, such as adipic and other dicarboxylic acids. Some of these additive materials may require vacuum and heat combinations to sublime, whereas others tend to diffuse or evaporate from the material. A short list of sublimable materials can be found in the Handbook of Chemistry and Physics, 60th Ed. pages C-722-723. Many of the listed materials can be readily used with this invention. A combination of several additive materials may be desirable to provide a removable material which can absorb appropriate wavelengths for laser ablation.

Porous layer 20 is heated to the softening point under pressure and attached to the substrate surface to achieve a bonded laminate. The pressure and temperature parameters are chosen so that the additive material does not significantly sublime, diffuse, or evaporate during the attachment. The outer porous layer surface can have another coating of the additive material added to refresh the surface after lamination.

Either an adaptive laser, such as described in aforementioned Eichelberger et al., U.S. Pat. No. 4,835,704, or a mask process is then used to form via openings 24 over selected chip pads 16, as shown in **FIG. 3**. Although, layers such as porous PTFE are not typically laser ablatable using the preferred wavelengths, the process of filling the pores of porous layer 20 with additive material causes the porous layer to be laser ablatable, as further discussed below.

After the vias are cleaned, a layer of electrically conductive material is applied over porous layer 20 and patterned to form a pattern of electrical conductors 22 which, in a preferred embodiment, includes a bonding pad 26. In one embodiment the pattern of electrical conductors

comprises a buffer layer of metallization such as titanium or chromium covered by a layer of copper which in turn is covered by a second buffer layer. These metals can be patterned with standard photoresist techniques, as discussed in Eichelberger et al., U.S. 4,783,695.

As shown in **FIGs. 4 and 5**, the additive material is then removed from from the additive-filled porous layer 20 to form an additive-free porous layer 20a. FIG. 5 is a sectional side view similar to that of FIG. 3. FIG. 4 is an enlarged sectional side view along line 4-4' of FIG. 5. Substrate 10 can be heated (either with or without vacuum conditions, depending on the additive material) to sublime, diffuse, or evaporate the additive material. Because the additive material does not sublime directly through the pattern of electrical conductors 22, additive material under the pattern of electrical conductors has a longer release path 21a as compared with the release path 21b of additive material not under the pattern of electrical conductors. The longer release path may require a longer heating period.

The removal of additive material dyes dissolved or dispersed in a polymer matrix occurs through a mechanism of interdiffusion. Dye molecules such as anthraquinone or alizarin are relatively small molecules and fit between the spaces of the coiled polymer chains which preferably make up the porous layer. When heated above the sublimation temperature, the individual dye molecules, in the gas phase, will vent or pass through these spaces and be released from the porous layer.

Because the additive material is removed after the application of the pattern of electrical conductors, the metal does not significantly protrude into the porous layer and thus has a smooth surface as required for low loss high frequency applications.

Although this invention has been discussed with the concept of using a porous material, the porous layer may alternatively comprise a polymer without specially formed pores. The interdiffusion rate will be slower for such polymers than for porous materials because there will be less volume of free space; however, the sublimable additive material molecules still diffuse through the spaces in polymers without specially formed pores to the surrounding atmosphere. The diffusion rate depends on the temperature, pressure, polymer thickness, and permeability of the polymer matrix.

Certain light frequencies, such as UV (ultraviolet), aid in the decomposition of the additive material. UV light acts to scission the material and thus create smaller molecules which can move easily and pass out of the porous materials.

FIGs. 6-9 are views showing steps in a process for applying a low dielectric constant porous layer similar to the process steps shown in FIGs. 1-5 with the addition of an amorphous adhesive 28 having a low dielectric constant, such as available from DuPont under the name AF 1600 or 2400 Teflon polytetrafluoroethylene, that maintains excellent adhesion to the porous layer after the additive material is removed. Another potentially useful adhesive with a low dielectric constant is polyphenylene oxide. These low dielectric adhesives are preferably doped with an ultraviolet light absorbing dye as discussed in aforementioned Cole et al., U.S. Patent No. 5,169,678.

In this embodiment, porous layer 20 is immersed and soaked in the additive material which is dissolved in a solvent. Ion implantation, pressure, or a combination of pressure and heat can be used to increase the permeation of the additive material throughout the porous layer.

After the porous layer and additive material have dried, adhesive 28 is either applied to porous layer 20 or applied to the substrate surface directly. It is helpful to position the additive material in the pores of the porous layer prior to the application and lamination of the porous layer to the substrate surface to prevent the adhesive from wicking or protruding into the pores. Thus the removal of the additive material from the porous layer can be accomplished while maintaining sufficient adhesion of the porous layer to the surface.

FIGs. 7-9 illustrate views of process steps similar to those of FIGs. 2, 3, and 5, respectively, but do not require as much heat to obtain adhesion of the porous layer to the desired surface. When AF Teflon polytetrafluoroethylene is used as an adhesive, the porous layer can attain adequate adhesion to substrate and chip surfaces in the temperature range of 225 ^{o}C - 250 ^{o}C. The step of forming a via opening 24 through porous layer 20 includes forming a corresponding via through adhesive 28.

The addition of the thin adhesive 28 increases the dielectric constant above the surface because dielectric constants generally act in series and are proportional to the relative thicknesses of the adjacent materials. When the porous layer is much thicker than the adhesive, however, the dielectric constant can approach that of the porous layer and be suitably low.

FIGs. 10-11 are views showing steps in a process for applying multiple low dielectric constant porous layers. In **FIG. 10**, a second additive filled porous layer 30 is applied with a second adhesive 32 to the outer surface of porous layer 20a of the structure shown in FIG. 9. The second porous layer and all subsequent layers can be processed as described with respect to FIGs. 7-9 above by

forming a via opening 34 extending to a portion of the pattern of electrical conductors 22, applying a second pattern of electrical conductors 36, and removing the additive material to result in the structure shown in **FIG. 11**. The second adhesive is thin and therefore does not fill the lower vias 24, thus providing an air dielectric constant (about 1) in the metallized via areas.

In a multilayer structure, not all the layers need be applied as additive material filled porous layers. Other materials, such as Kapton polyimide (Kapton is a trademark of E.I. DuPont de Nemours and Co.), for example, can be used in combination with porous layers. The high speed or high frequency porous layers need only be placed where desirable.

Instead of removing the additive material after each layer is applied, several layers can be processed before attempting to remove the additive material. When removing additive material from several layers simultaneously a longer heating period will be required than the period for removing additive material from a single layer.

In one embodiment, the porous layers and adhesives all comprise polytetrafluoroethylene. This embodiment uses two different DuPont AF Teflon polytetrafluoroethylene materials such as AF 1600 for adhesives 28 and 32 and AF 2400 for porous layers 20 and 30. These two materials have sufficiently different melting points so that when AF 2400 is a solid the AF 1600 can melt and function as a bonding glue.

AF Teflon polytetrafluoroethylene materials can have various sublimable materials added that will enable 248-365 nm laser ablation and that can be subsequently be removed by heat or heat and vacuum conditions. Several examples of such additive materials include the above-

discussed low melting temperature waxes, anthraquinone and its derivatives, and other sublimable organic solids. Using these additive materials enables a material that is optically transparent to approximately 200 nm to be laser processable at more conventional laser frequencies such as pulsed excimer lasers at frequencies of 248 nm, 266 nm, 308 nm, and 351 nm, and ion argon or krypton lasers at frequencies of at 350-365 nm and 325 nm, respectively, and subsequently be removed.

The AF Teflon polytetrafluoroethylene layers will release the additive material easily because the materials can be heated near the Tg (glass transition temperature) where the additive material is passed by permeation through the softened material with ease. This process is time, thickness, temperature, and pressure dependent.

An AF 2400 Teflon polytetrafluoroethylene porous layer can be film cast onto a release plate and an AF 1600 Teflon polytetrafluoroethylene adhesive material can be applied over the top of the porous layer without cracking it, enabling a composite structure that can then be laminated to a PC board or MCM structure.

This embodiment can be used to reduce the impedance loading which occurs when using high dielectric constant materials. Some circuit chip manufacturers employ air bridges to obtain low impedance loading on critical areas of GaAs microcircuits. Typically, when these chips are situated in an integrated circuit, any overlying and underlying material must be removed in the area of the air bridges for optimal performance. This invention may reduce the need to remove material and thus enable new chip interconnection structures to be fabricated.

FIGs. 12-16 are views showing steps in a doping process for enabling laser ablation of low dielectric

constant porous layer 40. The porous layer is first applied to a substrate 10 surface, as discussed with respect to FIG. 2, but without the additive material. Then, in a preferred embodiment, a laser ablatable mask material 42, such as Kapton polyimide for example, is deposited over the outer surface of the porous layer. A via opening 46 over a portion of an electrical conductor 44 is formed in the mask material revealing the porous layer, as shown in **FIG. 12**. The via is preferably formed with an argon laser, but can also be formed using other conventional methods such as plasma or reactive ion etching, for example.

As shown in **FIG. 13**, the additive material can be supplied to porous layer 40 in a pressure vessel 50 through a pressure port 52 using a heat source 54. The dopant may comprise a light absorbing dye such as discussed in aforementioned Cole et al., U.S. Patent No. 5,169,678. Mask material 42 limits doping or diffusion to the localized areas 48 where the vias have been formed to cause permeation of the of the additive material for enabling laser ablation at CW argon ion laser frequencies. If desired, mask material 42 can also be applied over the side edges of the porous layer to prevent doping of the side edges. Slight doping which may occur along the edges of the porous layer, however, does not present any problems.

FIG. 14 illustrates a doped region ready for laser processing. Once the desired via areas are doped with the additive material to enable localized laser ablation, the mask material can be removed, as shown in **FIG. 15,** and a laser can be used to produce vias in the porous layer where the additive material was doped because of the selective absorption of the excimer laser energy in the doped via areas. After via formation, any remaining dopant material can be removed by a process such as sublimation, for

example, leaving the material again transparent to the excimer laser's light energy, as shown by via 56 in **FIG. 16**.

FIGs. 17-19 are views showing steps in a process for forming a low dielectric constant printed circuit board. First, a porous layer 110 is filled with additive material as described with respect to FIG. 2. The porous layer is preferably coated on both sides with thin layers of an adhesive material 112a and 112b, comprising a material such as AF 1600 or 2400 Teflon polytetrafluoroethylene, which in turn are coated with respective layers of metallization 114a and 114b, comprising a material such as copper, as shown in **FIG. 17**. In one embodiment DuPont FEP or PFA Teflon polytetrafluoroethylene is applied with a pinch roll laminator such as used in PC board processing.

Next, as shown in **FIG. 18**, holes 116 are punched or drilled through the porous material, adhesive, and metallization, and, as shown in **FIG. 19**, the layers of metallization are patterned to form metallization lines on the board. In one embodiment, the patterning is performed using a layer of photoresist (not shown) which is removed after patterning. If desired, any adhesive left exposed after the patterning of the metallization layer can be removed by RIE (reactive ion etching). After the metallization lines are fabricated, electronic components can be inserted in the board, and removal of the additive material is accomplished by sublimation, evaporation, and/or diffusion, as discussed above.

While only certain preferred features of the invention have been illustrated and described herein, many modifications and changes will occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

WHAT IS CLAIMED IS:

1. A method for applying a low dielectric constant material over a substrate, comprising the steps of:

dispersing an additive material in the low dielectric constant layer;

attaching the layer to a surface of the substrate; and

removing the additive material from the layer.

2. The method of claim 1, wherein the step of removing the additive material from the layer comprises a process selected from the group consisting of sublimation, evaporation, and diffusion.

3. The method of claim 2, wherein the additive material is sublimable in the layer.

4. The method of claim 2, wherein the layer comprises a material selected from the group consisting of polymers and ceramics.

5. The method of claim 4, wherein the layer comprises a porous layer having pores.

6. The method of claim 2, wherein the substrate supports a circuit chip having chip pads on a connection surface and wherein the step of attaching the layer to the surface of the substrate includes attaching the layer to the connection surface of the circuit chip, and further including, prior to removing the additive material from the layer, the steps of:

forming at least one via in the layer extending to at least one of the chip pads; and

applying pattern of electrically conductive material over the layer, the pattern of electrically conductive material extending into the at least one via.

7. The method of claim 6, wherein the layer comprises a polymer layer.

8. The method of claim 7, wherein the polymer layer comprises a porous layer having pores.

9. The method of claim 8, wherein the porous layer comprises a material selected from the group consisting of polytetrafluoroethylene, polyethylene, and polystyrene.

10. The method of claim 9, wherein the additive material comprises a material selected from the group consisting of wax, anthraquinone, and sublimable organic solids.

11. The method of claim 8, wherein the step of attaching the porous layer to the substrate surface includes using an adhesive between the porous layer and the substrate surface.

12. The method of claim 11, wherein the adhesive comprises an adhesive selected from the group consisting of polytetrafluoroethylene and polyphenylene oxide.

13. The method of claim 8, further including, after applying the pattern of electrical conductors, the steps of:

attaching an additional porous layer having dispersed additive material therein to the surface of the the porous

layer and the pattern of electrical conductors with an adhesive; and

forming an additional via in the additional porous layer extending to a portion of the pattern of electrically conductive material; and

applying an additional pattern of electrically conductive material over the additional porous layer, the additional pattern of electrically conductive material extending into the additional via; and

removing the additive material from the additional porous layer.

14. The method of claim 13, wherein the steps of removing the additive material from the porous layer and removing the additive material from the additional porous layer occur simultaneously.

15. The method of claim 13, wherein the porous layer and additional porous layer comprise a first polytetrafluoroethylene material and the adhesive comprises a second polytetrafluoroethylene material, the second polytetrafluoroethylene material having a lower melting point than the first polytetrafluoroethylene material.

16. A method for applying and ablating a low dielectric constant material over a substrate, comprising the steps of:

attaching a low dielectric constant porous polymer layer to a surface of the substrate;

applying mask material over the polymer layer;

forming a via in the mask material extending through to the polymer layer;

diffusing an additive material in a region of the polymer layer through the via in the mask material;

removing the mask material; and

ablating at least some of the polymer layer in the region where the additive material was diffused.

17. The method of claim 16, further including the final step of removing any remaining additive material from the polymer layer by sublimation.

18. The method of claim 17, wherein the polymer layer comprises a polytetrafluoroethylene and the mask material comprises a polyimide.

19. A method for fabricating a low dielectric constant printed circuit board, comprising the steps of:

dispersing an additive material in the low dielectric constant layer;

applying an adhesive over at least one side of the low dielectric constant layer;

applying a metallization layer over the adhesive;

providing a plurality of holes through the low dielectric constant layer, the adhesive, and the metallization layer;

patterning the metallization layer; and

removing the additive material from the low dielectric constant layer.

20. The method of claim 19 wherein the step of removing the additive material from the low dielectric constant layer comprises a process selected from the group consisting of sublimation, evaporation, and diffusion.

21. The method of claim 20, wherein the additive material is sublimable in the low dielectric constant layer.

22. The method of claim 20, wherein the low dielectric constant layer comprises a polymer layer.

23. The method of claim 22, wherein the polymer layer comprises a porous layer having pores.

24. The method of claim 23, wherein the porous layer comprises a material selected from the group consisting of polytetrafluoroethylene, polyethylene, and polystyrene.

25. The method of claim 24, wherein the additive material comprises a material selected from the group consisting of wax, anthraquinone, and sublimable organic solids.

26. A structure, comprising:

a substrate;

a circuit chip having chip pads and supported by the substrate;

a low dielectric constant porous layer over the substrate and circuit chip, the porous layer having at least one via therein aligned with at least one of the chip pads; and

a pattern of electrical conductors extending over a portion of the porous layer and into the at least one via.

27. The structure of claim 26, wherein the porous layer comprises a polymer layer.

28. The structure of claim 27, wherein the polymer layer comprises a material selected from the group consisting of polytetrafluoroethylene, polyethylene, and polystyrene.

29. The structure of claim 26, further including an adhesive between the porous layer and the substrate surface.

30. The structure of claim 29, wherein the adhesive comprises an adhesive selected from the group consisting of polytetrafluoroethylene and polyphenylene oxide.

31. The structure of claim 26, further including:

an additional porous layer over the surface of the porous layer and the pattern of electrical conductors;

an adhesive between the porous layer and the additional porous layer, the additional porous layer having an additional via extending through to at least a portion of the pattern of electrically conductive material; and

an additional pattern of electrically conductive material over the additional porous layer, the additional pattern of electrically conductive material extending into the additional via.

32. The structure of claim 31, wherein the porous layer and additional porous layer comprise a first polytetrafluoroethylene material and the adhesive comprises a second polytetrafluoroethylene material, the second polytetrafluoroethylene material having a lower melting point than the first polytetrafluoroethylene material.

33. A low dielectric constant printed circuit board, comprising:

a low dielectric constant layer;

an adhesive overlying at least one side of the low dielectric constant layer;

a patterned metallization layer over the adhesive; and

a plurality of holes through the low dielectric constant layer, the adhesive, and the metallization layer.

34. The printed circuit board of claim 33, wherein the low dielectric constant layer comprises a porous material.

35. The printed circuit board of claim 34, wherein the low dielectric constant layer comprises a polymer layer.

36. The printed circuit board of claim 35, wherein the polymer layer comprises a material selected from the group consisting of polytetrafluoroethylene, polyethylene, and polystyrene.

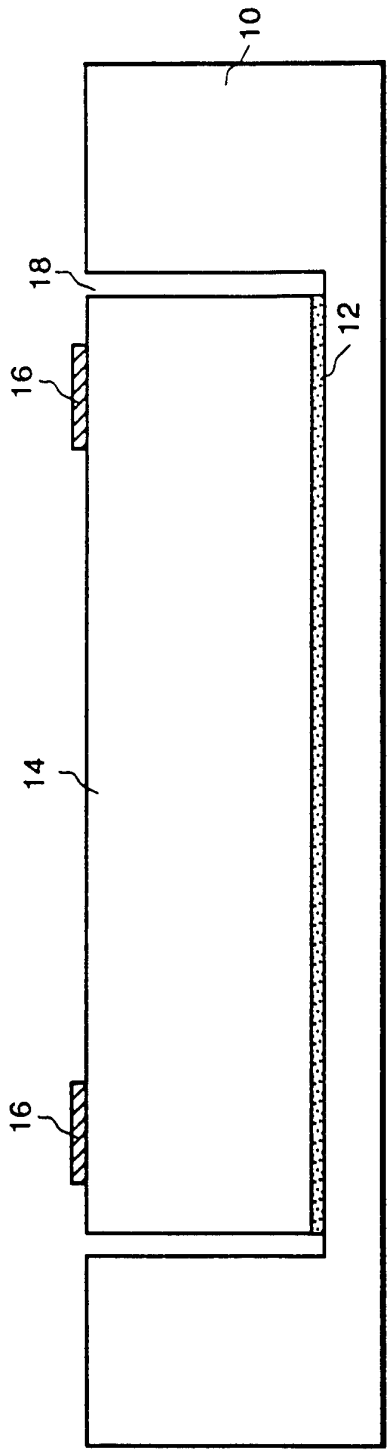


FIG. 1

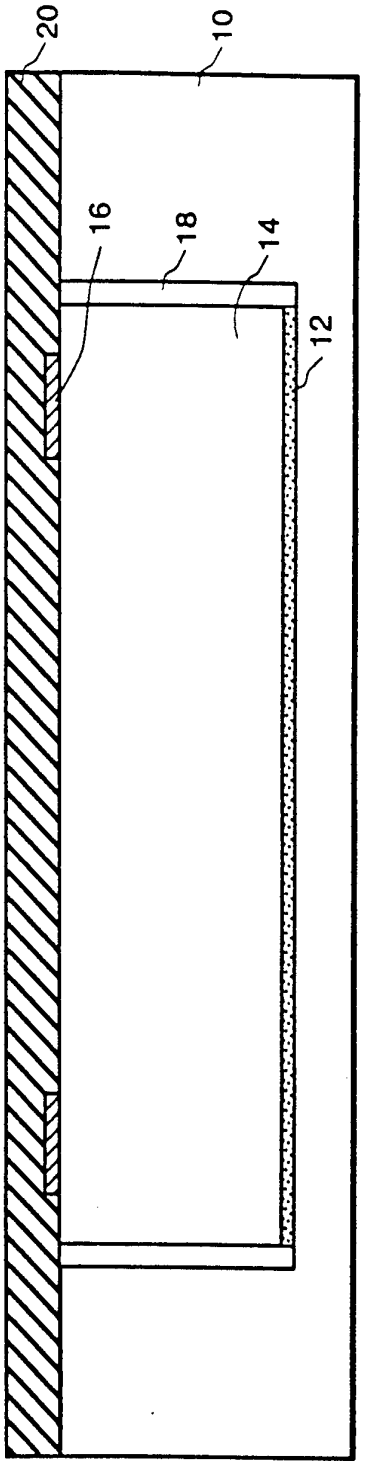


FIG. 2

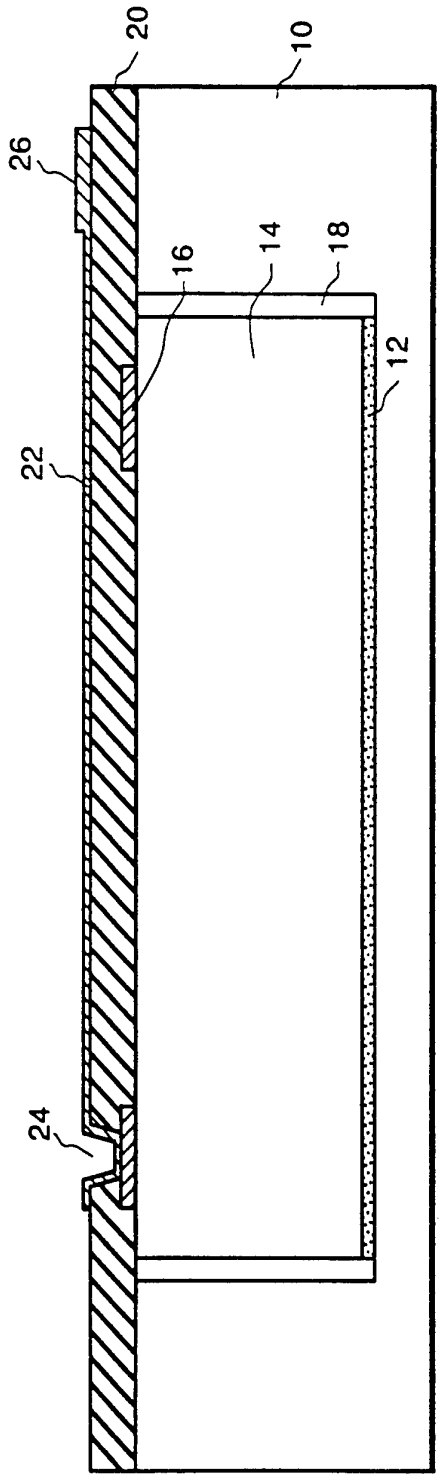


FIG. 3

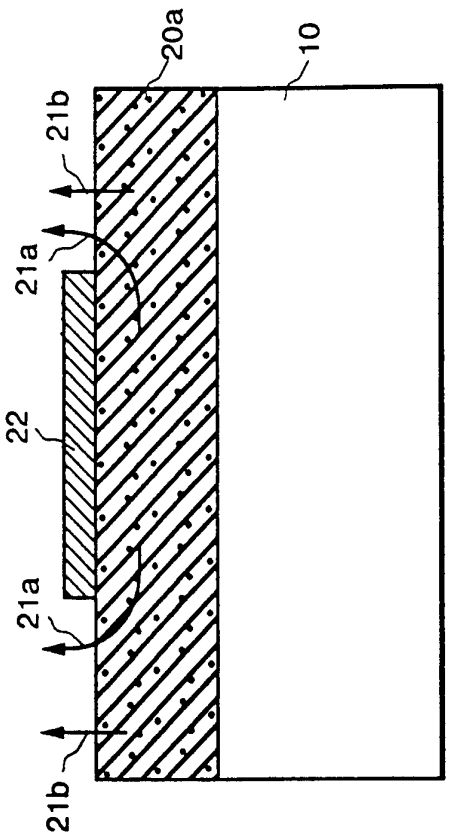


FIG. 4

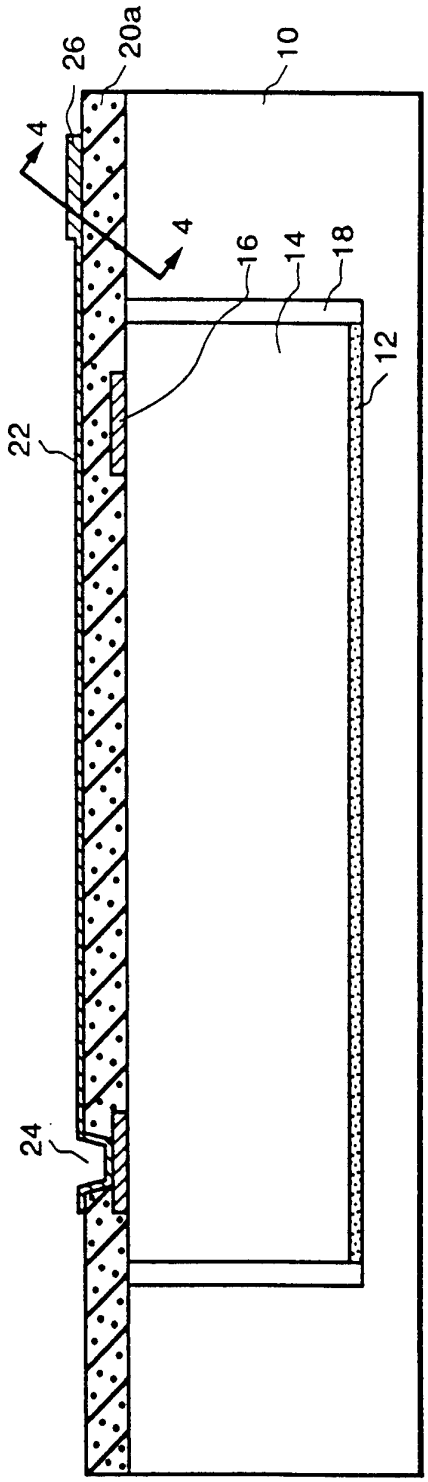
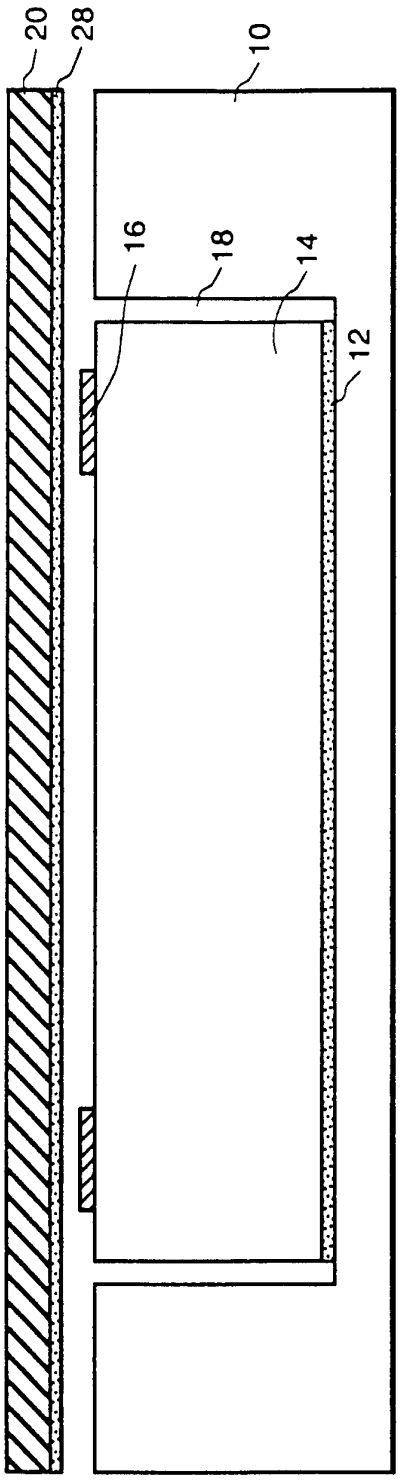


FIG. 5



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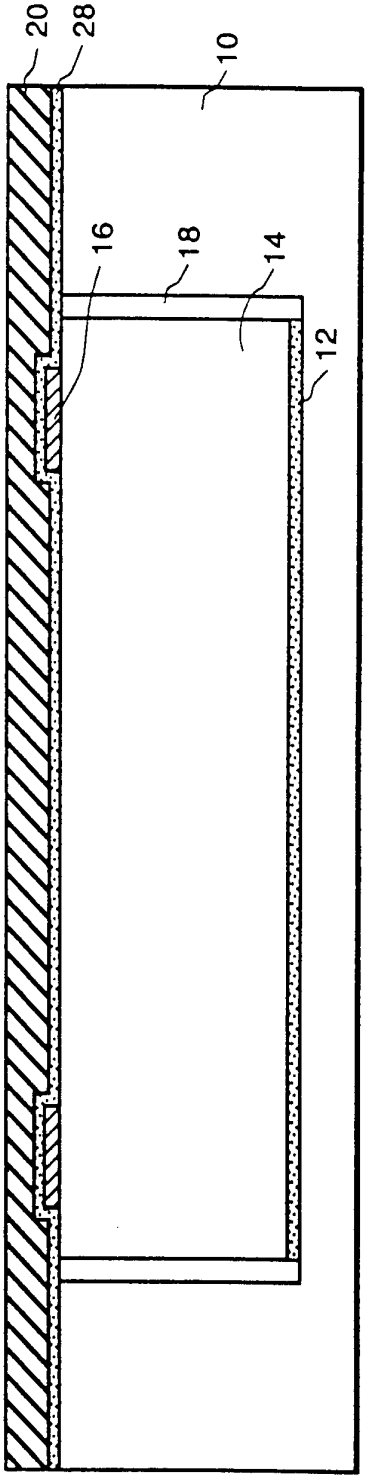

FIG. 7

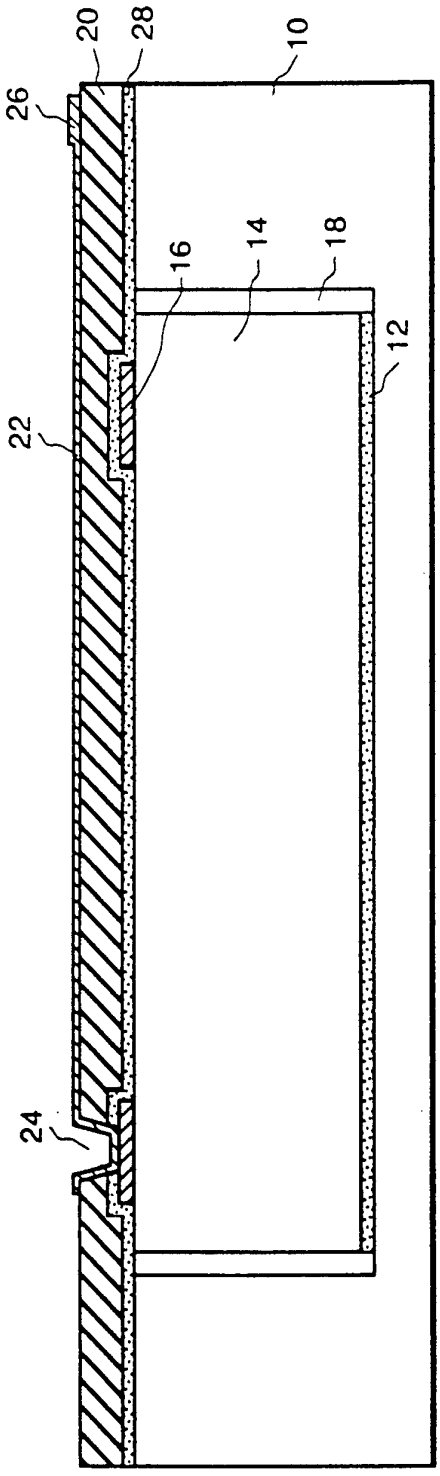

FIG. 8

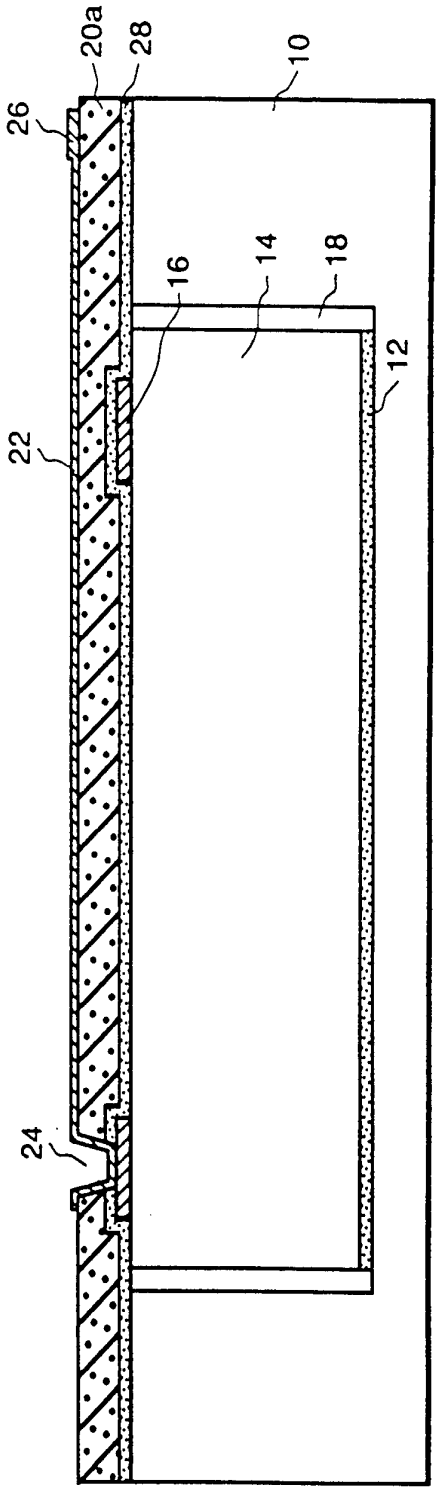

FIG. 9

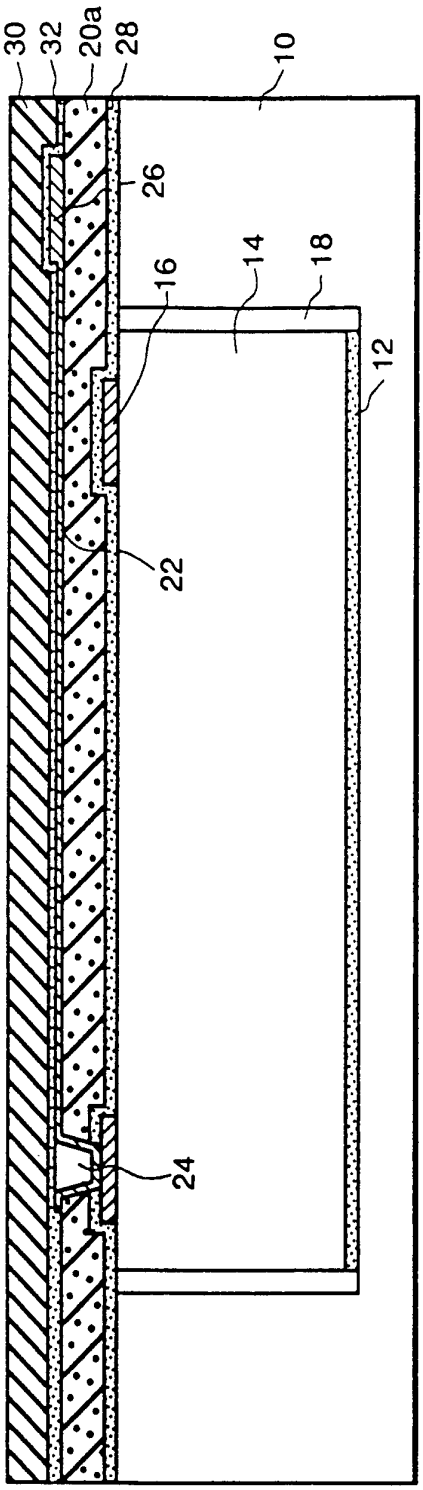
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FIG. 10

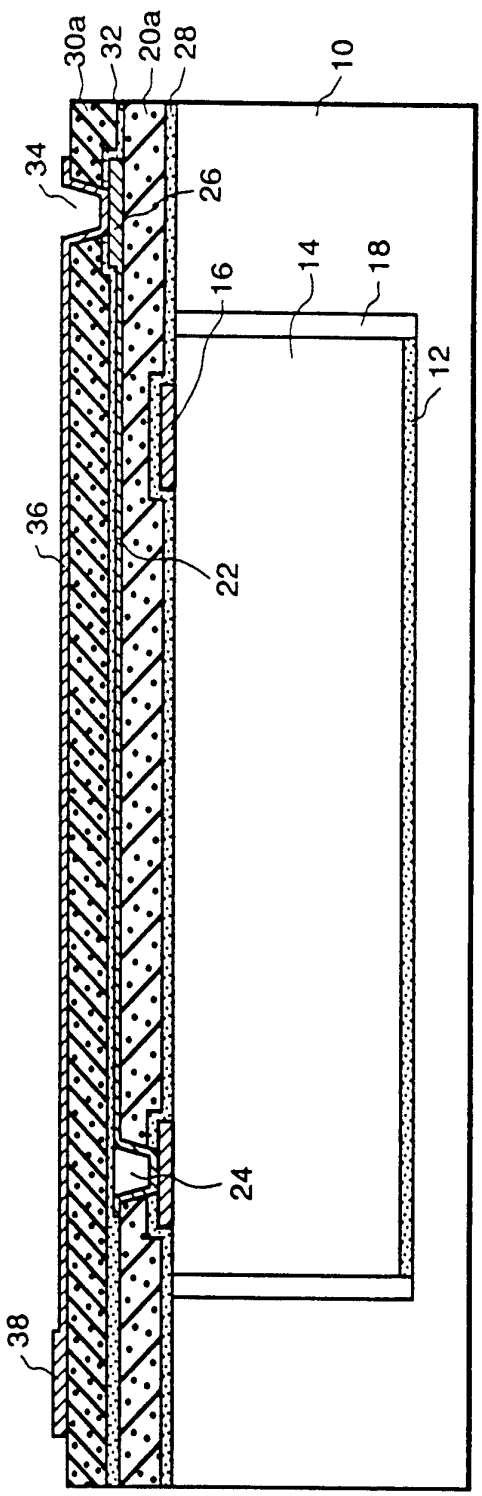
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FIG. 11

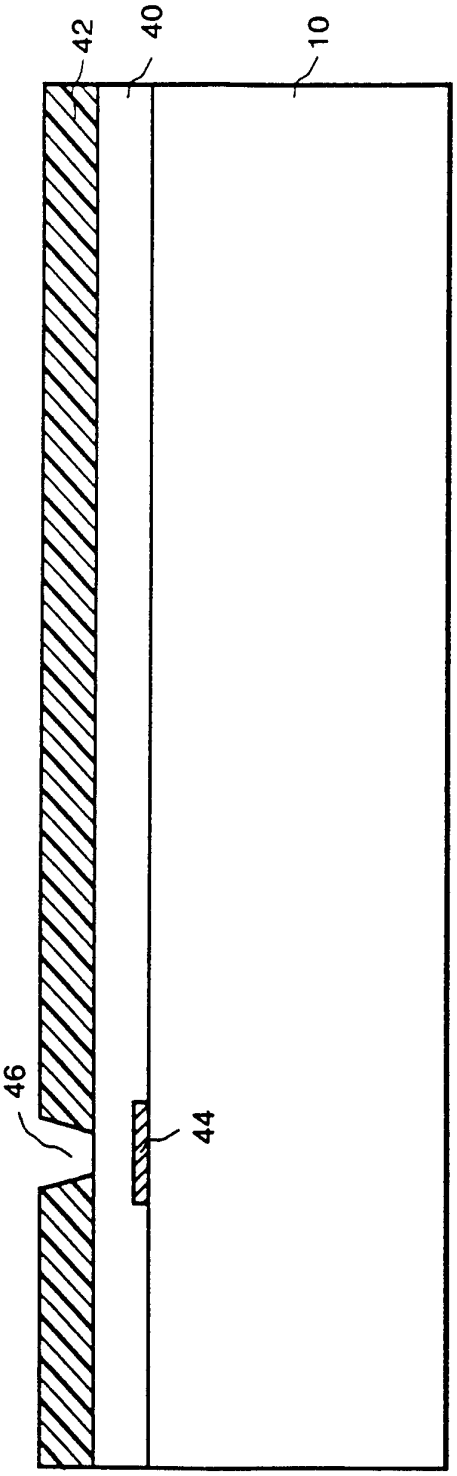

FIG. 12

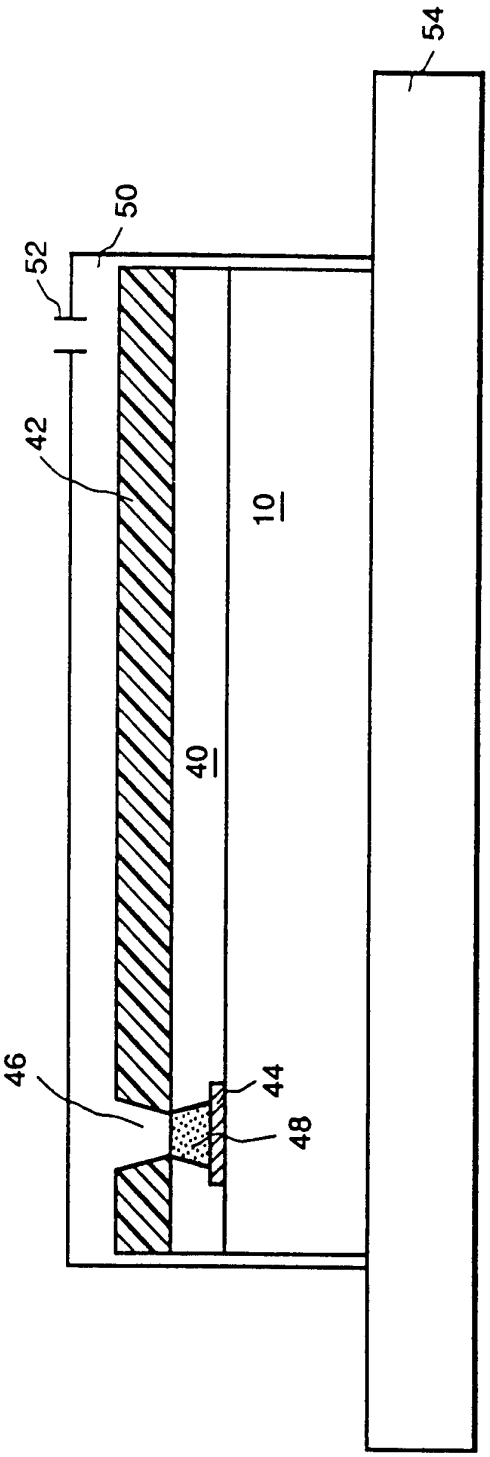

FIG. 13

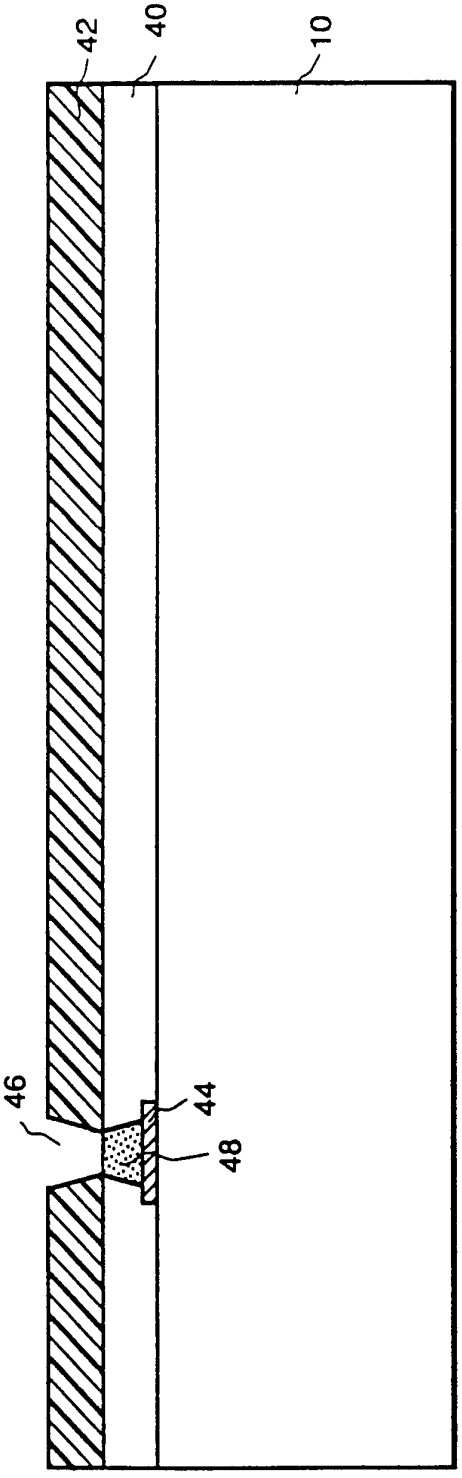

FIG. 14

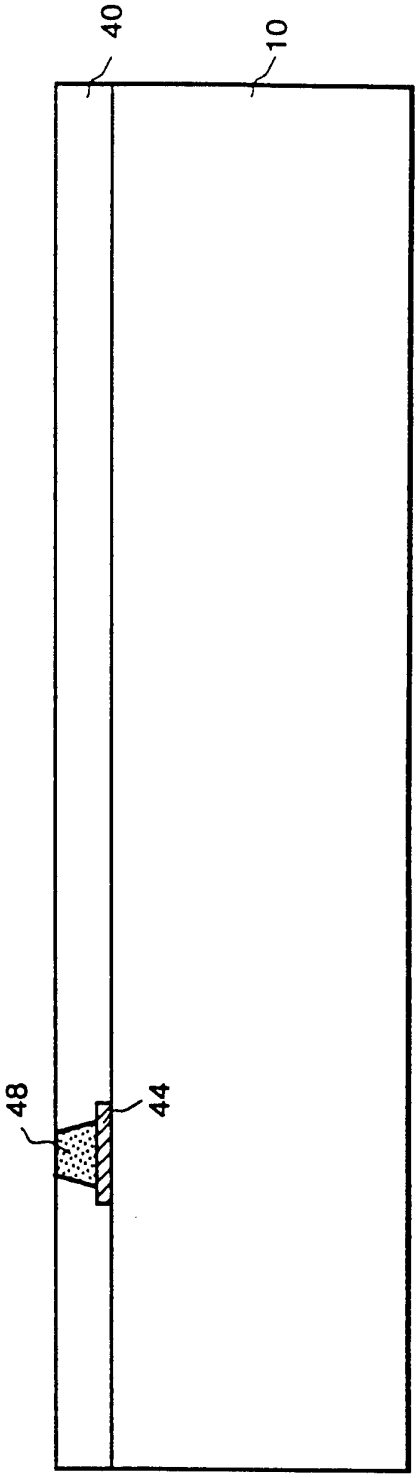

FIG. 15

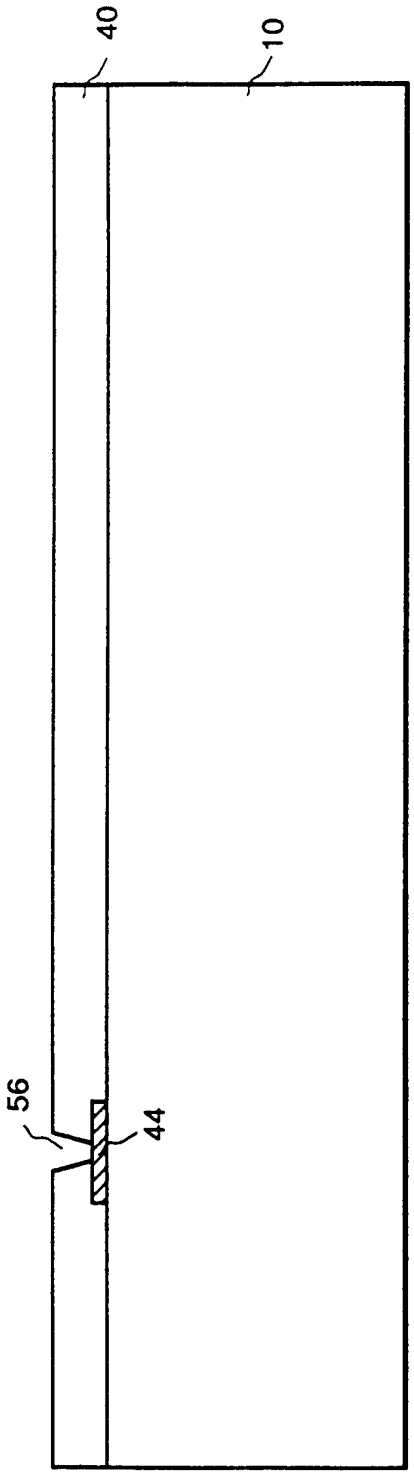

FIG. 16

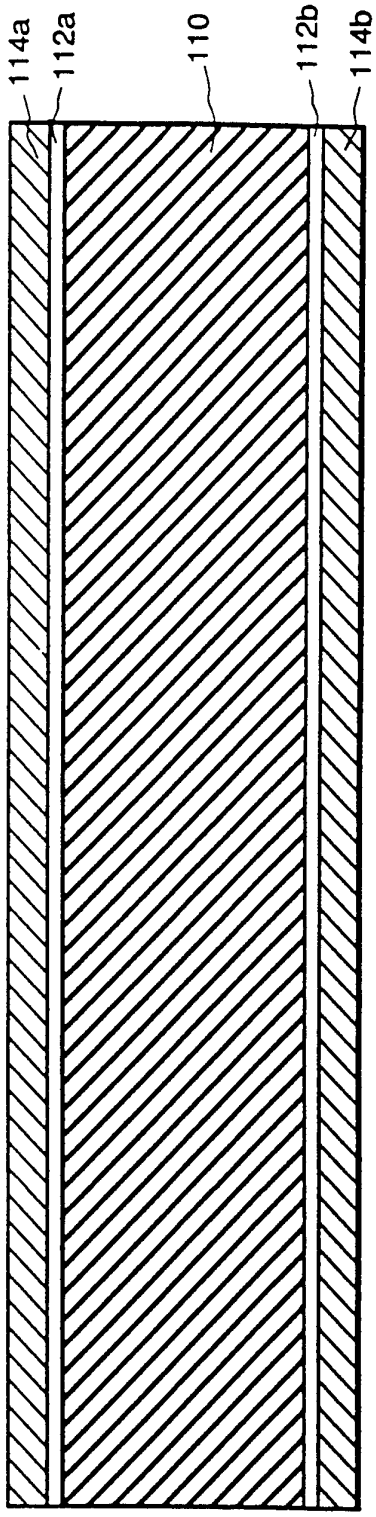

FIG. 17

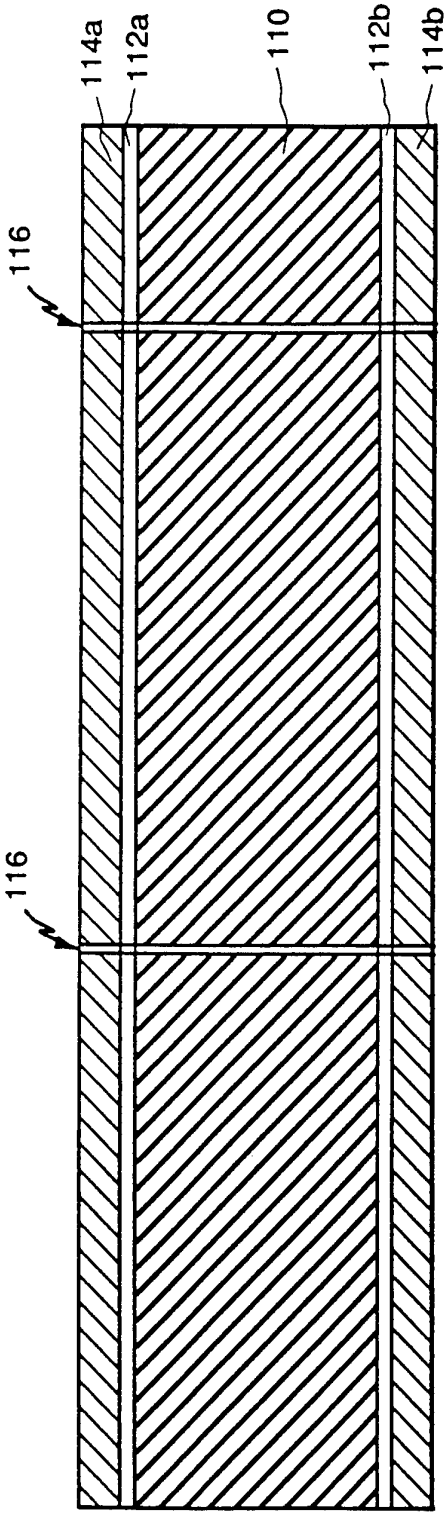
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FIG. 18

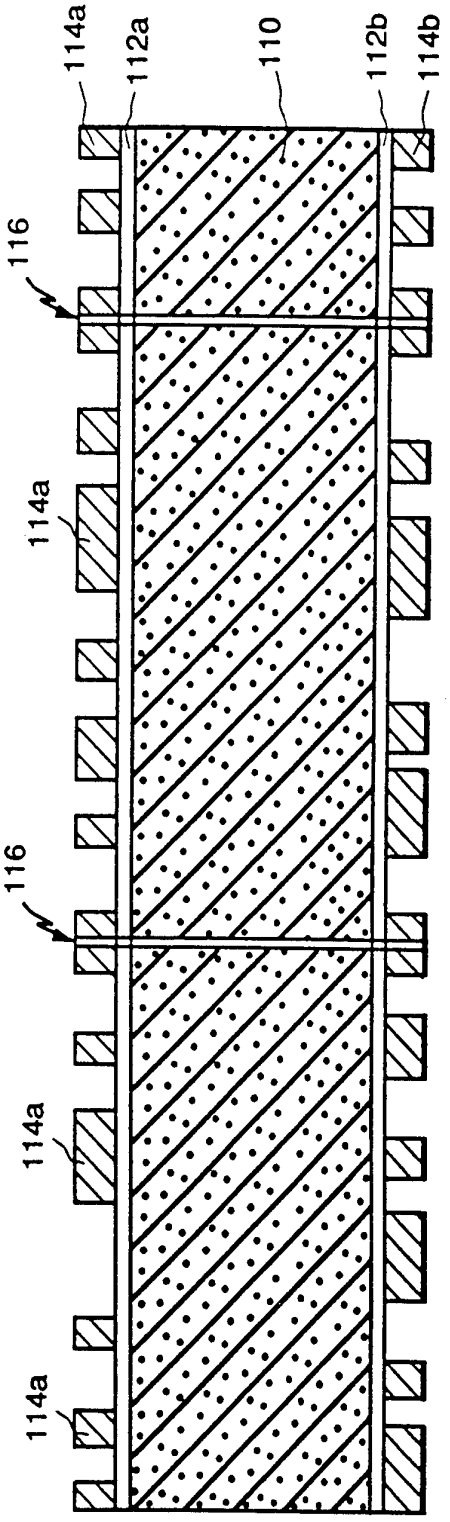
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FIG. 19

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 95/05983

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H05K1/03 H01L23/532 H01L23/538

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H05K H01L G03F B23K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 4, no. 28 (E-001) 8 March 1980 & JP,A,55 001 109 (FUJITSU LTD) 7 January 1980 see abstract	1-3,5
A	---	10
A	EP,A,0 333 132 (NEC CORP.) 20 September 1989 see claims	1,4,5, 7-9,26, 27,31

A	GB,A,2 266 181 (MITSUBISHI DENKI KK) 20 October 1993 see claims	1,4,5, 7-9,26, 27,31

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 August 1995	13. 09. 95

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Mes, L

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	MATERIALS LETTERS, vol.8, no.8, August 1989, AMSTERDAM NL pages 278 - 282, XP000084704 J.K. YAMAMOTO ET AL. 'Fabrication of controlled porosity in a tape cast glass ceramic substrate material' see the whole document	1,2,4,5
A	US,A,5 034 801 (FISCHER) 23 July 1991 see claims	6-9,13, 26-28,31
Y	US,A,5 302 547 (WOJNAROWSKI ET AL.) 12 April 1994 see column 4, line 61 - column 5, line 36; figure 1	16,18
Y	MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS (MATERIALS SCIENCE OF HIGH TEMPERATURE POLYMERS FOR MICROELECTRONICS SYMPOSIUM, ANAHEIM US, 29 APRIL-2 MAY 1991), vol.227, 1991, PITTSBURGH US pages 253 - 258 S. LAZARE ET AL. 'UV-laser photoablation of thermostable polymers: polyimides, polyphenylquinoxaline and teflon AF' see page 255 - page 258	16,18
A	US,A,5 169 678 (COLE ET AL.) 8 December 1992 cited in the application see column 4, line 65 - column 5, line 4 see column 7, line 64 - column 8, line 10	16,18
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X	WO,A,93 24313 (M-RAD ELECTROMAGNETIC TECHNOLOGY) 9 December 1993 see the whole document	33-36
A	IBM TECHNICAL DISCLOSURE BULLETIN., vol.31, no.7, December 1988, NEW YORK US pages 25 - 26, XP000023792 'Fabrication of printed circuit boards using insulation layers with low dielectric constant' see the whole document	22-24, 33-36

1

INTERNATIONAL SEARCH REPORT

formation on patent family members

Inter nal Application No
PCT/US 95/05983

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