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[72] Inventor **Larkin B. Scott**
Fort Worth, Tex.

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[73] Assignee **The Perkin-Elmer Corporation**
Norwalk, Conn.

[54] **COMPARATOR CIRCUIT ARRANGEMENT**
6 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** **340/146.2,** 307/235
[51] **Int. Cl.** **G06f 7/02**
[50] **Field of Search** 340/146.2; 307/231; 340/172; 307/235; 328/146

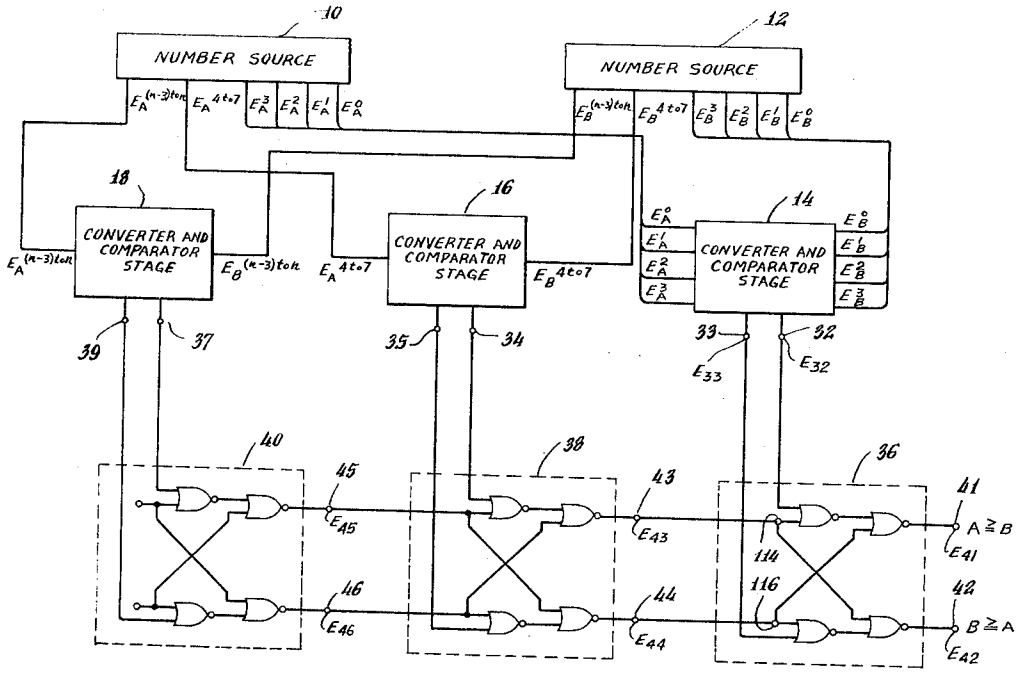
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Primary Examiner—Eugene G. Botz
Attorney—Edward R. Hyde, Jr.

ABSTRACT: Circuit means are provided for converting a first number *A* which occurs in digital form to a first plurality of analog representations and a second number *B* which occurs in digital form to a second plurality of analog representations; for comparing the amplitude of the numbers in analog form; for providing a plurality of digital representations indicative of these relative analog magnitudes; and for comparing the digital representations thereby providing an indication as to the relative magnitudes of the numbers *A* and *B*.



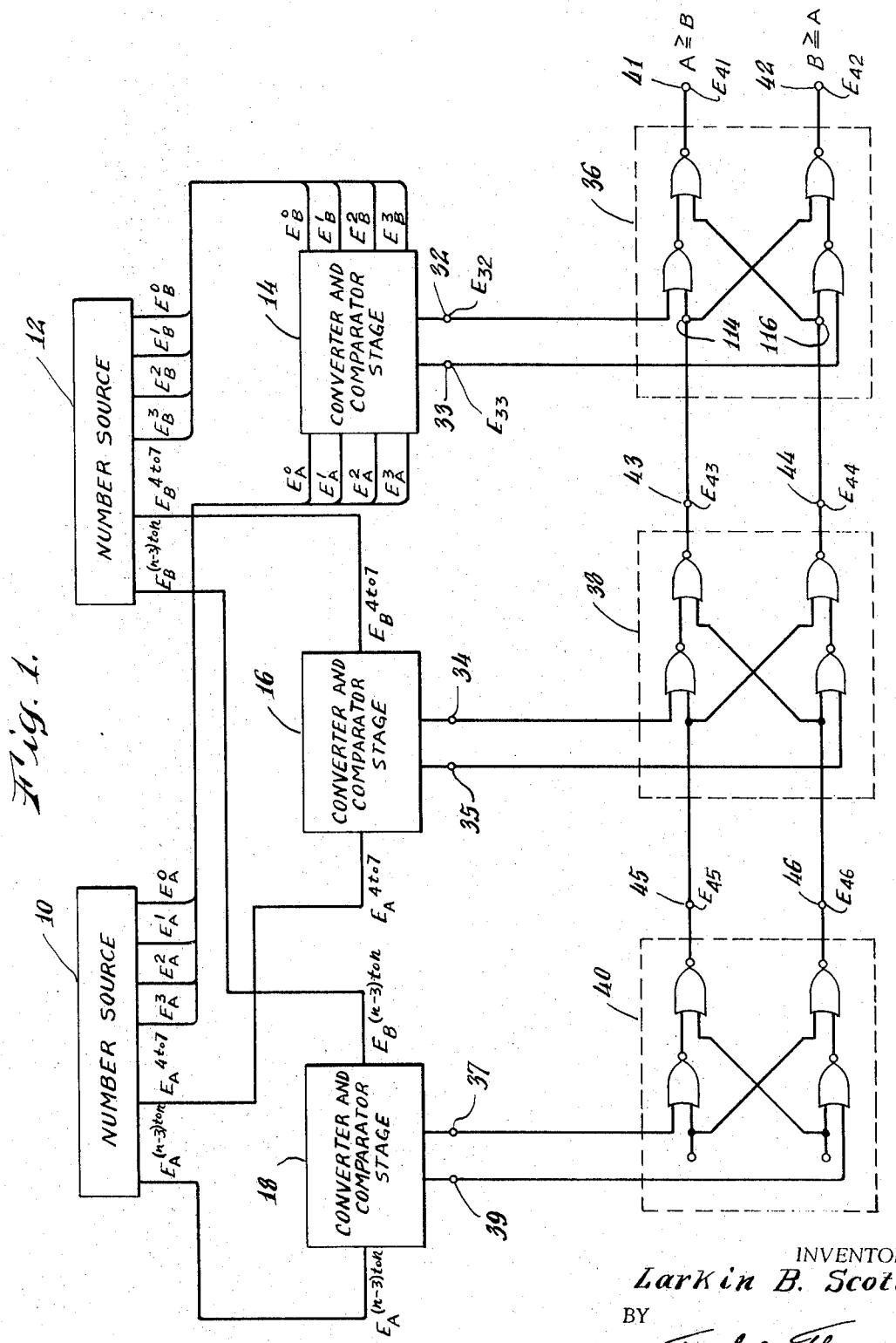


Fig. 1.

INVENTOR.
Larkin B. Scott
BY
Frank J. Thompson
ATTORNEY.

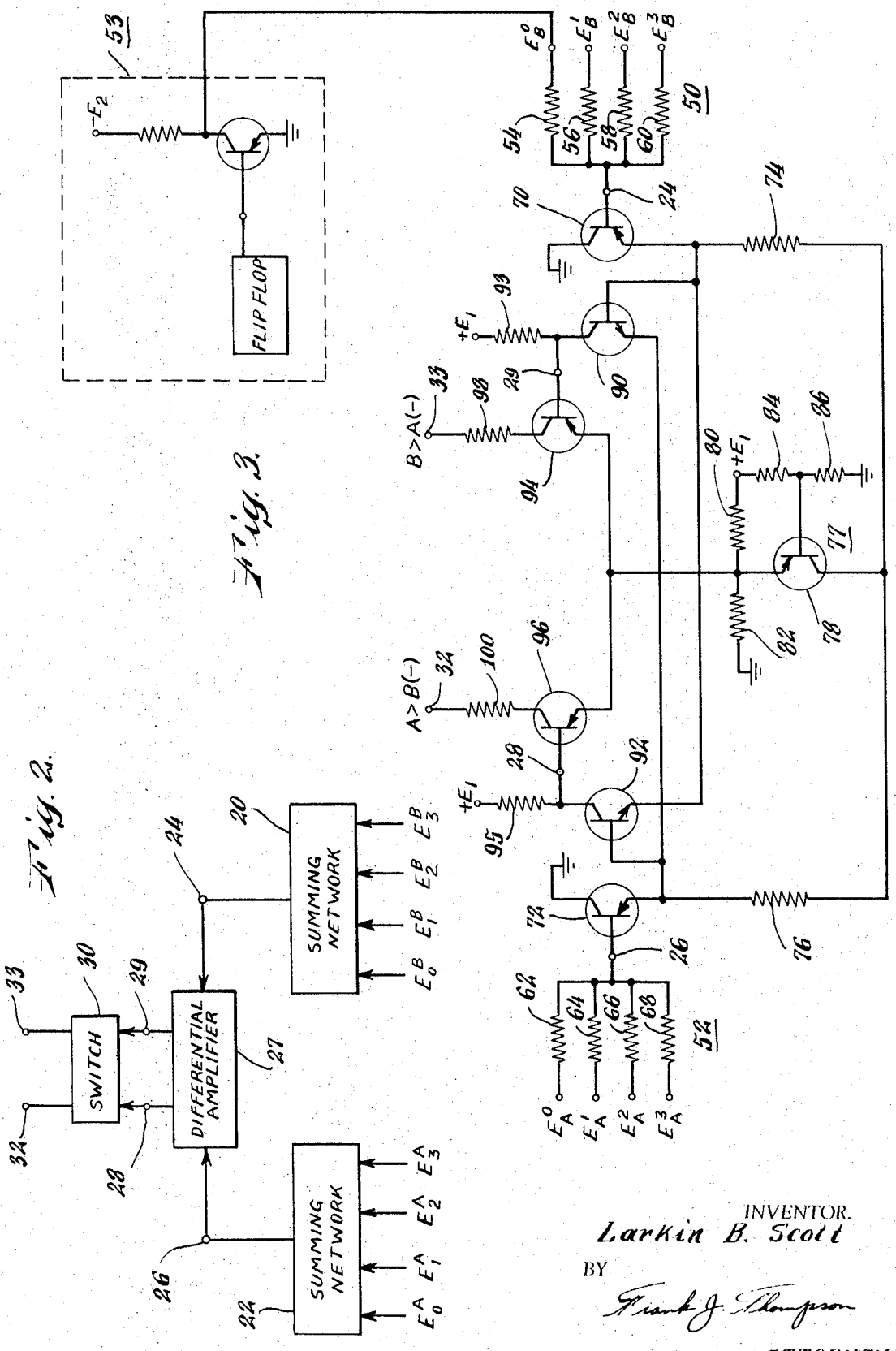


Fig. 2.

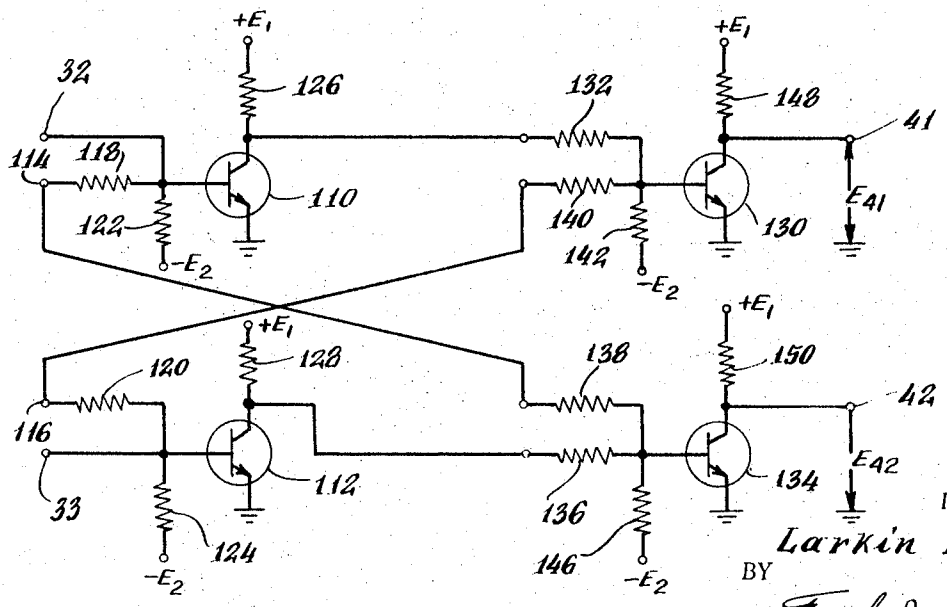
Fig. 3.

INVENTOR.
Larkin B. Scott
BY
Frank J. Thompson
ATTORNEY.

Fig. 5.

$E_{A'}$	$E_{B'}$	E_A	E_B	E_{AOUT}	E_{BOUT}
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0

Fig. 4.



INVENTOR.
Larkin B. Scott
BY
Frank J. Thompson
ATTORNEY.

COMPARATOR CIRCUIT ARRANGEMENT

This invention relates to circuit arrangements for comparing two numbers and for providing an output voltage indicative of the relative magnitude of the numbers. The invention relates more particularly to a comparator for comparing numbers occurring in digital form

There are many applications in which it is desirable to compare the magnitude of two numbers occurring in digital form and to provide an indication as to which is the larger and the smaller of the two. The need for such a comparison exists, for example, in many forms of digital computers and in other digital equipment. The digits of a number are generally represented electrically by discrete, predetermined voltage levels. For example, in a digital numbering system having a radix–2, each digit of the number can alternatively assume two discrete electrical values and thus can be represented by a bistable electrical device such as two switching contacts or a flip-flop circuit. The digits of the number can also be represented electronically by the presence or absence of pulses. The digital form is distinguished from an analog representation wherein the complete number is represented by a single voltage level, for example. The analog voltage level can assume any of many levels corresponding to the magnitude of the particular number being represented. Since in an analog arrangement, two numbers are represented by voltage levels derived from separate sources, a relatively uncomplex arrangement can be provided to effect comparison of these numbers. However, because digital numbers are represented by a plurality of voltages for example, it is necessary to compare corresponding digits of the same order of the two numbers in order to provide an indication as to the relative magnitude of the numbers. This arrangement therefore requires a relatively larger number of circuit components and is thus substantially more expensive than a comparator for comparing numbers occurring in analog form.

It is an object of the present invention to provide an improved circuit arrangement for comparing two numbers occurring in digital form.

It is another object of the present invention to provide a comparator for digital numbers requiring relatively less components and which is relatively less expensive than prior comparators.

In accordance with a feature of the present invention, circuit means are provided for converting a first number *A* which occurs in digital form to a first plurality of analog representations and a second number *B* which occurs in digital form to a second plurality of analog representations; for comparing the amplitude of the numbers in analog form; for providing a plurality of digital representations indicative of these relative analog magnitudes; and for comparing the digital representations thereby providing an indication as to the relative magnitudes of the numbers *A* and *B*.

These and other features and objects of the invention will be apparent with reference to the following specification and drawings wherein:

FIG. 1 is a block diagram illustrating an embodiment of the invention;

FIG. 2 is a block diagram illustrating in more detail a converter and comparator stage of FIG. 1;

FIG. 3 is a schematic circuit diagram of the converter and comparator of FIG. 2;

FIG. 4 is a schematic circuit diagram of a logic circuit shown in block form in FIG. 1; and

FIG. 5 is a logic truth table for the logic circuit of FIG. 1.

In FIG. 1, a source 10 of a first number *A* in digital form and a source 12 of a second number *B* in digital form are shown coupled to converter and comparator stages 14, 16 and 18. These sources, which may comprise registers in digital equipment, each provide output voltages representing *n* digits of the particular number. Although numbering systems of other radix may be provided, the sources 10 and 12 provide output voltages representing numbers in binary form. Included in each source is a plurality of stages having bistable elements.

The bistable elements can comprise for example, electronic flip-flop circuits or an electromechanical arrangement of switch contacts such as is provided by relays. For simplification of the drawings, a plurality of source voltages E_B^0 to E_B^3 and E_A^0 to E_A^3 are shown derived from associated stages and applied to the converter 14 via a single cable. Similarly, a plurality of voltages E_B^{4to7}, E_A^{4to7}, $E_B^{((n13)\ to\ n)}$, and $E_A^{((n13)\ to\ n)}$ representing higher order digits of the numbers are also shown applied via associated cables to other comparator stages in FIG. 1.

Each of the comparator stages 14, 16 and 18 are adapted to convert that portion of the numbers *A* and *B* represented by the digital input voltage to analog form, to compare the magnitude of the analog voltages, and to provide a digital output voltage indicative as to the relative magnitude of the analog voltages. FIG. 2 is a block diagram illustrating the stage 14 in greater detail. The converter and comparator 14 includes a circuit means for converting the plurality of digital input voltages E_B^0 to E_b^3 to a single analog representation and the plurality of digital input voltages E_A^0 to E_A^3 similarly to an analog representation. In FIG. 2 this conversion means is shown to be the summing networks 20 and 22. The output of these networks occurring at terminals 24 and 26 respectively are analog voltage levels indicative of the magnitudes of the numbers represented by the four, lowest order, and least significant digits of the numbers *A* and *B*. These analog voltages are applied simultaneously to a circuit means, shown to be a difference amplifier 27, for indicating their relative difference in amplitude and providing an output voltage indication. The amplifier output voltage indication is in digital form and occurs at terminals 28 and 29. At times, the particular circuit arrangement employed may render it impractical to provide a difference amplifier output voltage indication at the logic voltage levels employed throughout the comparator apparatus. Thus, an electronic switch 30 is included for providing the desired digital output representation at logic levels corresponding to those employed in the comparator apparatus. The output voltage at terminals 32 and 33 is therefore in digital form, is indicative of the relative magnitudes of the lower order digits of the numbers *A* and *B*, and occurs at voltage levels compatible with logic voltage levels employed in other portions of the comparator apparatus. In a similar manner, output voltages occurring at terminals 34 and 35 are indicative of the relative magnitudes of higher order, more significant digits of the numbers *A* and *B*, while output voltages occurring at terminals 37 and 39 are indicative of the relative magnitudes of the highest order, most significant digits.

In accordance with a feature of the invention, the comparison and digital indication of the relative magnitudes of the numbers A and B is provided at terminals 32 and 33. In accordance with another feature of the invention, when the numbers A and B include a number of digits *n* which renders the comparison in a single stage 14 impractical, then pluralities of digits are compared independently and the output indication of the converter-comparator stages are then compared. An arrangement of this type is illustrated in FIG. 1. The output of the converter-comparator stages 14, 16 and 18 are applied to a digital comparator comprising associated logic circuits 36, 38 and 40 respectively. These logical circuits include an arrangement of NOR gates, the circuit of which is described in more detail hereinafter. Each of the logical circuits function to provide an output voltage indicative of the relative magnitudes of the digital output representations derived from the associated comparator. However, the logic of these circuits is arranged to provide that the lower order logical circuits are governed by the relative magnitudes of more significant digits in providing an output voltage. When a more significant digit of *A* is greater than an equivalent significant digit of *B*, then *A* is greater than *B*. The higher order logical circuit then generates a voltage which controls all lower order logical circuits. Under these conditions, the outputs from lower orders are independent of the magnitudes of lower order digits of *A* and *B*. For example, the logical circuit 36 is adapted, when E

$_{43}$ and E_{44} each represent a logical **0**, to compare the voltages E_{32} and E_{33} and to indicate at terminals **41** and **42** which of the two is the greater. However, when the digits E_A^n is greater than E_B^n, then outputs of logic circuits **36** and **38** will be governed by E_{45} and is independent of the relative magnitudes of E_A^{0to7} and E_B^{0to7}.

A logical expression relating input and output voltages for the logic circuit is given by:

$$E_{AO}=E_A'+(E_A\cdot\overline{E_B'}:) \qquad (1)$$

Similarly

$$E_{BO}=E_B'+(E_B\cdot\overline{E_A'}) \qquad (2)$$

where E_{AO}, E_{BO} are the output voltages from a logic circuit, E_A and E_B are input voltages from an associated converter-comparator stage, and E_A' and E_B' input voltages coupled from the next higher order logic circuit. For example, with respect to the logic circuit **36** of FIG. **1**,

$$E_A=E_{32},\ E_B=E_{33},\ E_A'=E_{43},\ E_B'=E_{44}$$

The expression of equation 1 may be rearranged with the aid of DeMorgans's Theorem and other well-known Boolean algebra relations to a formula readily recognizable with respect to the NOR circuit arrangement of FIG. **1**. This expression is:

$$\overline{\overline{E_{AO}}=\overline{E_A'}+E_A+E_B} \qquad (3)$$

and

$$\overline{\overline{E_{BO}}=\overline{E_B'}+E_B+E_A} \qquad (4)$$

A truth table is shown in FIG. **5** illustrating the various logical outputs for the various logic input combinations to a logic circuit.

The output of the logical circuit **36** is thus an indication as to the relative magnitudes of the digital numbers *A* and *B*. Thus, the arrangement of FIG. **1** avoids a digit by digit comparison as referred to previously and compares two digital numbers in a manner which reduces the number of components previously required.

Circuit arrangements for effecting the conversion and comparison of stages **14**, **16** and **18** and the logical comparison of stages **36**, **38** and **40** are illustrated in FIGS. **3** and **4**. FIG. **3** illustrates a circuit arrangement for the analog converter, difference amplifier and switch arrangement of FIG. **2**. A digital to analog converter is provided for each group of input digital voltages and comprises two resistive summing networks, indicated generally as **50** and **52**. Each of these networks includes a resistor associated with an applied digital voltage and having a value of resistance weighted in accordance with the order of the digit in the number.

Input voltages are derived from stages of the sources **10** and **12** and are applied to these resistances. A typical stage of these sources is indicated generally as **53** in FIG. **3**. Weighting of the resistors **54** to **60** and **62** to **68** is accomplished in a well-known manner for providing the desired conversion. For example, for a number of radix (2) and having *n* digits, the value of resistance corresponding to a digit of order *k* can be determined by selecting a value of resistance R_n for the *n*th order and then calculating the value of resistance for the lower order *k*. This calculation is made according to the equation

$$R_k=R_n\times 2^{(n1k)} \qquad (5)$$

where $k=0$ for the least significant digit. For the converter of FIG. **3**, the resistances would thus have the values:

$R60=R68=R_n$, where the value of R_n is preselected. According to equation (5), $R58=R66=2\times_n$; $R56=R64=4\times R_n$ and $R54=R62=8\times R_n$.

In the particular arrangement of this circuit for which component values are indicated hereinafter, the weighted resistors of the networks **50** and **52** provide approximately 1 volt steps from 15 volts, when the input digit voltages represent a number having a logical value of 0, to 0 volts when each input digit has a logical value of 1. Generally, the degree of circuit reliability will decrease as the number of resistors in the networks **50** and **52** increases and corresponding voltage differentials decrease. As indicated, and in accordance with a feature of the invention, a plurality of converter-comparator stages are provided. By the use of a plurality of these stages, the number of resistors in the networks **50** and **52** can be appropriately preselected to provide the desired degree of accuracy and reliability.

Analog output voltages which appear between terminal **24** and ground and between terminal **26** and ground are applied to associated emitter follower amplifier stages having transistor amplifying devices **70** and **72**. Collector electrodes of these transistors are connected to ground potential and the emitter electrodes are returned through resistors **74** and **76** to a current regulator stage **77**. The current regulator stage **77** includes a transistor **78** having a collector electrode coupled in series with the resistors **74** and **76** and having an emitter electrode maintained at a positive potential by a voltage divider formed by the resistors **80** and **82**. Base electrode biasing current for this transistor is provided by a second voltage divider formed by the resistors **84** and **86**. The operation of this current regulator stage is described in more detail hereinafter.

The circuit of FIG. **3** and other circuits described hereinafter are arranged to function at positive logical levels; i.e., Truth or a logic 1 is represented by a relatively positive voltage level and Falsity or logic 0 is represented by a relatively more negative voltage level, generally near ground potential. Digital voltages applied to converter resistors **54** through **60** and representing a relatively larger number cause a more positive voltage to appear at terminal **33** than a relatively smaller number applied to these same resistors. A similar result occurs with respect to the voltages applied to the resistors of network **52** and to the voltage occurring at terminal **32**.

Voltages at the emitter electrodes of transistors **70** and **72** are applied to base and emitter electrodes of transistors **90** and **92** of a nonlinear differential amplifier. The emitter of the transistor **90** is connected to the output of the emitter follower transistor **72** while its base electrode is connected to the output of the emitter follower transistor **70**. Similarly, the emitter of the transistor **92** is connected to the output of the emitter follower transistor **70** while its base electrode is connected to the output of the emitter follower transistor **72**. An operating potential is derived from a source of potential $+E_1$ and is applied to collector electrodes of these transistors through load resistors **93** and **95**. In operation, when the voltage at terminal **24** is more negative than the voltage at terminal **26**, then the bias on the transistor **90** is increased while the bias on the transistor **92** is simultaneously decreased. The collector current of the transistor **90** decreases correspondingly and the transistor **90** is driven to collector current cutoff while the transistor **92** is driven to collector current saturation. The differential amplifier is thus adapted to distinguish between the analog voltages at the terminals **24** and **26** and to cause an accompanying saturation and cutoff in the associated transistors. The differential amplifier thereby provides digital voltages at terminals **28** and **29** which are indicative of the relative magnitudes of the digital input voltages E_A^{0to3} and E_B^{0to3}.

Since the differential amplifier is required to distinguish between voltage levels over a range of voltages and provide a digital output, it is operated in a nonlinear manner. In doing so, the amplifier is arranged to respond only to a minimum preselected voltage deviation between the input analog voltages. Deviations between these analog voltages which are less than the preselected minimum will not cause an output change. A dead band or tolerance band is thereby provided. This band is established in the arrangement of FIG. **3** by virtue of the base-emitter diode voltage of the transistors **92** and **90**, which as indicated hereinafter are silicon transistors. Alternatively, voltage dropping means such as diodes can be coupled in the base leads of other types of transistors when the desired voltage drop cannot be obtained from the base-emitter diode

of the transistor. In a particular arrangement of this circuit for which component values are enumerated hereinafter, the transistor is adapted to respond to a voltage differential of 0.5 volts or greater.

The emitters of **94** and **96** are kept at a constant voltage by the regulating action of **78**.

Although the voltages at the collector of the transistors **90** and **92** are in digital form and are representative of the magnitude of the input numbers E_A^{0to3} and E_B^{0to3}, it is not always feasible to provide voltages at these collectors which are compatible with the logical voltage levels used throughout the apparatus. Accordingly, transistors **94** and **96** are provided for matching the converter and comparator to the voltage levels of associated logic circuits. The collectors of the transistors **90** and **92** are coupled to base electrodes of switching transistors **94** and **96** respectively and drive the latter transistors to cutoff or saturation. The switching transistor collector electrodes are coupled via resistors **98** and **100** and terminals **33** and **32** respectively to NOR gates in the logical circuit **36** (FIG. **4**).

The circuit arrangement for the logic stages **36**, **38** and **40** of FIG. **1** for comparing the digital outputs from an associated converter and comparator stage along with a digital output of a more significant logic stage is illustrated in FIG. **4**. The logic circuit of FIG. **4** includes NOR gates formed by transistors **110** and **112**. Inputs to this circuit are derived from the collector electrode of the transistors **94** and **96**, (FIG. **3**) as indicated, and from a higher order similar logical stage when appropriate. The input from the higher order logical stage, such stage **38**, is applied to terminals **114** and **116** respectively. An indication from a higher order logical circuit that E_A is greater than E_B is represented by a logic **1** and a relatively positive voltage level. The logic circuit **36** includes input resistors **118** and **120** and resistors **122** and **124** coupled to a source of bias potential ($-E_2$). Operating potential is applied to the collector electrodes of transistors **110** and **112** via load resistors **126** and **128** respectively. The output of NOR gate transistor **110** is applied via a resistor **132** to a transistor **130** of a successive NOR gate. The output of NOR gate transistor **112** is similarly applied via a resistor **136** to a transistor **134** of successive NOR gate. Input voltages from the preceeding logical stage, as for example stage **38**, are also cross coupled, as indicated, via a resistor **138** to the transistor **134** and via a resistor **140** to the transistor **130**. Bias is established at the base of the transistors **130** and **134** by resistors **142** and **146** respectively. Operating potential is derived from a source $+E_1$ and is applied to the collector electrodes of these transistors through resistors **148** and **150**. The output from this logical circuit is provided at terminals **41** and **42**. Similarly, output terminals **43** and **44** are provided for logic stage **38** (FIG. **1**) and output terminals **45** and **46** are provided for logic stage **40**. Since a higher order digital representative voltage is not applied to the logical circuit **40**, and since it is at times desirable to employ similar circuit modules in the circuit arrangement, the more significant digit input terminals are grounded. Alternatively, the output voltages of terminals **37** and **39** can be applied to more significant input terminals of the logical stage **38**.

The circuit arrangement of FIG. **4** operates in accordance with the logical expressions **1** through **4**. Positive input voltage levels or negative going pulses to NOR gate transistors **110**, **112**, **130** and **134** represent a logic **1** while more negative levels represent a logic **0**. A **1** output at terminal **41**, represented by a relatively positive voltage level, indicates that the number E_A^{0to0} is greater than or equal to the number E_B^{0to0} and conversely a **1** or relatively positive voltage level at terminal **42** indicates that the opposite is true. When inputs to the logical circuit are equal the output at terminals **41** and **42** will be relatively negative and equal. A truth table for various logical input combinations at terminals **32**, **33**, **114**, and **116** is shown in FIG. **5** along with the corresponding outputs at terminals **41** and **42**. As indicated previously, an input positive level from a higher order logic stage such as at terminal **114** will govern the operation of the FIG. **4** circuit. For example, an indication from logical stage **38** that more significant digits of *A* are greater than *B* causes relatively positive and negative voltages at terminals **114** and **116** respectively. Accordingly, a positive voltage at terminal **114** causes transistors **110** and **134** to conduct and a relatively negative appears at their collector electrodes. A corresponding negative voltage at terminal **116** causes transistor **130** to cut off, Thus the inputs to transistor **130** are both negative, **130** cuts off, and its collector electrode appears relatively positive. The inputs to terminal **32** and **33** will control the output only when inputs to terminals **114** and **116** are both negative, i.e., the more significant digits of *A* and *B* are equal.

The output voltages at terminals **41** and **42** can be employed with suitable buffers to operate relays, etc. in accordance with a desired control function which is to accompany the comparison. In addition, terminals **41** and **42** can be coupled to further logical circuits such as an AND gate to effect some function which is to accompany equality of the numbers *A* and *B*.

While other component values and arrangements may be selected in practicing the present invention, the following components, voltages and signal levels have been successfully employed in a particular arrangement of the invention.

Transistors:
NPN—92, 94, 110, 112, 130, 134—Sprague type TN-59.
PNP—72, 78, 96, 94, 70—2N 3638 (Epoxy).

Resistors:
60, 68—30.1^k, 1%, mil type Rn 60 Filmister.
58, 66—15^k, 1%, mil type Rn 60 Filmister.
56, 64—7.5^k, 1%, mil type Rn 60 Filmister.
54, 62—3.74^k, 1%, mil type Rn 60 Filmister.
74, 76—68^k, ¼ watt, 10%.
80, 84—2.2^k, ¼ watt, 10%.
82, 86—2.2^k, ¼ watt, 10%.
93, 95—2.2^k, ¼ watt, 10%.
98, 100—5.6^k, ¼ watt, 10%.
122, 124, 142, 146—75^k, ¼ watt, 10%.
118, 120, 132, 138, 136, 140—7.5^k, ¼ watt, 10%.
126, 128, 148, 150—4.7^k, ¼ watt, 10%.

$+E_1 = +28^v \quad -E_2 = -12^v$

Input levels to networks 50 and 52:
Logic $1 = 0^v$
Logic $0 = +15^v$

Output levels—
Terminal 41:
A=B=Logic $1 = 0^v$
A B=Logic $0 = +28^v$
Terminal 42:
B=A=Logic $1 = 0^v$
B A=Logic $0 = +28^v$

An improved circuit arrangement has thus been described for comparing numbers occuring in digital form, which requires relatively fewer components, and which is accompanied by greater circuit economy.

While a particular embodiment of the invention has been described hereinbefore, it will be understood that various changes and modifications can be provided therein without departing from the spirit of the invention or the scope of the appended claims.

I claim:

1. A comparator circuit arrangement comprising:
first and second resistive summing networks for summing a plurality of digital voltages applied to each network and for providing equivalent analog output voltages,
means for applying a plurality of digital voltages representing a first number *A* to said first resistive network and a plurality of digital voltages representing a second number B to said second resistive network,
first and second emitter follower amplifier stages and a differential amplifier having first and second transistor amplifying devices,
means coupling said first and second resistive networks to said first and second emitter follower amplifiers respectively,
means coupling an output voltage from said first emitter follower amplifier to base and emitter electrodes of said first

and second transistor amplifying devices respectively,

means coupling an output voltage from said second emitter follower amplifier to emitter and base electrode of said first and second transistor amplifying devices respectively, and

said resistive networks and amplifier stages arranged for providing a digital output voltage indicative of the relative magnitudes of the numbers *A* and *B*.

2. A comparator circuit arrangement comprising:

first circuit means providing a plurality of output voltages representative of a first number *A* having *n* digits,

second circuit means providing a plurality of output voltages representative of a second number *B* having *n* digits,

third and fourth circuit means each adapted to convert first and second pluralities of digital voltages to first and second analog voltages respectively and for providing first and second digital output voltages indicative of the relative amplitudes of the analog voltages,

means coupling a plurality of voltages representing less significant digits of said numbers *A* and *B* from said first and from said second circuit means respectively to said third circuit means and coupling a plurality of voltages representing more significant digits of said numbers *A* and *B* from said first and from said second circuit means to said fourth circuit means,

a digital comparator circuit adapted to provide an output voltage indicative of the relative magnitude of a plurality of digital numbers applied thereto, and

means coupling the digital voltages from said third and fourth circuit means to said comparator circuit.

3. The comparator of claim **2** wherein said third and fourth circuit means each include first and second digital to analog voltage converters and a differential amplifier coupled to said converter and adapted to compare and provide a digital output voltage representative of the relative magnitude of said analog voltages.

4. The comparator of claim **2** wherein:

said third circuit means provides digital output voltages E_A when the less significant digits of *A* represent a number larger than the less significant digits of *B* as an output voltage E_B when the less significant digits of *B* represent a number larger than the less significant digits of *A*,

said fourth circuit means provides a digital output voltage E'_A when the more significant digits of *A* represent a number larger than the more significant digits of *B* and as output voltage E'_B when the more significant digits of *B* represent a number larger than the more significant digits of *B*, and

said digital comparator circuit includes a circuit arrangement for providing an output voltage E_{AO} when the number *A* is larger than the number *B* and an output voltage E_{BO} when the number B is larger than the number *A*.

5. The comparator of claim **4** wherein said digital comparator circuit is arranged to provide the output voltage E_{AO} in accordance with the logical relation:

$$E_{AO}=E_A'+(E_A\cdot\overline{E_B'})$$

6. The comparator of claim **4** wherein said digital comparator circuit is arranged to provide the output voltage E_{AO} in accordance with the logical relation:

$$E_{AO}=\overline{\overline{E_A'}+\overline{E_A}+E_B'}$$