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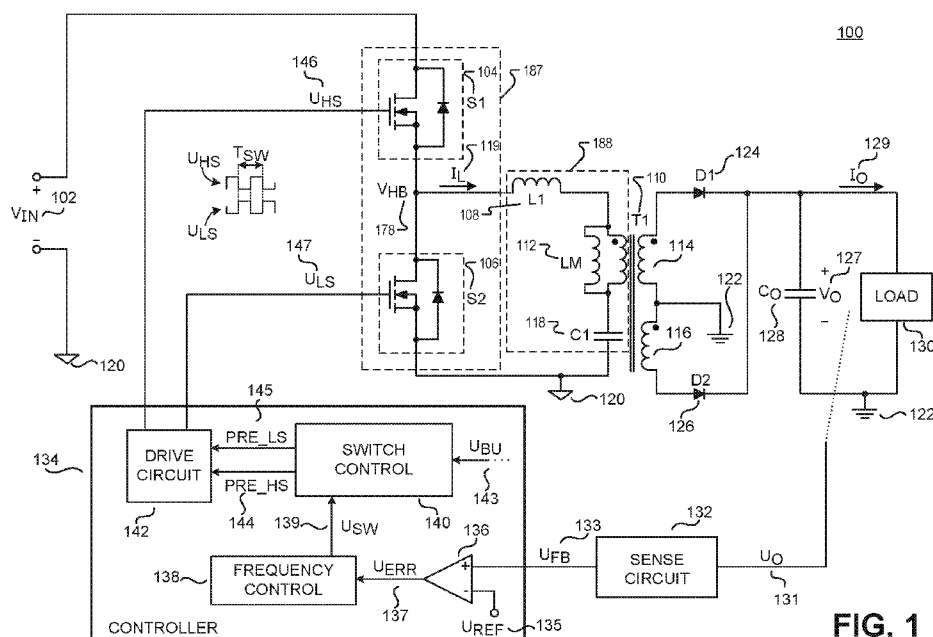


FIG. 1

(57) **Abstract:** A resonant power converter includes a drive circuit coupled to control switching a switching circuit coupled to a resonant tank circuit. A switch control circuit is coupled to control the drive circuit to control the switching of the switching circuit in response to a switching frequency signal. The switch control circuit is further coupled to control a burst mode of the controller in response to a burst signal. An initial active pulse of the switching circuit when entering the burst mode is an active partial pulse. A final active pulse of the switching circuit when exiting the burst mode is an active full pulse resulting in a passive partial pulse following the first and second switches being turned off to exit the burst mode. A frequency control circuit is coupled to generate the switching frequency signal in response to a feedback signal.



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SWITCH CONTROL FOR RESONANT POWER CONVERTER

BACKGROUND INFORMATION

Field of the Disclosure

[0001] The present invention relates generally to switched mode power converters, and more specifically to resonant power converters.

Background

[0002] Electronic devices use power to operate. Switched mode power converters are commonly used due to their high efficiency, small size, and low weight to power many of today's electronics. Conventional wall sockets provide a high voltage alternating current. In a switching power converter, the high voltage alternating current (ac) input is converted to provide a well-regulated direct current (dc) output through an energy transfer element. The switched mode power converter usually provides output regulation by sensing one or more inputs representative of one or more output quantities and controlling the output in a closed loop. In operation, a switch is utilized to provide the desired output by varying the duty cycle (typically the ratio of the on time of the switch to the total switching period), varying the switching frequency, or varying the number of pulses per unit time of the switch in a switched mode power converter. Varying the duty cycle may be referred to as pulse width modulation (PWM) control, while varying the switching frequency may be referred to as pulse frequency modulation (PFM) control.

[0003] One type of switched mode power converter topology is a resonant switched mode power converter, which utilizes a resonant inductance-capacitance (L-C) circuit as part of the power conversion process. In general, resonant switched mode power converters with PFM control may have some advantages compared to non-resonant converters, such as operating at higher switching frequencies with lower switching loss, utilize smaller magnetic elements (and therefore utilize smaller packaging), and still operate with high efficiency. Resonant power converters generally do not have waveforms with sharp edges (*e.g.*, waveforms having high di/dt or dv/dt) and as such electromagnetic interference (EMI) performance may be improved and allows the use of smaller EMI filters as compared to non-resonant converters.

[0004] LLC converters are a type of resonant switched mode power converter, which utilizes the resonance between two inductors and a capacitor. LLC converters are popular due to the savings on cost and size by utilizing the magnetizing and leakage inductance of the power converter's energy transfer element as part of the resonance component of the LLC converter. In addition, LLC converters can achieve stability when they are operated at above resonance (*i.e.*, operated at a switching frequency greater than the resonant frequency of the LLC) with zero voltage switching, which can result in lower switching losses.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

[0006] **FIG. 1** illustrates a functional block diagram of an example resonant power converter and controller in accordance with the teachings of the present invention.

[0007] **FIG. 2** illustrates a timing diagram showing example waveforms for various currents and signals of the resonant power converter and controller of **FIG. 1** in accordance with the teachings of the present invention.

[0008] **FIG. 3A** illustrates a functional block diagram of an example resonant power converter and controller utilizing a bootstrap circuit in accordance with the teachings of the present invention.

[0009] **FIG. 3B** illustrates an example bootstrap control circuit of the controller of **FIG. 3A** in accordance with the teachings of the present invention.

[0010] **FIG. 3C** illustrates an example load sense circuit of the controller of **FIG. 3A** in accordance with the teachings of the present invention.

[0011] **FIG. 4** illustrates a timing diagram showing example waveforms for various voltages, currents, and signals of the resonant power converter and controller of **FIGs. 3A, 3B, and 3C** in accordance with the teachings of the present invention.

[0012] Corresponding reference characters indicate corresponding components throughout the several views of the drawings. Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of various embodiments of the present invention. Also, common but well-understood elements that are useful or necessary in a commercially feasible embodiment are often not depicted in order to facilitate a less obstructed view of these various embodiments of the present invention.

DETAILED DESCRIPTION

[0013] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

[0014] Reference throughout this specification to "one embodiment", "an embodiment", "one example" or "an example" means that a particular feature, structure or characteristic described in connection with the embodiment or example is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment", "in an embodiment", "one example" or "an example" in various places throughout this specification are not necessarily all referring to the same embodiment or example. Furthermore, the particular features, structures or characteristics may be combined in any suitable combinations and/or subcombinations in one or more embodiments or examples. Particular features, structures or characteristics may be included in an integrated circuit, an electronic circuit, a combinational logic circuit, or other suitable components that provide the described functionality. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

[0015] Resonant converters, such as LLC converters, typically include a resonant tank circuit that include a tank inductance and a tank capacitance, as found for instance in LLC circuits. Resonant converters may take advantage of soft switching control to provide output voltage without the associated high switching losses, high switching stress on the power switch, and high EMI caused by fast switching edges.

[0016] Soft switching the power switch of an LLC converter may also enable zero voltage switching (ZVS) in which the voltage across the power switch is zero when the power switch is turned on which may reduce the switching losses for the LLC converter. For the example of a half-bridge LLC converter, two power switches (referred to as a high side switch and a low side switch in a half bridge switching circuit) are used to control the transfer of energy to the output of the power converter. The power switches are controlled such that when one power switch is ON, the other power switch is OFF, and the two power switches are controlled to be ON for substantially equal amounts of time. In general, a switch that is ON (or closed), may conduct current, while a switch that is OFF (or open) does not typically conduct current. In one example, the first switch is ON while the second switch is OFF. The first switch is turned OFF with a non-zero current. After the first switch turns OFF, the voltage across the second

switch will typically fall. Soft switching generally refers to turning on the second switch as the voltage across the second switch reaches near-zero. Using this type of switching prevents energy loss from discharge of the capacitance across the terminals of the switch during switch turn-on. To achieve ZVS, the power switches are controlled such that there is a period of time, referred to as "dead time," where both power switches are OFF prior to one of the power switches turning ON. Further, during "dead time" period when both switches are OFF, the voltage across one of the power switches may be reduced to zero and once at zero volts, this switch could be turned ON with minimal switching loss (achieving ZVS).

[0017] Further, LLC converters may be designed to control the power switches to reduce power consumption at no load or low load operating conditions. One method for reducing power consumption at no load or low load operating conditions may be referred to as burst mode control. During no load or low load power conditions, the power switches are not continuously turned ON and OFF to deliver the required output power. Rather, the power switches may be controlled in burst mode, where they are sequentially turned ON and OFF for an interval of time (usually referred to as burst on time) followed by an interval of no switching (usually referred to as burst off time). However, the timing to enter and exit burst mode control may need to be controlled to ensure that the LLC converter maximizes the benefits of soft switching and ZVS.

[0018] Under steady burst-off conditions, the tank current through the resonant tank circuit of an LLC converter is substantially zero while the half bridge voltage (the voltage at the node between the high side and low side power switches of the half bridge switching circuit) is substantially half of the input voltage of the power converter. When entering into burst mode, the high side or low side switch is turned on when the resonant tank current is substantially zero, is turned off when the resonant tank current is substantially non-zero, and the waveform of the resonant tank current is substantially symmetrical around zero. As such, the high side or low side switch is turned on partway through a conduction cycle. This turning on of the high side or low side switch about partway through a conduction cycle when the resonant tank current is substantially zero may be referred to as a "partial cycle" or as a "partial pulse" herein.

[0019] Since during burst-off state, the resonant tank current is zero when the high side or low side switch is turned on, the partial cycle is hard-switched. Further, this hard-switched partial cycle is also an active hard-switched partial cycle since the switch control circuit actively turns on the switch after an interval of non-switching. However, the subsequent switching cycles or switching pulses during burst-on period of the switches after the initial active hard-switched partial cycle are soft-switched full cycles because the inductor current is non-zero when the high and low side switches are switched. By turning on the high side switch or the low side switch

with an active full cycle or an active full pulse, the LLC converter may operate with soft-switching and achieve ZVS.

[0020] When exiting burst mode, a passive partial cycle or partial pulse occurs after both the high side and low side switches are turned off due to the energy stored in the resonant tank discharging through the body diode of either the high side switch or the low side switch. This may be referred to as a passive partial cycle or as a passive partial pulse herein because neither the high side switch nor the low side switch are actively turned on by the switch control circuit when exiting the burst mode. The passive partial cycle or pulse at the end of burst mode allows for overall symmetry for the resonant tank. The passive partial cycle is also soft-switched due to a non-zero tank current at the start of this partial cycle.

[0021] To illustrate **FIG. 1**, a functional block diagram illustrating one example of a resonant power converter 100 including a switching circuit 187 coupled to an input of the resonant power converter 100 and an energy transfer element T1 110. A resonant tank circuit 188 is also coupled to the switching circuit 187. A controller 134 is coupled to generate first and second drive signals U_{HS} 146 and U_{LS} 147 to control switching of the switching circuit 187 to regulate a transfer of energy from the input to the output of the resonant power converter 100 through the energy transfer element T1 110. The resonant tank circuit 188 includes tank inductance and a tank capacitance. In the depicted example, the resonant tank circuit 188 is an LLC circuit such that the tank inductance includes a leakage inductance L1 108 and a transformer magnetizing inductance LM 112 of the energy transfer element T1 110. In the example, the tank capacitance includes capacitance C1 118. The leakage inductance and transformer magnetizing inductance can be either discrete components, or combined into a single transformer (with leakage and magnetizing elements). In the depicted example, the switching circuit 187 is a half bridge switching circuit that includes a first switch coupled to a second switch, which are coupled to the resonant tank circuit 188 of the resonant power converter 100. In the depicted example, the first and second switches of the switching circuit 187 are a high side switch S1 104 and a low side switch S2 106. It is appreciated that although the resonant power converter 100 illustrated in **FIG. 1** is configured as an LLC resonant converter coupled in a half-bridge topology, other resonant converter topologies may benefit from the teachings of the present disclosure.

[0022] In one example, a drive circuit 142 of the controller 134 is configured to generate the first and second drive signals when entering a burst mode to actively turn on one of the first and second switches of the switching circuit 187 to result in an active partial cycle when initially entering the burst mode. When exiting the burst mode, that same one of the first and second switches that was actively switched on for the active partial cycle at the beginning of the burst

mode, is switched on by the drive circuit for a final active full cycle of the burst mode, which results in a passive partial cycle after both of the first and second switches are turned off to exit the burst mode, due to the remaining resonant tank current being discharged through a body diode of the other one of the first and second switches during the passive partial cycle in accordance with the teachings of the present invention.

[0023] As illustrated, the resonant power converter 100 is coupled to receive an input voltage V_{IN} 102, which may be a rectified ac voltage, and provide output power to the load 130 coupled to the output of the resonant power converter 100. The switching circuit 187 in the depicted example is illustrated with high side switch S1 104 that is coupled to receive the input voltage V_{IN} 102 at one end, and coupled to the low side switch S2 106 at the other end. The low side switch S2 106 is further coupled to input return 120. The terminal between the high side switch S1 104 and the low side switch S2 106 may be referred to as the half bridge terminal of the switching circuit 187 with half bridge voltage V_{HB} 178. In the example shown, both the high side switch S1 104 and the low side switch S2 106 are illustrated as n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) along with their respective body diodes. The high side switch S1 104 and the low side switch S2 106 are controlled with first and second drive signals U_{HS} 146 and U_{LS} 147 such that the voltage across a primary winding 112 of the energy transfer element T1 110 is substantially a square wave.

[0024] As shown, the energy transfer element T1 110 includes the primary winding 112, a first output winding 114, and a second output winding 116. The primary winding 112 is coupled to the high side switch S1 104 and the low side switch S2 106 of switching circuit 187. Further, the resonant tank circuit 188 is coupled across the low side switch S2 106 in the illustrated example. As mentioned, the resonant tank circuit 188 in the illustrated example includes the inductance L1 108, inductance LM 112, and the capacitance C1 118. For the example shown, the leakage inductance (inductance L1 108) and the magnetizing inductance LM 112 of the energy transfer element T1 110 are used to provide the tank inductance for the resonant tank circuit 188 of the power converter 100. In some examples, one or more of the capacitance of capacitance C1 118 and the inductance of inductor L1 108 and LM 112, are embedded properties of the energy transfer element T1 110 such that one or more of capacitance C1 118 and inductance L1 108 and LM 112, are not discrete physical components. The current I_L 119 is the tank current through the resonant tank circuit 188. As shown in **FIG. 1**, the current I_L 119 is the current from half-bridge terminal V_{HB} 178 towards the energy transfer element T1 110.

[0025] In one example, the first output winding 114 and the second output winding 116 are center tapped, or in other words, the terminal between the first winding 114 and the second

winding 116 is coupled to output return 122. The first output winding 114 is also coupled to rectifier D1 124, while the second output winding 116 is coupled to the rectifier D2 126. Rectifiers D1 124 and D2 126 are illustrated as diodes, however a transistor used as a synchronous rectifier may also be used. Energy is transferred and rectified by rectifier D1 124 when the high side switch S1 104 is turned ON and the low side switch S2 106 is OFF. When the high side switch S1 104 is OFF and the low side switch S2 106 is ON, energy is transferred and rectified by rectifier D2 126. One end of the output capacitor C_O 128 is coupled to both rectifiers D1 124 and D2 126 (as shown, the cathode end of both rectifiers D1 124 and D2 126) while the other end is coupled to output return 122. The load 130 is coupled across the output capacitor C_O 128. An output is provided to the load 130, and may be provided as either an output voltage V_O 127, an output current I_O 129, or a combination of the two.

[0026] The resonant power converter 100 further includes circuitry to regulate the output, which is exemplified as output quantity U_O 131. The output quantity U_O 131 may be either an output voltage V_O 127, an output current I_O 129, or a combination of the two. A sense circuit 132 is coupled to sense the output quantity U_O 131 and to provide feedback signal U_{FB} 133, which is representative of the output quantity U_O 131. Feedback signal U_{FB} 133 may be a voltage signal or a current signal. There may be a galvanic isolation (not shown) between the controller 134 and the sense circuit 132. The galvanic isolation could be implemented by using devices such as an opto-coupler, a capacitor, or a magnetic coupling.

[0027] Controller 134 is coupled to receive the feedback signal U_{FB} 133 and outputs the high side drive signal U_{HS} 146, which controls the switching of high side switch S1 104, and the low side drive signal U_{LS} 147, which controls the switching of low side switch S2 106. The high side drive signal U_{HS} 146 and low side drive signal U_{LS} 147 control various switching parameters to control the transfer of energy from the input to the output of power converter 100. For a resonant converter, the output voltage is controlled by adjusting the switching frequency of the high side switch S1 104 and low side switch S2 106. For the example of a half-bridge LLC converter, the duty cycle for both the high side switch S1 104 and low side switch S2 106 are substantially equal and close to fifty percent (including the dead time).

[0028] Controller 134 is shown as including an error amplifier 136, a frequency control circuit 138, a switch control circuit 140, and a drive circuit 142. The error amplifier 136 is coupled to receive the feedback signal U_{FB} 133 (at its non-inverting input) and a reference signal U_{REF} 135 (at its inverting input). Error amplifier 136 amplifies the difference between the feedback signal U_{FB} 133 and the reference signal U_{REF} 135, and provides the amplified difference as error signal U_{ERR} 137 which is proportional function of the output quantity U_O 131 being regulated.

[0029] Frequency control circuit 138 is coupled to receive the error signal U_{ERR} 137, and outputs the switching frequency signal U_{SW} 139. The switching frequency signal U_{SW} 139 is representative of the switching frequency (or in other words, the switching period T_{SW}) of the high side switch S1 104 and the low side switch S2 106. In response to the error signal U_{ERR} 137, the frequency control circuit 138 determines the switching frequency for the power converter 100. In one example, if the error signal U_{ERR} 137 is positive (*i.e.*, the feedback signal U_{FB} 133 is greater than the reference signal U_{REF} 135, or "above target"), the frequency control circuit 138 increases the switching frequency (and the switching period T_{SW} is decreased). The larger the difference, the greater the switching frequency is increased. If the error signal U_{ERR} 137 is negative (*i.e.*, the feedback signal U_{FB} 133 is less than the reference signal U_{REF} 135, or "below target"), the frequency control circuit 138 decreases the switching frequency (and the switching period T_{SW} is increased). The greater the difference in magnitude, the greater the switching frequency is decreased. For an LLC converter, decreasing the switching frequency increases the power delivered to the output of the converter.

[0030] The switch control circuit 140 is shown as coupled to receive the switching frequency signal U_{SW} 139 and the burst signal U_{BU} 143, and outputs intermediate drive signals to control switching of the high side switch S1 104 and low side switch S2 106 during the burst mode. These intermediate drive signals output by switch control circuit 140 are illustrated in **FIG. 1** as the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145. In one example, the burst signal U_{BU} 143 is an enable signal, which indicates when the high side switch S1 104 and the low side switch S2 106 may be turned on. The burst signal U_{BU} 143 may be generated on the secondary side of the power converter 100 or may be generated in response to the error signal U_{ERR} 137. For the example shown, the switch control circuit 140 outputs the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145 to control the turning on and off of the high side switch S1 104 and low side switch S1 106, which may occur while the burst signal U_{BU} 143 is logic high.

[0031] In one example, the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145 are digital signals. When the burst signal U_{BU} 143 is logic low, the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145 are also logic low, and the high side switch S1 104 and low side switch S1 106 are disabled from switching. Under full load conditions, the burst signal U_{BU} 143 is logic high. Under no-load or low-load conditions, the burst signal U_{BU} 143 resembles a rectangular pulse waveform of varying lengths of logic high and logic low sections to provide the burst mode switching. The switch control circuit 140 utilizes the switching frequency signal U_{SW} 139 to set the switching frequency of the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145.

[0032] In addition, the switch control circuit 140 controls the high side switch S1 104 or the low side switch S2 106 to turn on with an initial active partial cycle. In other words, after the burst signal U_{BU} 143 transitions to a logic high, and indicates that switching of the power switches S1 104 and S2 106 should begin, the first switching event is an active partial cycle for either the high side switch S1 104 or the low side switch S2 106. As mentioned above, for an LLC converter, the power switches S1 104 and S2 106 are controlled such that they are on for substantially the same amount of time and that on-time may be referred to as a full conduction time/full conduction cycle. With an active partial cycle, one of the power switches is turned on for only part of the full conduction pulse/cycle. After the partial cycle, the power switches are turned on for the entire full conduction pulse/cycle. In one example, each power switch is turned on for approximately 25-75% of the full conduction time for an active partial cycle. In a further example, each power switch is turned on for 50% of the full conduction time for an active partial cycle. For the example shown, the high side switch S1 104 is turned on with an active partial cycle when the burst signal U_{BU} 143 indicates that switching should begin.

[0033] In one example, once the burst signal U_{BU} 143 transitions to a logic low, and therefore indicates that switching of the power switches S1 104 and S2 106 should be discontinued, the switch control circuit 140 controls the power switches S1 104 and S2 106 to stop switching at the end of the next full conduction cycle for which ever power switch turned on with the partial cycle. In one example, if it was the high side switch S1 104 that was turned on with an active partial cycle at the beginning of the burst cycle (indicated by the burst signal U_{BU} 143), the last active switching event would end with full conduction pulse/cycle of the high side switch S1 104 at the end of the burst cycle (as indicated with the burst signal U_{BU} 143 transitioning to a logic low). However, either switch could conduct the last full conduction cycle.

[0034] Drive circuit 142 is coupled to receive the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145, and outputs the high side drive signal U_{HS} 146 and the low side drive signal U_{LS} 147. Similar to the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145, the high side drive signal U_{HS} 146 and the low side drive signal U_{LS} 147 are output to control switching of the high side switch S1 104 and low side switch S2 106, respectively. In one example, the drive circuit 142 level shifts the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145 to suitable levels to drive the high side and low side switches S1 104 and S2 106. Further, the drive circuit 142 may amplify the current of the pre-high side drive signal PRE_HS 144 and pre-low side drive signal PRE_LS 145 such that the high side drive signal U_{HS} 146 and the low side drive signal U_{LS} 147 may sufficiently drive the high side switch S1 104 and low side switch S2 106, respectively.

[0035] FIG. 2 illustrates a timing diagram 200 of example waveforms for the burst signal U_{BU} 243, low side drive signal U_{LS} 247 and pre-low side drive signal PRE_LS 245, high side drive signal U_{HS} 246 and pre-high side drive signal PRE_HS 244, and the inductor current I_L 219, which correspond to similarly named and number signals shown in FIG. 1. As shown in FIG. 2, the low side drive signal U_{LS} 247 and pre-low side drive signal PRE_LS 245 are illustrated as one waveform, and the high side drive signal U_{HS} 246 and pre-high side drive signal PRE_HS 244 are also illustrated as one waveform, since in the depicted example the low side drive signal U_{LS} 247 and high side drive signal U_{HS} 246 are level shifted versions of the pre-low side drive signal PRE_LS 245 and the pre-high side drive signal PRE_HS 244, respectively.

[0036] During steady state burst-off conditions, the inductor current I_L 219 is substantially zero while the half bridge voltage at the half bridge terminal (*i.e.*, V_{HB} 178 in FIG. 1) is substantially half the input voltage $V_{IN}/2$. At time t_1 252, the burst signal U_{BU} 243 transitions to a logic high value, indicating that switching events of the high side switch S1 104 and the low side switch S2 106 should occur. In the example shown, the high side switch S1 104 is controlled to have an initial active partial cycle when switching begins. As such, when the burst signal U_{BU} 243 transitions to the logic high value at time t_1 252, the pre-high side drive signal PRE_HS 244 transitions to a logic high value and the high side drive signal U_{HS} 246 turns on the high side switch S1 104. As shown, since pulse 280 is the initial pulse of the burst mode interval, pulse 280 is a partial pulse, and therefore has a partial pulse width T_{PW} 248. The term partial pulse refers to a pulse width that is less than the full pulse width T_{FW} 249 when the power switches S1 104 and S2 106 are controlled with substantially 25-75% duty cycle. As shown in FIG. 2, the partial width T_{PW} 248 is about half the full pulse width T_{FW} 249.

[0037] When the high side switch S1 104 is hard switched on at time t_1 252, the inductor current I_L 219 increases from zero, and the current flows from the MOSFET of the high side switch S1 104 to input return 120 through the energy transfer element T1 110. The example shown in FIG. 2 controls the pre-low side drive signal PRE_LS 245 and the pre-high side drive signal PRE_HS 244 such that the partial pulse 280 occurs during the logic high in the pre-high side drive signal PRE_HS 244, however, in another example, the partial pulse 280 could have occurred during a logic high in the pre-low side drive signal PRE_LS 245.

[0038] At time t_2 253, the pre-high side drive signal PRE_HS 244 transitions to a logic low value and the high side switch S1 104 is turned off. After the dead time, the pre-low side drive signal PRE_LS 245 transitions to a logic high value, causing the low side drive signal U_{LS} 247 to turn on low side switch S2 106 at time t_2 253. This pulse is a soft switched pulse since the on low side switch S2 106 is turned on while the inductor current I_L 219 is non-zero. The first pulse for the low side switch S2 106 is also a full pulse in that the length of the pulse is

substantially the full pulse width T_{FW} 249. When the low side switch S2 106 is on, the slope of the inductor current I_L 219 changes (as shown by the decreasing inductor current I_L 219), and the flow of the inductor current I_L 219 changes direction from the energy transfer element T1 110 to the input return 120 through the MOSFET of the low side switch S2 106.

[0039] After the first partial pulse 280, the pre-low side drive signal PRE_LS 245 transitions to a logic high value and the pre-high side drive signal PRE_HS 244 transitions to a logic low value for the full pulse width T_{FW} 249 (and are not logic high at the same time) as long as the burst signal U_{BU} 243 is logic high. As such, the low side drive signal U_{LS} 247 and the high side drive signal U_{HS} 246, when active, can turn on the low side switch S2 106 and the high side switch S1 104 for the full pulse width T_{FW} 249 for their respective on times. Further, there is dead time between a pre-low side drive signal PRE_LS 245 and the pre-high side drive signal PRE_HS 244 pulse during which both signals are logic low. As illustrated, the switching period T_{SW} 239 (*i.e.*, 1/the switching frequency) is the time between leading edges of full pulse width T_{FW} 249 pulses for the pre-low side drive signal PRE_LS 245 or the pre-high side drive signal PRE_HS 244. The switching period T_{SW} 239 (*i.e.*, 1/the switching frequency) is determined by the frequency control circuit 138 shown in **FIG. 1**. During a full pulse of either the pre-low side drive signal PRE_LS 245 or the pre-high side drive signal PRE_HS 244, the inductor current I_L 219 varies or transitions between first and second inductor current values during the full pulses of the burst mode. In the depicted example, the first and second inductor current values that define the range of values during burst mode for inductor current I_L 219 are a peak current I_{PK} 250 and a minimum current I_{MIN} 251 as shown in **FIG. 2**. When the partial width T_{PW} 248 of the partial pulse 280 is substantially equal to half the width of the full pulse width T_{FW} 249, the magnitudes of the peak current I_{PK} 250 and a minimum current I_{MIN} 251 are substantially equal.

[0040] As shown in **FIG. 2**, the burst signal U_{BU} 243 transitions to a logic low value, indicating that switching of the power switches should cease, at time t_3 254. The partial pulse to enter burst mode was on the pre-high side drive signal PRE_HS 244. As such, the switching of both the power switches stops at the end of the next full pulse for the pre-high side drive signal PRE_HS 244. At time t_3 254, the burst signal U_{BU} 243 transitions to a logic low value during a full pulse 256 of the pre-low side drive signal PRE_LS 245, indicating an end of the burst mode interval. The switch control circuit 140 allows the full pulse 256 to complete for the pre-low side drive signal PRE_LS 245, and allows one more active full pulse 257 for the pre-high side drive signal PRE_HS 244 before switching is disabled. If the burst signal U_{BU} 243 had transitioned to a logic low value during a full pulse of the pre-high side drive signal PRE_HS 244, such as full pulse 255, switching would be disabled at the end of that pulse of the pre-high side drive signal PRE_HS 244, *i.e.*, the end of full pulse 255.

[0041] After time t_4 281, it is noted that the inductor current I_L 219 passively decreases from the peak current I_{PK} 250 to substantially zero, even though both the high side switch S1 104 and low side switch S2 106 are not actively switched on. In particular, at the end of the full pulse 257, energy is stored in the capacitance C1 118 of the power converter 100 and is discharged through the body diode of the low side switch S2 106 until the inductor current I_L 219 reaches substantially zero. Accordingly, when exiting the burst mode interval, a passive partial cycle or partial pulse occurs after both the high side and low side switches are turned off due to the energy stored in the resonant tank discharging through the body diode of either the high side switch or the low side switch. This may be referred to as a passive partial cycle or as a passive partial pulse herein because neither the high side switch nor the low side switch are actively turned on by the switch control circuit when exiting the burst mode. The passive partial cycle or pulse at the end of burst mode allows for overall symmetry for the resonant tank. As such, the inductor current I_L 219 and the half bridge voltage V_{HB} 178 return to steady state conditions, and the power converter is prepared for the next time the burst signal U_{BU} 243 transitions to a logic high value.

[0042] **FIG. 3A** illustrates a functional block diagram of a resonant power converter 300 with a bootstrap circuit 389 and a controller 334, which controls a switching circuit 387 including the high side switch S1 304 and the low side switch S2 306 such that there is an active partial cycle when entering burst mode, and a passive partial cycle when exiting burst mode. In addition, the controller 334 includes a bootstrap control circuit 363 to control bootstrap circuit 389 during a bootstrap period of the resonant power converter 300. The controller 334 may also optionally include a load sense circuit 373, which is not illustrated in **FIG. 3A**, but is detailed in **FIG. 3C**. The resonant power converter 300 illustrated in **FIG. 3A** is configured as an LLC resonant converter coupled in a half-bridge topology, however, other resonant converter topologies may benefit from the teachings of the present disclosure.

[0043] It is appreciated that resonant power converter 300 shown in **FIG. 3A** is similar to the resonant power converter 100 shown in **FIG. 1**, and that similarly named and numbered elements referenced below are coupled and function similar to as described above. As mentioned, one addition to power converter 300 of **FIG. 3A** is the inclusion of bootstrap circuit 389 coupled to the controller 334 and the switching circuit 387. In the depicted example, switching circuit 387 is a half bridge switching circuit including high side switch S1 304 and the low side switch S2 306, and the bootstrap circuit 389 includes a bootstrap diode 360, and bootstrap capacitors 358 and 359 as shown. During the bootstrap period, bootstrap circuit 389 is used to ensure that there is sufficient energy for the drivers within driver circuit 342 of controller 334 to drive the high side switch S1 304 and the low side switch S2 306 of the switching circuit

387. In particular, as shown in the depicted example, controller 334 includes two terminals (VCCH terminal 361 and VCC terminal 362), which are coupled internally to provide energy to circuitry within the controller 334. Specifically, in one example, the VCCH terminal 361 and the VCC terminal 362 are energy terminals that are coupled to provide power to the drivers within the drive circuit 342 that are used to turn on and off the high side switch S1 304 and the low side switch S2 306 of switching circuit 387 as shown.

[0044] In the depicted example, the bootstrap diode 360 is coupled between the VCC terminal 362 and the VCCH terminal 361. The bootstrap capacitor 359 is coupled between the VCC terminal 362 and input return 320. The bootstrap capacitor 358 is coupled between the VCCH terminal 361 and the half bridge terminal between the high side switch S1 304 and the low side switch S2 306 of the switching circuit 387. In one example, the bootstrap circuit 389 may be controlled to ensure there is sufficient energy at the VCCH terminal 361 to drive the high side switch S1 304 when the high side switch S1 304 is to be turned on during the initial active partial cycle when first entering the burst mode. In order to ensure that there is sufficient energy at the VCCH terminal 361 to drive the high side switch S1 304, the low side switch S2 306 is turned on during a bootstrap operation, which results in the voltage V_{HB} 378 at the half bridge terminal being pulled down through the low side switch S2 306 to substantially the same voltage as the input return 320 (*e.g.*, zero volts). As such, bootstrap diode 360 becomes forward biased and conducts, which enables in the VCCH terminal 361 to be precharged from the VCC terminal 362 through the bootstrap diode 360 during the bootstrap operation. After the VCCH terminal 361 has been charged, and there is sufficient energy for the drivers within driver circuit 342 of controller 334 to drive the high side switch S1 304 and the low side switch S2 306 of the switching circuit 387, the bootstrap operation is complete, and the low side switch S2 may then be turned off to complete the bootstrap operation in accordance with the teachings of the present invention.

[0045] During steady state burst-off conditions, the inductor current I_L 319 is substantially zero and the voltage V_{HB} 378 of the half bridge terminal is substantially half the input voltage V_{IN} 302. As will be discussed, the voltage V_{HB} 378 of the half bridge terminal is pulled to the voltage of the input return (*e.g.*, zero volts) by turning on the low side switch S2 306. However, turning on the low side switch S2 306 causes current to conduct, resulting in the inductor current I_L 319 no longer being zero and resonating. For the controller 334 to provide an active partial pulse followed by active full pulses, as discussed in detail above with respect to **FIGs. 1-2**, the converter 300 should return to steady state conditions. As such, the low side switch S2 306 is controlled to turn off when the inductor current I_L 319 can return to zero.

[0046] It should be appreciated that similarly named and numbered elements in **FIG. 3A** are coupled and function as described above. However the controller 334 further includes the bootstrap control circuit 363 and OR gate 364. Further, the controller 334 may also include a terminal to receive the current sense signal ILSENSE 365. The current sense signal ILSENSE 365 is representative of the inductor current I_L 319 of the resonant tank during the on-time of the power switch S1 304 and may be a current signal or a voltage signal. When the controller 334 includes the optional load sense circuit 373 (shown in **FIG. 3C**), the controller 334 also includes a terminal to receive the capacitive voltage sense signal VC1SENSE 369 representative of the voltage at the tank capacitance 318 of the resonant tank circuit 388, and may be a current signal or a voltage signal.

[0047] As shown, the bootstrap control circuit 363 is coupled to receive the current sense signal ILSENSE 365 and the burst signal U_{BU} 343. As mentioned above, the burst signal U_{BU} 343 indicates when the controller 334 should allow switching of the high side switch S1 304 and low side switch S2 306. In response to the current sense signal ILSENSE 365 and the burst signal U_{BU} 343, the bootstrap control circuit 363 outputs the delayed burst signal U_{BU}' 366 to the switch control circuit 340, and the bootstrap signal U_{BTS} 367 to the OR gate 364.

[0048] Bootstrap control circuit 363 determines when to enable the bootstrap period of the converter 300 by turning on the low side switch S2 306. The bootstrap signal U_{BTS} 367 is representative of enabling the bootstrap function of the controller 334. In one example, the bootstrap signal U_{BTS} 367 may be a rectangular pulse waveform with varying lengths of logic high and logic low sections. A logic high of bootstrap signal U_{BTS} 367 may represent enabling bootstrap and turning on the low side switch S2 306. A logic low of bootstrap signal U_{BTS} 367 may represent disabling bootstrap. In one example, in response to the burst signal U_{BU} 343, the bootstrap control circuit 363 outputs the bootstrap signal U_{BTS} 367 to enable bootstrap and turn on the low side switch S2 306 to precharge the VCCH terminal 361 just before a burst mode interval begins. For example, the bootstrap control circuit 363 enables the bootstrap period when the burst signal U_{BU} 343 enables switching. In response to the current sense signal ILSENSE 365, the bootstrap control circuit 363 outputs the bootstrap signal U_{BTS} 367 to disable bootstrap. In one example, the bootstrap control circuit 363 disables bootstrap after N number of zero crossing detections of the inductor current I_L 319. N can be greater than or equal to one. In one example, N may be equal to two.

[0049] The bootstrap control circuit 363 also delays the switch control circuit 340 from receiving the burst signal U_{BU} 343 as the delayed burst signal U_{BU}' 366 to provide sufficient time to precharge the VCCH terminal 361. The bootstrap control circuit 363 begins the delay in response to the burst signal U_{BU} 343 initially enabling the switching of the low side switch S2

306, and the delay ends when the bootstrap function is disabled (*i.e.*, the bootstrap signal U_{BTS} 367 falls to a logic low value).

[0050] The switch control circuit 340 is shown as receiving the switching frequency signal U_{SW} 339 (representative of the switching frequency of the high side switch S1 304 and low side switch S2 306) and the delayed burst signal U_{BU}' 366, and outputs the pre-low side signal 345 and pre-high side signal 344. The switch control circuit 340 functions as described with respect to the switch control circuit 140 of **FIG. 1**, however the switch control circuit 340 utilizes the delayed burst signal U_{BU}' 366 received from the bootstrap control circuit 363, rather than the burst signal U_{BU} 143 directly, to complete the bootstrapping operation prior to beginning the switching of the high side switch S1 304 and the low side switch S2 306.

[0051] The OR gate 364 is coupled to receive the pre-low side signal 345 and the bootstrap signal U_{BTS} 367, and outputs the signal 368. The OR gate 364 passes either the pre-low side signal 345 generated by the switch control circuit 340 or the bootstrap signal U_{BTS} 367 generated by the bootstrap control circuit 363 to the drive circuit 342 to enable the switching of the low side switch S2 306. Thus, if either the bootstrap signal U_{BTS} 367 is logic high, or the pre-low side signal 345 is logic high, the output 368 of the OR gate 364 is logic high, and the low side switch S2 306 is therefore turned on.

[0052] **FIG. 3B** illustrates the bootstrap control circuit 363 including a zero crossing detection circuit 385, counter and comparator 386, latch 370, monostable multivibrator (one shot) 371, and an AND gate 372. The one shot 371 is coupled to receive the burst signal U_{BU} 343, and outputs a pulse in response to a leading edge of the burst signal U_{BU} 343. Latch 370 is coupled to receive the output of the one shot 371 at the S input. The AND gate 372 is also coupled to receive the burst signal U_{BU} 343. Zero crossing detection circuit 385 is coupled to receive the current sense signal I_{LSENSE} 365, and outputs a signal indicating that a zero crossing in the current sense signal I_{LSENSE} 365 has been detected. The output of the zero crossing detection circuit 385 is received by the counter and comparator 386. The counter and comparator 386 determines if the number of detected zero crossings in the current sense signal I_{LSENSE} 365 is greater than or equal to N. The output of the counter and comparator 386 is received by the latch 370 at the R input. The Q output of the latch 370 is the bootstrap signal U_{BTS} 367, while the Q-bar output of the latch 370 is received by the AND gate 372. The output of AND gate 372 is the delayed burst signal U_{BU}' 366. In the example, the Q-bar output of the latch 370 is a complement of the Q output of the latch 370.

[0053] In operation, the one shot 371 receives the burst signal U_{BU} 343 and outputs a pulse, which sets the latch 370. As such, the bootstrap signal U_{BTS} 367 transitions to a logic high value to enable bootstrap and turn on the low side switch S2 306. In one example, when the low

side switch S2 306 is turned on, conduction may occur and the inductor current I_L 319 begins to oscillate or resonate. Once the bootstrap signal U_{BTS} 367 transitions to a logic high value, the counter and comparator 386 is reset. The latch 370 is not reset until the counter and comparator 386 has determined that the zero crossing detection circuit 385 has found N number of zero crossings of the inductor current I_L 319 in the current sense signal I_{LSENSE} 365. Once N number of zero crossings are detected, the latch 370 is reset, the bootstrap signal U_{BTS} 367 transitions to a logic low value, and the Q-bar output of the latch 370 transitions to a logic high value, indicating that bootstrap has been disabled. If the burst signal U_{BU} 343 is still logic high, the delayed burst signal U_{BU}' 366 transitions to a logic high value for as long as both the burst signal U_{BU} 343 and the Q-bar output of the latch 370 are logic high. Thus, it is noted that when the burst signal U_{BU} 343 is a logic high value, the delayed burst signal U_{BU}' 366 is the complement of the bootstrap signal U_{BTS} 367. As such, as long as the burst signal U_{BU} 343 is a logic high value, the delayed burst signal U_{BU}' 366 transitions to a logic high value as soon as the bootstrap signal U_{BTS} 367 transitions to a logic low value. In addition, as shown in it is appreciated that the inductor current I_L 319 is still substantially zero when the delayed burst signal U_{BU}' 366 transitions to the logic high value since the output of the zero crossing detection circuit 385 signals the counter and comparator 386 as soon as the inductor current I_L 319 has crossed zero.

[0054] FIG. 3C illustrates a load sense circuit 373, which may be included in the controller 334. The load sense circuit 373 may indirectly sense if there is a load 330 at the output of the power converter 300 by monitoring the capacitive voltage sense signal $VC1SENSE$ 369 at the beginning of bootstrap and at the end of bootstrap. If the capacitive voltage sense signal $VC1SENSE$ 369 is smaller at the end of bootstrap than it was at the beginning of bootstrap, then the load sense circuit 373 determines that energy was delivered to the output (and hence a load is present).

[0055] The burst signal U_{BU} 343 and the delayed burst signal U_{BU}' 366 may be utilized to signal the beginning and end of bootstrap period since the bootstrap period begins when the burst signal U_{BU} 343 transitions to a logic high value, and the delayed burst signal U_{BU}' 366 transitions to a logic high value when bootstrap period ends. However, the bootstrap signal U_{BTS} 367 may also be used. The load sense circuit 373 includes sample and hold circuits 374 and 375, and an operational amplifier 376. Sample and hold circuits 374 and 375 are coupled to receive the capacitive voltage sense signal $VC1SENSE$ 369. As shown, sample and hold circuit 374 receives the burst signal U_{BU} 343 while sample and hold circuit 375 receives the delayed burst signal U_{BU}' 366, and each sample and hold circuit is clocked by the respective signals to sample and hold the capacitive voltage sense signal $VC1SENSE$ 369 in response to the respective

signals. Operational amplifier 376 is coupled to receive the held outputs of the sample and hold circuits 374 and 375. As shown, the operational amplifier 376 receives the output of sample and hold circuit 374 at its non-inverting input, and the output of sample and hold circuit 375 at its inverting input. The output of the operational amplifier 376 is the output of the load sense circuit 373 and is referred to as the output load sense signal VOSENSE 377. The output load sense signal VOSENSE 377 is representative of whether a load (*e.g.*, load 330) coupled to the output of the power converter 300 has been detected.

[0056] In operation, the sample and hold circuit 374 samples and holds the value of the capacitive voltage sense signal VC1SENSE 369 when the burst signal U_{BU} 343 transitions to a logic high value. Sample and hold circuit 375 samples and holds the value of the capacitive voltage sense signal VC1SENSE 369 when the delayed burst signal U_{BU}' 366 transitions to a logic high value. As such, the operational amplifier 376 may amplify the difference in the capacitive voltage sense signal VC1SENSE 369 at the beginning and at the end of the bootstrap period. The larger the difference (*i.e.*, output load sense signal VOSENSE 377), the larger the load 330 at the output of the power converter 330.

[0057] FIG. 4 illustrates a timing diagram 400 showing example waveforms for signals shown in FIGS. 3A-3C including the burst signal U_{BU} 443, delayed burst signal U_{BU}' 466, bootstrap signal U_{BTS} 467, pre-low side signal PRE_LS 445, low side drive signal U_{LS} 447, pre-high side signal PRE_HS/high side drive signal U_{HS} 444/446 (shown as one waveform since the waveforms are substantially the same with the difference of level shifting), inductor current I_L 419, half bridge voltage V_{HB} 478 at the half bridge terminal, and the voltage V_{C1} 469 at capacitance C1 318.

[0058] During steady state conditions, the inductor current I_L 419 is substantially equal to zero while the half bridge voltage V_{HB} 478 and the voltage V_{C1} 469 are substantially half the input voltage, or $V_{IN}/2$, of the power converter 300. At time t_1 452, the burst signal U_{BU} 443 transitions to a logic high value indicating that switching of the power switches is enabled. As such, bootstrapping is enabled and the bootstrap signal U_{BTS} 467 transitions to a logic high value. Since the bootstrap signal U_{BTS} 467 is logic high, the delayed burst signal U_{BU}' 466 remains logic low while the output of the OR gate is logic high and the low side drive signal U_{LS} 447 transitions to a high value such that the low side switch S2 306 is turned on. Once turned on, current conduction begins, and the inductor current I_L 419 begins to oscillate or resonate as shown. Further, the half bridge voltage V_{HB} 478 falls to substantially zero while the voltage V_{C1} 469 also begins to fall.

[0059] For the example shown, the number N is equal to two and bootstrap does not end until two zero crossings in the inductor current I_L 419 have been detected. The first zero

crossing is detected at time t_2 453, while the second zero crossing is detected at time t_3 454. At time t_3 454, bootstrapping is disabled and the bootstrap signal U_{BTS} 467 transitions to a logic low value. The inductor current I_L 419 is substantially zero and the half bridge voltage V_{HB} 478 increases to half the input voltage $V_{IN}/2$. As such, the power converter has returned to steady state conditions. However, it should be appreciated that bootstrapping could have been disabled after the first zero crossing at time t_2 453 after the magnitude of the inductor I_L 419 had reached its peak, as the inductor current I_L 419 would return to zero through the body diode of the low side switch S2 306.

[0060] At time t_3 454, the delayed burst signal U_{BU}' 466 transitions to a logic high value, enabling burst mode and allowing the switch control circuit to control switching the high side switch S1 304 and the low side switch S2 306. As mentioned above, the switch control circuit 340 enables switching of the high side switch S1 304 and the low side switch S2 306 to include a partial active pulse 480, followed by full active pulses (including, for example, pulses 455, 456, and 457). At time t_4 481, the burst signal U_{BU} 443 and the delayed burst signal U_{BU}' 466 transition to a logic low value. Switching is disabled at the end of the next full active pulse. For the example shown, the transition of the burst signal U_{BU} 443 and the delayed burst signal U_{BU}' 466 occur during pulse 456, and the switching is therefore disabled at the trailing edge of pulse 456 (time t_5 484). When exiting the burst mode, a passive partial cycle occurs after time t_5 484 due to the remaining resonant tank current inductor I_L 419 being discharged through a body diode of one of the power switches of the switching circuit in accordance with the teachings of the present invention.

[0061] When the controller 334 also utilizes a load sense circuit 373, the load 330 may be indirectly sensed using the capacitance voltage V_{C1} 469. The solid line 482 illustrates the capacitance voltage V_{C1} 469 when there is no load is present at the output of the power converter 300, while the dashed line 483 illustrates the capacitance voltage V_{C1} 469 when a load 330 is present at the output. As shown, when there is no load present at the output of the power converter 300, the capacitance voltage V_{C1} 469 returns to substantially the steady state voltage (*i.e.*, the same voltage as the capacitance voltage V_{C1} 469 at time t_1 452) at the end of bootstrapping (time t_3 454). With a load 330 is present at the output of the power converter 300, the capacitance voltage V_{C1} 469 is less than steady state voltage since energy is transferred to the load 330 output of the power converter 300. As such, the capacitance voltage V_{C1} 469 at time t_3 454 is less than the voltage capacitance voltage V_{C1} 469 at time t_1 452.

[0062] The above description of illustrated examples of the present invention, including what is described in the Abstract, are not intended to be exhaustive or to be limitation to the precise forms disclosed. While specific embodiments of, and examples for, the invention are

described herein for illustrative purposes, various equivalent modifications are possible without departing from the broader spirit and scope of the present invention. Indeed, it is appreciated that the specific example voltages, currents, frequencies, power range values, times, etc., are provided for explanation purposes and that other values may also be employed in other embodiments and examples in accordance with the teachings of the present invention.

CLAIMS

What is claimed is:

1. A controller for use in a resonant power converter, comprising:
 - a drive circuit coupled to generate first and second drive signals to control switching of first and second switches of a switching circuit coupled to a resonant tank circuit of the resonant power converter;
 - a switch control circuit coupled to control the drive circuit to control the switching of the first and second switches of the switching circuit in response to a switching frequency signal to regulate a transfer of energy from an input of the resonant power converter to an output of the resonant power converter, wherein the switch control circuit is further coupled to control the drive circuit in response to a burst signal to control a burst mode of the controller, wherein an initial active pulse of the switching circuit when entering the burst mode is an active partial pulse, and wherein a final active pulse of the switching circuit when exiting the burst mode is an active full pulse resulting in a passive partial pulse following both of the first and second switches being turned off to exit the burst mode; and
 - a frequency control circuit coupled to generate the switching frequency signal in response to a feedback signal representative of the output of the resonant power converter.
2. The controller of claim 1, further comprising an error amplifier coupled to receive the feedback signal and a reference signal, wherein the error amplifier is coupled to generate an error signal coupled to be received by the frequency control circuit in response to a comparison of the feedback signal to the reference signal.
3. The controller of claim 1, wherein a first one of the first and second switches of the switching circuit is coupled to be turned on for the active partial pulse during the initial active pulse of the switching circuit when entering the burst mode,
 - wherein said first one of the first and second switches of the switching circuit is coupled to be turned on for the final active pulse of the switching circuit when exiting the burst mode, and
 - wherein a tank current of the resonant tank circuit discharges through a body diode of a second one of the first and second switches of the switching circuit during the passive partial pulse following said both of the first and second switches being turned off to exit the burst mode.

4. The controller of claim 1, wherein a tank current of the resonant tank circuit is coupled to vary and transition between first and second tank current values during active full pulses of the switching circuit during the burst mode.

5. The controller of claim 4, wherein the tank current is zero prior to entering the burst mode, and wherein the tank current is equal to one of the first and second tank current values at an end of the initial active pulse of the switching circuit when entering the burst mode.

6. The controller of claim 5, wherein the tank current is equal to said one of the first and second tank current values at an end of the final active pulse of the switching circuit when exiting the burst mode, and wherein the tank current is equal to zero at an end of the passive partial pulse following said both of the first and second switches being turned off to exit the burst mode.

7. The controller of claim 1, further comprising a bootstrap control circuit coupled to generate a bootstrap signal and a delayed burst signal in response to the burst signal and a tank current sense signal representative of the tank current of the resonant tank circuit,

wherein the drive circuit is further coupled to control in response to the bootstrap signal a bootstrap circuit coupled to the controller and to the switching circuit, and

wherein the switch control circuit is further coupled to receive the delayed burst signal to control the drive circuit to control the burst mode of the controller in response to the delayed burst signal.

8. The controller of claim 7, wherein the switch control circuit is coupled to generate first and second intermediate drive signals, wherein the drive circuit is coupled to generate the first and second drive signals to control the switching of the first and second switches of the switching circuit in response to the first and second intermediate drive signals.

9. The controller of claim 8, further comprising an OR gate including first and second inputs, wherein the first input of the OR gate is coupled to receive a first one of the first and second intermediate drive signals from the switch control circuit, wherein the second input of the OR gate is coupled to receive the bootstrap signal from the bootstrap control circuit, wherein the OR gate includes an output coupled to a first input of the drive circuit, wherein the drive circuit includes a second input coupled to receive a second one of the first and second intermediate drive signals from the switch control circuit, wherein the drive circuit is coupled to generate the

first and second drive signals in response to the output of the OR gate and the second one of the first and second intermediate drive signals from the switch control circuit.

10. The controller of claim 7, wherein the bootstrap control circuit comprises:

a zero crossing detection circuit coupled to receive the tank current sense signal to detect zero crossings in the tank current during a bootstrap period;

a counter and comparator circuit coupled to an output of the zero crossing detection circuit to determine when the tank current has crossed zero a threshold number of times during the bootstrap period;

a one shot circuit having an input coupled to receive the burst signal;

a latch circuit coupled to the one shot circuit and the counter and comparator circuit, wherein an output of the one shot circuit is coupled to set the latch circuit in response to the burst signal, wherein an output of the counter and comparator circuit is coupled to reset the latch circuit in response to the tank current crossing zero the threshold number of times, wherein the latch has a first output coupled to output the bootstrap signal, wherein the latch has a second output that is a complement of the first output of the latch; and

an AND gate including a first input coupled to the second output of the latch, wherein the AND gate including a second input coupled to receive the burst signal, wherein the AND gate includes an output coupled to generate the delayed burst signal.

11. The controller of claim 10, wherein the tank current is coupled to resonate during the bootstrap period, wherein the tank current crossing zero said threshold number of times indicates an end of the bootstrap period.

12. The controller of claim 7, wherein the resonant tank circuit includes a tank capacitance coupled to a tank inductance, wherein the controller further comprises a load sense circuit, wherein the load sense circuit includes:

a first sample and hold circuit coupled to receive a tank capacitance voltage sense signal, wherein the first sample and hold circuit is coupled to be clocked in response to the burst signal;

a second sample and hold circuit coupled to receive the tank capacitance voltage sense signal, wherein the second sample and hold circuit is coupled to be clocked in response to the delayed burst signal; and

an operational amplifier coupled to receive an output of the first sample and hold circuit and an output of the second sample and hold circuit, wherein the operational amplifier is coupled

to output a load sense signal in response to a difference between the output of the first sample and hold circuit and the output of the second sample and hold circuit.

13. The controller of claim 7, wherein the first and second switches of the switching circuit include a low side switch coupled to a high side switch with a terminal between the low side switch and the high side switch, wherein the bootstrap circuit includes:

- a bootstrap diode coupled between first and second energy terminals of the controller;
- a first bootstrap capacitor coupled between the first energy terminal and an input return of the resonant power converter; and
- a second bootstrap capacitor coupled between the second energy terminal and the terminal of the switching circuit,

wherein, in response to the bootstrap signal, the drive circuit is further coupled to turn on the low side switch during a bootstrap period to charge the second energy terminal from the first energy terminal through the bootstrap diode.

14. The controller of claim 1, wherein the switching circuit is a half bridge switching circuit including the first and second switches coupled to the resonant tank circuit.

15. A resonant power converter, comprising:

- a half bridge switching circuit coupled to an input of the resonant power converter;
- an energy transfer element coupled to the half bridge switching circuit and an output of the resonant power converter;

- a resonant tank circuit coupled to the half bridge switching circuit, the resonant tank circuit including a tank inductance and a tank capacitance coupled to the half bridge switching circuit, wherein the tank inductance includes a magnetizing inductance a leakage inductance of the energy transfer element; and

- a controller coupled to the half bridge switching circuit, wherein the controller includes:
 - a drive circuit coupled to generate first and second drive signals to control switching of first and second switches of a half bridge switching circuit coupled to the resonant tank circuit;

- a switch control circuit coupled to control the drive circuit to control the switching of the first and second switches of the half bridge switching circuit in response to a switching frequency signal to regulate a transfer of energy from the input of the resonant power converter to the output of the resonant power converter, wherein the switch control circuit is further coupled to control the drive circuit in response to a burst signal to control a burst mode of

the controller, wherein an initial active pulse of the half bridge switching circuit when entering the burst mode is an active partial pulse, and wherein a final active pulse of the half bridge switching circuit when exiting the burst mode is an active full pulse resulting in a passive partial pulse following both of the first and second switches being turned off to exit the burst mode; and
a frequency control circuit coupled to generate the switching frequency signal in response to a feedback signal representative of the output of the resonant power converter.

16. The resonant power converter of claim 15, wherein the controller further comprises an error amplifier coupled to receive the feedback signal and a reference signal, wherein the error amplifier is coupled to generate an error signal coupled to be received by the frequency control circuit in response to a comparison of the feedback signal to the reference signal.

17. The resonant power converter of claim 15, wherein a first one of the first and second switches of the half bridge switching circuit is coupled to be turned on for the active partial pulse during the initial active pulse of the half bridge switching circuit when entering the burst mode,

wherein said first one of the first and second switches of the half bridge switching circuit is coupled to be turned on for the final active pulse of the half bridge switching circuit when exiting the burst mode, and

wherein a tank current of the resonant tank circuit discharges through a body diode of a second one of the first and second switches of the half bridge switching circuit during the passive partial pulse following said both of the first and second switches being turned off to exit the burst mode.

18. The resonant power converter of claim 15, wherein a tank current of the resonant tank circuit is coupled to vary and transition between first and second tank current values during active full pulses of the half bridge switching circuit during the burst mode.

19. The resonant power converter of claim 18, wherein the tank current is zero prior to entering the burst mode, and wherein the tank current is equal to one of the first and second tank current values at an end of the initial active pulse of the half bridge switching circuit when entering the burst mode.

20. The resonant power converter of claim 19, wherein the tank current is equal to said one of the first and second tank current values at an end of the final active pulse of the half bridge switching circuit when exiting the burst mode, and wherein the tank current is equal to

zero at an end of the passive partial pulse following said both of the first and second switches being turned off to exit the burst mode.

21. The resonant power converter of claim 15, further comprising a bootstrap circuit coupled to the controller and the half bridge switching circuit.

22. The resonant power converter of claim 21, wherein the controller further comprises a bootstrap control circuit coupled to generate a bootstrap signal and a delayed burst signal in response to the burst signal and a tank current sense signal representative of the tank current of the resonant tank circuit, wherein the drive circuit is further coupled to control the bootstrap circuit in response to the bootstrap signal, and wherein the switch control circuit is further coupled to receive the delayed burst signal to control the drive circuit to control the burst mode of the controller in response to the delayed burst signal.

23. The resonant power converter of claim 22, wherein the switch control circuit is coupled to generate first and second intermediate drive signals, wherein the drive circuit is coupled to generate the first and second drive signals to control the switching of the first and second switches of the half bridge switching circuit in response to the first and second intermediate drive signals.

24. The resonant power converter of claim 23, wherein the controller further comprises an OR gate including first and second inputs, wherein the first input of the OR gate is coupled to receive a first one of the first and second intermediate drive signals from the switch control circuit, wherein the second input of the OR gate is coupled to receive the bootstrap signal from the bootstrap control circuit, wherein the OR gate includes an output coupled to a first input of the drive circuit, wherein the drive circuit includes a second input coupled to receive a second one of the first and second intermediate drive signals from the switch control circuit, wherein the drive circuit is coupled to generate the first and second drive signals in response to the output of the OR gate and the second one of the first and second intermediate drive signals from the switch control circuit.

25. The resonant power converter of claim 22, wherein the bootstrap control circuit comprises:

a zero crossing detection circuit coupled to receive the tank current sense signal to detect zero crossings in the tank current during a bootstrap period;

a counter and comparator circuit coupled to an output of the zero crossing detection circuit to determine when the tank current has crossed zero a threshold number of times during the bootstrap period;

a one shot circuit having an input coupled to receive the burst signal;

a latch circuit coupled to the one shot circuit and the counter and comparator circuit, wherein an output of the one shot circuit is coupled to set the latch circuit in response to the burst signal, wherein an output of the counter and comparator circuit is coupled to reset the latch circuit in response to the tank current crossing zero the threshold number of times, wherein the latch has a first output coupled to output the bootstrap signal, wherein the latch has a second output that is a complement of the first output of the latch; and

an AND gate including a first input coupled to the second output of the latch, wherein the AND gate including a second input coupled to receive the burst signal, wherein the AND gate includes an output coupled to generate the delayed burst signal.

26. The resonant power converter of claim 25, wherein the tank current is coupled to resonate during the bootstrap period, wherein the tank current crossing zero said threshold number of times indicates an end of the bootstrap period.

27. The controller of claim 22, wherein the controller further comprises a load sense circuit, wherein the load sense circuit comprises:

a first sample and hold circuit coupled to receive a tank capacitance voltage sense signal, wherein the first sample and hold circuit is coupled to be clocked in response to the burst signal;

a second sample and hold circuit coupled to receive the tank capacitance voltage sense signal, wherein the second sample and hold circuit is coupled to be clocked in response to the delayed burst signal; and

an operational amplifier coupled to receive an output of the first sample and hold circuit and an output of the second sample and hold circuit, wherein the operational amplifier is coupled to output a load sense signal in response to a difference between the output of the first sample and hold circuit and the output of the second sample and hold circuit.

28. The resonant power converter of claim 22, wherein the first and second switches of the half bridge switching circuit include a low side switch coupled to a high side switch with a half bridge terminal between the low side switch and the high side switch, wherein the bootstrap circuit includes:

a bootstrap diode coupled between first and second energy terminals of the controller;

a first bootstrap capacitor coupled between the first energy terminal and an input return of the resonant power converter; and

a second bootstrap capacitor coupled between the second energy terminal and the half bridge terminal,

wherein, in response to the bootstrap signal, the drive circuit is further coupled to turn on the low side switch during a bootstrap period to charge the second energy terminal from the first energy terminal through the bootstrap diode.

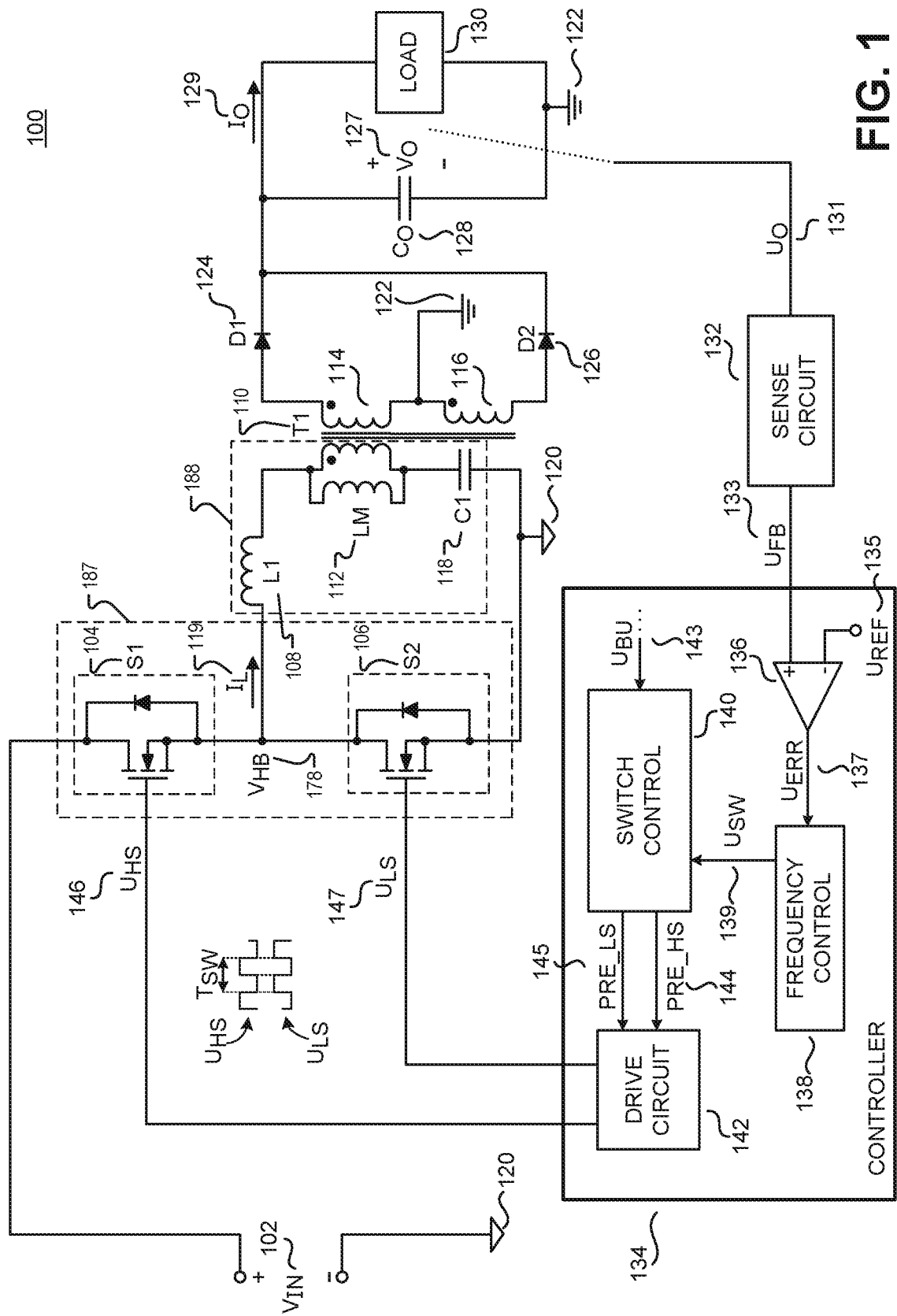


FIG. 1

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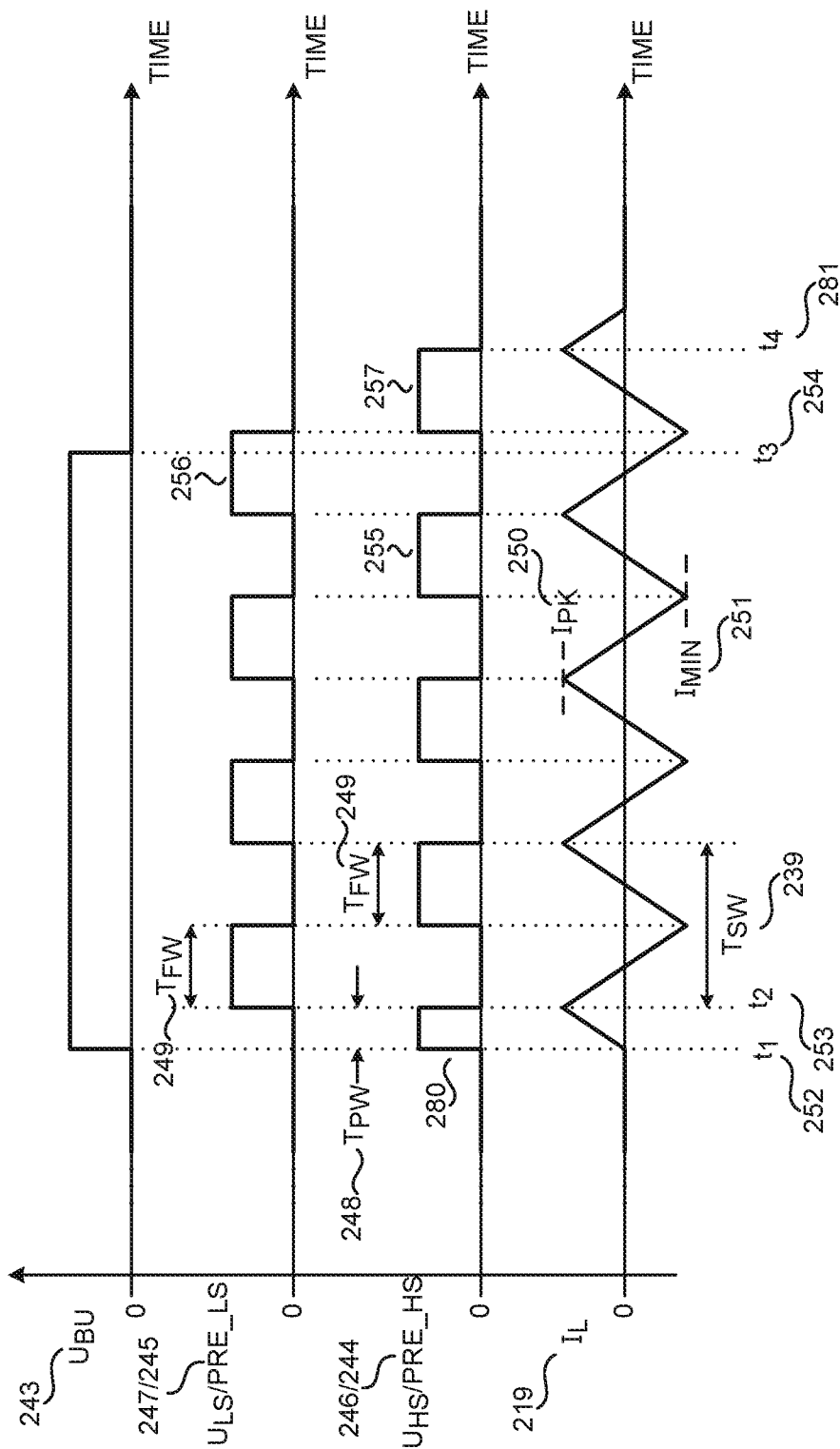


FIG. 2

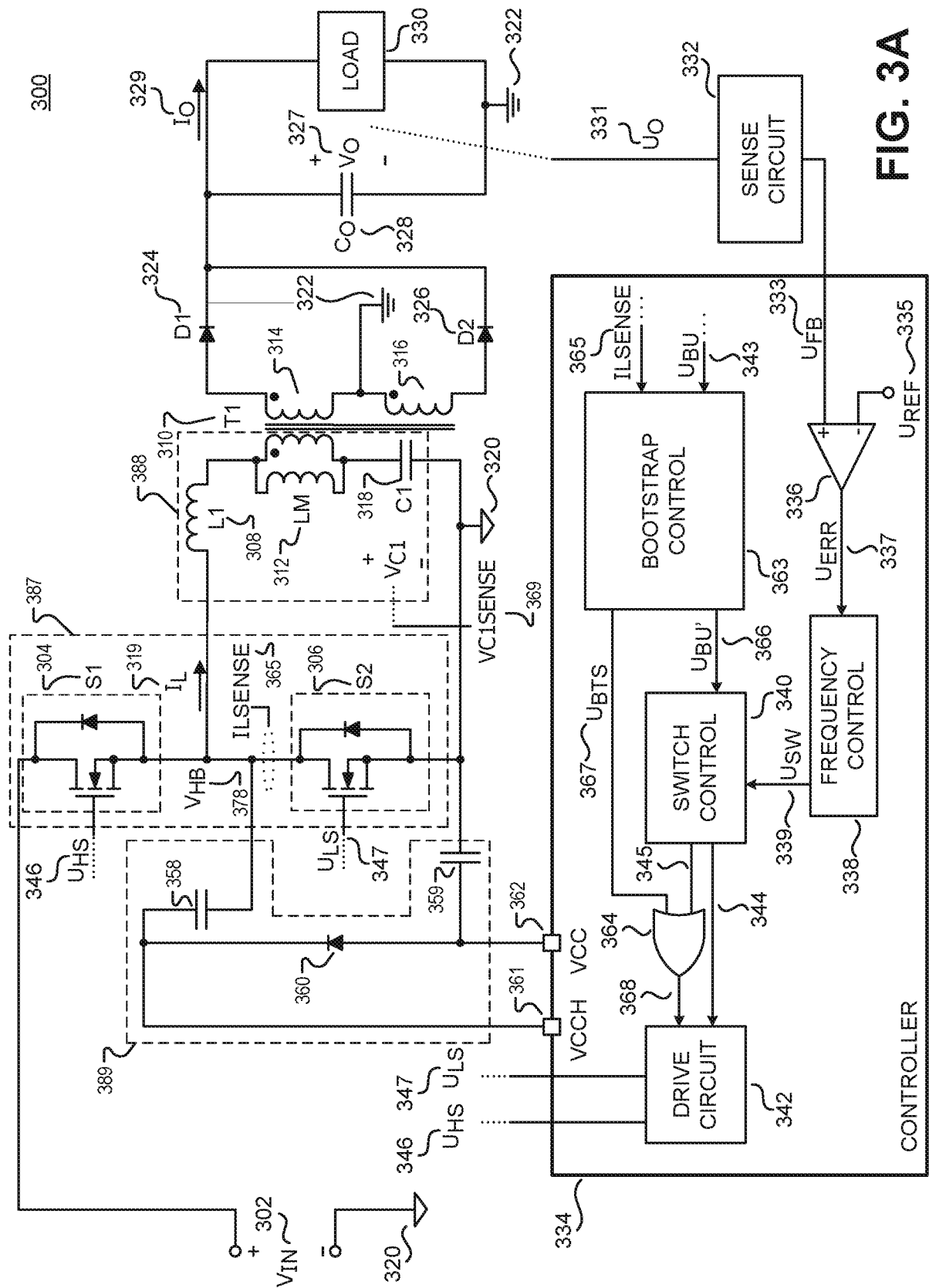


FIG. 3A

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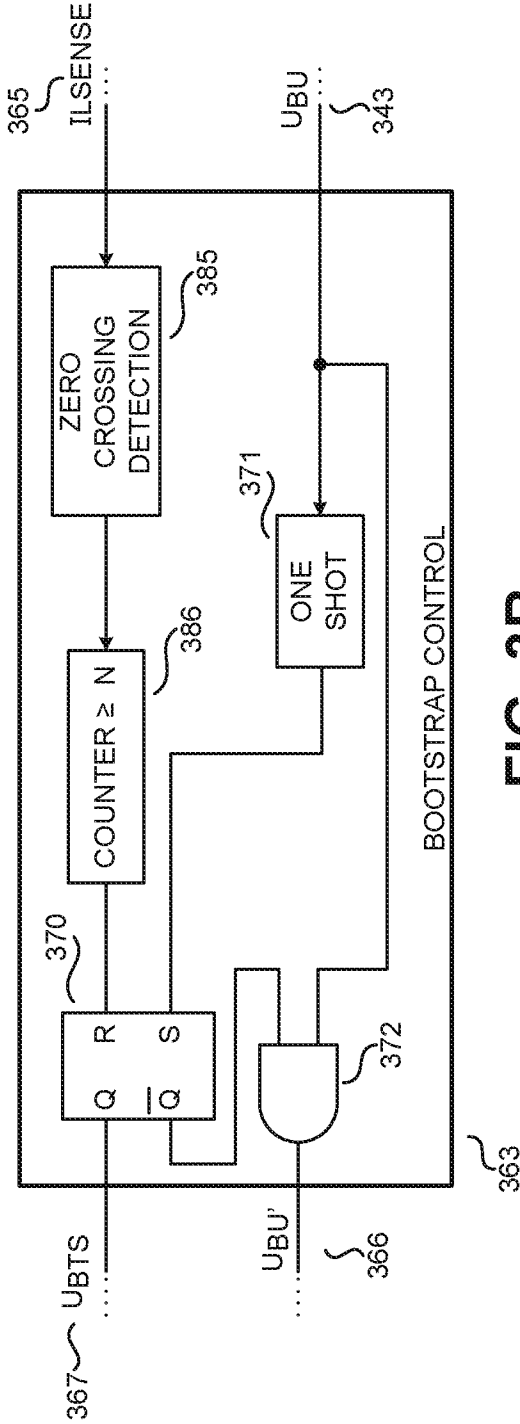


FIG. 3B

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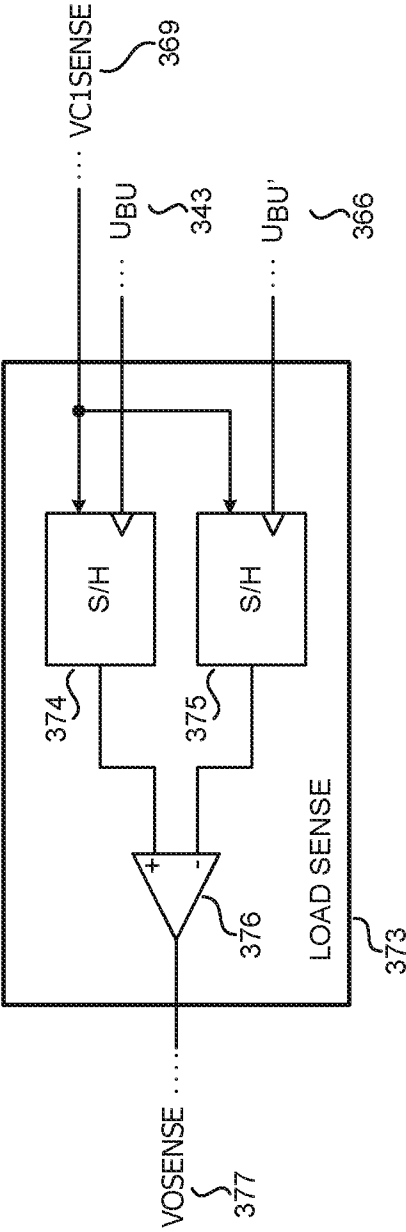


FIG. 3C

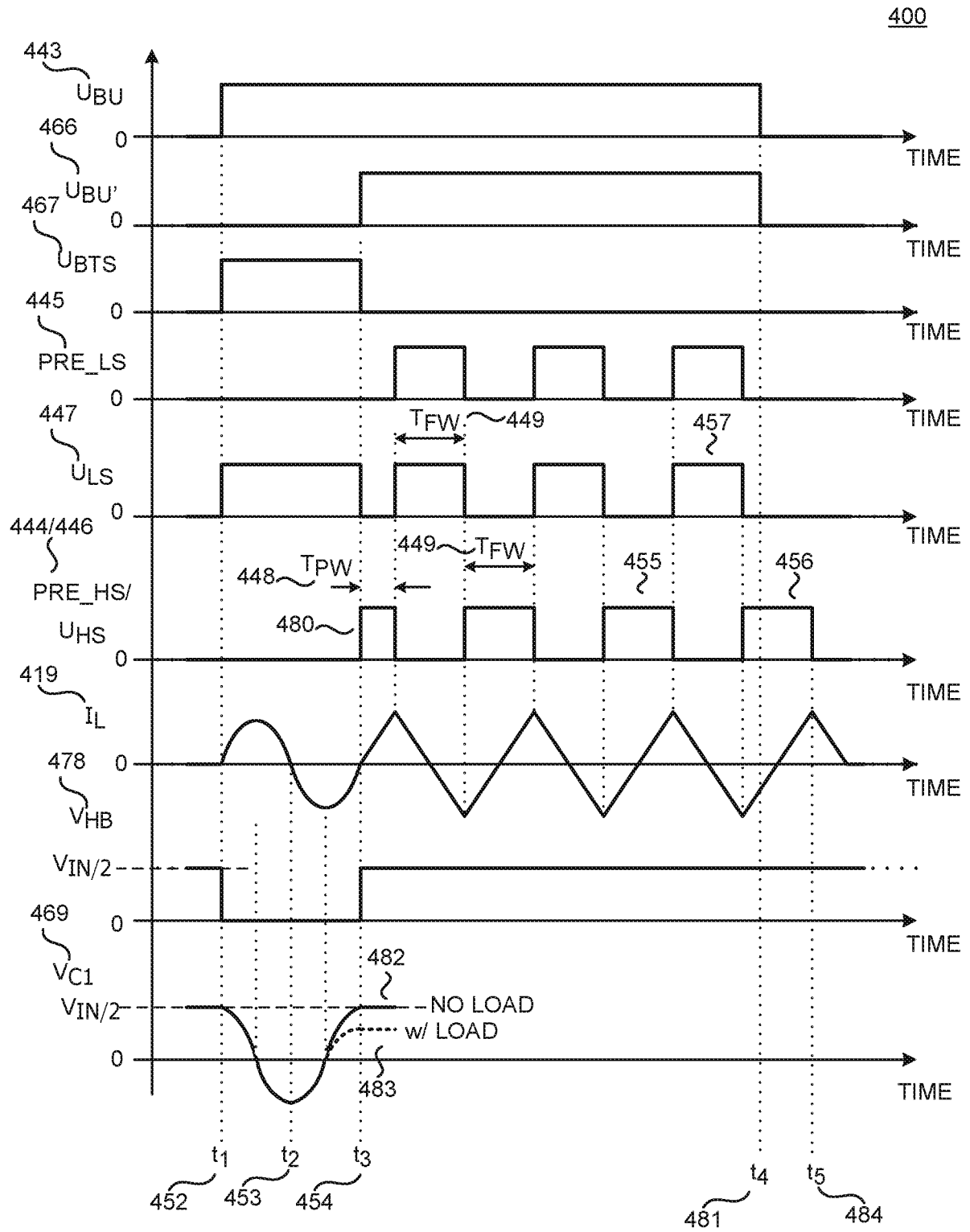


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2016/063409

A. CLASSIFICATION OF SUBJECT MATTER

INV. H02M1/00 H02M3/337 H02M1/08 H02M1/36
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2016/294297 A1 (FEI CHAO [US] ET AL) 6 October 2016 (2016-10-06) abstract paragraphs [0083], [0085], [0088]; figures 1, 3, 6, 14, 17A, 18A	1-6, 14-20 7-10, 13, 21-25, 28 11, 12, 26, 27
Y A	US 2015/263629 A1 (STULER ROMAN [CZ] ET AL) 17 September 2015 (2015-09-17) abstract paragraphs [0025], [0026]; figure 1	7-10, 13, 21-25, 28 1-6, 11, 12, 14-20, 26, 27
X A	US 2014/312789 A1 (FENG WEIYI [US] ET AL) 23 October 2014 (2014-10-23) abstract paragraphs [0047], [0048]; figures 1, 2, 6A	1, 15 2-14, 16-28

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

1 August 2017

Date of mailing of the international search report

08/08/2017

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/063409

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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			TW 201537871 A 01-10-2015
			US 2015263629 A1 17-09-2015
US 2014312789	A1	23-10-2014	NONE