

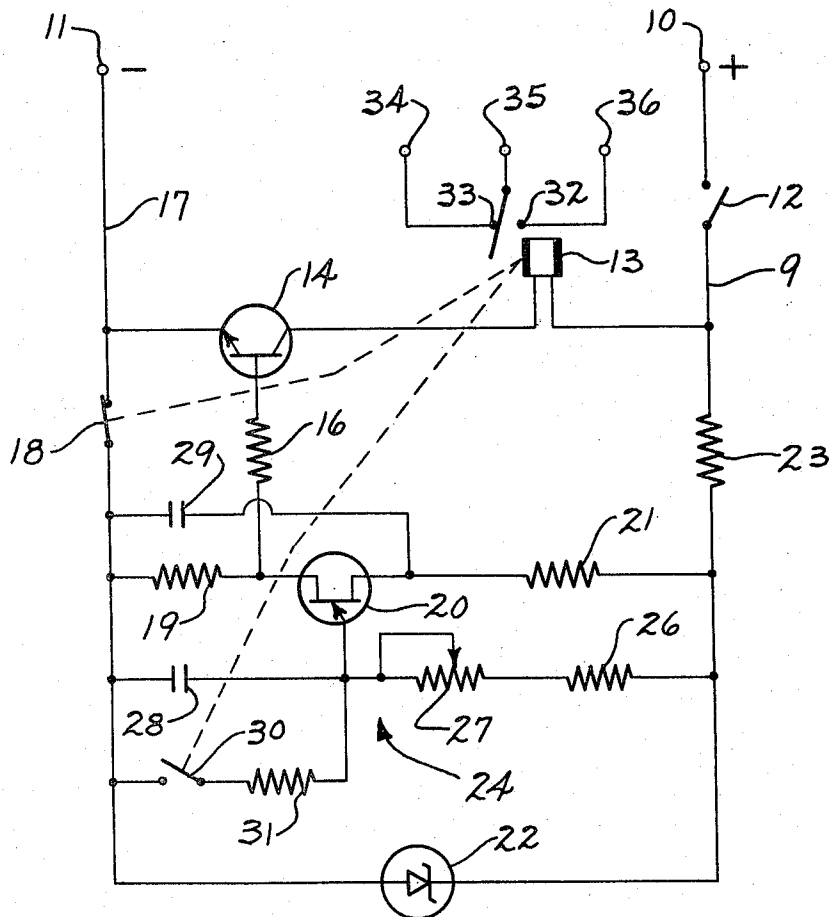
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DELAYED PULL IN TIME DELAY RELAY

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3,303,396

## DELAYED PULL IN TIME DELAY RELAY

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mesne assignments, to Master Specialties Company,  
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This invention relates in general to time delay circuits and more specifically to such circuits in which the operation of a relay is delayed for a predetermined time after a source of line voltage is applied.

A time delay circuit for energizing a relay which is comprised of solid state components has many applications in aircraft, missile and other environments which require a readily-packaged, rugged unit capable of a relatively high accuracy throughout a wide range of operating conditions. In order to keep the unit compact, it is desirable to use relatively low values of capacitance in the timing circuits and to use a relay having a small number of contacts utilized in latching circuits wherever possible. Furthermore, it is desirable to latch the energized relay as quickly as possible after it operates.

Accordingly a principal object of the present invention is to incorporate the foregoing features in a single improved delayed pull in time delay relay circuit.

Another object of the present invention is to furnish a solid state circuit for use with a relay in which a unijunction transistor is operated for predetermined time period after the line voltage is applied to the circuit in order to operate the relay. A novel latching circuit is provided which operates upon opening a normally closed contact. The novel latching circuit requires less time than a circuit where latching is accomplished by waiting until the relay wipers move from a normally open to a closed or latching position. A time constant charging capacitor in the emitter circuit of the unijunction transistor may be considerably smaller because of the novel latching circuit and the normally closed contact included in the latching circuit uses only a single contact of the relay permitting utilization of the remaining contacts for other purposes.

A further object of the present invention is to provide an inexpensive and compact time delay circuit using a unijunction transistor for initiating operation of a relay with a novel latching circuit that permits the relay to remain turned on even after the unijunction transistor turns off.

Other objects and advantages of this invention will be apparent from the following detailed description when considered in connection with the accompanying drawing which consists of a single figure of a preferred embodiment of the present invention.

Supply lines 9 and 17 are connected to a source of direct current supply voltage through input terminals 10 and 11 respectively. Using the semiconductor devices illustrated in this preferred embodiment, the terminal 10 is connected to the positive side of the voltage supply. A switch 12 in supply line 9 completes the circuit and may be manually controlled for starting the delay or may be automatically controlled. If it is desired, depending upon the application of the circuit, the switch 12 may be a fault switch which is operated by the occurrence of a monitored condition.

A relay 13 is connected between the supply lines 9 and 17 through the emitter to collector circuit of an NPN transistor 14. The transistor 14 is turned on only when a sufficient current pulse is available through a base resistor 16 after a set time delay. Supply line 17 connected to the terminal 11 includes a normally closed contact 18 connected between the emitter electrode of transistor 14

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and the lower end of a resistor 19 in the first base circuit of a unijunction transistor 20.

The unijunction transistor 20, sometimes called a double base diode, has its second base electrode connected through a compensating resistor 21 to the supply line 9. Stabilization is accomplished by regulating zener diode 22 connected from supply line 17 to the supply line 9 through a dropping resistor 23. The zener diode 22 enters its zener breakdown region and establishes a regulated voltage across a time constant charging circuit 24 connected to the emitter electrode of unijunction transistor 20. Circuit 24 includes resistors 26 and 27 as well as a capacitor 28. It may be desirable to provide an adjustable resistor 27 which may be a potentiometer to furnish a variable time delay. Further stability is gained by the addition of a capacitor 29 from the second base of the unijunction transistor 20 to the supply line 17.

In addition to controlling contact 18, the relay 13 may have a normally open contact 30 connected through a resistor 31 across a capacitor 28 in the emitter circuit of the unijunction transistor 20. The relay may conveniently be a double pole double throw type with contacts 32 and 33 connected to a load through terminals 34, 35, and 36.

In operation, when the switch 12 is closed, the voltage across the zener diode 22 is sufficient to cause it to enter its zener breakdown region and establish a constant voltage across the time constant circuit 24. The transistor 14 is biased to cut-off and the relay 13 is de-energized. The unijunction transistor 20 has a characteristic such that the emitter-to-lower or first base terminal is back biased. After a predetermined time period, the capacitor 28 charges to a peak voltage sufficient to cause holes to be injected into the emitter and the unijunction transistor 20 enters a negative resistance portion of its characteristic curve. The current through the emitter-to-first base circuit of the unijunction transistor 20 increases sharply, providing a source of current through the resistor 16 which causes the transistor 14 to turn on and energize the relay 13.

Once relay 13 is energized, there is a tendency for the relay to drop out as the supply of current for the base of the transistor 14 diminishes, particularly if the time constant capacitor 28 is relatively small and able to hold only a small charge. Therefore a latch circuit is provided which includes the normally closed contact 18. When contact 18 opens, as the wipers are removed from the closed position and over to close the normally open contact 30, the current through the zener diode 22 must now pass through resistors 19 and 16 to act as the base current supply for the transistor 14. The latching circuit is able to operate just as soon as contact 18 opens up and there is no need to wait the added time until the wipers complete their travel from a normally closed position to a normally open position.

Once the contact 30 closes, it serves to discharge most of the remaining energy of the capacitor 28 which allows the unijunction transistor 20 to turn off. The circuit is now ready to be reset which is done by simply opening switch 12.

It is understood that the load circuit connected to available terminals 34, 35 and 36 of the relay 13 is controlled upon operation of the relay 13 by the aforesaid delayed trigger circuit and it remains latched when current through normally closed contact 18 is diverted to serve as an alternate supply for the base of transistor 14.

Many modifications and variations of the present invention are possible in light of the above teachings. It is therefore understood that the invention may be practiced within the scope of the claims otherwise than as specifically herein described.

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What I claim is:

1. A time delay relay circuit, comprising, in combination, a pair of terminals for connection to a source of direct current, a first transistor having emitter, collector and base electrodes with the emitter-collector circuit connected in series with a relay across said terminals, a time delay device having an initial condition of non-conduction and including a capacitor and a unijunction transistor operably connected to said terminals to conduct a predetermined time after application of said source of direct current thereto, said time delay device operatively connected to said base of said first transistor whereby delayed conduction by said time delay device will turn on said first transistor and whereby current through the emitter-collector circuit of said first transistor will actuate said relay, a first means responsive to actuation of said relay to divert additional current from said terminals to said base of said first transistor to hold said transistor on said first means comprising a normally closed switch connected in parallel with the emitter base circuit of said

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transistor which, when opened by said relay, causes additional current to flow to said base to hold said first transistor on, and a second means responsive to actuation of said relay to return said time delay device to its initial condition.

2. The time delay circuit of claim 1 wherein said second means responsive to actuation of said relay is a normally open switch operatively connected to said time delay device, which, when closed by said relay, discharges said capacitor to return said device to its initial condition.

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