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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, California 95054 (US).

(72) Inventor: **SIPRAK, Domagoj**; Gmunder Strasse 3, Munchen, BY 81379 (DE).

(74) Agents: **WATSON, Mark** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

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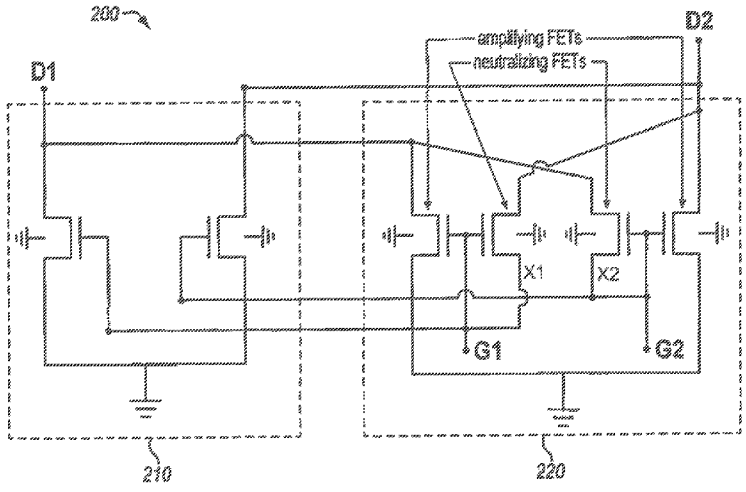
FIG. 2



(57) Abstract: An integrated circuit (IC) comprises an array of neutralized field-effect transistors (FETs), each including a non-neutralized FET pair and a non-neutralized FET pair.

NEUTRALIZED BUTTERFLY FIELD-EFFECT TRANSISTOR

FIELD

The present disclosure generally relates to millimeter wave field-effect transistors (FETs).

BACKGROUND

Millimeter-wave circuits having antenna beamforming arrays may be designed for a range of applications in the microwave electromagnetic spectrum. Millimeter-wave microstrip patch antennas and end-fire antennas are designed to operate in the electromagnetic spectrum ranging from 30 GHz to 300 GHz, corresponding to wavelengths ranging from 10 mm to 1 mm. Applications for these circuits include personal area networking (PAN), broadband wireless networking and communication, wireless portable devices, wireless computers, servers, workstations, laptops, ultra-laptops, handheld computers, telephones, cellular telephones, pagers, walkie-talkies, routers, switches, bridges, hubs, gateways, wireless access points (WAP), personal digital assistants (PDA), televisions, motion picture experts group audio layer 3 devices (MP3 player), global positioning system (GPS) devices, electronic wallets, optical character recognition (OCR) scanners, medical devices (e.g., cancer diagnostics), cameras, security screening (e.g., people screening at airports and security areas like hotels, conference rooms, sport stadiums, etc.), radar for range and velocity detection in cars (e.g., self autonomous driving cars) or for gesture sensing radar-sensors (e.g., replacing the keyboard device for tactile internet experience) and so forth.

Such millimeter-wave applications implement a neutralized differential pair field-effect transistor (FET) configuration to achieve a high gain and stability. Conventional neutralization methods wire a pair of FETs (e.g., FET1 & FET2) that are sized to their total channel width W1 (e.g., according to a required RF power) with properly sized neutralization capacitors (Cn1 & Cn2). The neutralization capacitor can be a metal capacitor, a MOS capacitor, a pn-junction diode or any other type of capacitor.

A problem occurs, however, if neutralization capacitors Cn are used that are not based on a drain to gate capacitance of FETs 1 and 2 process mismatch, or process variations degrade the possible performance of the device significantly or lead to unstable behavior. In addition, usage of large sized FETs 1 and 2 causes the design to

be sensitive to wiring parasitic between the FETs, the neutralization capacitors Cn and the ground wiring. This approach typically suffers from a requirement of having to implement very accurate models for the FET capacitances and the neutralization capacitances, which often fails and requires long design iterations.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic of one embodiment of a neutralized FET configuration.

Figure 2 illustrates one embodiment of a neutralized FET configuration.

Figures 3A & 3B illustrate embodiments of an integrated circuit (IC) having a neutralized FET array, with **Figures 3C & 3D** showing embodiments of a butterfly structure.

Figures 4A – 4C illustrate embodiments of a butterfly waveguide structure at the neutralized FET array IC.

Figure 5A – 5E illustrate another embodiment of a butterfly waveguide structure.

Figure 6A – 6G illustrate embodiments of an IC having neutralized and non-neutralized FET pairs.

Figure 7 illustrates a system in which the neutralized FET array IC may be implemented.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth in order to provide a thorough understanding of various embodiments. However, various embodiments of the invention may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to obscure the particular embodiments of the invention.

Figure 1 illustrates a schematic of one embodiment of a neutralized FET, or cross-coupled pair, configuration 100. In one embodiment, configuration 100 includes a pair of FET transistors (FET1 and FET2), and a Miller-Capacitance (Cgd) that is neutralized by a 180° phase shifted signal coupled via a neutralization capacitance (Cn). In such an embodiment, the gain is enhanced by eliminating the Miller effect, while stability is achieved by partially eliminating or modifying the feedback from drain to gate. The Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. In one embodiment,

the selection of Cn significantly impacts the stability and gain of the transistors and often leads to failure of the device (e.g., it shows insufficient gain or instable behavior).

As discussed above, conventional neutralization methods wire FET1 and FET2 with neutralization capacitors Cn1 & Cn2, resulting in various problems. According to one embodiment, a neutralized FET configuration is provided that features a compact layout (e.g., area < 3.8 um^2) that achieves neutralization through parallel connection of non-neutralized FET pair and a one-to-one (1:1) matched neutralized FET pair. In such an embodiment, the neutralization is discretely realized by combining or cascading different amounts of non-neutralized FET pairs with fully 1:1 matched neutralized FET pairs.

Figure 2 illustrates one embodiment of a neutralized FET configuration 200. As shown in **Figure 2**, configuration 200 includes non-neutralized FET pair 210 and neutralized FET pair 220. In one embodiment, total channel width is achieved by the parallel connection of the mini-circuits 210 and 220. In such an embodiment the influence of parasitic wiring between FETs and neutralization caps Cn and in a differential ground (Gnd) is very small due to the small channel width of the FETs used in the individual non-neutralized FET pair 210 and the fully 1:1 matched neutralized FET pairs 220. Thus, the neutralization is achieved within a larger, distributed array of non-neutralized and neutralized FET pairs compared to the lumped neutralization described above. Accordingly, configuration 200 is implemented in an array to provide for discrete distributed neutralization.

In one embodiment, the gate terminals of non-neutralized FET pair 210 and neutralized FET pairs 220 are contacted from both sides (e.g., via G1 and G2), leading to improved gain. Additionally, the drains are connected to two drain terminals (e.g., at D1 and D2). Thus, configuration 200 includes inductance cancellation through antiparallel running alternating currents (ac) in both the gate and drain wiring, which avoids distributed effects to reduce the gain in larger arrays. Inductance cancellation will be described in more detail below with reference to **Figures 6**. In a further embodiment, configuration 200 features a small differential source impedance, resulting from the compact layout (e.g., a small area (e.g., < 3,8 um^2), in order to avoid gain degradation via source degeneration. In yet a further embodiment, a reduced number of drain contacts reduces drain to gate and drain to source capacitance to lower the drain output capacitance.

In one embodiment, the X1 and X2 nodes at the source of the neutralizing FETs are connected to gate G1 and G2, respectively. This results in a compact layout. In another embodiment, the X1 and X2 nodes are each connected by a high ohmic resistor to the ground of the neutralized FET. The high ohmic resistor may be selected from a value between 1 kOhm and 25 kOhm. This emobodiment may have a higher gain but a less compact layout, which can lower the gain due to distributed effects in larger arrays.

Figures 3A & 3B illustrate embodiments of an integrated circuit (IC) 300 having a neutralized FET array. In one embodiment, IC 300 includes the an array of neutralized FETs 310, having a configuration of FET 200, wired to the rest of the circuit (e.g., G1, G2, D1 and D2) via waveguide structures 320. In such an embodiment, waveguide structures 320 include a butterfly configuration (or shape) coupled/routed at a 45° angle. In a further embodiment, IC 300 includes six metal layers (M1 – M6), with the first layer (M1) being a differential radio frequency (RF) ground shield. As shown in **Figure 3A**, array 310 is coupled to G2 and D1 via waveguides 320 in layers M4 and M5, and G1 and D2 via waveguides 320 in layer M6. This configuration enables the crossover of waveguides 320 for coupling at the gates and drains. **Figure 3B** shows a more detailed view of the waveguide crossovers at IC 300.

In another embodiment, G2 and D1 may be coupled to array 310 in a single metal level. In this embodiment, the width of the lines for the part of the butterfly structure for the gates G1 and G2 may be different from the width of the lines forming the part of the butterfly structure for the drains D1 and D2. In addition different types of 45° lines may be used.. **Figure 3C** discloses one embodiment in which the line type may have a smaller width in a section routed at a 45° angle compared to end sections routed at a 0° angle. **Figure 3D** discloses another embodiment, the line type may have the same width in the section routed at the 45° angle and the end sections routed at the 0° angle.

According to one embodiment, sails may be provided to waveguides 320 in areas outside of the crossover areas to improve the phase balance, matching of capacitive loading and wave impedance. **Figure 4A** illustrates one embodiment of IC 300 having sails at layer M6 and layers M4 and M5. **Figure 4B** illustrates an embodiment of a more detailed view of sails at waveguides 320 in layers M4 and M5 of IC 300, while **Figure 4C** illustrates an embodiment of a more detailed view of sails

at waveguides 320 in layer M6.

In another embodiment, G1 and G2 ports, as well as D1 and D2 ports, may be equalized by alternating the butterfly waveguide 320 structure with alternating/interleaved lines in M6 and M4 connected parallel with M5 comprising loading and de-loading nodes. **Figure 5A** illustrates one embodiment of an alternating line butterfly waveguide configuration for D1 and D2. As shown in **Figure 5A**, loading nodes (e.g., L1 and L2) and de-loading nodes (e.g., D2) are implemented. According to one embodiment, L1 represents a capacitance-loading node for drain 1 and L2 represents a capacitance-loading node for drain 2. Similarly, D2 represents a capacitance de-loading node for drain 2. In such an embodiment, the loading nodes feature under-crossing, while the de-loading nodes feature over-crossing. In a further embodiment, an arrangement of the loading and de-loading nodes may provide that the sum of loading and de-loading nodes is equal for each of D1 and D2 to achieve a balanced capacitive loading for each of D1 ad D2.

Figure 5B illustrates one embodiment of the alternating butterfly waveguide 320 layout at IC 300. As shown in **Figure 5B**, nodes 520 are included within the waveguide structure 320. **Figures 5C & 5D** illustrate more detailed views of IC 300. **Figure 5C** shows a loading under-crossing in which vias 522 and 524 are placed under a node 520 in order to form an under-crossing node 526. Conversely, **Figure 5D** illustrates a de-loading over-crossing in which a via 524 is placed over a node 520. **Figure 5E** illustrates one embodiment of a compact form of an alternating line butterfly waveguide 320 structure. Such a compact geometry/form may also be used for the embodiment shown in **Figures 3A & 3B** with a butterfly waveguide structure having no alternating/interleaved lines comprising loading and de-loading nodes. This compact form/geometry is better suited for connecting transformers while the non compact form (e.g., shown in **Figures 3A & 3B**) better suits the connection to transmission lines.

According to one embodiment, neutralized FET configuration 200 may feature various design factors of neutralization (e.g., under- neutralization ($Cn < Cgd$) or over-neutralization ($Cn > Cgd$)) that result in the highest stable gain. In such an embodiment, FET pair cells of differently neutralized and non-neutralized FETs may be cascaded to achieve such a result. **Figure 6A** illustrates one embodiment of a fully 1:1 matched neutralized differential FET pair 220 implemented at/thru layers gate metal (see layout in **Figure 6A**), M1, M2 and M3 of IC 300. In this embodiment, G1

is implemented/contacted in/via layer M3 and M2 and G2 in/via layer M3 and M2. In such an embodiment, the gate of both amplifying FETs of the neutralized FET pair is connected from both sides via M3 (one side) and M2 + M1 bridge (other side). The source of the amplifying FETs is connected to the differential RF Gnd 610 in layer M1. Additionally, this configuration includes a reduced number of contacts 620 for the drain of the amplifying FET and the source of the neutralizing FET. **Figure 6B** illustrates one embodiment of a non-neutralized differential FET pair 210 implemented at layers M1 (e.g., an M1 bridge 650 is used to connect gate from both sides 640 and 645), M2 and M3 of IC 300, also including a reduced number of drain contacts 620.

According to one embodiment, neutralized differential FET pair 220 may be configured to become over-neutralized by adding inter-metal capacitors. In an over-neutralized configuration Cn > Cgd. **Figure 6C** illustrates one embodiment of an over-neutralized differential FET pair 220 having inter-metal finger capacitors constructed at G1 (layer M4) to D2 (layers M5/M4) and G2 (layer M4) to D1 (layers M5/M4). **Figure 6D** illustrates one embodiment of an over-neutralized differential FET pair 220 having intra-metal plate capacitors also constructed at G1 (layer M4) to D2 (layers M5) and G2 (layer M4) to D1 (layers M5). Capacitors may also be included in non-neutralized differential FET pair 210 for realizing an under-neutralized or over-neutralized FET.

In an under-neutralized configuration Cn < Cgd. **Figure 6E** illustrates one embodiment of an under-neutralized or over-neutralized differential FET pair 210 having inter-metal finger capacitors constructed at G1 (layer M4) to D2 (layers M5/M4) and G2 (layer M4) to D1 (layers M5/M4).

In one embodiment, inductance cancellation/reduction occurs through antiparallel running currents. As shown in **Figure 6D**, induction is reduced (or cancelled) by a negative mutual inductance between currents running in opposite directions through G1 and G2. In a further embodiment, differential RF ground shield 610 in layer M1 forms a loop, which performs as a transformer with respect to the gate and drain lines running above. This reduces the inductance of the gate and drain line due to the transformer action between the gate and drain lines and the ground shield loop.

In one embodiment, cascading multiple neutralized butterfly FETs, as shown in **Figure 3A**, provides a butterfly phase balancing feature. Such cascading may be

necessary at high millimeter wave frequencies if the gain of one butterfly FET is not sufficient for the application. Butterfly FETs of different or same total width are cascaded using interstage matching networks for impedance matching reasons. Cascading multiple neutralized butterfly FETs, such as in **Figure 3A**, provides the feature of phase (or signal run time) equalization (e.g., improving the phase balance or reducing the FOM phase imbalance between the signals from gate1 to drain 1 and gate 2 to drain 2) between gate1 to drain 1 and gate 2 to drain 2 due to the fact that drain1 of first butterfly FET in first metal level connects to gate1 of second butterfly FET in second metal level and drain 2 of first butterfly FET in second metal level connects to gate 2 of second butterfly FET in first metal level with all wiring metals running over a RF ground shield which forms with wires a waveguide structure (**See Figure 6F**).

A further embodiment may implement cascading of two butterfly FETs. In this embodiment, the second butterfly FET is flipped 180° around the x-axis (e.g., axis of single propagation (**See Figure 6G**). Thus, the signal entering at G1 as well as the signal entering at G2 traverse four different wires of the butterfly till they extit at D2 and D1 respectively. This equalizes the phase of signal G1 to D2 and signal G2 to D1. In addition when cascading an even number of butterfly FETs drain current is taken always on opposite sides (e.g., if the first Butterfly FET drains current from upper drain1, then the second Butterfly FET will drain current from the lower drain2). This balances and reduces the current induced IR drops (e.g., equals resistive+inductive voltage drops due to changing currents during signal amplification) from two power supply lines to the upper and lower drain terminals.

The above-described FET configuration provides wiring access to a neutralized FET array, and improves the gain of the neutralized transistor by augmenting the FET MOS capacitors having a low quality factor with metal based capacitors with higher quality factor from a butterfly waveguide structure.

Figure 7 illustrates one embodiment of a block diagram of a system 700 in which a millimeter wave IC (e.g., IC 300) may be implemented. System 700 may comprise, for example, a communication system having multiple nodes. A node may comprise any physical or logical entity having a unique address in system 700. Examples of a node may include, but are not necessarily limited to, a computer, server, workstation, laptop, ultra-laptop, handheld computer, telephone, cellular telephone, personal digital assistant (PDA), router, switch, bridge, hub, gateway,

wireless access point (WAP), and so forth. The unique address may comprise, for example, a network address such as an Internet Protocol (IP) address, a device address such as a Media Access Control (MAC) address, and so forth. The embodiments are not limited in this context.

The nodes of system 700 may be arranged to communicate different types of information, such as media information and control information. Media information may refer to any data representing content meant for a user, such as voice information, video information, audio information, text information, alphanumeric symbols, graphics, images, and so forth. Control information may refer to any data representing commands, instructions or control words meant for an automated system. For example, control information may be used to route media information through a system, or instruct a node to process the media information in a predetermined manner.

The nodes of system 700 may communicate media and control information in accordance with one or more protocols. A protocol may comprise a set of predefined rules or instructions to control how the nodes communicate information between each other. The protocol may be defined by one or more protocol standards as promulgated by a standards organization, such as the Internet Engineering Task Force (IETF), International Telecommunications Union (ITU), the Institute of Electrical and Electronics Engineers (IEEE), and so forth.

The integrated circuits, neutralized FETs, systems, and methods described herein are beneficial in devices, circuits and systems compliant with millimeter wave based wireless communication and connectivity standards such as: 5^{th} generation wireless systems (5G); 802.11ad, WiGig; next-generation 60 GHz connectivity; IEEE 802.11ay (WiGig 2); millimeter wave sensors such as millimeter wave based radar and imaging.

System 700 may be implemented as a wireless communication system and may include one or more wireless nodes arranged to communicate information over one or more types of wireless communication media. An example of a wireless communication media may include portions of a wireless spectrum, such as the radio-frequency (RF) spectrum or frequency spectrum in the millimeter wave range (30-300 GHz). The wireless nodes may include components and interfaces suitable for communicating information signals over the designated wireless spectrum, such as one or more antennas, wireless transmitters/receivers ("transceivers"), amplifiers,

filters, control logic, and so forth. Examples for the antenna may include an internal antenna, an omni-directional antenna, a monopole antenna, a dipole antenna, an end fed antenna, a circularly polarized antenna, a micro-strip antenna, a micro-strip patch antenna, end-fire antenna, a diversity antenna, a dual antenna, an antenna array for beamforming reasons or electronic beam steering functionality, and so forth.

Referring again to **Figure 7**, system 700 may comprise node 702, 704, and 706 to form a wireless communication network, such as, a PAN, for example. Although **Figure 7** is shown with a limited number of nodes in a certain topology, it may be appreciated that system 700 may include more or less nodes in any type of topology as desired for a given implementation. The embodiments are not limited in this context.

In one embodiment, system 700 may comprise node 702, 704, and 706 each may comprise a transceiver 708, 710, and 712, respectively, and a CMOS integrated circuit device 750. The CMOS integrated circuit device 750 may comprise any one of antenna systems 100, 400, 500, and 600 to form a wireless communication network through wireless links 752, 754, 756, for example.

References to "one embodiment", "an embodiment", "example embodiment", "various embodiments", etc., indicate that the embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term "coupled" along with its derivatives, may be used. "Coupled" is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

As used in the claims, unless otherwise specified the use of the ordinal adjectives "first", "second", "third", etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

The following clauses and/or examples pertain to further embodiments or examples. Specifics in the examples may be used anywhere in one or more embodiments. The various features of the different embodiments or examples may be

variously combined with some features included and others excluded to suit a variety of different applications. Examples may include subject matter such as a method, means for performing acts of the method, at least one machine-readable medium including instructions that, when performed by a machine cause the machine to performs acts of the method, or of an apparatus or system for facilitating hybrid communication according to embodiments and examples described herein.

Some embodiments pertain to Example 1 that includes an integrated circuit (IC) comprising an array of neutralized field-effect transistors (FETs), each including a non-neutralized FET pair and a neutralized FET pair.

Example 2 includes the subject matter of Example 1, wherein the neutralization FET pair comprises a fully one-to-one (1:1) matched neutralized FET pair.

Example 3 includes the subject matter of Examples 1 and 2, wherein the neutralization is realized by combining or cascading different amounts of non-neutralized FET pairs with the fully 1:1 matched neutralized FET pairs.

Example 4 includes the subject matter of Examples 1-3, wherein the total channel width of each neutralized FET is achieved by the parallel connection of the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair.

Example 5 includes the subject matter of Examples 1-4, wherein the neutralized FET comprises drain wiring wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first drain terminal and a second drain terminal of the IC.

Example 6 includes the subject matter of Examples 1-5, wherein the neutralized FET comprises gate wiring wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first gate terminal and a second gate terminal.

Example 7 includes the subject matter of Examples 1-6, wherein the neutralized FET is configured to cancel inductance in both the gate and drain wiring.

Example 8 includes the subject matter of Examples 1-7, further comprising a plurality of waveguide structures to couple the array of neutralized FETs to the first and second drain terminals and the first and second gate terminals.

Example 9 includes the subject matter of Examples 1-8, wherein the waveguide structures have a butterfly configuration.

Example 10 includes the subject matter of Examples 1-9, wherein the waveguide structures are routed at a 45° angle.

Example 11 includes the subject matter of Examples 1-10, wherein the first gate terminal and the second drain terminal are located at a first layer of the IC, and the second gate terminal and the first drain terminal are located at second and third layers of the IC.

Example 12 includes the subject matter of Examples 1-11, wherein waveguide structures coupling the array of neutralized FETs to the first gate terminal and the second drain terminal cross over the waveguide structures coupling the array of neutralized FETs to the second gate terminal and the first drain terminal.

Example 13 includes the subject matter of Examples 1-12, further comprising one or more sails provided to the waveguide structures outside of the crossover areas.

Example 14 includes the subject matter of Examples 1-13, further comprising interleaved/alternating lines including loading nodes and de-loading nodes coupled to alternate the waveguide structures.

Example 15 includes the subject matter of Examples 1-14, wherein the loading nodes comprise an under-crossing and the de-loading nodes comprise an over-crossing.

Example 16 includes the subject matter of Examples 1-15, wherein the IC comprises one or more capacitors coupled to the fully 1:1 matched neutralized FET pairs to provide over- neutralized configuration.

Example 17 includes the subject matter of Examples 1-16, wherein the one or more capacitors comprise inter-metal finger capacitors.

Example 18 includes the subject matter of Examples 1-17, wherein the one or more capacitors comprise intra-metal plate capacitors.

Example 19 includes the subject matter of Examples 1-18, wherein the IC comprises one or more capacitors coupled to the non-neutralized FET pairs to provide one of an over-neutralized and an under- neutralized configuration.

Example 20 includes the subject matter of Examples 1-19, wherein an even number of neutralization FET pairs are cascaded to provide phase equalization and balancing of IR drops in supply lines.

Some embodiments pertain to Example 21 that includes a neutralized field-effect transistor (FET) comprising a non-neutralized FET pair and a fully one-to-one (1:1) matched neutralized FET pair.

Example 22 includes the subject matter of Example 21, wherein total channel width of the neutralized FET is achieved by the parallel connection of the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair.

Example 23 includes the subject matter of Examples 1 and 22, further comprising drain wiring, wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first drain terminal and a second drain terminal of the IC.

Example 24 includes the subject matter of Examples 1-23, further comprising gate wiring, wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first gate terminal and a second gate terminal.

Example 25 includes the subject matter of Examples 1-24, wherein the neutralized FET is configured to cancel inductance in both the gate and drain wiring.

Some embodiments pertain to Example 26 that includes a millimeter-wave microstrip antenna comprising an integrated circuit (IC), including an array of neutralized field-effect transistors (FETs), each including a non-neutralized FET pair and a neutralized FET pair.

Example 27 includes the subject matter of Example 21, wherein the neutralization FET pair comprises a fully one-to-one (1:1) matched neutralized FET pair.

Although embodiments of the invention have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

CLAIMS

What is claimed is:

1. An integrated circuit (IC) comprising:

an array of neutralized field-effect transistors (FETs), each including:

a non-neutralized FET pair; and

a neutralized FET pair.

2. The IC of claim 1, wherein the neutralization FET pair comprises a fully one-to-one (1:1) matched neutralized FET pair.

3. The IC of claim 2, wherein the neutralization is realized by cascading different amounts of non-neutralized FET pairs with the fully 1:1 matched neutralized FET pairs.

4. The IC of claim 2, wherein the total channel width of each neutralized FET is achieved by the parallel connection of the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair.

5. The IC of claim 4, wherein the neutralized FET comprises drain wiring wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first drain terminal and a second drain terminal of the IC.

6. The IC of claim 5, wherein the neutralized FET comprises gate wiring, wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first gate terminal and a second gate terminal.

7. The IC of claim 6, wherein the neutralized FET is configured to cancel inductance in both the gate and drain wiring.

8. The IC of claim 6, further comprising a plurality of waveguide structures to couple the array of neutralized FETs to the first and second drain terminals and the first and second gate terminals.

9. The IC of claim 8, wherein the waveguide structures have a butterfly configuration.

10. The IC of claim 9, wherein the waveguide structures are routed at a 45° angle.

11. The IC of claim 8, wherein the first gate terminal and the second drain terminal are located at a first layer of the IC, and the second gate terminal and the first drain terminal are located at second and third layers of the IC.

12. The IC of claim 11, wherein waveguide structures coupling the array of neutralized FETs to the first gate terminal and the second drain terminal cross over the waveguide structures coupling the array of neutralized FETs to the second gate terminal and the first drain terminal.

13. The IC of claim 12, further comprising one or more sails provided to the waveguide structures outside of the crossover areas.

14. The IC of claim 12, further comprising interleaved/alternating lines including loading nodes and de-loading nodes coupled to alternate the waveguide structures.

15. The IC of claim 14, wherein the loading nodes comprise an under-crossing and the de-loading nodes comprise an over-crossing.

16. The IC of claim 4, wherein the IC comprises one or more capacitors coupled to the fully 1:1 matched neutralized FET pairs to provide over- neutralized configuration.

17. The IC of claim 16, wherein the one or more capacitors comprise inter-metal finger capacitors.

18. The IC of claim 16, wherein the one or more capacitors comprise intra-metal plate capacitors.

19. The IC of claim 4, wherein the IC comprises one or more capacitors coupled to the non-neutralized FET pairs to provide one of an over-neutralized and an under-neutralized configuration.

20. The IC of claim 2, wherein an even number of neutralization FET pairs are cascaded to provide phase equalization and balancing of current-resistance drops in supply lines.

21. A neutralized field-effect transistor (FET) comprising:

a non-neutralized FET pair; and

a fully one-to-one (1:1) matched neutralized FET pair.

22. The neutralized FET of claim 21, wherein total channel width of the neutralized FET is achieved by the parallel connection of the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair.

23. The neutralized FET of claim 21, further comprising drain wiring, wherein the non-neutralized FET pair and the fully 1:1 matched neutralized FET pair are each coupled to a first drain terminal and a second drain terminal of the IC.

24. A millimeter-wave microstrip antenna comprising an integrated circuit (IC), including:

an array of neutralized field-effect transistors (FETs), each including:

a non-neutralized FET pair; and

a neutralized FET pair.

25. The antenna of claim 24, wherein the neutralization FET pair comprises a fully one-to-one (1:1) matched neutralized FET pair.

FIG. 1

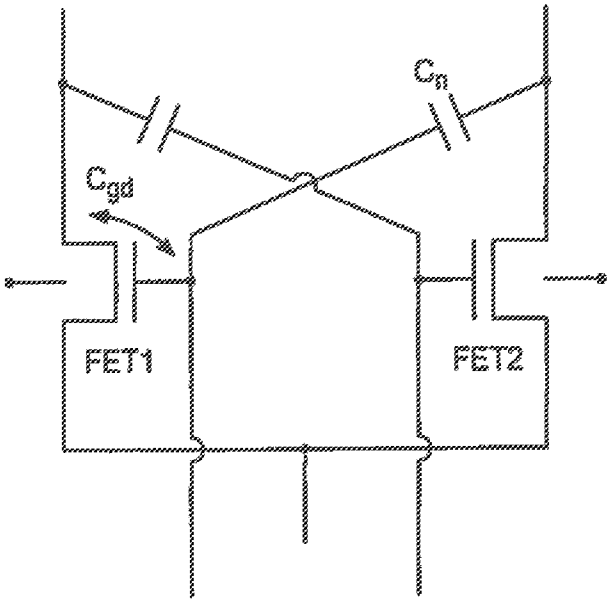
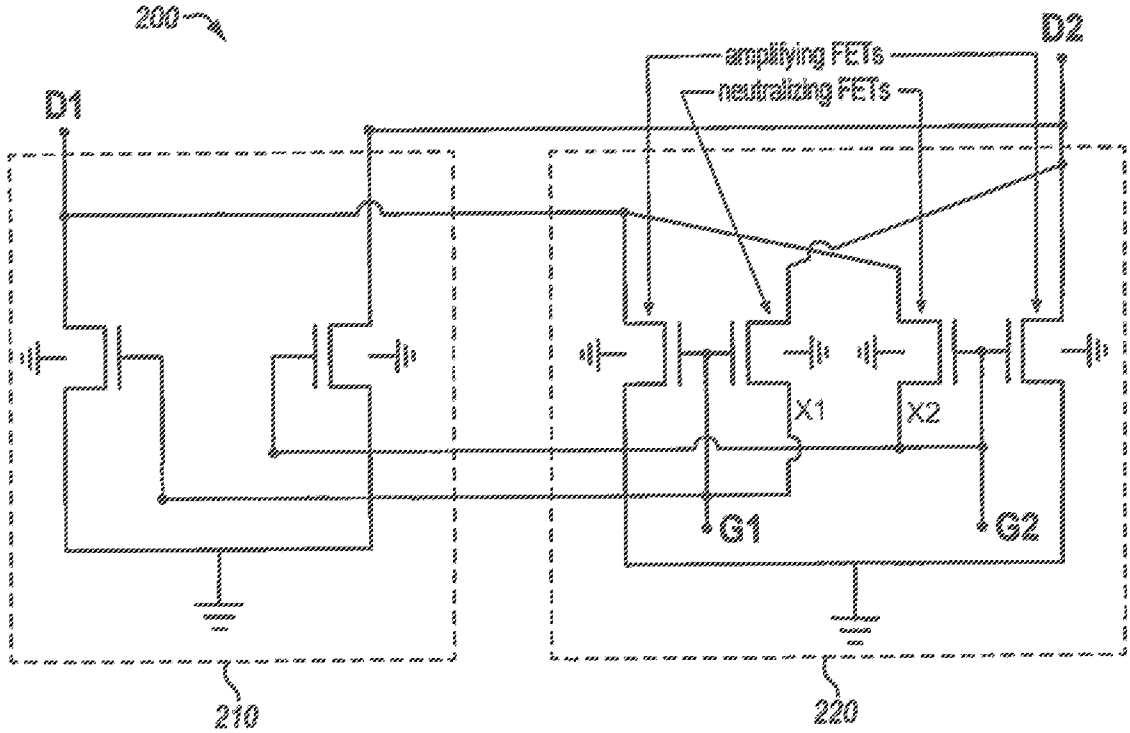

C_n
C_{gd}
FET1
FET2

FIG. 2


200
D1
D2
amplifying FETs
neutralizing FETs
X1
X2
G1
G2
210
220

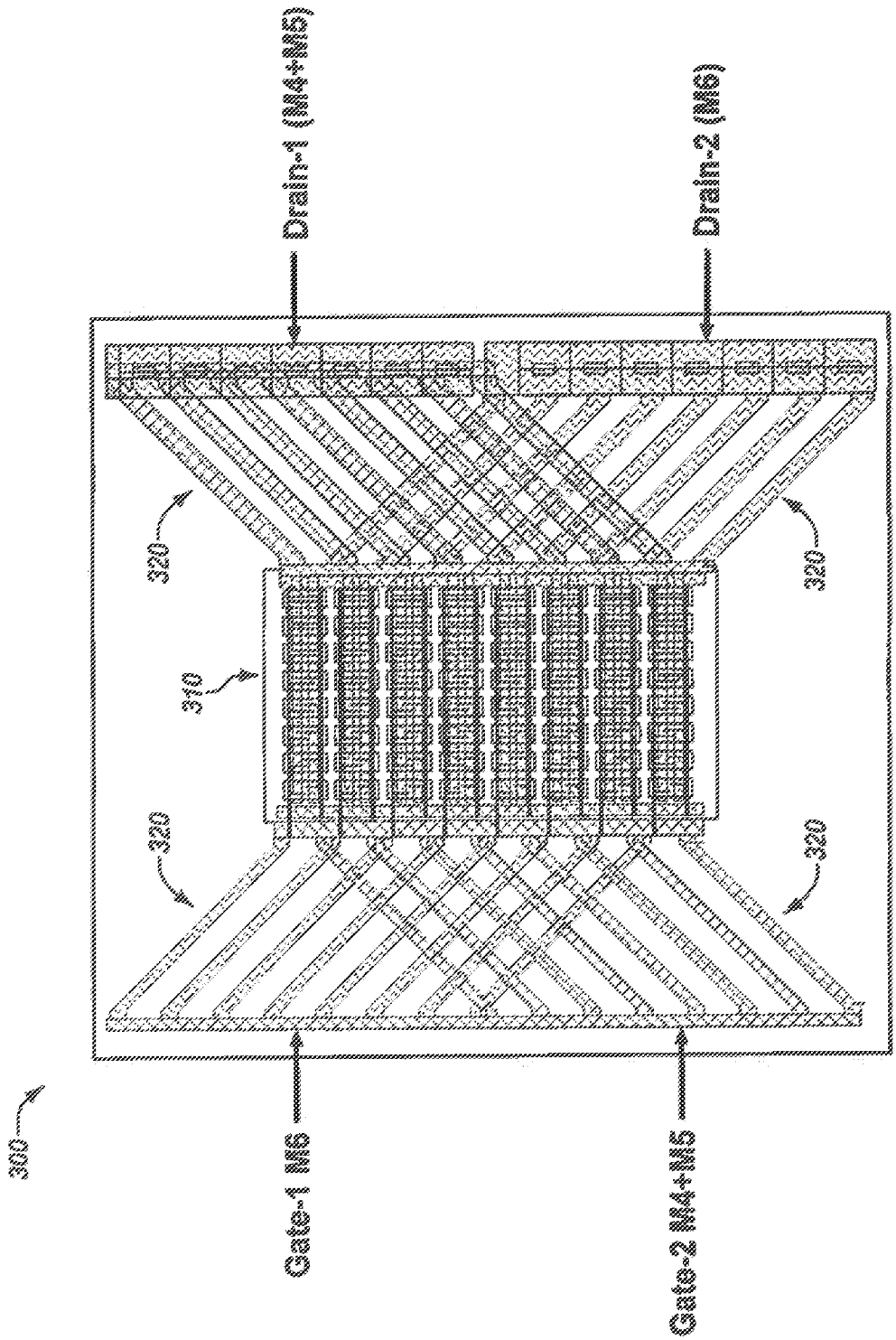

Drain-1 (M4+M5)
Drain-2 (M6)
320
320
310
320
320
300
Gate-1 M6
Gate-2 M4+M5

FIG. 3A

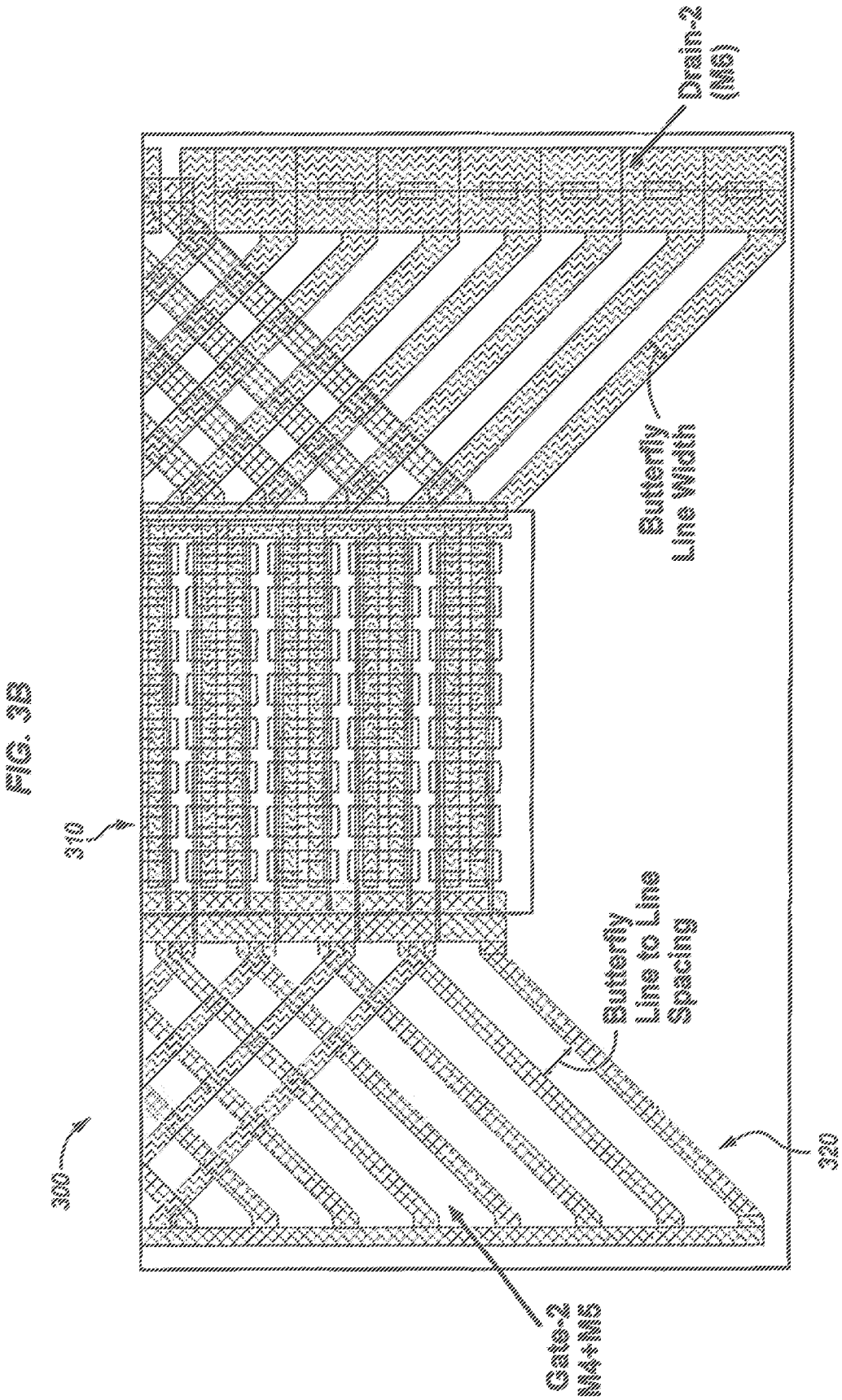

Bridge
Butterfly Line Width
Butterfly Line to Line Spacing
Cell Width

FIG. 1B

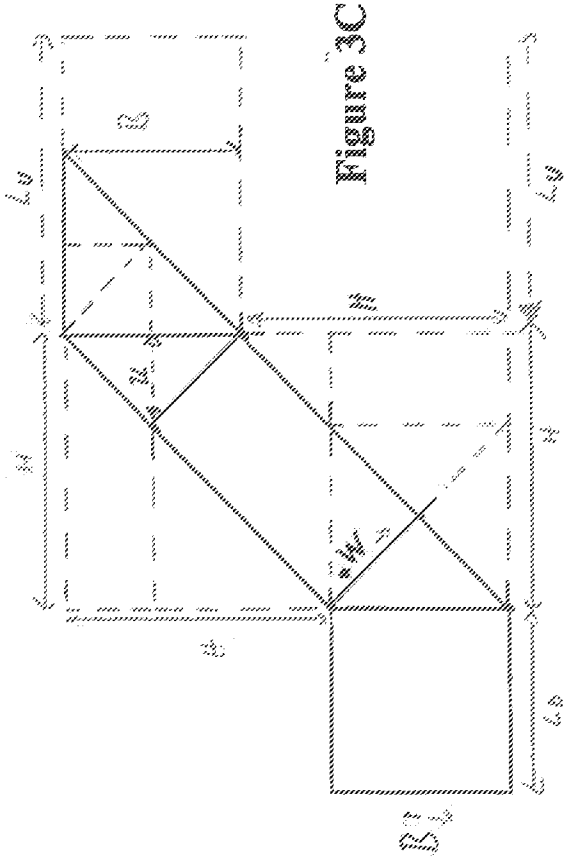


Figure 3C

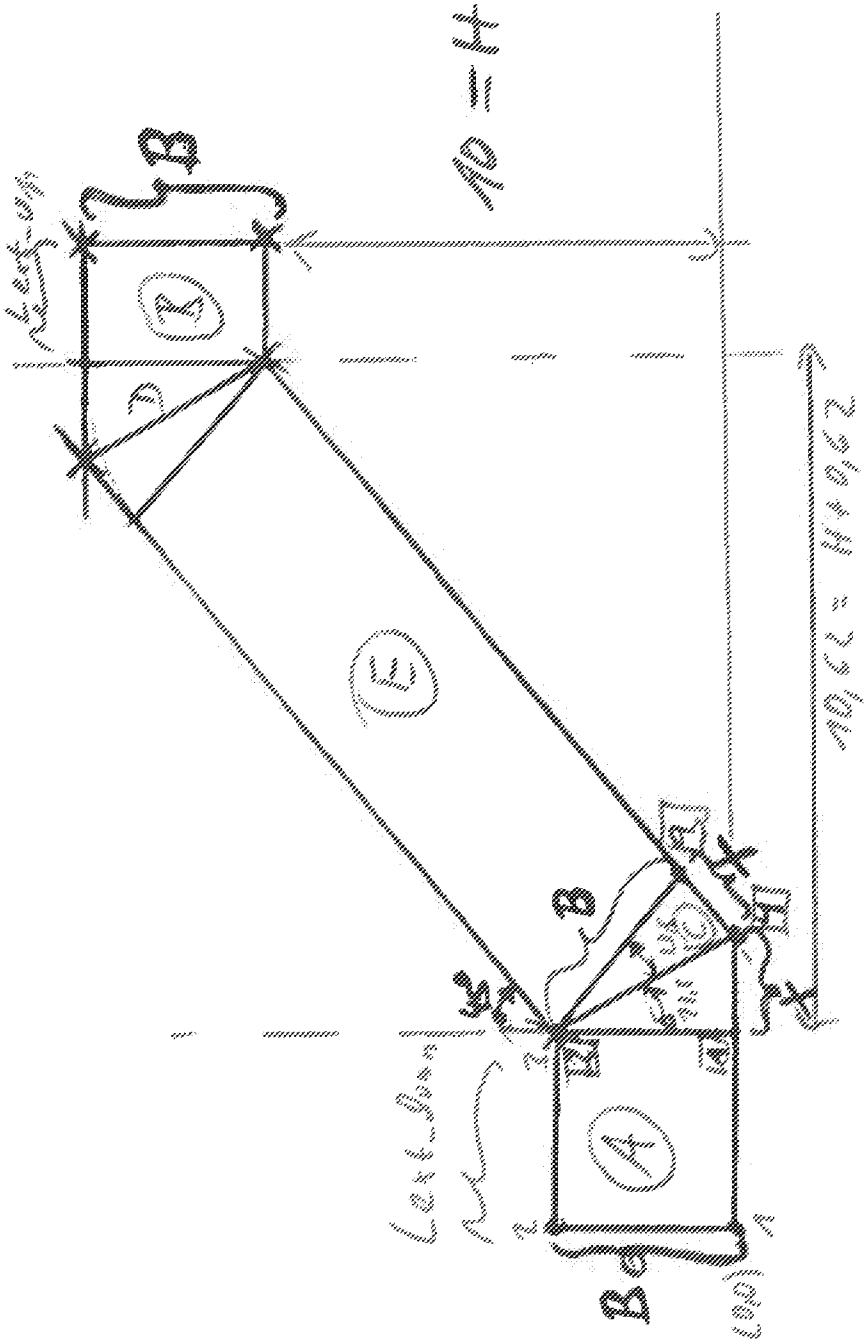


Figure 3D

FIG. 4A

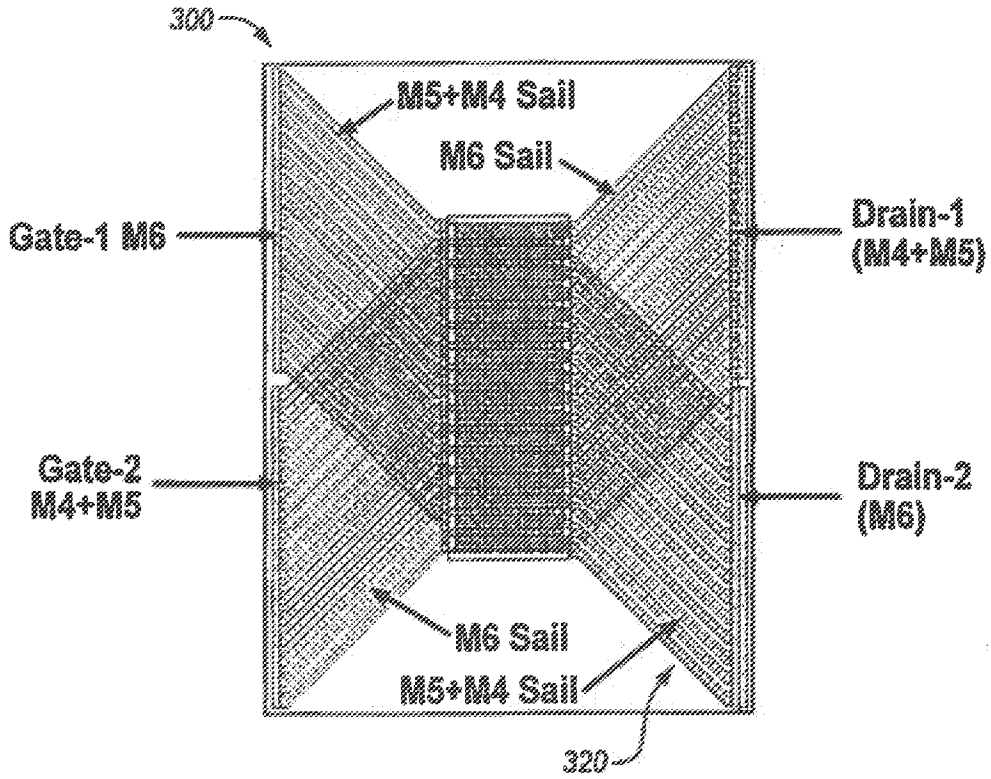

300
M5+M4 Sail
M6 Sail
Gate-1 M6
Drain-1
(M4+M5)
Gate-2
M4+M5
Drain-2
(M6)
M6 Sail
M5+M4 Sail
320

FIG. 4B

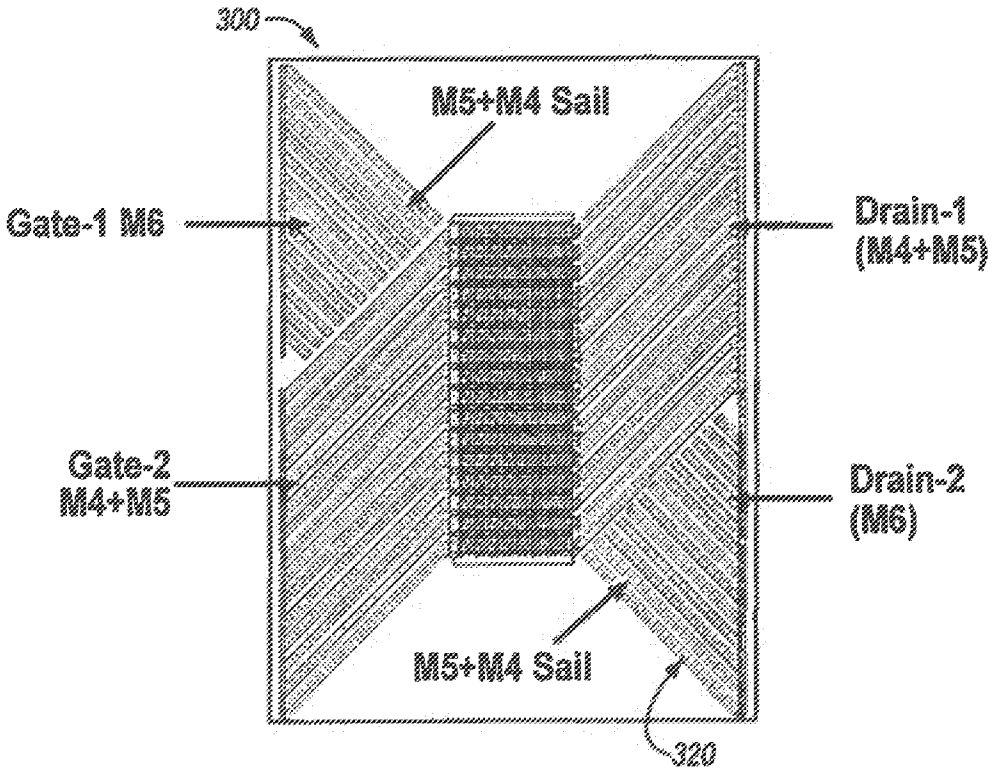

300
M5+M4 Sail
Gate-1 M6
Drain-1
(M4+M5)
Gate-2
M4+M5
Drain-2
(M6)
M5+M4 Sail
320

FIG. 4C

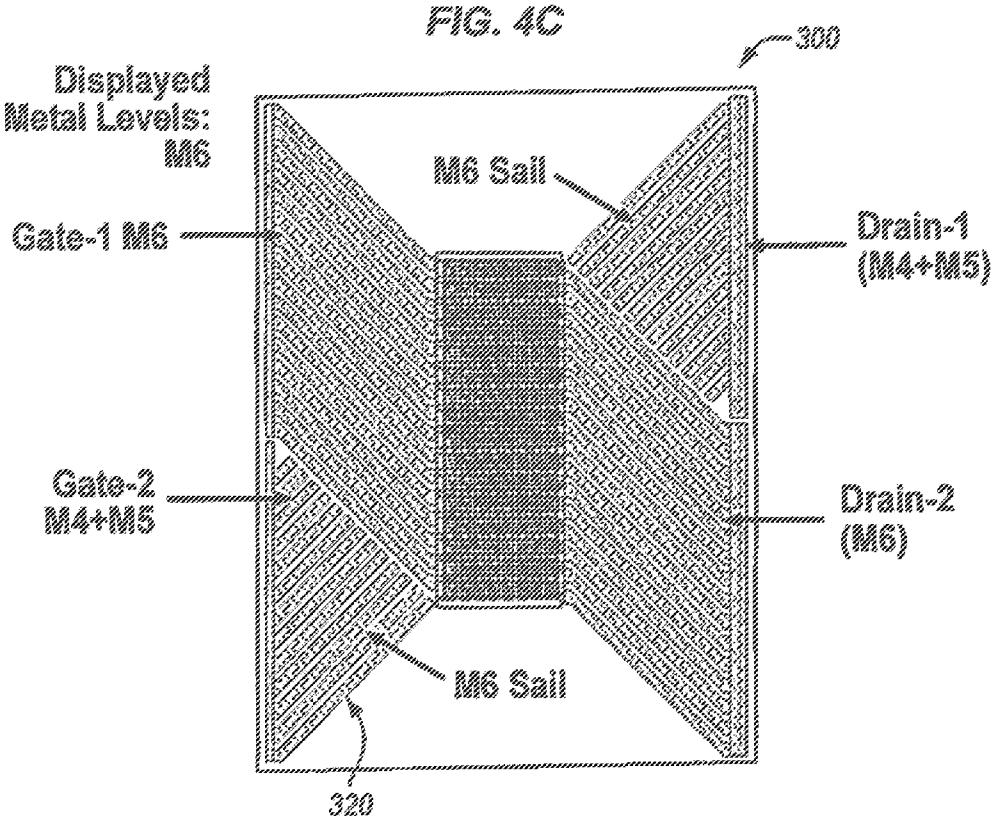
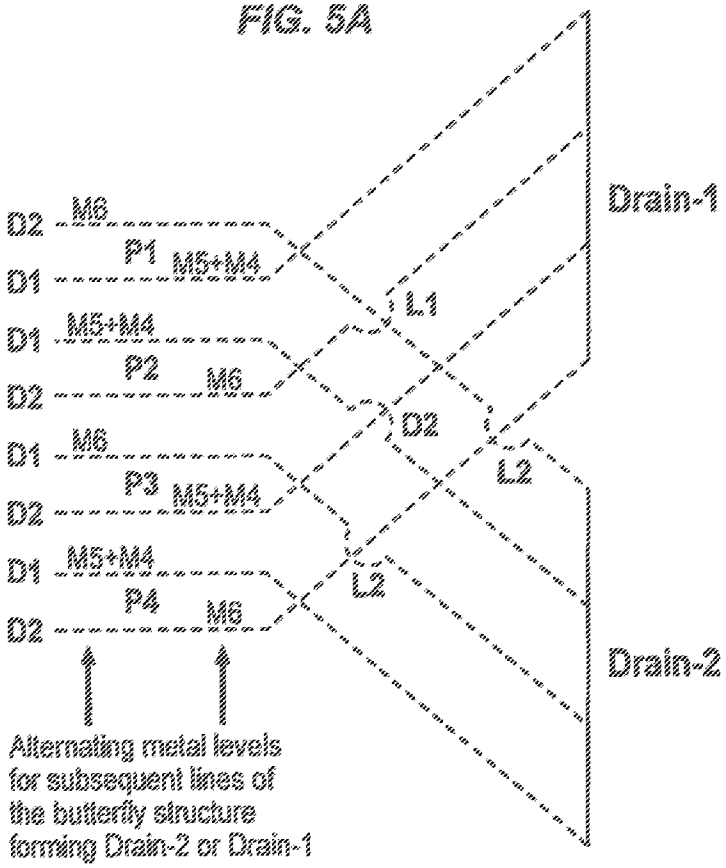

300
Displayed Metal Levels: M6
M6 Sail
Gate-1 M6
Drain-1 (M4+M5)
Gate-2 M4+M5
Drain-2 (M6)
M6 Sail
320

FIG. 5A


Drain-1
D2
M6
P1
M5+M4
D1
L1
D1
M5+M4
P2
D2
M6
D2
D1
M6
P3
L2
D2
M5+M4
D1
M5+M4
P4
L2
D2
M6
Drain-2
Alternating metal levels for subsequent lines of the butterfly structure forming Drain-2 or Drain-1

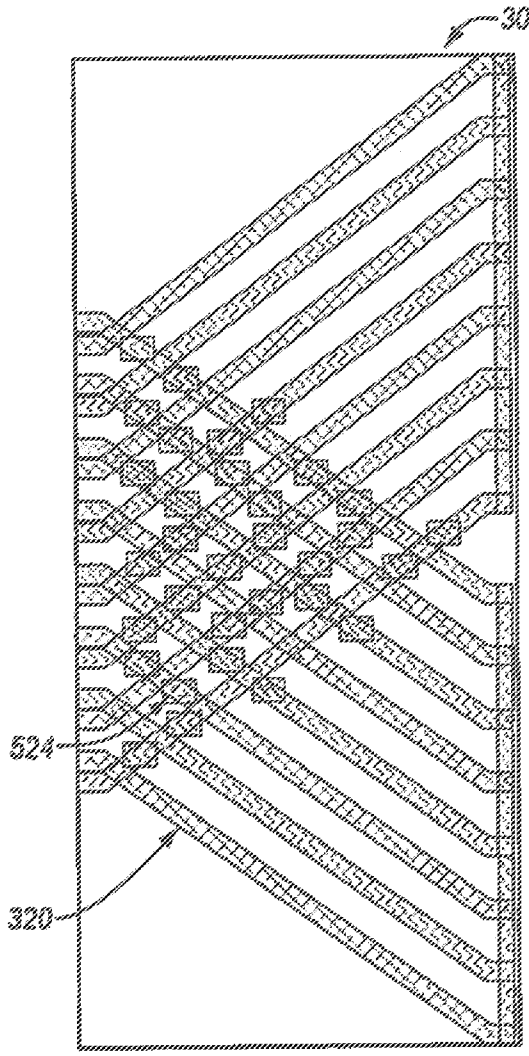


FIG. 5B

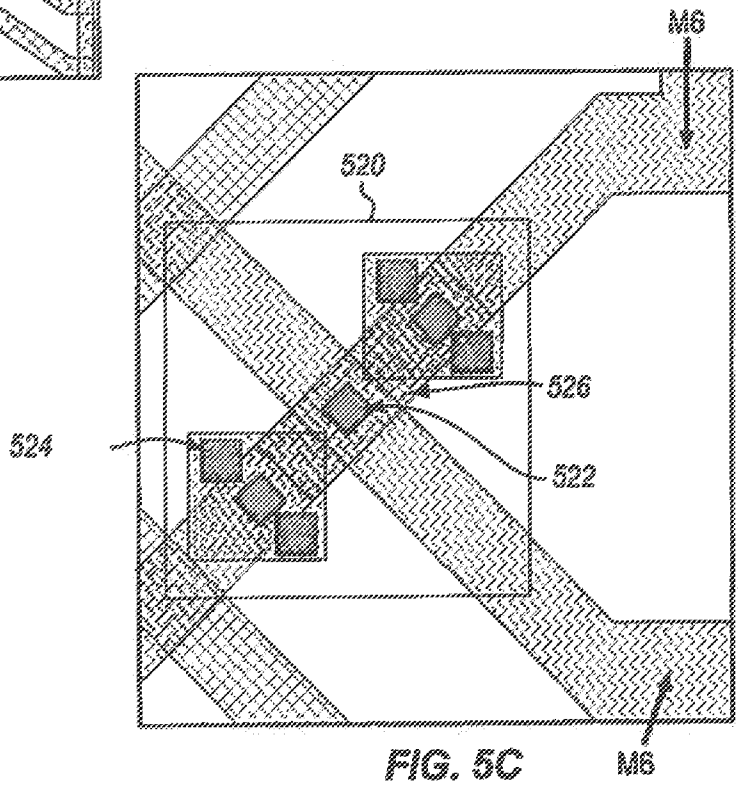


FIG. 5C

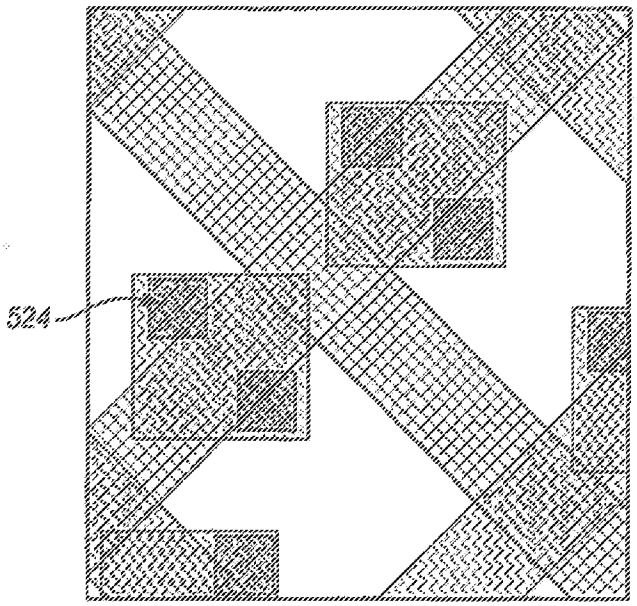


FIG. 5D

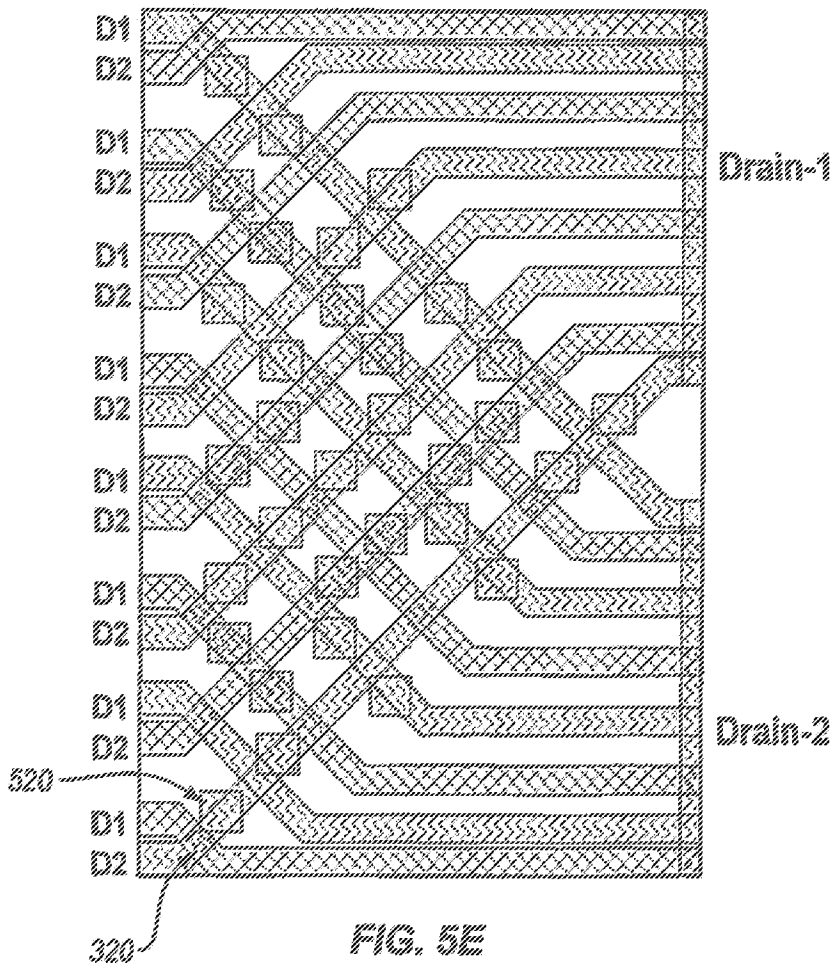


FIG. 5E

FIG. 6A

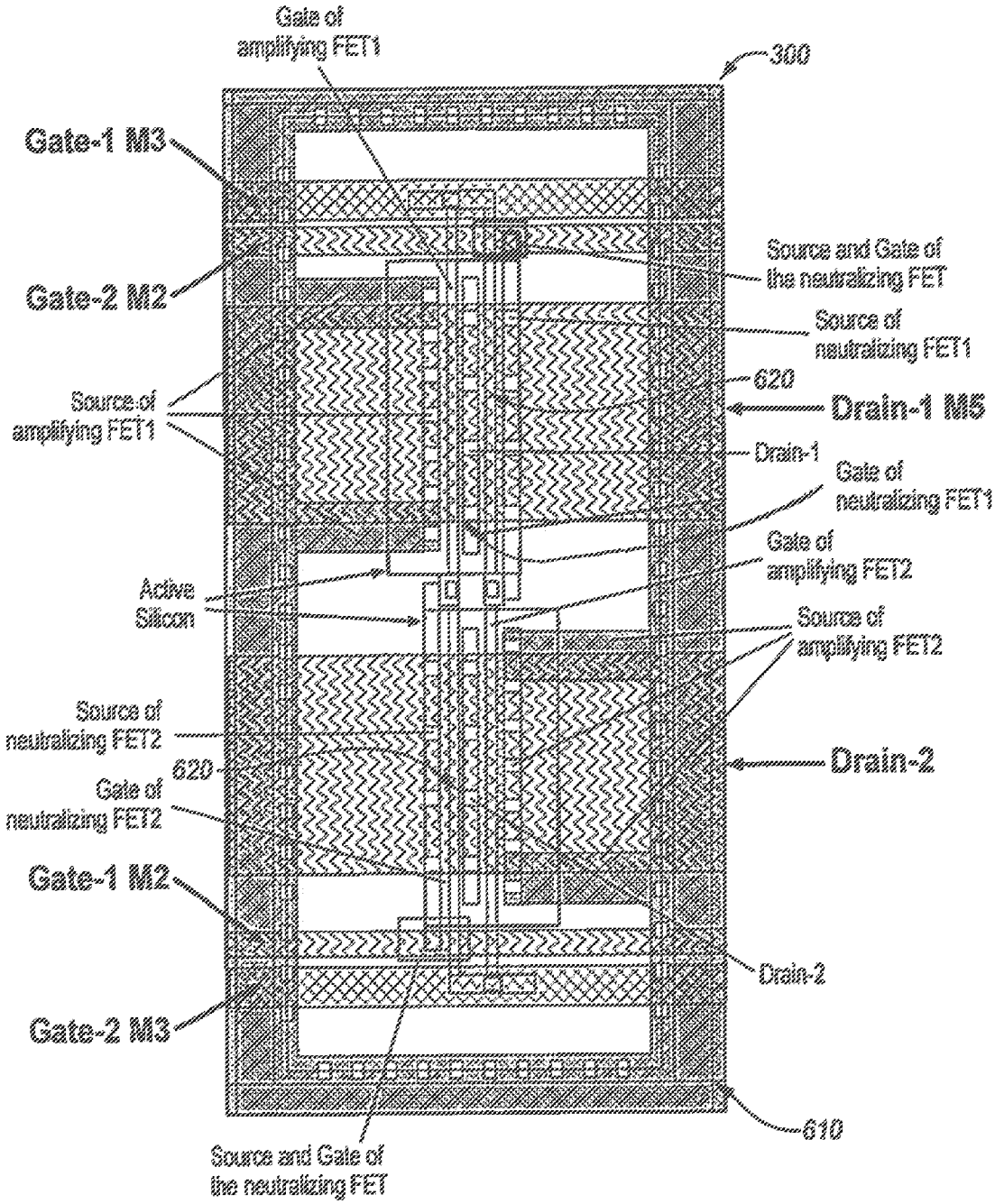

Gate of amplifying FET1
300
Gate-1 M3
Gate-2 M2
Source and Gate of the neutralizing FET
Source of neutralizing FET1
620
Drain-1 M5
Source of amplifying FET1
Drain-1
Gate of neutralizing FET1
Gate of amplifying FET2
Active Silicon
Source of amplifying FET2
Source of neutralizing FET2
620
Drain-2
Gate of neutralizing FET2
Gate-1 M2
Drain-2
Gate-2 M3
610
Source and Gate of the neutralizing FET

FIG. 6B

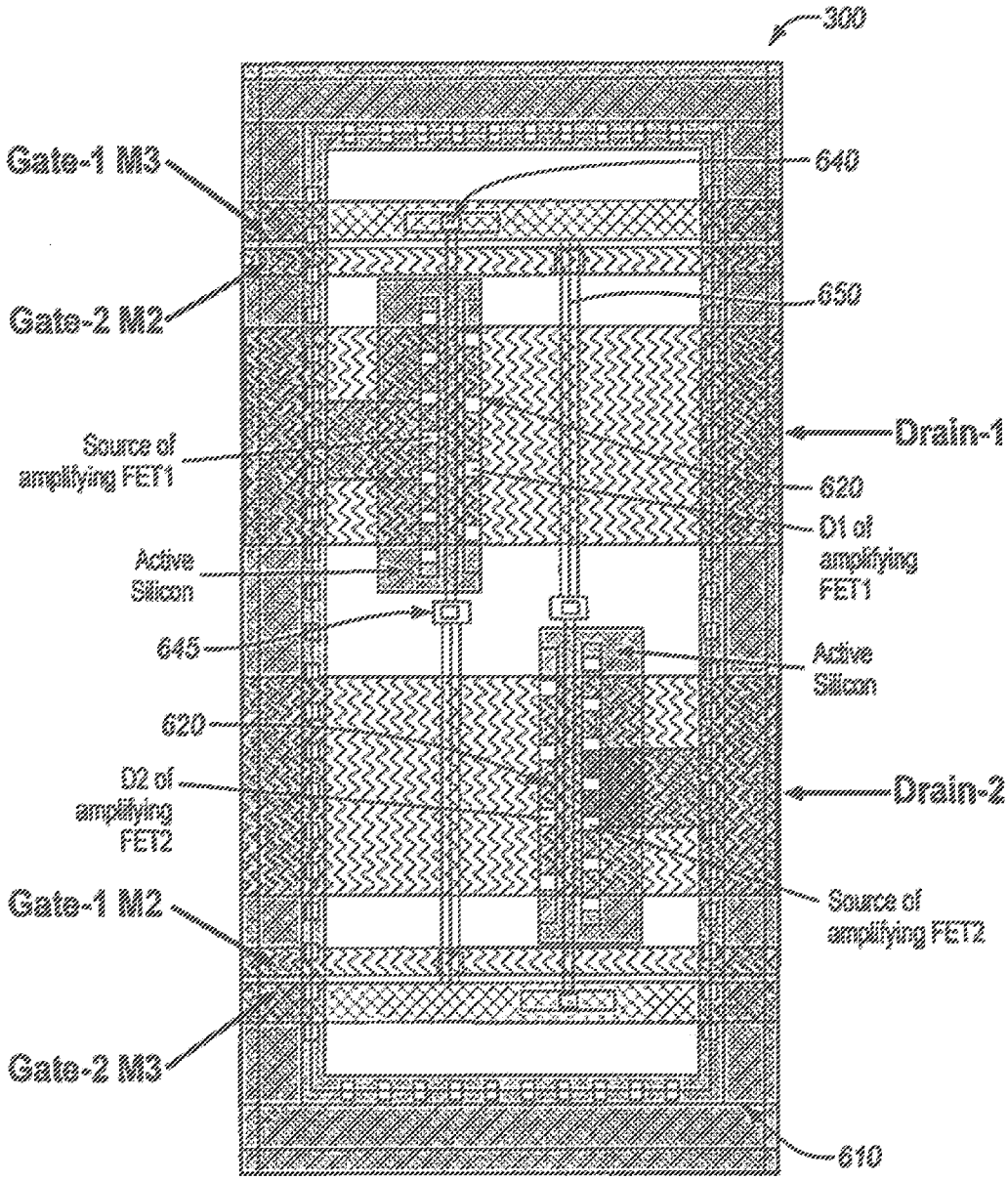

300
Gate-1 M3
640
Gate-2 M2
650
Drain-1
Source of amplifying FET1
620
D1 of amplifying FET1
Active Silicon
645
Active Silicon
620
D2 of amplifying FET2
Drain-2
Gate-1 M2
Source of amplifying FET2
Gate-2 M3
610

FIG. 6C

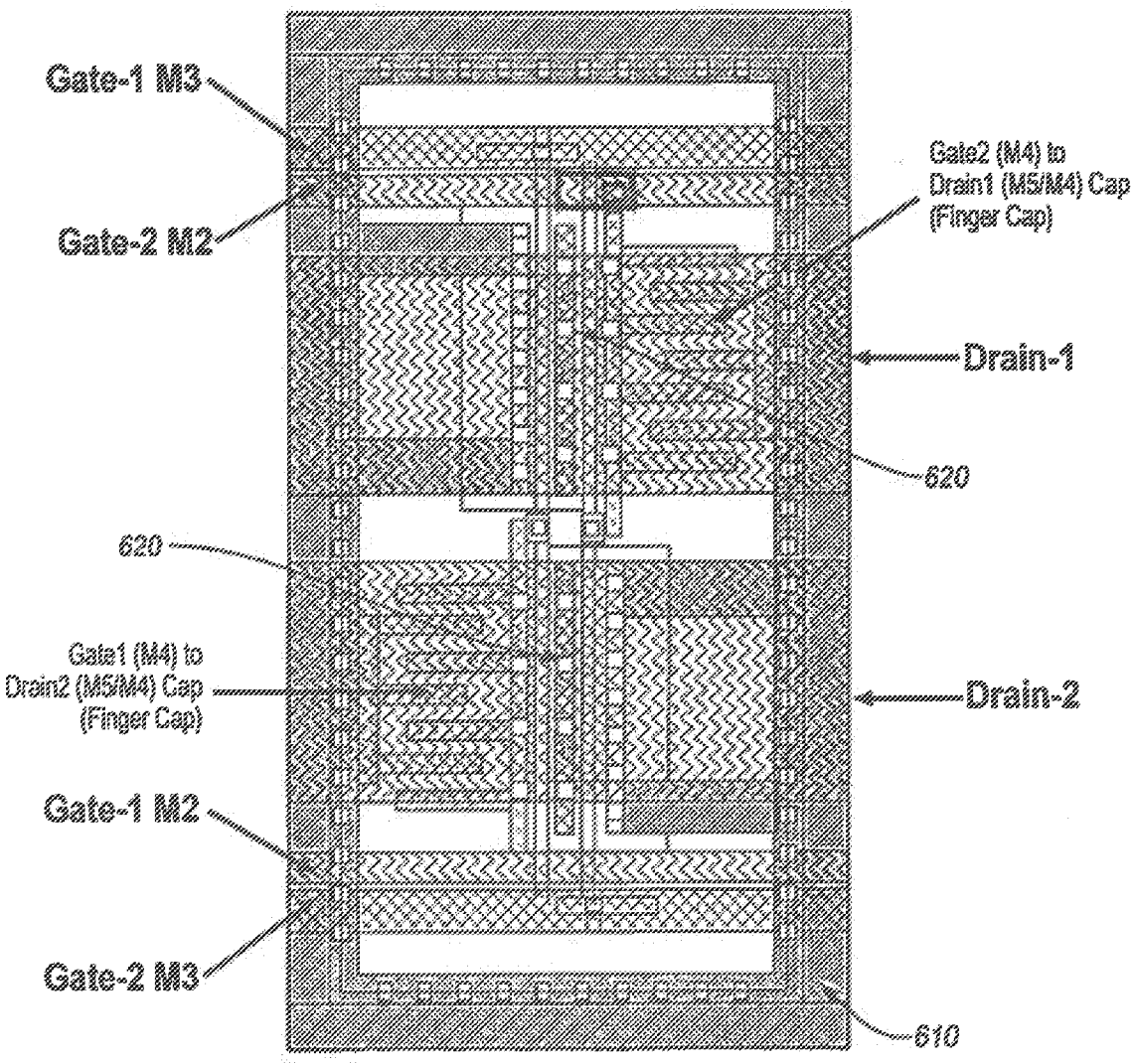

Gate-1 M3
Gate-2 M2
Gate2 (M4) to Drain1 (M5/M4) Cap (Finger Cap)
Drain-1
620
620
Gate1 (M4) to Drain2 (M5/M4) Cap (Finger Cap)
Drain-2
Gate-1 M2
Gate-2 M3
610

FIG. 6D

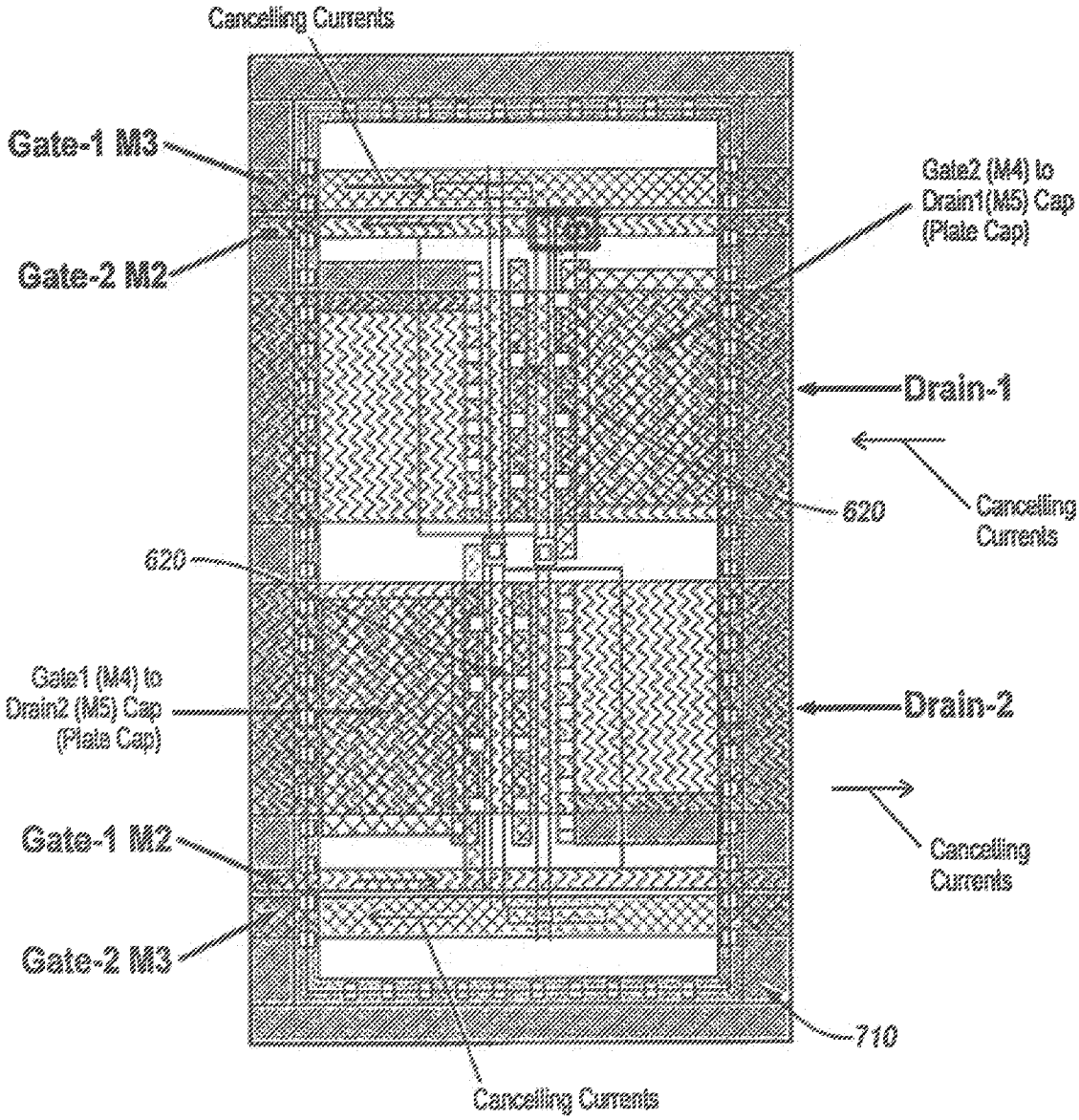
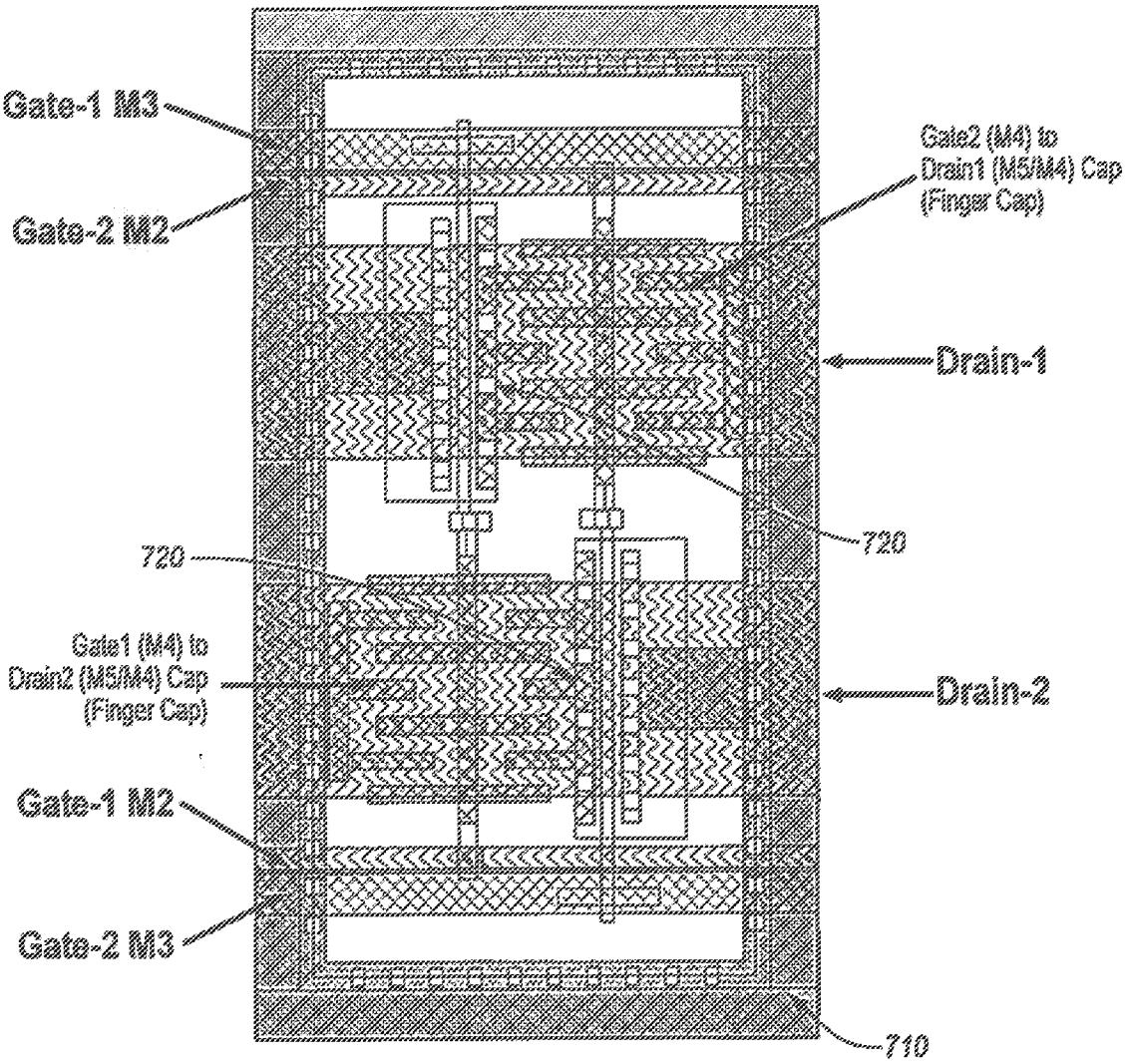

Cancelling Currents
Gate-1 M3
Gate-2 M2
Gate2 (M4) to Drain1(M5) Cap (Plate Cap)
Drain-1
Cancelling Currents
620
620
Gate1 (M4) to Drain2 (M5) Cap (Plate Cap)
Drain-2
Cancelling Currents
Gate-1 M2
Gate-2 M3
710
Cancelling Currents

FIG. 6E


Gate-1 M3
Gate-2 M2
Gate2 (M4) to Drain1 (M5/M4) Cap (Finger Cap)
Drain-1
720
720
Gate1 (M4) to Drain2 (M5/M4) Cap (Finger Cap)
Drain-2
Gate-1 M2
Gate-2 M3
710

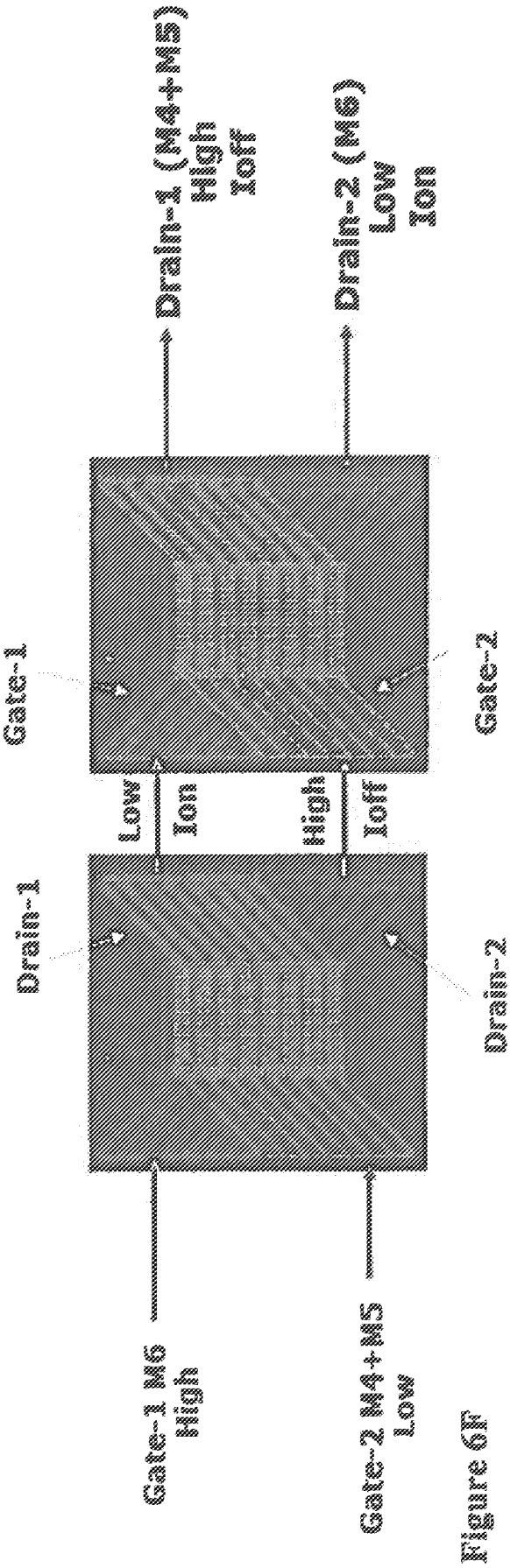


Figure 6F

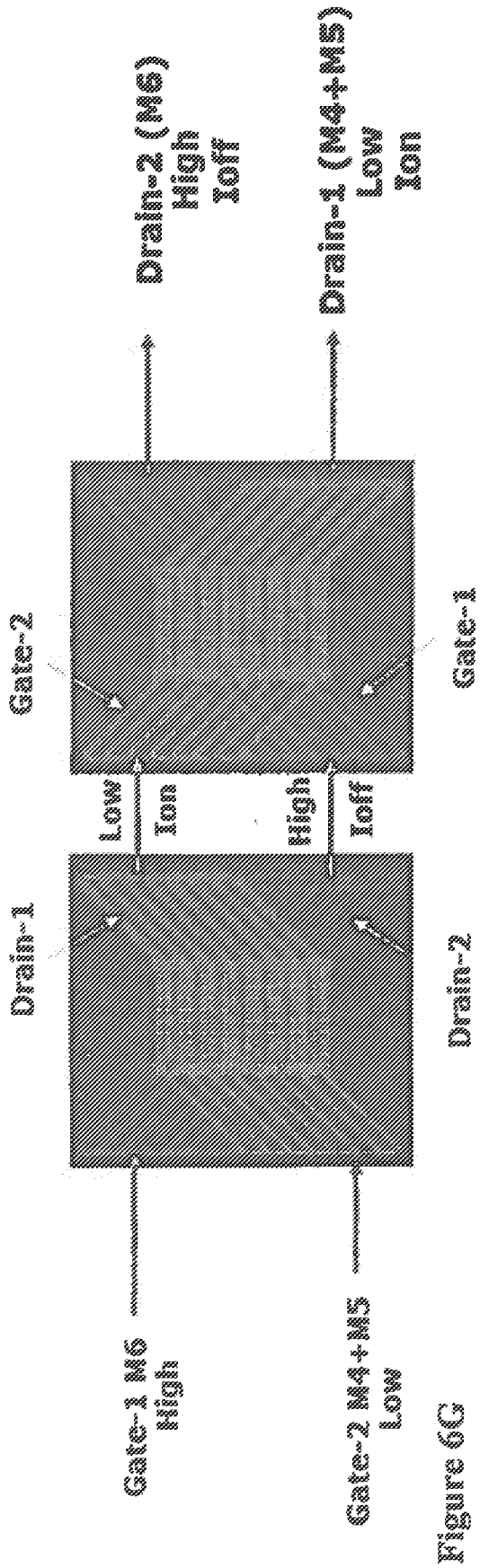


Figure 6G

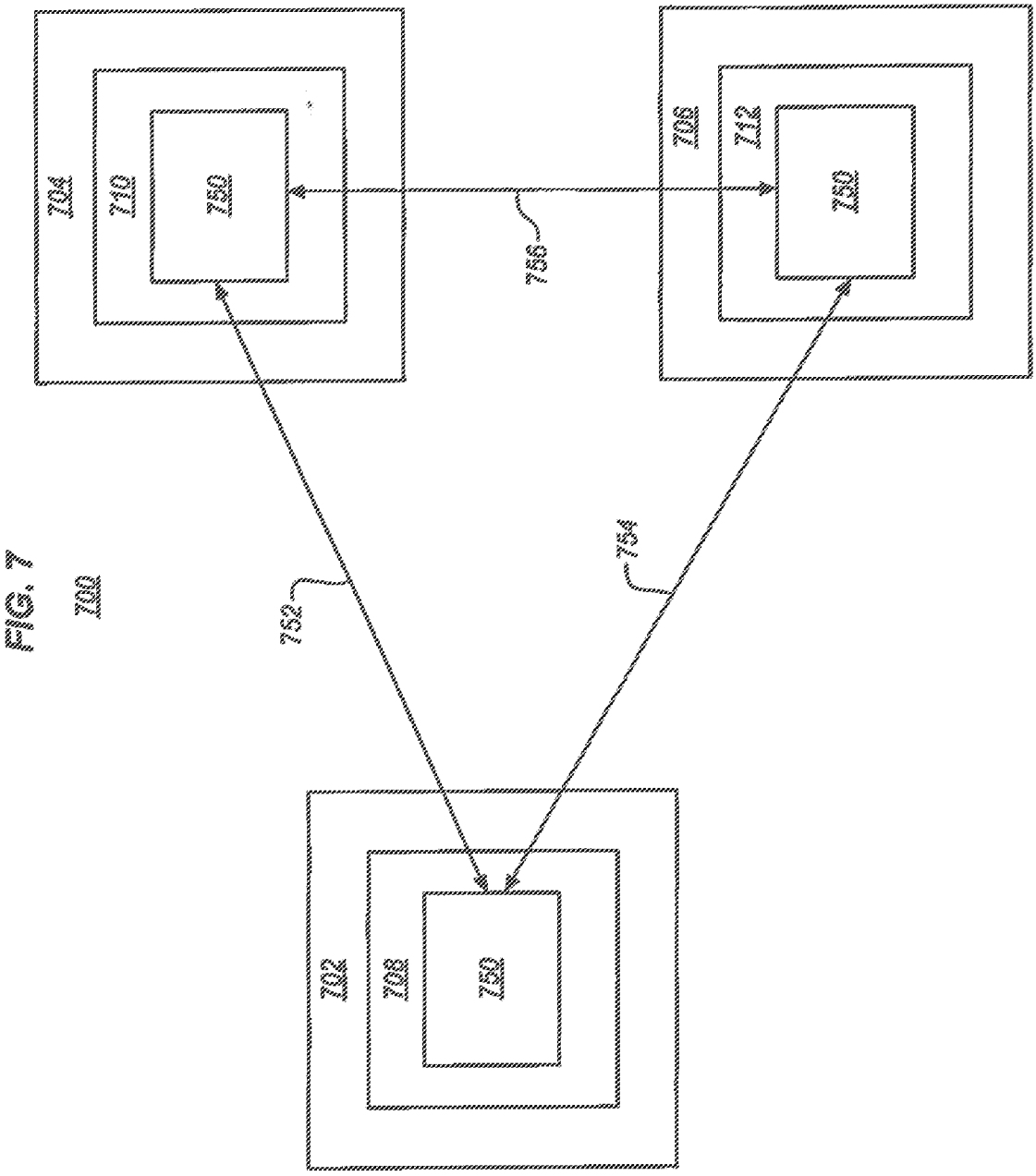


FIG. 7

700

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/025520

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H03B 19/14; H03F 3/45; H03K 5/22; G01R 19/00; H03F 1/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: neutralization, FET, pair, match

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006-0284670 A1 (SALEM EID et al.) 21 December 2006 See paragraphs [0046]-[0074] and figures 8-10.	1-2,21,24-25
A		3-20,22-23
A	US 2013-0257483 A1 (JOHN F. BULZACCHELLI) 03 October 2013 See paragraphs [0021]-[0047] and figures 1-4.	1-25
A	US 2014-0139274 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 22 May 2014 See paragraphs [0032]-[0042] and figures 1-4.	1-25
A	US 2012-0068769 A1 (TONG WANG et al.) 22 March 2012 See paragraphs [0023]-[0058] and figures 1-4.	1-25
A	US 2015-0349721 A1 (AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE. LTD.) 03 December 2015 See paragraphs [0037]-[0046] and figures 3A-6.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 December 2016 (27.12.2016)	**28 December 2016 (28.12.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/025520

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 4305472 B2	29/07/2009
		US 7256646 B2	14/08/2007
US 2013-0257483 A1	03/10/2013	US 8624632 B2	07/01/2014
US 2014-0139274 A1	22/05/2014	CN 103840769 A	04/06/2014
		US 2014-0140450 A1	22/05/2014
		US 2015-0130517 A1	14/05/2015
		US 2015-0155858 A1	04/06/2015
		US 8917805 B2	23/12/2014
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		US 9419595 B2	16/08/2016
US 2012-0068769 A1	22/03/2012	JP 2012-065168 A	29/03/2012
		JP 5228017 B2	03/07/2013
		US 8344805 B2	01/01/2013
US 2015-0349721 A1	03/12/2015	CN 105281678 A	27/01/2016
		US 9490759 B2	08/11/2016