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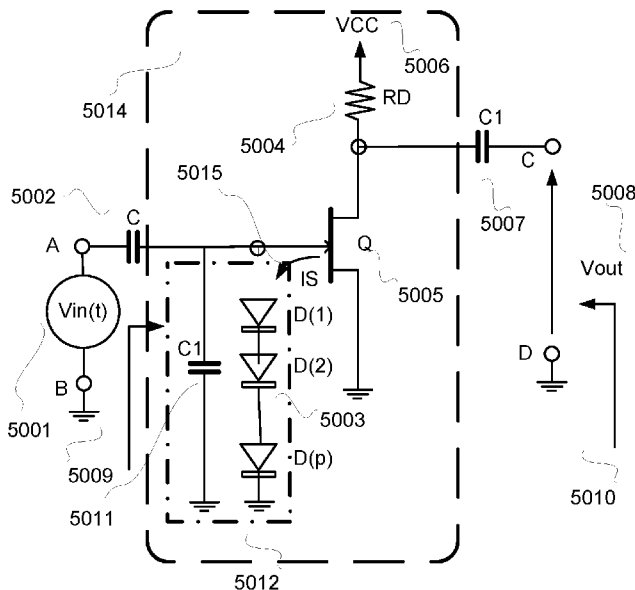
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FIG. 5



(57) Abstract: A microphone circuit including a JFET or MOSFET transistor, one input of an impedance network connected to the transistor's gate, a terminal of a source resistor connected to the transistor's source, another terminal of the source resistor connected to ground, a bypass capacitor connected in parallel to the source resistor, one terminal of a load resistor connected to the transistor's drain, VCC_LOW connected to another terminal of the load resistor, an input of an op-amplifier connected to the transistor's source through a bi-directional low-pass-filter, another input of the op-amplifier connected to reference voltage, an output of the op-amplifier connected to another terminal of the input impedance network through an LPF, an energy detector connected to the transistor's drain via a coupling capacitor, an LPF connected to the energy detector output, and an LPF connected to the output of the energy detector, the input impedance network connected to a microphone.

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ADAPTIVE-SNR ULTRA-LOW-POWER ULTRA-LOW-NOISE MICROPHONE

FIELD

The method and apparatus disclosed herein are related to the field of electronic circuitry, and, more particularly, but not exclusively to systems and methods providing ultra-low-power and an ultra-low-noise microphone buffer having adaptive signal-to-noise ratio (SNR).

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 62/191,452, filed July 12, 2015, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

Today, 2015, microphones are used nearly anywhere, in smartphones - where we have about 3 microphones for a smartphone, cellphones, Bluetooth earring devices, wired earring devices, toys, billions of microphones are sold every year. not only that, currently there are about 2 billion smartphones around the world, the smartphone, is basically a cellphone with internet connection palm computer and sensors, the smartphone keep each one of us to be connected to the internet, with "Google Play" for Android phones and "App Store" for iOS based phones, each one of us can download an application - for gaming, for Global Positioning System, for service providers etc., all in all the smartphone, which is connected to the internet and has the ability to run applications make our lives much more comfortable and easy.

In recent years more and more devices are being connected to the internet, such as air conditions, washing machines, clothes dryers, electrical water boilers. There are many advantages of connecting a device to the internet, for example connecting electrical water boiler, washing machine and clothes dryer machine, will help us to save money. The reason is that the rates of electricity depend on the time of the hour, usually in the morning

time, residential electricity will cost less, since there is no much of demand, but at nights the residential electricity cost will be high because of two much of demand. Therefore one can activate the washing machine and drying machine in power saving mode, and the machines will contact the electricity utility company computer via the internet, and will get the rates as a function of time, then it would be possible to activate these machines only during low cost residential electricity rate.

With respect to air conditioners and smart sensors it is possible to have the "brain" of the air condition as a neural network on the internet, and hence activate it smartly, having many sensors around the house which are also connected to the internet.

Even further, it is possible to have a battery-based electricity generator, that will charge the battery when there is low demand - this may vary from time to time - and hence it is possible to get a generator that stores the electricity energy during low demand and hence during low rates and that would generate the energy at home during times where the rates are high - these battery based generator must be connected to the internet to be able to connect the electric utility company for getting the times when it is possible to charge the generator battery.

The above is called today the "Internet of Things" (IoT) or Internet of Everything (IoE). The benefits of connecting a device to the internet are:

Ability to smart control the device, having the brain on the net or the ability to control each device from our palm of our hands, Ability to monitor and get information about the device, for service for example, for off date usage, Ability to locate devices, Ability to have whole internet information in each device even a tooth brush or a screw driver, Ability to get deals, All on all, the connection of the devices to the internet will make our lives much more efficient, It is claimed that by 2020 more than 50,000,000,000 devices would be connected to the internet such as electrical devices: air-conditioners, drying machines, washing machine, battery-based generator, light bulbs, electricity outlets, electrical water boilers, gas-based water boilers, TV, Tools, such as screw driver or hammer, Bath related devices such as tooth brush and Bed room related devices.

It is clear that some IoT, or IoE devices that would be connected to the internet would have a local power source - such as electrical water boilers and air conditions - these IoT , IoE devices can use Wi-Fi, Bluetooth (BT), ZigBee or any other wireless standard or

Power line to connect the device to the home local router and hence to the internet etc., but some devices such as glasses, tools, clothes, bath room moveable devices such as tooth brush, toys would not an energy source.

Therefore if implemented by electromagnetic radio frequency (RF) communication. Power is a big issue and such receiver would need to be implemented either as a periodically turn on /window turn on or as a wake receiver that basically detects a presence of energy in some band, and later check if it was valid marker. These two step process would usually save a lot of power, as the marker check is done only when a signal is detected.

However in the ISM band or in radio frequency band there is a lot of noise, and an implementation of selective band wakeup receiver is not an easy task with high bandwidth.

There is thus a widely recognized need for, and it would be highly advantageous to have, a system and method providing a microphone, and/or a microphone buffer circuit, devoid of the above limitations.

SUMMARY

According to one exemplary embodiment there is provided a device and a method for a microphone including a JFET and MOSFET transistor, an impedance network, where a first input terminal of the impedance network is connected to a gate terminal of the transistor, a source resistor, where a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal, a bypass capacitor (CS) connected in parallel to the source resistor, a load resistor (RD), where a first terminal of the load resistor is connected to a drain terminal of the transistor, a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, where the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier, an op-amplifier, where a first input terminal of the op-amplifier is connected to the source terminal of the transistor through a bi-directional low-pass-filter transistor, a second input terminal of the op-amplifier is connected to a controlled reference voltage Vref, a first power supply terminal of the op-amplifier is connected to the inverted voltage, a second supply terminal of the op-amplifier is

connected to the main supply voltage, and an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter, and an input electrets capacitor source connected in parallel to the input impedance network, an ultra-low-power envelope/energy detector connected to drain terminal D of the transistor via coupling capacitor, a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector, and a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

According to another exemplary embodiment there is provided an SNR monitor including a first input connected to a third low-pass-filter output, a second input connected to a fourth low-pass-filter output, one of: a third analog input, and a third digital input, that determines the required SNR, a first output connected to a control input of a controlled V_{ref} , and an optional second output connected to a control input of an optional controlled charge pump..

According to yet another exemplary embodiment there is provided a device and a method for a microphone including a transistor including at least one of a JFET and MOSFET transistor, an impedance network, where a first input terminal of the impedance network is connected to a gate terminal of the transistor, a source resistor, where a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal, a bypass capacitor (CS) connected in parallel to the source resistor, a load resistor (RD), where a first terminal of the load resistor is connected to a drain terminal of the transistor, a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage $-VEE$, where the low voltage is connected to a second terminal of the load resistor, and the inverted voltage $-VEE$ is connected to a first power supply node of an op-amplifier, an op-amplifier, where a first input terminal of the op-amplifier is connected to the source terminal of the transistor through a bi-directional low-pass-filter transistor, a second input terminal of the op-amplifier is connected to a controlled reference voltage V_{ref} , a first power supply of the op-amplifier terminal is connected to the inverted voltage, a second supply terminal of the op-amplifier is connected to the main supply voltage, and an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter, and an input source including a MEMS capacitor, where a first terminal of the MEMS capacitor is connected to ground, and a second terminal of the

MEMS capacitor is connected to a first terminal of a MEMS bias network, the MEMS bias network, where a second terminal of the MEMS bias network is connected to a bias voltage VBB, and a coupling capacitor, where a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor, an ultra-low-power envelope/energy detector connected to drain terminal of the transistor via a coupling capacitor, a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector, and a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

According to still another exemplary embodiment there is provided a device and a method for a microphone including a transistor including at least one of a JFET and MOSFET transistor, an impedance network, where a first input terminal of the impedance network is connected to a gate terminal of the transistor, a source resistor, where a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal, a bypass capacitor (CS) connected in parallel to the source resistor, a load resistor (RD), where a first terminal of the load resistor is connected to a drain terminal of the transistor, a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, where the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier, the op-amplifier, where a first input terminal of the op-amplifier is connected to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter, where a first input terminal of the differential bi-directional low-pass-filter is connected to a second terminal of the load resistor, a second input terminal of the op-amplifier is connected to a second output terminal of a differential bi-directional low-pass-filter, where a second input terminal of the differential bi-directional low-pass-filter is connected to the first terminal of the load resistor, a first power supply of the op-amplifier terminal is connected to the inverted voltage, a second supply terminal of the op-amplifier is connected to the main supply voltage, and an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter, an input electrets capacitor source connected in parallel to the input impedance network, an ultra-low-power envelope/energy detector connected to drain terminal of the

transistor via a coupling capacitor, a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector, and a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

Further according to another exemplary embodiment there is provided a device and a method for a microphone including a transistor including at least one of a JFET and MOSFET transistor, an impedance network, where a first input terminal of the impedance network is connected to a gate terminal of the transistor, a source resistor, where a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal, a bypass capacitor (CS) connected in parallel to the source resistor, a load resistor (RD), where a first terminal of the load resistor is connected to a drain terminal of the transistor, a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage $-VEE$, where the low voltage is connected to a second terminal of the load resistor, and the inverted voltage $-VEE$ is connected to a first power supply node of an op-amplifier, an op-amplifier, where a first input terminal of the op-amplifier is connected to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter, where a first input terminal of the differential bi-directional low-pass-filter is connected to a second terminal of the load resistor, a second input terminal of the op-amplifier is connected to a second output terminal of a differential bi-directional low-pass-filter, where a second input terminal of the differential bi-directional low-pass-filter is connected to the first terminal of the load resistor, a first power supply of the op-amplifier terminal is connected to the inverted voltage, a second supply terminal of the op-amplifier is connected to the main supply voltage, and an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter, and an input source including a MEMS capacitor, where a first terminal of the MEMS capacitor is connected to ground and a second terminal of the MEMS capacitor is connected to a first terminal of a MEMS bias network, a MEMS bias network connected with it second terminal to a bias voltage VBB , and the MEMS bias network, where a second terminal of the MEMS bias network is connected to a bias voltage VBB , and a coupling capacitor, where a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor.

Still further according to another exemplary embodiment the input impedance network includes a plurality of low-leakage diodes connected in series where a first diode cathode terminal is the first terminal of the input impedance network, a first diode anode terminal is connected to a second diode cathode terminal, and an anode terminal of diode N is the second terminal to the input impedance network.

Yet further according to another exemplary embodiment the input impedance network is includes a plurality of low-leakage diodes connected in series where a first diode anode terminal is the first terminal of the input impedance network, a first diode cathode terminal is connected to a second diode anode terminal, and a cathode terminal of diode N is the second terminal of the input impedance network.

Even further according to another exemplary embodiment the input impedance network includes of a parallel diode network including a first diode network including a plurality of diodes connected in series where a first diode cathode terminal is the first terminal of the input impedance network, a first diode anode terminal is connected to a second diode cathode terminal, and an anode terminal of diode N is the second terminal of the input impedance network, and a second diode network including a plurality of diodes connected in series where a first diode anode terminal is the first terminal of the input impedance network, a first diode cathode terminal is connected to a second diode anode terminal, and a cathode terminal of diode N is the second terminal to the input impedance network.

Additionally, according to another exemplary embodiment the input impedance network includes at least two series of two-terminal sub-networks where a first terminal of a first sub-network is the first terminal of the input impedance network, a second terminal of a last sub network is the second terminal of the input impedance network and where a sub-network includes a two low-leakage identical diodes connected in parallel in opposite polarity.

According to yet another exemplary embodiment the charge pump is a controlled charge pump.

According to still another exemplary embodiment the MEMS bias impedance network includes a plurality of low-leakage diodes connected in series, where a first diode cathode terminal is the first terminal of the MEMS bias impedance network, a first diode

anode terminal is connected to a second diode cathode terminal, and an anode terminal of diode N is the second terminal to the MEMS bias impedance network.

Further according to another exemplary embodiment the MEMS bias impedance network includes plurality of low-leakage diodes connected in series, where a first diode anode terminal is the first terminal of the MEMS bias impedance network, a first diode cathode terminal is connected to a second diode anode terminal, and a cathode terminal of diode N is the second terminal to the MEMS bias impedance network.

Yet further according to yet another exemplary embodiment the MEMS bias impedance network includes a parallel diode network including a first and a second diode networks, the first diode network including a plurality of diodes connected in series, where a first diode cathode terminal is the first terminal of the MEMS bias impedance network, a first diode anode terminal is connected to a second diode cathode terminal, an anode terminal of diode N is the second terminal of the MEMS bias impedance network, and a second diode network including a plurality of diodes connected in series, where a first diode anode terminal is the first terminal of the MEMS bias impedance network, a first diode cathode terminal is connected to a second diode anode terminal, and a cathode terminal of diode N is the second terminal to the MEMS bias impedance network.

Still further according to yet another exemplary embodiment the MEMS bias impedance network includes of at least two series of two-terminal sub-networks where a first terminal of a first sub-network is the first terminal of the MEMS bias impedance network and a second terminal of a last sub network is the second terminal of the MEMS bias impedance network, where a sub network s includes two low-leakage identical diodes connected in parallel in opposite polarity.

Unless otherwise defined, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the relevant art. The materials, methods, and examples provided herein are illustrative only and not intended to be limiting. Except to the extent necessary or inherent in the processes themselves, no particular order to steps or stages of methods and processes described in this disclosure, including the figures, is intended or implied. In many cases the order of process steps may vary without changing the purpose or effect of the methods described.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments are described herein, by way of example only, with reference to the accompanying drawings. With specific reference now to the drawings in detail, it is stressed that the particulars shown are by way of example and for purposes of illustrative discussion of the preferred embodiments only, and are presented in order to provide what is believed to be the most useful and readily understood description of the principles and conceptual aspects of the embodiment. In this regard, no attempt is made to show structural details of the embodiments in more detail than is necessary for a fundamental understanding of the subject matter, the description taken with the drawings making apparent to those skilled in the art how the several forms and structures may be embodied in practice.

In the drawings:

Fig. 1 is a simplified block-diagram of a wakeup receiver implementation;

Fig. 2 is a simplified flow chart that describes the state machine of a transceiver;

Fig. 3 is a simplified electric schematic of a microphone element connected to a microphone buffer based on a JFET transistor;

Fig. 4 is a simplified electric schematic of an AC-equivalent circuit for noise/gain analysis of the circuit of Fig. 3;

Fig. 5 is a simplified electric schematic of a first exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage;

Fig. 6 is a simplified electric schematic of a second exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage;

Fig. 7 is a simplified electric schematic of a third exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage;

Fig. 8 is a simplified electric schematic of a fourth exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage;

Fig. 9 is a simplified electric schematic of an AC and noise equivalent circuit of Figure 5;

Fig. 10 is a simplified electric schematic of an AC and noise equivalent circuit of Fig. 7;

Fig. 11 is a simplified schematic illustration of the distortion due to the diodes network;

Fig. 12 is a simplified illustration of an Electret Condenser Microphone (ECM) ultra-low-noise ultra-low-power microphone with a feedback from the source gate;

Fig. 13 is a simplified illustration of an Electret Condenser Microphone (ECM) ultra-low-noise ultra-low-power microphone with a feedback from the drain gate;

Fig. 14 is a simplified illustration of a Micro Electrical Mechanical System Microphone (MEMS) ultra-low-noise ultra-low-power microphone with a feedback from the source gate;

Fig. 15 is a simplified illustration of a Micro Electrical Mechanical System Microphone ultra-low-noise ultra-low-power microphone with a feedback from the drain gate;

Fig. 16 is a simplified illustration of an ECM Adaptive-SNR ultra-low-power ultra-low-noise with no current feedback;

Fig. 17 is a simplified illustration of a MEMS microphone Adaptive-SNR ultra-low-power ultra-low-noise - with no current feedback; and

Fig. 18 is a simplified electric schematic of a circuit generating ultra-low-noise biasing voltage VBB.

DETAILED DESCRIPTION

The invention in embodiments thereof comprises systems and methods for an adaptive-SNR ultra-low-power and an ultra-low-noise microphone buffer. The principles and operation of the devices and methods according to the several exemplary embodiments presented herein may be better understood with reference to the following drawings and accompanying description.

Before explaining at least one embodiment in detail, it is to be understood that the embodiments are not limited in its application to the details of construction and the arrangement of the components set forth in the following description or illustrated in the

drawings. Other embodiments may be practiced or carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein is for the purpose of description and should not be regarded as limiting.

In this document, an element of a drawing that is not described within the scope of the drawing and is labeled with a numeral that has been described in a previous drawing has the same use and description as in the previous drawings. Similarly, an element that is identified in the text by a numeral that does not appear in the drawing described by the text, has the same use and description as in the previous drawings where it was described.

The drawings in this document may not be to any scale. Different figures may use different scales and different scales can be used even within the same drawing, for example different scales for different views of the same object or different scales for the two adjacent objects.

The purpose of embodiments described below is to provide at least one system and/or method for ultra-low-power and an ultra-low-noise microphone, and/or a buffer circuit for a microphone, having adaptive signal-to-noise ratio (SNR). More particularly, but not exclusively, the microphone buffer may be used with battery-operated devices that have relatively long time operating in standby mode, and/or where immediate wakeup procedure is required. However, the systems and/or methods as described herein may have other embodiments in similar technologies of local area communication.

Fig. 1 is a simplified block-diagram of a wakeup receiver implementation, according to one exemplary embodiment.

As shown in Fig. 1, signal supply 1001 may be connected to level 1 signal detection module, 1003 for detection of signal presence 1011 in a particular bandwidth. If such signal exist, signal 1005 may turn on a signature and/or valid marker detection circuit 1006, which may consume more power. If the marker is valid, signal 1009 may switch on the transceiver power supply 1007, turning on the transceiver 1010. Alternatively, the wakeup receiver may periodically turn on the signal detection power supply using signal 1002. At that time the signal 1011 presence testing is done.

Implementing a periodically turn-on wakeup receiver, as shown and described with reference to Fig. 1, and common with Bluetooth low energy (BLE), may cause a delayed response of the transceiver, and consume a lot of power. For example, a BLE-based

transceiver using a CR2032 battery may last only 8-14 months. The CR2032 battery may be too big for devices, such as glasses, buttons (Used with pens or shirts), toothbrush, etc. Moreover, as the ISM band is highly populated, the number of false alarm may be too high, even if an envelope detector is implemented. It would not be easy to implement an effective bandwidth signal presence envelope detector.

Acoustic communication may enable a device to work for several years using a battery much smaller than the CR2032 (a 235mah battery). Particularly by using the bandwidth between 14000 Hz and 20000 Hz, particularly if this 6000Hz band is divided into sub-bands of, for example, 500Hz each. Power consumed by acoustic communication may be 2000 times smaller compared with RF communication.

A signal transducer converting acoustic signal to electrical signal is, for example, a microphone. A common microphone may consume 17-500 μ A. A highly efficient 17 μ A microphone may consume a 1.47mAh battery in about 90 hours. The 1.47mAh battery is calculated for a battery size of 2.5mmX2.5mmX1mm using the technology of the common CR2032 battery (having diameter of 20mm and thickness of 3mm).

Moreover, a common microphone may have signal-to-noise ratio (SNR) of about 68dB, which limits the communication range. Therefore there is a need to have extremely low power wakeup receiver consuming 50-100 nWatt. Using a 3V battery, 50-100 nWatt is translated to 17nA-33nA, enabling 10 years of operation.

Fig. 2 is a simplified flow chart that describes the state machine of a transceiver, according to one exemplary embodiment.

As shown in Fig. 2, a first state 2001 an acoustic signal may be searched using ultra-low-power microphone, and ultra-low-power signal detection circuit, which may consume about 50nWatt by a using low-frequency acoustic signal.

When the presence of an acoustic signal is detected 2005, the state machine transits to the check preamble/marker/beacon state 2002. If a false alarm 2006 is determined, the state machine transits to the switch-off state 2004, sending a switch-off signal 2009, and returns to the first state 2001. If the preamble/marker/beacon is valid 2007, the acoustic transceiver is turned on (wakeup), and the state machine transits to the wakeup state 2003, where the transceiver performs the required operation.

Acoustic-based transceivers, such as for IoT or IoE applications, may not be content-based transceivers, and may need to work 'on-demand' only. Therefore, most of the time such transceivers may be in standby state 2001 of Fig. 2.

Microphones are important as an input device for acoustic/audio waves for the increasing market of the smartphones/tablets/cellphones, requiring higher SNR for better acoustic echo canceling, and better audio quality. Such microphones also require extremely low-power to enable hands-free acoustic/audio activation, such as the android "OK Google".

Moreover, for the IoT IoE devices microphones are important as an 'antenna', converting the acoustic communication signal to electrical signal. Such devices require many years of battery-based operation, and thus have to consume less than 50 nWatt. To enable a large communication range, such microphones require SNR better than 70db. For example, enabling communication range up to 20-30 meters using 96dB SPL signal.

Analysis of prior art microphones SNR

Fig. 3 is a simplified electric schematic of a microphone element connected to a microphone buffer based on a JFET transistor, according to one exemplary embodiment.

Fig. 3 describes a microphone element 3001, described here as a source of signal, usually coupled to the microphone buffer 3009 via a coupling capacitor 3002. The microphone buffer 3009 may include a gate bias resistor RG 3003, active element 3005 such as a JFET or a MOSFET transistor, a load resistor RD 3004 and a power supply VCC 3006. The output is coupled via a coupling capacitor.

The buffer 3009, may be used to transfer the signal from the acoustic transducer source 3001, showing a low capacitance at the input 3009, and low output impedance at the output 3010

Noise gain analysis of prior art buffer

The following analysis may be suitable for any kind of microphone including, but not limited to, an Electret Condenser Microphone (ECM), and a Micro Electronic Mechanical Systems (MEMS) microphone.

Fig. 4 is a simplified electric schematic of an AC-equivalent circuit for noise/gain analysis of the circuit of Fig. 3, according to one exemplary embodiment.

We assume that the active element 3005, JFET of Fig. 3 is in saturation mode i.e. where we get gain. As described by Fig. 4, there are a few noise sources for the circuit of Fig. 3

RG: Thermal noise from RG 4003, described by a serial voltage source 4004 and the noise is given by:

Eq. 1 $V_{n,RG}^2 = 4KTR_G\Delta f$, where K is the Boltzmann constant and T is temperature in Kelvin degrees.

RD: Thermal noise from RD 4009, described by a serial voltage source 4004 and the noise is given by:

Eq. 2 $V_{n,RD}^2 = 4KTR_D\Delta f$ where K is the Boltzmann constant and T is temperature in Kelvin degrees.

Current noise in the drain source.

Here we may neglect the 1/f noise, which appears at very low frequencies, the drain source current noise is given by:

$$\text{Eq. 3 } i_{n,d}^2 = \frac{8}{3}KTg_m\Delta f$$

Current noise from the gate 4006 and is given by:

$$\text{Eq. 4 } i_{n,d}^2 = 2I_Sq\Delta f$$

The noise in microphones may be calculated by considering an A-weighted filter 4013. A-weighted filter 4013 may simulate the human ear's frequency response, and may be given by Eq. 5.

$$\text{Eq. 5 } A(f) = 10^{(2/20)} \frac{12200^2 f^4}{(f^2 + 20.6^2)(f^2 + 12200^2)\sqrt{(f^2 + 107.7^2)(f^2 + 739.7^2)}}$$

Vout 4010 is given by:

$$\text{Eq. 6 } v_{out} = -g_m v_{in} \left(\frac{j\omega R_G C}{1 + j\omega R_G C} \right) R_D$$

Vn,out denotes the output of the filter 4014, and is given by:

$$\begin{aligned}
 \text{Eq. 7 } v_{n,out}(f)\sqrt{\Delta f} - g_m \sqrt{4KTR_G \Delta f} \left(\frac{1}{1 + j\omega R_G C} \right) R_D A(f) - \\
 - g_m \sqrt{2I_S q \Delta f} \left(\frac{R_G}{1 + j\omega R_G C} \right) R_D A(f) + \\
 + R_D \sqrt{\frac{8}{3} KT g_m \Delta f} A(f) + \sqrt{4KTR_D \Delta f} A(f)
 \end{aligned}$$

where $\omega = 2\pi f$ assuming $\omega R_G C \gg 1$ in Eq. 6 and Eq. 7 becomes

$$\text{Eq. 8 } v_{out} = -g_m v_{in} R_D$$

$$\begin{aligned}
 \text{Eq. 9 } v_{n,out}(f)\sqrt{\Delta f} \approx -g_m \sqrt{4KTR_G \Delta f} \left(\frac{1}{j2\pi f R_G C} \right) R_D A(f) - \\
 - g_m \sqrt{2I_S q \Delta f} \left(\frac{1}{j2\pi f C} \right) R_D A(f) + R_D \sqrt{\frac{8}{3} KT g_m \Delta f} A(f) + \sqrt{4KTR_D \Delta f} A(f)
 \end{aligned}$$

To find the Root Mean Square noise, one should add the RMS noise elements in a Δf bandwidth (Δf denotes a small bandwidth) on $f_1=0\text{Hz}$ to $f_2=20000\text{Hz}$ or

$$\begin{aligned}
 \text{Eq. 10 } v_{n,out}^2 &= \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df \\
 &= g_m^2 4KTR_D^2 \left(\frac{1}{4\pi^2 R_G C^2} \right) \int_{f_1}^{f_2} \frac{|A(f)|^2}{f^2} df + g_m^2 2I_S q R_D^2 \left(\frac{1}{4\pi^2 C^2} \right) \int_{f_1}^{f_2} \frac{|A(f)|^2}{f^2} df + \\
 &\quad \frac{8}{3} KT g_m R_D^2 \int_{f_1}^{f_2} |A(f)|^2 df + 4KTR_D \int_{f_1}^{f_2} |A(f)|^2 df
 \end{aligned}$$

Or if

$$\text{Eq. 11 } \xi_1 = \int_{f_1}^{f_2} \frac{|A(f)|^2}{f^2} df, \xi_2 = \int_{f_1}^{f_2} |A(f)|^2 df \text{ then}$$

$$\text{Eq. 12 } v_{n,out}^2 = \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df =$$

$$= g_m^2 4KTR_D^2 \left(\frac{1}{4\pi^2 R_G C^2} \right) \xi_1 + g_m^2 2I_S q R_D^2 \left(\frac{1}{4\pi^2 C^2} \right) \xi_1 + \frac{8}{3} K T g_m R_D^2 \xi_2 + 4KTR_D \Delta f \xi_2$$

For $f_1=0\text{Hz}$, $f_2=20000\text{Hz}$ one can show using Eq. 5 that

$$\text{Eq. 13 } \xi_1 = 0.0026, \xi_2 = 12474$$

As the gain is defined by $G = g_m R_D$ then Eq. 12 may be written as

$$\begin{aligned} \text{Eq. 14 } v_{n,out}^2 &= \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df = \\ &= G^2 4KT \left(\frac{1}{4\pi^2 R_G C^2} \right) \xi_1 + G^2 2I_S q \left(\frac{1}{4\pi^2 C^2} \right) \xi_1 + G \frac{8}{3} KTR_D \xi_2 + 4KTR_D \xi_2 \end{aligned}$$

and the noise equivalent at the input is

$$\begin{aligned} \text{Eq. 15 } v_{n,in}^2 &= \frac{v_{n,out}^2}{G^2} = \frac{1}{G^2} \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df = \\ &= 4KT \left(\frac{1}{4\pi^2 R_G C^2} \right) \xi_1 + 2I_S q \left(\frac{1}{4\pi^2 C^2} \right) \xi_1 + \frac{8}{3G} KTR_D \xi_2 + \frac{4KTR_D \xi_2}{G^2} \end{aligned}$$

Analysis of noise terms

For $4KT \left(\frac{1}{4\pi^2 R_G C^2} \right) \xi_1$ it is clear that having large C and large R_G will decrease

the noise, however for ECM or MEMS microphones $C=5\text{pf}-10\text{pF}$ In This kind of microphones SNR is limited in the range of 58dB-67dB this may be due to the small size R_G , which is usually in the range of 25M Ω -100 M Ω for a common microphone (we assume $R_G=100\text{M } \Omega$.)

$$\text{Eq. 16A } \sqrt{4KT \left(\frac{1}{4\pi^2 R_G C^2} \right) \xi_1} = 10.4\mu\text{v}$$

Increasing RG to 1G will give a noise of about 3uv for RG=1G and microphone sensitivity of -38dBv =12.6mV the reflected (not taking into account other terms) SNR

from this noise is $20 \log_{10} \left(\frac{12.6mv / \sqrt{2}}{3uv} \right) = 69.45dB$.

Table 1 and table 1A summarizes the A-weighted noise and SNR for various C & RG values.

Table 1: Equivalent A-weighted noise at the input induced by Rg for various Rg and C values

C/Rg	5pF	10pF	30pF	56pF	100pF
25MOhm	41.77 μV	20.89μV	6.96μV	37.3μV	2.09μV
100MOhm	20.89μV	10.44μV	3.48μV	18.6μV	1.04μV
1GOhm	6.6μV	3.3μV	1.1μV	5.9μV	0.33μV
10GOhm	2.09μV	1.04μV	0.35μV	1.9μV	0.1μV

Table 1A: SNR with A weighted noise at the input induced by Rg for various Rg and C values.

C/Rg	5pf	10pf	30pf	56pf	100pf
25MOhm	46.6[dB]	52.6[dB]	62.16[dB]	67.6[dB]	72.6[dB]
100MOhm	52.6[dB]	58.6[dB]	68.16[dB]	73.6[dB]	78.6[dB]
1GOhm	62.6[dB]	68.6[dB]	78.16[dB]	83.6[dB]	88.6[dB]
10GOhm	72.6[dB]	78.6[dB]	88.16[dB]	93.6[dB]	98.6[dB]

For $2I_s q \left(\frac{1}{4\pi^2 C^2} \right) \xi_1$ where Is, 4012 is the leakage current, it is clear that having smaller leakage current will decrease the noise from the JFET hate leakage current, C again is 5pf-10pf, for Is=1000pa one get:

Eq. 16B $\sqrt{2I_s q \left(\frac{1}{4\pi^2 C^2} \right) \xi_1} = 14.5uv$

and for $I_s=1\text{pA}$ one gets $0.46\mu\text{V}$ and for $I_s=0.2\text{pA}$ one gets $0.21\mu\text{V}$ for microphone with $-38\text{dBV}=12.6\text{mV}$ sensitivity and $I_S=1000\text{pA}$, 1pA and 0.2pA .

$$\text{The reflected SNR is: } I_s=1000\text{pa} \rightarrow 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{14.5\text{uv}} \right) = 55\text{dB}$$

$$I_s=1\text{pa} \rightarrow 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.46\text{uv}} \right) = 85\text{dB}$$

$$I_s=0.2\text{pA} \rightarrow 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.21\text{uv}} \right) = 92.6\text{dB}$$

Table 2 and table 2A summarizes the input equivalent a weighted noise and the associated SNR for -38dBV sensitivity:

Table 2: Equivalent A weighted noise at the input induced by JFET leakage noise current for different leakage and C values.

C/ I_s	5pf	10pf	30pf	56pf	100pf
1000pA	29.03 μV	14.52 μV	4.84 μV	2.59 μV	1.45 μV
100pA	9.18 μV	4.59 μV	1.53 μV	0.82 μV	0.46 μV
2pA	1.3 μV	0.65 μV	0.22 μV	0.12 μV	0.06 μV
1pA	0.92 μV	0.46 μV	0.15 μV	0.08 μV	0.05 μV

Table 2A: SNR with A weighted noise at the input induced by JFET leakage noise current for different leakage and C values

C/ R_g	5pf	10pf	30pf	56pf	100pf
1000pA	49.74[dB]	55.76[dB]	65.30[dB]	70.72[dB]	75.76[dB]
100pA	59.74[dB]	65.76[dB]	75.30[dB]	80.72[dB]	85.76[dB]
2pA	76.3[dB]	82.75[dB]	92.30[dB]	97.71[dB]	102.75[dB]
1pA	79.74[dB]	85.76[dB]	95.30[dB]	100.72[dB]	105.76[dB]

For other two terms $\frac{8}{3G}KTR_D\xi_2$ and $\frac{4KTR_D\xi_2}{G^2}$ we assume a JFET with

IDSS=0.5mA, $V_p=-1V$, and $R_D=1000\text{ Ohm}$, which are typical values (here we neglected the C_{gs} that gives attenuation at the input by 2 and therefore usually one selects $R_D=2000\text{ Ohm}$).

Using these values it is clear that

$$g_m = \frac{2}{V_p} \sqrt{I_D I_{DSS}} = \frac{2I_{DSS}}{V_p} \{ \text{at } V_{GS} = 0 \} = 0.001(\text{ohm})^{-1} \text{ and } G = g_m R_D = 1$$

For $\frac{8}{3G}KTR_D\xi_2$ it is clear that smaller R_D will decrease the noise as well as larger

G. This is possible by increasing the current, for typical ECM or MEMS microphones.

$$\text{Eq. 16C} \quad \sqrt{\frac{8}{3G}KTR_D\xi_2} = 0.37\mu\text{v}$$

And for $-38\text{dBv}=12.6\text{mV}$ microphone the reflected SNR here

$$\text{is } 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.37\mu\text{v}} \right) = 87.6\text{dB}.$$

This number may be easily increased by lowering R_D , by using enlarged IDSS JFET, for example by using JFET with IDSS=5ma we can use $R_D=100\text{ohm}$ and in this

$$\text{case the SNR will be } 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.123\mu\text{v}} \right) = 97.2\text{dB}$$

For $\frac{4KTR_D\xi_2}{G^2}$ it is clear that decreasing R_D and increasing G will decrease this

term, for typical ECM and/or MEMS microphones we have:

$$\text{Eq. 16D} \quad \sqrt{\frac{4KTR_D\xi_2}{G^2}} = 0.45\mu\text{v}$$

Which for -38dBv microphone sensitivity reflects an SNR of

$$20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.45\mu\text{v}} \right) = 85.9\text{dB} \text{ as before by decreasing } R_D \text{ by 10 by using JFET with}$$

IDSS=5ma the reflected SNR would become $20 \log_{10} \left(\frac{12.6mv / \sqrt{2}}{0.45uv} \right) = 96dB$

Conclusions:

As one can see the limiting factor for the SNR is the RG, then the leakage current while the last two term are easily decreased by using JFET with larger IDSS and hence smaller RD. On the other hand C may be increased by putting a parallel to gate and source a second capacitor that may decrease the noise coming from RG 4003 and the noise due to the leakage IS 4012. The capacitor may cause attenuation that may be compensated by increasing the gm trans-conductance of the JFET 4005, by increasing the drain current.

Fig. 5, Fig. 6, Fig. 7 and Fig. 8 describe the solution for the RG problem with a possible parallel capacitor C1.

Fig. 5 is a simplified electric schematic of a first exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage, according to one exemplary embodiment.

Fig. 6 is a simplified electric schematic of a second exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage, according to one exemplary embodiment.

Fig. 7 is a simplified electric schematic of a third exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage, according to one exemplary embodiment.

Fig. 8 is a simplified electric schematic of a fourth exemplary circuit for eliminating RG in the buffer and decreasing noise due to leakage, according to one exemplary embodiment.

Circuits of Fig. 5, Fig. 6, Fig. 7 and Fig. 8 are based on a network of diodes 6012, 7012, 8012 and 9012 and capacitor C1 5011, 6011, 7011 and 8011.

Analysis of serial diodes network connection

Reference is now made to Fig. 5. Fig. 5A describes in details the diodes 5003 with the capacitor C1 5011.

Fig. 9 is a simplified electric schematic of an AC and noise equivalent circuit of Figure 5, according to one exemplary embodiment.

The noise of each diode Da(1), Da(2)...Da(p) 5003 of Fig. 5 is given by:

$$\text{Eq. 17 } i_{n, Da(k)}^2 = (2I_S + I_0)q\Delta f$$

Diode small signal resistance

The small signal diode resistance is given by:

$$\left[\frac{I_0}{\left(\frac{KT}{q}\right)} e^{\left(\frac{V_D}{\left(\frac{KT}{q}\right)}\right)} \right]^{-1} = \left(\frac{KT}{qI_0}\right) e^{-\left(\frac{V_D}{\left(\frac{KT}{q}\right)}\right)} \approx \left(\frac{KT}{qI_0}\right) \left(\frac{KT}{qV_D}\right)_{\text{For small } V_D, V_D \ll \frac{KT}{q}}$$

$$\text{If a diode with } I_0 \approx I_S \text{ is selected then } V_{D(DC)} = \frac{KT}{q} \ln(2) = 0.69 \frac{KT}{q} = 17.3\text{mv}_{\text{at } 25\text{deg}}$$

in this case the diode small signal resistance is given by $\left(\frac{KT}{2qI_S}\right)$.

It may be important to select a diode that may not have higher leakage current than the I_S . This may help reducing diode noise. And, if $I_0 \approx I_S$, then the DC voltage on the diode may be small, such that connecting 10-20 diodes in series may not create a high voltage drop on the diodes.

Diode current noise calculation and reduction

The reason for connecting diodes in series is to reduce the distortion resulting from the diodes. First we show that connecting a diodes in series reduces the total diode noise.

One can transform the diodes 5003, circuit of Fig. 5A using the Thevenin theorem and get the following total current with the following total resistance.

Eq.

18

$$i_{n,diodes} = \frac{\sqrt{(2I_S + I_0)q\Delta f \left(\frac{KT}{2qI_S}\right)^2 + (2I_S + I_0)q\Delta f \left(\frac{KT}{2qI_S}\right)^2 + \dots + (2I_S + I_0)q\Delta f \left(\frac{KT}{2qI_S}\right)^2}}{p \left(\frac{KT}{2qI_S}\right)} =$$

$$= \frac{\sqrt{(2I_S + I_0)q\Delta f}}{\sqrt{p}}$$

And the total resistance is $p \left(\frac{KT}{2qI_S}\right)$, which does not give any thermal noise, as it is just the slope of the diode current, having C1.

The total current noise is the square sum of the diode noise and the gate leakage noise 5014a, and is given by:

$$\text{Eq. 19 } i_{n,diodes+jfet}^2 = \frac{(2I_S + I_0)q\Delta f}{p} + 2I_S q\Delta f \approx 2I_S q\Delta f \text{ for } p \geq 10$$

We can conclude that Eq. 15 now will take the form:

$$v_{n,in}^2 = \frac{v_{n,out}^2}{G^2} = \frac{1}{G^2} \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df$$

$$\text{Eq. 20 } = 2I_S q \left(\frac{1}{4\pi^2 (C + C_1)^2} \right) \xi_1 + \frac{8}{3G} KTR_D \xi_2 \left[\frac{(C + C_1)}{C} \right]^2 +$$

$$+ \frac{4KTR_D \xi_2}{G^2} \left[\frac{(C + C_1)}{C} \right]^2$$

One can see from equation 20 that C1 helps reducing the current noise from the PN junction of the JFET and the diode noise. Also, connecting diodes in series helps with reducing the diode current noise. The noise from the JFET current at the output 5007a and the noise from RD at the output 5010a is reflected to the input by a factor greater than 1

$\left[\frac{(C + C_1)}{C} \right]^2$. For 1pA leakage current we had $I_S = 1\text{pA} \rightarrow 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.46\text{uv}} \right) = 85\text{dB}$. It

is possible to increase this term by 10dB by adding $C_1 = 2C$. This requires that G compensates the $\left[\frac{(C + C_1)}{C} \right]^2$. Therefore it requires that $G = 10$, still having $R_D = 100\text{ohm}$,

which requires gm=0.1, or Id=100ma. This is possible when using JFET with IDSS=100mA.

Distortion analysis

The equation of a diode is given by:

$$\begin{aligned}
 \text{Eq. 21} \quad I_D &= I_0 \left(e^{\left(\frac{V_D}{\left(\frac{KT}{q}\right)}\right)} - 1 \right) = I_0 \left(\left(\frac{V_D}{V_T}\right) + \frac{1}{2!} \left(\frac{V_D}{V_T}\right)^2 + \frac{1}{3!} \left(\frac{V_D}{V_T}\right)^3 + \frac{1}{4!} \left(\frac{V_D}{V_T}\right)^4 + \dots \right) \\
 &= I_0 \left((x) + \frac{1}{2!} (x)^2 + \frac{1}{3!} (x)^3 + \frac{1}{4!} (x)^4 + \dots \right) \text{ where } V_T = \frac{KT}{q} \text{ and } x = \frac{V_D}{V_T}
 \end{aligned}$$

It is clear that for 1pA-10pA the impedance of a diode is about 25mV/(2*1e-12)=12.5GOhm, which means that all Von will be developed if we have C=10pF 5002a at even low frequencies like 100Hz. Also, it is known that the voltage on a microphone acoustic element is about its sensitivity, which is about 12mV. This means that 12mV/25mc=x=0.5 will generate relatively high distortion. By adding several diodes the Vin voltage may be divided over all the diodes, and hence by having for example p=25 we have x=0.5mv/25mv=1/50. This means that the next that the distortion will come

from $\frac{1}{2!} \left(\frac{V_D}{V_T}\right)^2$, as

$$\frac{1}{2!} \left(\frac{V_D}{V_T}\right)^2 = \frac{1}{2!} \left(\frac{V_D(dc) + Vin/P}{V_T}\right)^2 = \frac{1}{2!} \left(\frac{V_D(dc)}{V_T} + 2 \frac{V_D(dc)}{V_T} \frac{Vin}{P} + \left(\frac{Vin/P}{V_T}\right)^2\right)$$

Therefore showing that the distortion current is $I_0 \frac{1}{2!} \left(\frac{Vin/P}{V_T}\right)^2$ for I0=10pA,

C=10pf and f=100Hz, p=1.

The maximum sensitivity of the distortion voltage may therefore be:

Analysis of serial diodes network connection of Figs. 7 and 8.

Reference is now made to Fig. 7 and Fig. 7A describes in details the diodes 7003, 7013 with the capacitor C1 7011.

Fig. 10 is a simplified electric schematic of an AC and noise equivalent circuit of Fig. 7, according to one exemplary embodiment.

As shown in Fig. 7, a dual branch network of p diodes per each network is connected between the gate (input) and ground, typically including a first network 7003 and a second network 7013. If $V_{gs}=V$ then each diode of the first network 7003 gets a voltage of V/p while each diode of the second network gets $-V/p$.

As V is very small, the current flowing on the first network is equal to about $I_0 \left((V/p) + \frac{1}{2!} (V/p)^2 + \frac{1}{3!} (V/p)^3 + \frac{1}{4!} (V/p)^4 \dots \right)$ and for the second network 7013 $-I_0 \left((V/p) - \frac{1}{2!} (V/p)^2 + \frac{1}{3!} (V/p)^3 - \frac{1}{4!} (V/p)^4 \dots \right)$ with V/p is the voltage across $Da(1), Da(2) \dots Da(p)$ the first diode branch 7015a and $-V/p$ is the voltage across $Db(1), Db(2) \dots Db(p)$ the second diode branch 7017a.

Part of the JFET leakage is 7003a may flow through the first branch 7015a and another part may flow through the second branch 7017a

The noise of each diode $Da(1), Da(2) \dots Da(p)$ 7003 of Fig. 7 is given by:

Eq. 22 $i_{n, Da(k)}^2 = (2\alpha I_S + I_0) q \Delta f$ where αI_S is the current flowing into the first diode branch from the JFET leakage.

The reason for connecting diodes in series is reducing the distortion. The input voltage V may be divided by P for each diode as well as reducing the noise resulting from the diode noise current. First we show that connecting diodes in series reduces the total diode noise.

One can transform the diodes of branch 7003 of the circuit of Fig. 7A using the Thevenin theorem and get the following total current with the following total resistance

Eq. 22 $i_{n,diodes} =$

$$= \frac{\sqrt{(2\alpha I_S + I_0)q\Delta f \left(\frac{2KT}{qI_0} e^{-\frac{V_D}{KT}} \right)^2 + (2\alpha I_S + I_0)q\Delta f \left(\frac{2KT}{qI_0} e^{-\frac{V_D}{KT}} \right)^2 + \dots + (2\alpha I_S + I_0)q\Delta f \left(\frac{2KT}{qI_0} e^{-\frac{V_D}{KT}} \right)^2}{p \left(\frac{2KT}{qI_0} e^{-\frac{V_D}{KT}} \right)^2} =$$

$$= \frac{\sqrt{(2\alpha I_S + I_0)q\Delta f}}{\sqrt{p}}$$

And the total resistance is $p \left(\frac{2KT}{qI_0} e^{-\frac{V_D}{KT}} \right)$, which does not give any thermal noise

as it is just the slope of the diode current, having C1. The same applies to the second diode network 7013.

The total current noise is the square sum of the first diode branch current noise the second diode branch current noise and the gate leakage noise 5014a and is given by:

$$\text{Eq. 23 } i_{n,diodes+jfet}^2 = \frac{(2\alpha I_S + I_0)q\Delta f}{p} + \frac{(2(1-\alpha)I_S + I_0)q\Delta f}{p} + 2I_S q\Delta f =$$

$$= \frac{(2I_S + 2I_0)q\Delta f}{p} + 2I_S q\Delta f \approx 2I_S q\Delta f \text{ for } p \geq 10$$

We can conclude that Eq. 15 now will take the form

$$\text{Eq. 24 } v_{n,in}^2 = \frac{v_{n,out}^2}{G^2} = \frac{1}{G^2} \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df$$

$$= 2I_S q \left(\frac{1}{4\pi^2 (C + C_1)^2} \right) \xi_1 + \frac{8}{3G} KTR_D \xi_2 \left[\frac{(C + C_1)}{C} \right]^2 + \frac{4KTR_D \xi_2}{G^2} \left[\frac{(C + C_1)}{C} \right]^2$$

One can see from equation 24 that C1 helps reducing the current noise from the PN junction of the JFET and the diode noise. Connecting diodes in series also helps reducing the diode current noise. The noise from the JFET current at the output 5007a and the noise

from RD at the output 5010a may be reflected to the input by a factor greater than 1

$$\left[\frac{(C+C_1)}{C} \right]^2$$

For 1pA leakage current we had $I_s=1\text{pa} \rightarrow 20 \log_{10} \left(\frac{12.6\text{mv} / \sqrt{2}}{0.46\text{uv}} \right) = 85\text{dB}$. It is therefore possible to increase this term by 10dB by adding $C_1=2C$. This requires that G may compensate the $\left[\frac{(C+C_1)}{C} \right]^2$ requiring that $G=10$. Having $R_d=100\text{ohm}$ requires $g_m=0.1$, or $I_d=100\text{ma}$, which is possible using JFET with $I_{DSS}=100\text{mA}$.

Distortion analysis

The equation of a diode is given by:

$$\begin{aligned} \text{Eq. 25 } I_D &= I_0 \left(e^{\left(\frac{V_D}{\left(\frac{KT}{q} \right)} \right)} - 1 \right) = \\ &= I_0 \left(\left(\frac{V_D}{V_T} \right) + \frac{1}{2!} \left(\frac{V_D}{V_T} \right)^2 + \frac{1}{3!} \left(\frac{V_D}{V_T} \right)^3 + \frac{1}{4!} \left(\frac{V_D}{V_T} \right)^4 \dots \right) = \\ &= I_0 \left((x) + \frac{1}{2!} (x)^2 + \frac{1}{3!} (x)^3 + \frac{1}{4!} (x)^4 \dots \right) \text{ where } V_T = \frac{KT}{q} \text{ and } x = \frac{V_D}{V_T} \end{aligned}$$

At DC the first diode branch 7003 may force a positive voltage across the diode branch. This may appear to the second diode branch 7013 as a negative voltage. To find this voltage one can write.

$$\text{Eq. 26 } I_s = I_0 \left(e^{\left(\frac{V_D}{\left(\frac{KT}{q} \right)} \right)} - 1 \right) - I_0 \left(e^{\left(\frac{V_D}{\left(\frac{KT}{q} \right)} \right)} - 1 \right)$$

$$\text{mark } x = e^{\left(\frac{V_D}{\left(\frac{KT}{q} \right)} \right)} \text{ solve } \frac{I_s}{I_0} = x - 1 - \frac{1}{x} + 1 \text{ if } \frac{I_s}{I_0} = 1$$

Meaning that the diode may have leakage in the same order as JFET. This will result at 25 degrees with $x=1.618$ and $V_D = 12mv$.

As each diode in the first branch 7003 gets V/p and on the second branch 7013 gets $-V/p$ and the current for both branches is the subtraction of the currents between branch 7003 and 7013.

Then the diode on the first branch 7003 would have $12mV+V/p$ and on the second branch $-12mV-V/p$, where, as explained above, the $12mV$ results from the leakage I_s 7013 flowing from the transistor Q 7005 to the diodes on branch 7003.

Eq. 27 gives the current difference between the branches 7003, 7013

$$\begin{aligned}
 \text{Eq. 27 } I_{on_diode_branches_7003_7013} &= \\
 &= I_0 \left((x) + \frac{1}{2!}(x)^2 + \frac{1}{3!}(x)^3 + \frac{1}{4!}(x)^4 \dots \right) - I_0 \left((-x) + \frac{1}{2!}(x)^2 + \frac{1}{3!}(-x)^3 + \frac{1}{4!}(x)^4 \dots \right) \\
 \text{where } V_T &= \frac{KT}{q} \text{ and } x = \frac{V/p + 12mv}{V_T} = 2I_0 \left((x) + \frac{1}{3!}(x)^3 \dots \right) = \\
 &= 2I_0 \left(\left(\frac{V/p}{V_T} \right) + \frac{1}{3!} \left(\frac{12mv}{V_T} \right)^3 \left(1 + 3 \left(\frac{V/p}{12mv} \right)^2 + 3 \left(\frac{V/p}{12mv} \right) + \left(\frac{V/p}{12mv} \right)^3 \right) \dots \right)
 \end{aligned}$$

If we have $C=10pf$ 7002a at even low frequencies like 100Hz, It is clear that for $1pa-10pa$ the impedance of a diode is about $25mv/(2*1e-12)=12.5Gohm$, which means that all Vin will be developed on the input.

The distortion voltage at the input would come from the voltage drop on C and from the distortion elements described by Eq. 27.

For Very small V/p (Assuming microphone acoustic element is about its sensitivity which is about $12mV$ this means that $12mV/10=1.2mV$).

$$\text{The term } 3 \left(\frac{V/p}{12mv} \right)^2 \frac{1}{3!} \left(\frac{12mv}{V_T} \right)^3 = 2I_0 \frac{1}{2} \left(\frac{V/p}{1} \right)^2 \left(\frac{12mv}{V_T} \right) \approx I_s \left(\frac{V/p}{1} \right)^2 \left(\frac{12mv}{V_T} \right)$$

generates the distortion.

Fig. 11 is a simplified schematic illustration of the distortion due to the diodes network, according to one exemplary embodiment.

One can show that the distortion is given by

Eq. 28 $I_s \left(\frac{V_{in}/p}{1} \right)^2 \left(\frac{12mv}{V_T} \right) \left(\frac{1}{j\omega C} \right)$ and therefore in dB we have

Eq. 29 $Distotion[dB] = 20 \log 10 \left[\frac{I_s \left(\frac{V_{in}/p}{1} \right)^2 \left(\frac{12mv}{V_T} \right) \left(\frac{1}{\omega C} \right)}{V_{in}} \right]$.

Eq. 29, shows that putting series of diodes will decrease the distortion

For a current of 2pA, 10pF, p=1, and Vin=12mV, f=100 (at sensitivity level) we have distortion of 23nV. In audio this may be acceptable.

Distortion source

For low Is leakage of 1pA-10pA, with a single diode, the impedance of the diode will be 2500MOhm-25GOhm (with 10pA) at 100Hz, and C 7002a of 10pF, we have the impedance of 100MOhm. This will give a voltage of 1/25 from the input and for one diode this would mean that for maximal sensitivity the distortion would be 1/25*1/8, which is pretty high. With a p diodes in series and parallel branches 7003 and 7013 we have for maximal sensitivity – assuming p=10 – 1/25*1/6*(1.2/25).^3=1/1.3M, which reflects Distortion of more than 120dB.

Reason for diodes in series

There are two reasons for connecting diodes in series in each branch 7003 and 7013. The first reason is based on Eq. 22, as this connection reduces the current noise from the diode total noise current. The second reason is to divide the voltage across each diode such that the term (V/p)/25mv will be small enough.

Reason for parallel branches

Parallel branches eliminate the even distortion components, as shown by equation 26.

Adaptive-SNR ultra-low-power low noise microphone circuit

Fig. 12, Fig. 13, Fig. 14 and Fig. 15 describe an ultra-low-noise and ultra-low-power microphone circuits.

Fig. 12 is a simplified illustration of an Electret Condenser Microphone (ECM) ultra-low-noise ultra-low-power microphone with a feedback from the source gate, according to one exemplary embodiment.

Fig. 13 is a simplified illustration of an Electret Condenser Microphone (ECM) ultra-low-noise ultra-low-power microphone with a feedback from the drain gate, according to one exemplary embodiment.

Fig. 14 is a simplified illustration of a Micro Electrical Mechanical System Microphone (MEMS) ultra-low-noise ultra-low-power microphone with a feedback from the source gate, according to one exemplary embodiment.

Fig. 15 is a simplified illustration of a Micro Electrical Mechanical System Microphone ultra-low-noise ultra-low-power microphone with a feedback from the drain gate, according to one exemplary embodiment.

Fig. 16 is a simplified illustration of an ECM Adaptive-SNR ultra-low-power ultra-low-noise with no current feedback, according to one exemplary embodiment.

Fig. 17 is a simplified illustration of a MEMS microphone Adaptive-SNR ultra-low-power ultra-low-noise - with no current feedback, according to one exemplary embodiment.

Fig. 12 shows an adaptive-SNR ultra-low-power ultra-low-noise microphone. This microphone circuit may provide the minimum required power for the required 10021 SNR. The low noise part is achieved by using a diode based input impedance 10002, as described by Fig. 5, Fig. 6, Fig.7 and Fig. 8. The input impedance may include a parallel capacitor C1 described as 5011, 6011, 7011 and 8011 in Fig. 5, Fig. 6, Fig. 7 and Fig. 8, respectively.

To get the low power performance a wide JFET transistors is used in which the IDSS current is high. Eq. 30 describes the relation between V_{GS} and I_D of the JFET 1009, of Fig. 10.

$$\text{Eq. 30 } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \Rightarrow g_m = -\frac{2}{V_P} \sqrt{I_D I_{DSS}}$$

Recall from equation 24 given here as:

$$\begin{aligned}
 \text{Eq. 31 } v_{n,in}^2 &= \frac{v_{n,out}^2}{G^2} = \frac{1}{G^2} \int_{f_1}^{f_2} |v_{n,out}(f)|^2 df \\
 &= 2I_s q \left(\frac{1}{4\pi^2 (C + C_1)^2} \right) \xi_1 + \frac{8}{3G} KTR_D \xi_2 \left[\frac{(C + C_1)}{C} \right]^2 + \\
 &\quad + \frac{4KTR_D \xi_2}{G^2} \left[\frac{(C + C_1)}{C} \right]^2
 \end{aligned}$$

The reflected noise at the input may include three elements. The first element is $2I_s q \left(\frac{1}{4\pi^2 (C + C_1)^2} \right) \xi_1$ from the PN junction of the JFET 10009 combined with the current noise of the input impedance leakage current diodes 10002. The second element is $\frac{8}{3G} KTR_D \xi_2 \left[\frac{(C + C_1)}{C} \right]^2$ resulting from the JFET 10009 current noise between drain (D) and source (S). The third element is $\frac{4KTR_D \xi_2}{G^2} \left[\frac{(C + C_1)}{C} \right]$ resulting from the (RD) load resistor 10006.

The first element may be decreased using C1 5011, 6011, 7011 and 8011 in the input impedance, and may also be reduced by using JFET with ultra-low leakage. The second and third elements may be decreased by increasing the gain G. For JFET 10009 in the saturation region we have

$$\text{Eq. 32 } G = g_m R_D$$

Therefore the second and third noise elements become:

$$\text{Eq. 33 } \frac{8}{3G} KTR_D \xi_2 \left[\frac{(C + C_1)}{C} \right]^2 = \frac{8}{3g_m} KT \xi_2 \left[\frac{(C + C_1)}{C} \right]^2$$

$$\text{Eq. 34 } \frac{4KTR_D \xi_2}{G^2} \left[\frac{(C + C_1)}{C} \right]^2 = \frac{4KT}{g_m^2 R_D} \left[\frac{(C + C_1)}{C} \right]^2$$

One can see from Eq. 33 and Eq. 34 that the second and third reflected input noise depend on gm. Therefore we may want to have a large gm. One can use a wide JFET 10009, such that IDSS is extremely high, such that to get some gm, $\frac{2}{V_P} \sqrt{I_D I_{DSS}}$ we will

need to use low I_D . For example, using a common microphone, a JFET transistor with $V_p=1V$, and $I_{DSS}=0.5mA$, with $V_{GS}=0$, will give some g_{m0} . One can use an $I_{DSS}=150\mu A$ to $300\mu A$ JFET with low leakage such as MX-16 of MOXTEK with $V_p=-8V$ with such transistor to get the same g_{m0} we need a $I_D=500\mu A/300=1.7\mu A$, in order to have the JFET in saturation region we need $V_{DS} \geq V_{GS} - V_p$ with such I_D we have:

$$\text{Eq. 35 } V_{DS} \geq V_{GS} - V_p = |V_p| \sqrt{\frac{I_D}{I_{DSS}}} = \frac{|V_p|}{300} = \frac{8}{300} = 27\text{ mV}$$

With $1.7\mu A$, we also assume about 20mV for R_S 10007 and R_D 10006 (10mV each) this would mean 92nWatt of power consumption.

The circuit of Fig. 12 includes a DC-to-DC switched capacitors voltage converter (charge pump) 10004 that receives supply voltage VCC and generates VCC_LOW, which is the voltage that drives the microphone buffer 10003. This voltage, as suggested, is about 20mV-50mV, with low total power consumption.

Voltage buffer 10003 may include an active element JFET 10009, which may be implemented using Metal Oxide Semiconductor FET (MOSFET) too. The buffer 10003 includes a load resistor R_D 10005, which is used for amplification. V_{out} 10011 is taken via coupling capacitor C_1 10010.

To set the required I_D , which insures with the VCC_LOW that JFET 10009 is in saturation mode, a current control block 10005 is added. This current control block includes an ultra-low-power comparator 10015 and two Low Pass Filters 10012 and 10013. The filters may block the noise coming from the ultra-low-power comparator. The comparator typically consumes few nano-Amperes in a very low gain bandwidth, but may have high noise at its input (a few micro Volts) and high noise at its output. LPF1 is a bi-directional low-pass-filter that may block the noise coming from the "-" input of the ultra-low-power comparator 10015, and may allow to get a sampled voltage from the R_S 10007, which transform the I_D into $I_D \cdot R_S$.

This voltage $I_D \cdot R_S$ is compared with V_{ref} 10014 and when the feedback is voltage $V_{ref} = I_D \cdot R_S$ hence $I_D = V_{ref}/R_S$, if $I_D \cdot R_S > V_{ref}$ the comparator may generate a negative voltage that is supplied to the gate of the JFET 10009 through LPF2 and the input impedance network 10002. This negative voltage may decrease the current.

At different acoustic wave pressure at some given I_d we will get different SNRs. The proposed microphone circuitry may have a control loop including an ultra-low-power envelope/energy detector 10016, LPF3 10018 and LPF4 10019 connected to the Energy/envelope detector 10016, which may generate short term average (LPF3, 10018) and long term average (LPF4 10019). The SNR is the relation between the two. The long term average may indicate the noise, while the short term average may indicate the signal. An SNR monitor circuit 10020 may analyze the long and short term averages of the envelope/energy detector 10016, and, based on the required SNR 10021, may change the V_{ref} 10014 and hence the I_d , and therefore can decrease or increase I_d based in the required SNR.

The input impedance network 10002 may include a diodes network as described by Fig. 5 5003, Fig. 6 6003, Fig. 7 7003 or Fig. 8 8003. As a very low current I_s 5015, 6015, 7015 and 8015 is flowing through the diode network, and as the leakage I_s 5015, 6015, 7015 and 8015 is the same order of the diode leakage, this may mean that each diode may have about KT/q voltage, or about 25mV, during DC.

To have high gain, a bypass capacitor CS 10008 is added in parallel to RS 10007.

The charge pump 10004 supplies two voltages: VCC_LOW to drive the microphone buffer 10003 and $-VEE$ for the ultra-low-power comparator 10015. The electret element 10001, which is a capacitor with a polarized element, may have high voltage on its terminals. This voltage may be discharged using the diode networks. An optional low resistor for low noise (50 Ohm-100 Ohm) RE 10001a may be added to allow a controlled discharge of the electrets element 10001 during manufacturing. This may limit the discharge current such that the diodes in the diode network 10002 may not be harmed. A parallel capacitor to the input impedance 10002 C1 such as 5011, 6011, 7011 & 8011 may be added in the input impedance. This C1 allows reduction of the noise due to the leakage current from the gate of the JFET 10009.

Fig. 13 is an improved version of the ultra-low-power ultra-low-noise microphone of Fig. 12. The circuit of Fig. 13 is similar to the one of Fig. 12, except for the feedback part. In the circuit of Fig. 13 there is no need for RS 10007 resistor and CS 10008 capacitor. Instead, the current to voltage is taken from the (RD) load resistor 1106, through LPF1a 1112. The purpose of LPF1a is to pass the voltage $I_d * RD$ to the comparator. Then -

Vref 1114 is added, giving a voltage of $I_d \cdot R_D - V_{ref}$ between the "-" and "+" terminals of the comparator 1115. If $I_d \cdot R_D - V_{ref} < 0$, a positive voltage is created at the output of the comparator 1115, which increases the current I_d 1107.

The advantage of the circuit of Fig. 13 is the reduction of the VCC_LOW by about the voltage on RS 10007. This may decrease the VCC_LOW, and hence may create a microphone buffer 1103 with a lower power consumption.

The SNR control is done as in Fig. 12, by first ultra-low-power envelope/energy detector 1116, and a two low pass filters, LPF3 1118, and LPF4 1119, an SNR monitor 1120, that according to the required SNR 1121, would generate the required Vref 1114 by signal 1122 and may optionally change VCC_LOW by signal 1123.

Fig. 14 describes a similar microphone buffer to the one of Fig. 12 using Micro Electronic Mechanical System (MEMS) microphone. The circuit is similar to the circuit of Fig. 12, except for the electret element 10001. The electret element 10001 is replaced with a MEMS unit 1201 including a MEMS bias impedance network 1201b and a MEMS capacitor 1201, which translate the acoustic wave pressure into variation in capacitance. These variations, with the assumption of constant charge on the MEMS capacitor, may be translated into voltage variations, as

$$V_{BB} C_{electret} = (V_{BB} + \Delta V)(C_{electret} + \Delta C) \Rightarrow \Delta V = -V_{BB} \frac{\Delta C}{C_{electret}}$$

The voltage variations are coupled to the microphone buffer 1203 through Cc c-coupling capacitor 1216.

VBB is the bias voltage for the MEMS capacitor, this voltage may be positive or negative and is generated using the switch capacitor charge pump 1204, in order to generate "clean" VBB sometimes it is required to generate a higher voltage and to pass it through Low-pass-filter and a buffer - which is normally implemented using op-amplifier, the op-amplifier output is further filtered with high resistors and capacitors.

Fig. 18 is a simplified electric schematic of a circuit generating ultra-low-noise biasing voltage VBB, according to one exemplary embodiment.

The low noise VBB biasing circuit of Fig. 18 may block the noise from the VBB 1602 using LPF 1601, and pass the voltage using a unity gain amplifier 1603. The output

of this amplifier, which is assumed to be low power, may have some noise that is further blocked by a second LPF 1605 the cleaned VBB is at the output 1606.

The MEMS bias impedance network 1201b is a diode network as described in Fig. 5, Fig. 6, Fig. 7 and Fig. 8 5013, 6013, 7013 and 8013.

Fig. 15, is similar to Fig. 14 with the difference that the current feedback is taken from Rd 1306. The signal is passed through a differential low-pass-filter LPF1a 1312 and -Vref 1314 is added, similar to Fig. 13. This may decrease the required VCC_LOW generated by the charge pump 1304 and hence power consumption will be reduced.

Fig. 16 is a microphone buffer similar to the microphone buffer of Fig. 13, however, without any current control feedback (implemented by using LPF1a 1112, Vref 1114 Op-amplifier 1115 and LPF2 1113). The control of the operating point of the JFET 1409 is done by signal 1422 generated from the SNR monitor 1420. This type of circuit may not set the current exactly, but would have the advantage of setting fast the operating point. Fig. 17 is similar to Fig. 16, and is suitable for MEMS based microphones.

It is appreciated that certain features, which are, for clarity, described in the context of separate embodiments, may also be provided in combination in a single embodiment. Conversely, various features, which are, for brevity, described in the context of a single embodiment, may also be provided separately or in any suitable sub-combination.

Although descriptions have been provided above in conjunction with specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, it is intended to embrace all such alternatives, modifications and variations that fall within the spirit and broad scope of the appended claims. All publications, patents and patent applications mentioned in this specification are herein incorporated in their entirety by reference into the specification, to the same extent as if each individual publication, patent or patent application was specifically and individually indicated to be incorporated herein by reference. In addition, citation or identification of any reference in this application shall not be construed as an admission that such reference is available as prior art.

CLAIMS

We claim

1. A microphone comprising:
 - a transistor comprising at least one of a JFET and MOSFET transistor;
 - an impedance network, wherein a first input terminal of the impedance network is connected to a gate terminal of the transistor;
 - a source resistor, wherein a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal;
 - a bypass capacitor (CS) connected in parallel to the source resistor;
 - a load resistor (RD), wherein a first terminal of the load resistor is connected to a drain terminal of the transistor;
 - a charge pump generating a low voltage power supply V_{CC_LOW} and an inverted voltage $-V_{EE}$, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage $-V_{EE}$ is connected to a first power supply node of an op-amplifier;
 - an op-amplifier, wherein
 - a first input terminal of the op-amplifier is connected to the source terminal of the transistor through a bi-directional low-pass-filter transistor;
 - a second input terminal of the op-amplifier is connected to a controlled reference voltage V_{ref} ;
 - a first power supply terminal of the op-amplifier is connected to the inverted voltage;
 - a second supply terminal of the op-amplifier is connected to the main supply voltage; and
 - an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter; and
 - an input electrets capacitor source connected in parallel to the input impedance network;
 - an ultra-low-power envelope/energy detector connected to drain terminal D of the transistor via coupling capacitor;

a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector; and

a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

2. An SNR monitor comprising:

a first input connected to a third low-pass-filter output;

a second input connected to a fourth low-pass-filter output;

one of: a third analog input, and a third digital input, that determines the required SNR:

a first output connected to a control input of a controlled V_{ref} ; and

an optional second output connected to a control input of an optional controlled charge pump.

3. A microphone comprising:

a transistor comprising at least one of a JFET and MOSFET transistor;

an impedance network, wherein a first input terminal of the impedance network is connected to a gate terminal of the transistor;

a source resistor, wherein a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal;

a bypass capacitor (CS) connected in parallel to the source resistor;

a load resistor (RD), wherein a first terminal of the load resistor is connected to a drain terminal of the transistor;

a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage $-VEE$, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage $-VEE$ is connected to a first power supply node of an op-amplifier;

an op-amplifier, wherein

a first input terminal of the op-amplifier is connected to the source terminal of the transistor through a bi-directional low-pass-filter transistor;

a second input terminal of the op-amplifier is connected to a controlled reference voltage V_{ref} ;

a first power supply of the op-amplifier terminal is connected to the inverted voltage;

a second supply terminal of the op-amplifier is connected to the main supply voltage; and

an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter; and

an input source comprising:

a MEMS capacitor, wherein a first terminal of the MEMS capacitor is connected to ground, and a second terminal of the MEMS capacitor is connected to a first terminal of a MEMS bias network;

the MEMS bias network, wherein a second terminal of the MEMS bias network is connected to a bias voltage V_{BB} ; and

a coupling capacitor, wherein a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor;

an ultra-low-power envelope/energy detector connected to drain terminal of the transistor via a coupling capacitor;

a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector; and

a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

4. A microphone comprising:

a transistor comprising at least one of a JFET and MOSFET transistor;

an impedance network, wherein a first input terminal of the impedance network is connected to a gate terminal of the transistor;

a source resistor, wherein a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal;

a bypass capacitor (CS) connected in parallel to the source resistor;

a load resistor (RD), wherein a first terminal of the load resistor is connected to a drain terminal of the transistor;

a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier;

the op-amplifier, wherein

a first input terminal of the op-amplifier is connected to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter, wherein a first input terminal of the differential bi-directional low-pass-filter is connected to a second terminal of the load resistor;

a second input terminal of the op-amplifier is connected to a second output terminal of a differential bi-directional low-pass-filter, wherein a second input terminal of the differential bi-directional low-pass-filter is connected to the first terminal of the load resistor;

a first power supply of the op-amplifier terminal is connected to the inverted voltage;

a second supply terminal of the op-amplifier is connected to the main supply voltage; and

an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter;

an input electrets capacitor source connected in parallel to the input impedance network;

an ultra-low-power envelope/energy detector connected to drain terminal of the transistor via a coupling capacitor;

a third low-pass-filter connected to the output of the ultra-low-power envelope/energy detector; and

a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

5. A microphone comprising:

a transistor comprising at least one of a JFET and MOSFET transistor;

an impedance network, wherein a first input terminal of the impedance network is connected to a gate terminal of the transistor;

a source resistor, wherein a first terminal of the source resistor is connected to a source terminal of the transistor, and a second terminal of the source resistor is connected to a ground terminal;

a bypass capacitor (CS) connected in parallel to the source resistor;

a load resistor (RD), wherein a first terminal of the load resistor is connected to a drain terminal of the transistor;

a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier;

an op-amplifier, wherein

a first input terminal of the op-amplifier is connected to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter, wherein a first input terminal of the differential bi-directional low-pass-filter is connected to a second terminal of the load resistor;

a second input terminal of the op-amplifier is connected to a second output terminal of a differential bi-directional low-pass-filter, wherein a second input terminal of the differential bi-directional low-pass-filter is connected to the first terminal of the load resistor;

a first power supply of the op-amplifier terminal is connected to the inverted voltage;

a second supply terminal of the op-amplifier is connected to the main supply voltage; and

an output terminal of the op-amplifier is connected to a second terminal of the input impedance network through a second low pass filter; and

an input source comprising:

a MEMS capacitor, wherein a first terminal of the MEMS capacitor is connected to ground and a second terminal of the MEMS capacitor is connected to a first terminal of a MEMS bias network;

a MEMS bias network connected with its second terminal to a bias voltage V_{BB}; and

the MEMS bias network, wherein a second terminal of the MEMS bias network is connected to a bias voltage V_{BB}; and

a coupling capacitor, wherein a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor.

6. The microphone according to any of claims 1 - 4, wherein the input impedance network comprises:

a plurality of low-leakage diodes connected in series wherein:

a first diode cathode terminal is the first terminal of the input impedance network;

a first diode anode terminal is connected to a second diode cathode terminal; and

an anode terminal of diode N is the second terminal to the input impedance network.

7. The microphone according to any of claims 1 - 4, wherein the input impedance network is comprises a plurality of low-leakage diodes connected in series wherein:

a first diode anode terminal is the first terminal of the input impedance network;

a first diode cathode terminal is connected to a second diode anode terminal; and

a cathode terminal of diode N is the second terminal of the input impedance network.

8. The microphone according to any of claims 2 and 4, wherein the input impedance network comprises of a parallel diode network comprising:

a first diode network comprising a plurality of diodes connected in series wherein

a first diode cathode terminal is the first terminal of the input impedance network;

a first diode anode terminal is connected to a second diode cathode terminal; and

an anode terminal of diode N is the second terminal of the input impedance network; and

a second diode network comprising a plurality of diodes connected in series wherein:

a first diode anode terminal is the first terminal of the input impedance network;

a first diode cathode terminal is connected to a second diode anode terminal; and

a cathode terminal of diode N is the second terminal to the input impedance network.

9. The microphone according to any of claims 1 - 4, wherein the input impedance network comprises at least two series of two-terminal sub-networks wherein:

a first terminal of a first sub-network is the first terminal of the input impedance network;

a second terminal of a last sub network is the second terminal of the input impedance network and

wherein a sub-network comprises a two low-leakage identical diodes connected in parallel in opposite polarity.

10. The microphone according to any of claims 1 - 4, wherein the charge pump is controlled.

11. The microphone according to any of claims 2 and 4, wherein the MEMS bias impedance network comprises a plurality of low-leakage diodes connected in series, wherein:

a first diode cathode terminal is the first terminal of the MEMS bias impedance network;

a first diode anode terminal is connected to a second diode cathode terminal; and

an anode terminal of diode N is the second terminal to the MEMS bias impedance network.

12. The microphone according to any of claims 2 and 4, wherein the MEMS bias impedance network comprises plurality of low-leakage diodes connected in series, wherein:

a first diode anode terminal is the first terminal of the MEMS bias impedance network;

a first diode cathode terminal is connected to a second diode anode terminal; and

a cathode terminal of diode N is the second terminal to the MEMS bias impedance network.

13. The microphone according to any of claims 2 and 4, wherein the MEMS bias impedance network comprises a parallel diode network comprising:

a first diode network comprising a plurality of diodes connected in series, wherein

a first diode cathode terminal is the first terminal of the MEMS bias impedance network;

a first diode anode terminal is connected to a second diode cathode terminal;

an anode terminal of diode N is the second terminal of the MEMS bias impedance network; and

a second diode network comprising a plurality of diodes connected in series, wherein

a first diode anode terminal is the first terminal of the MEMS bias impedance network;

a first diode cathode terminal is connected to a second diode anode terminal; and

a cathode terminal of diode N is the second terminal to the MEMS bias impedance network.

14. The microphone according to any of claims 2 and 4, wherein the MEMS bias impedance network comprises of at least two series of two-terminal sub-networks wherein a first terminal of a first sub-network is the first terminal of the MEMS bias impedance network and a second terminal of a last sub network is the second terminal of the MEMS

bias impedance network, wherein a sub network s comprises two low-leakage identical diodes connected in parallel in opposite polarity.

15. A method for sensing an acoustic signal, the method comprising:
 - connecting a first input terminal of an impedance network to a gate terminal of a transistor comprising at least one of a JFET and MOSFET transistor;
 - connecting a first terminal of a source resistor to a source terminal of the transistor, and a second terminal of the source resistor to a ground terminal;
 - connecting a bypass capacitor (CS) in parallel with the source resistor;
 - connecting a first terminal of a load resistor (RD) to a drain terminal of the transistor;
 - connecting a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier;
 - connecting a first input terminal of the op-amplifier to the source terminal of the transistor through a bi-directional low-pass-filter transistor;
 - connecting a second input terminal of the op-amplifier to a controlled reference voltage Vref;
 - connecting a first power supply terminal of the op-amplifier to the inverted voltage;
 - connecting a second supply terminal of the op-amplifier to the main supply voltage;
 - and
 - connecting an output terminal of the op-amplifier to a second terminal of the input impedance network through a second low pass filter; and
 - connecting an input electrets capacitor source in parallel with the input impedance network;
 - connecting an ultra-low-power envelope/energy detector to drain terminal D of the transistor via coupling capacitor;
 - connecting a third low-pass-filter to the output of the ultra-low-power envelope/energy detector; and
 - connecting a fourth low-pass-filter to the output of the ultra-low-power envelope/energy detector.

16. An SNR monitor comprising:
a first input connected to a third low-pass-filter output;
a second input connected to a fourth low-pass-filter output;
one of: a third analog input, and a third digital input, that determines the required SNR;
a first output connected to a control input of a controlled V_{ref} ; and
an optional second output connected to a control input of an optional controlled charge pump.
17. A method for sensing an acoustic signal, the method comprising:
connecting a first input terminal of an impedance network to a gate terminal of a transistor comprising at least one of a JFET and MOSFET transistor;
connecting a first terminal of a source resistor to a source terminal of the transistor, and a second terminal of the source resistor to a ground terminal;
connecting a bypass capacitor (CS) in parallel with the source resistor;
connecting a first terminal of a load resistor (RD) to a drain terminal of the transistor;
connecting a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage $-VEE$, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage $-VEE$ is connected to a first power supply node of an op-amplifier;
connecting a first input terminal of the op-amplifier to the source terminal of the transistor through a bi-directional low-pass-filter transistor;
connecting a second input terminal of the op-amplifier to a controlled reference voltage V_{ref} ;
connecting a first power supply terminal of the op-amplifier to the inverted voltage;
connecting a second supply terminal of the op-amplifier to the main supply voltage;
and
connecting an output terminal of the op-amplifier to a second terminal of the input impedance network through a second low pass filter; and
connecting an input source comprising:

a MEMS capacitor, wherein a first terminal of the MEMS capacitor is connected to ground, and a second terminal of the MEMS capacitor is connected to a first terminal of a MEMS bias network;

the MEMS bias network, wherein a second terminal of the MEMS bias network is connected to a bias voltage VBB; and

a coupling capacitor, wherein a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor.

connecting an ultra-low-power envelope/energy detector to drain terminal of the transistor via a coupling capacitor;

connecting a third low-pass-filter to the output of the ultra-low-power envelope/energy detector; and

connecting a fourth low-pass-filter to the output of the ultra-low-power envelope/energy detector;

18. A method for sensing an acoustic signal, the method comprising:

connecting a first input terminal of an impedance network to a gate terminal of a transistor comprising at least one of a JFET and MOSFET transistor;

connecting a first terminal of a source resistor to a source terminal of the transistor, and a second terminal of the source resistor to a ground terminal;

connecting a bypass capacitor (CS) in parallel with the source resistor;

connecting a first terminal of a load resistor (RD) to a drain terminal of the transistor;

connecting a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier;

connecting a first input terminal of the op-amplifier to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter;

connecting a first input terminal of the differential bi-directional low-pass-filter to a second terminal of the load resistor;

connecting a second input terminal of the op-amplifier to a second output terminal of a differential bi-directional low-pass-filter;

connecting a second input terminal of the differential bi-directional low-pass-filter to the first terminal of the load resistor;

connecting a first power supply of the op-amplifier terminal to the inverted voltage;

connecting a second supply terminal of the op-amplifier to the main supply voltage;

connecting an output terminal of the op-amplifier to a second terminal of the input impedance network through a second low pass filter;

connecting an input electrets capacitor source in parallel to the input impedance network;

connecting an ultra-low-power envelope/energy detector to drain terminal D of the transistor via a coupling capacitor;

connecting a third low-pass-filter to the output of the ultra-low-power envelope/energy detector; and

connecting a fourth low-pass-filter connected to the output of the ultra-low-power envelope/energy detector.

19. A method for sensing an acoustic signal, the method comprising:

connecting a first input terminal of an impedance network to a gate terminal of a transistor comprising at least one of a JFET and MOSFET transistor;

connecting a first terminal of a source resistor to a source terminal of the transistor, and a second terminal of the source resistor to a ground terminal;

connecting a bypass capacitor (CS) in parallel with the source resistor;

connecting a first terminal of a load resistor (RD) to a drain terminal of the transistor;

connecting a charge pump generating a low voltage power supply VCC_LOW and an inverted voltage -VEE, wherein the low voltage is connected to a second terminal of the load resistor, and the inverted voltage -VEE is connected to a first power supply node of an op-amplifier;

connecting a first input terminal of the op-amplifier to a controlled reference voltage connected to first output terminal of a differential bi-directional low-pass-filter;

connecting a first input terminal of the differential bi-directional low-pass-filter to a second terminal of the load resistor;

connecting a second input terminal of the op-amplifier to a second output terminal of a differential bi-directional low-pass-filter;

connecting a second input terminal of the differential bi-directional low-pass-filter to the first terminal of the load resistor;

connecting a first power supply of the op-amplifier terminal to the inverted voltage;

connecting a second supply terminal of the op-amplifier to the main supply voltage;

connecting an output terminal of the op-amplifier to a second terminal of the input impedance network through a second low pass filter; and

connecting an input source comprising:

a MEMS capacitor, wherein a first terminal of the MEMS capacitor is connected to ground and a second terminal of the MEMS capacitor is connected to a first terminal of a MEMS bias network;

a MEMS bias network connected with its second terminal to a bias voltage V_{BB} ; and

the MEMS bias network, wherein a second terminal of the MEMS bias network is connected to a bias voltage V_{BB} ; and

a coupling capacitor, wherein a first terminal of the coupling capacitor is connected to the second terminal of the MEMS capacitor, and with a second terminal of the coupling capacitor is connected to the gate terminal of the transistor.

FIG. 1

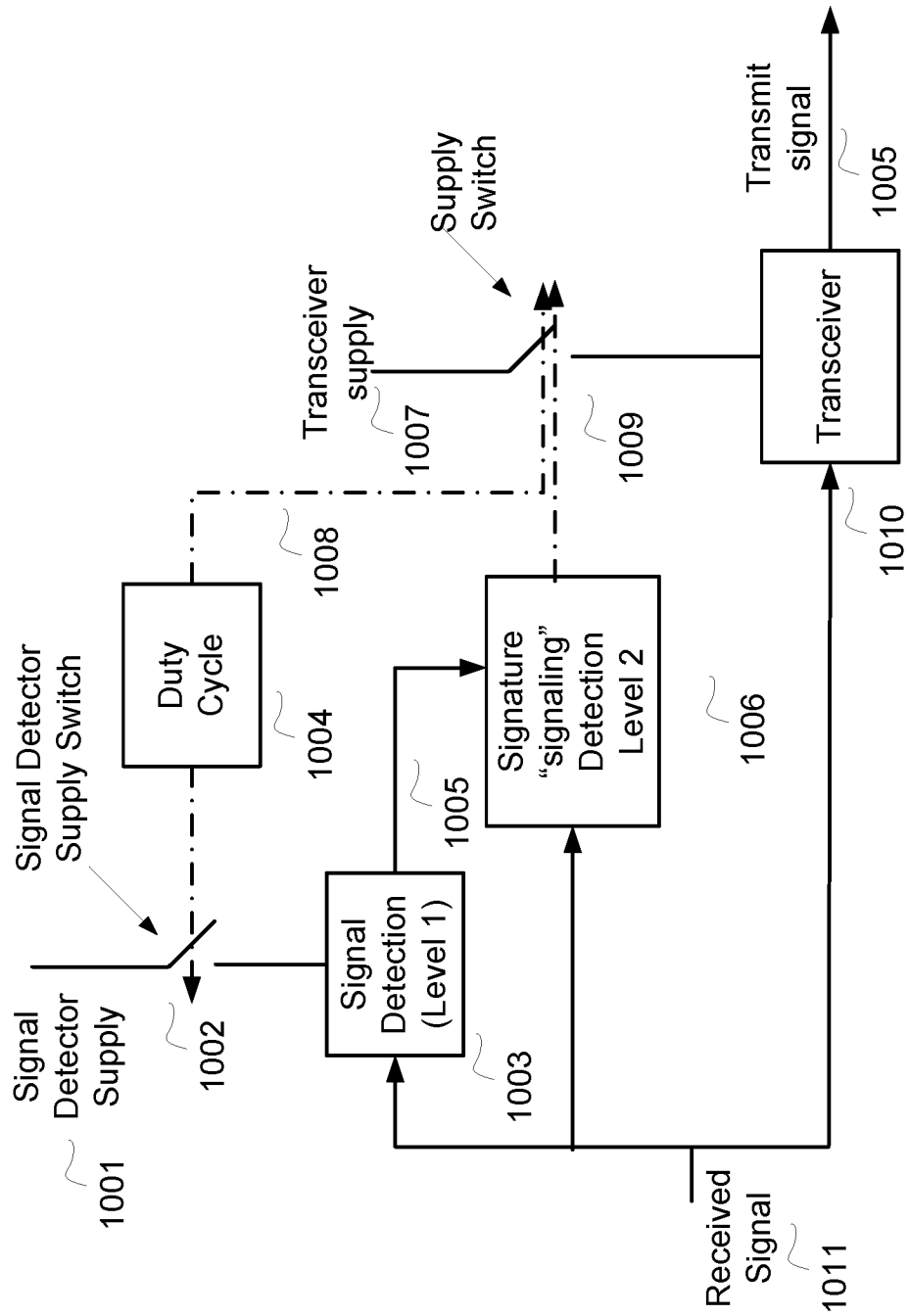


FIG. 2

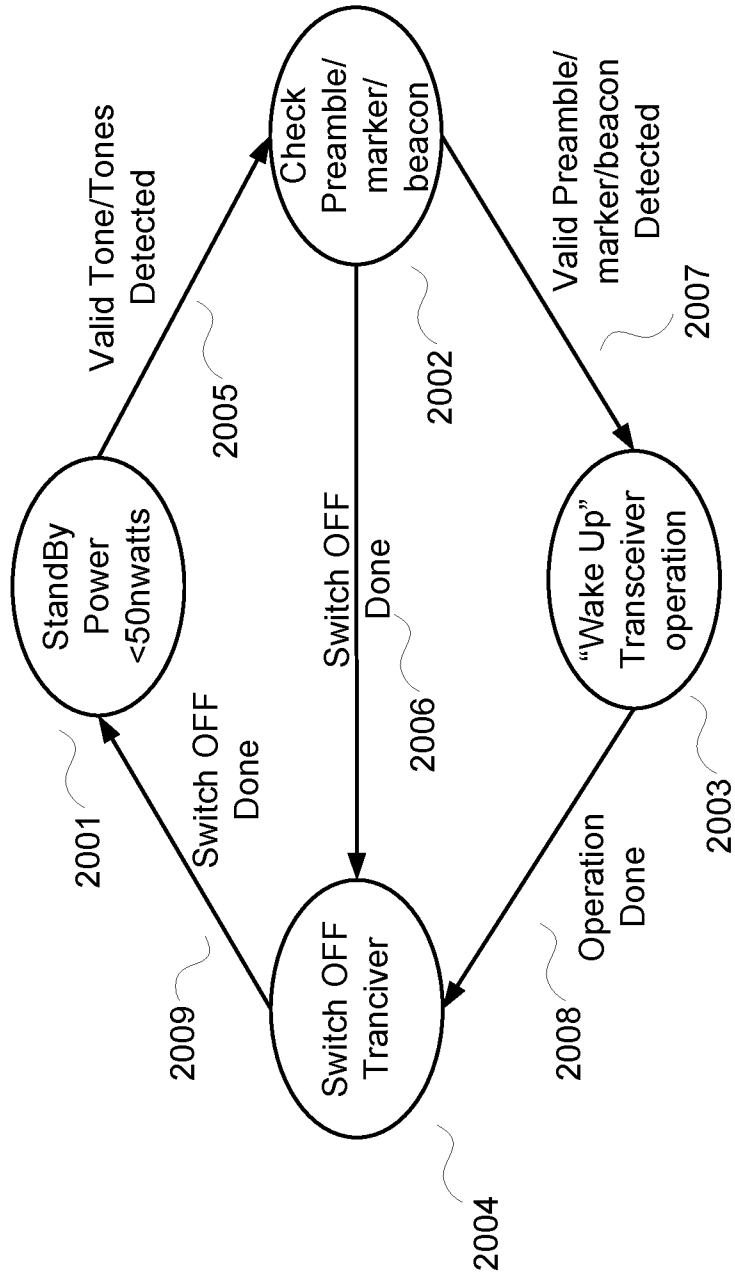


FIG. 3

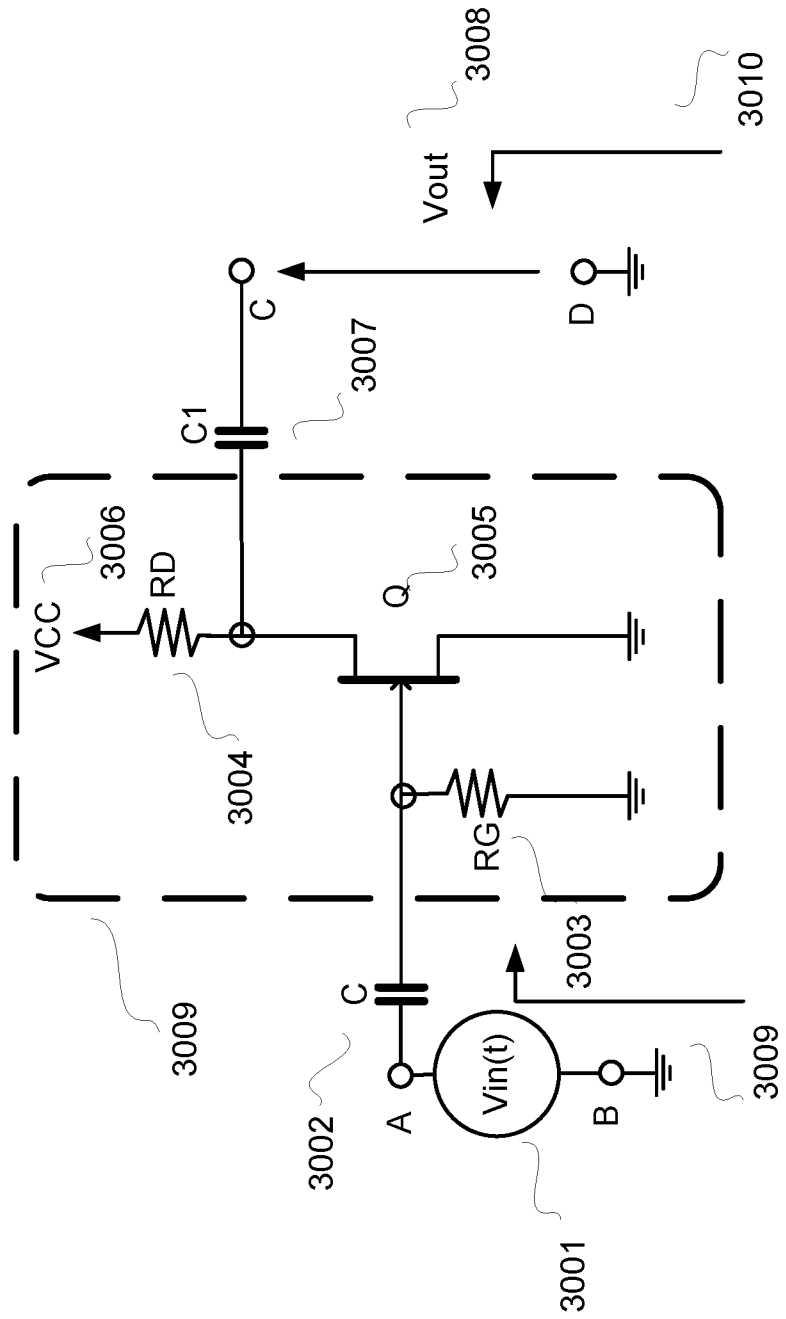


FIG. 4

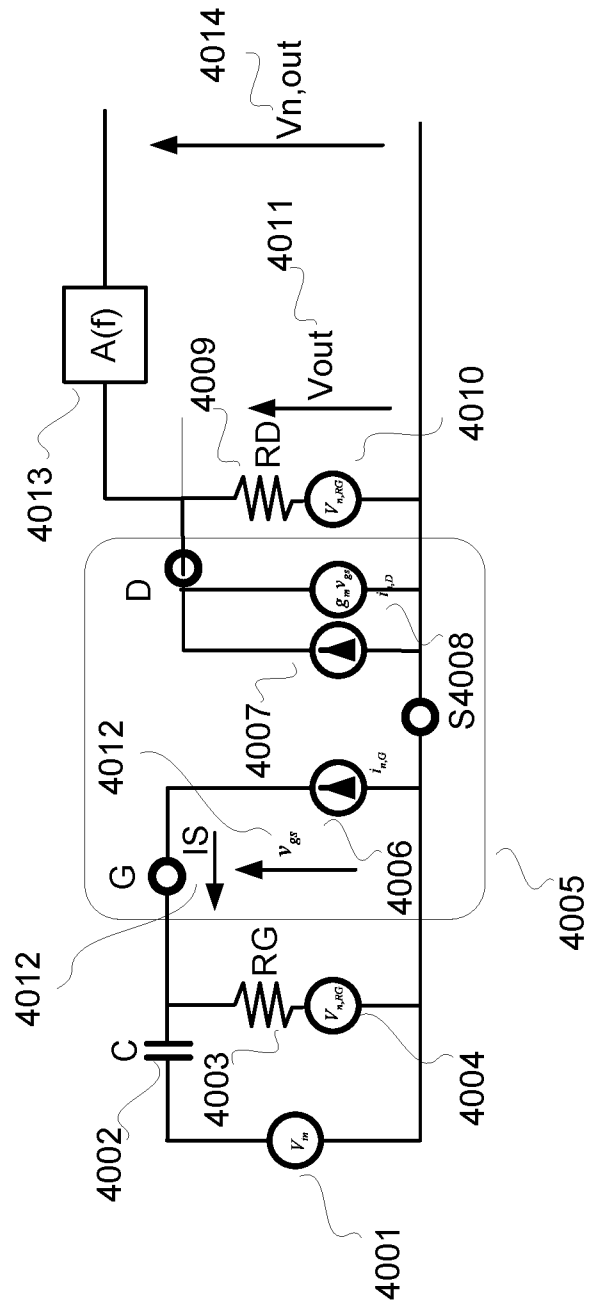


FIG. 5

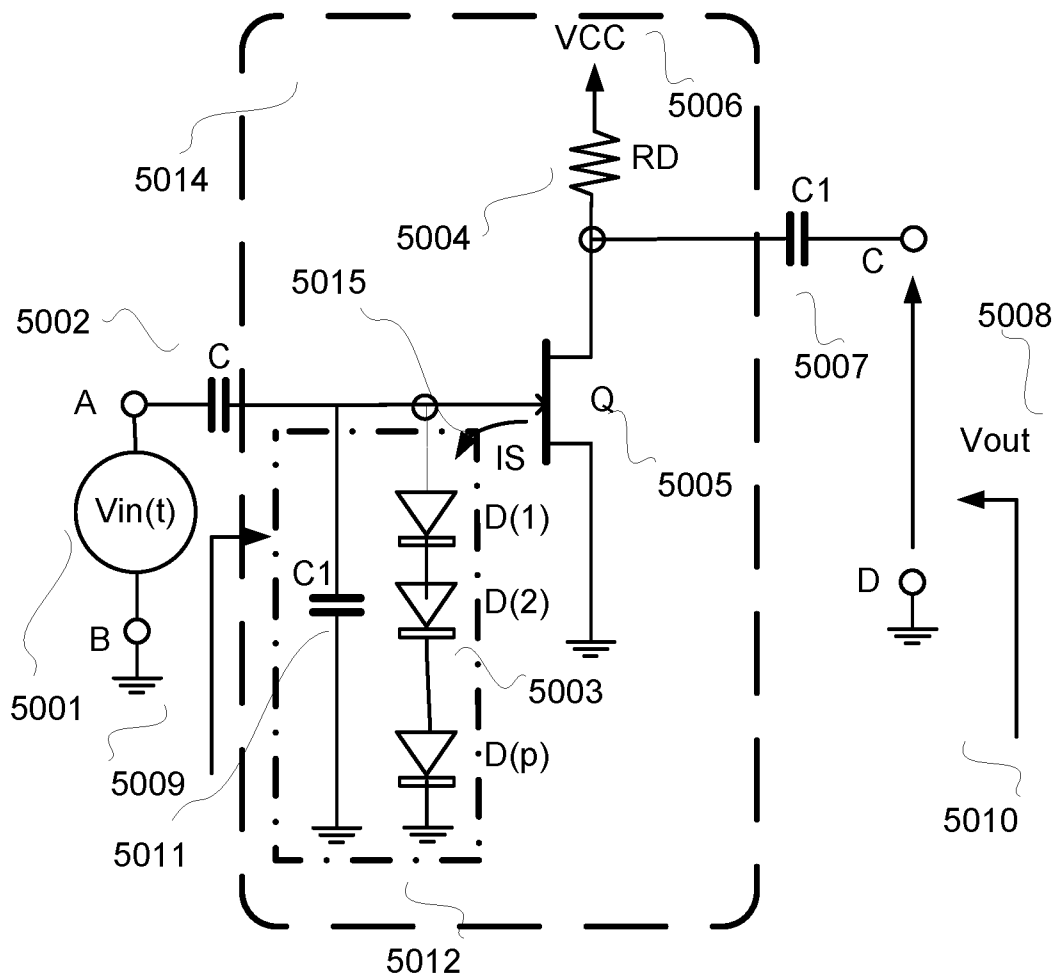


FIG. 6

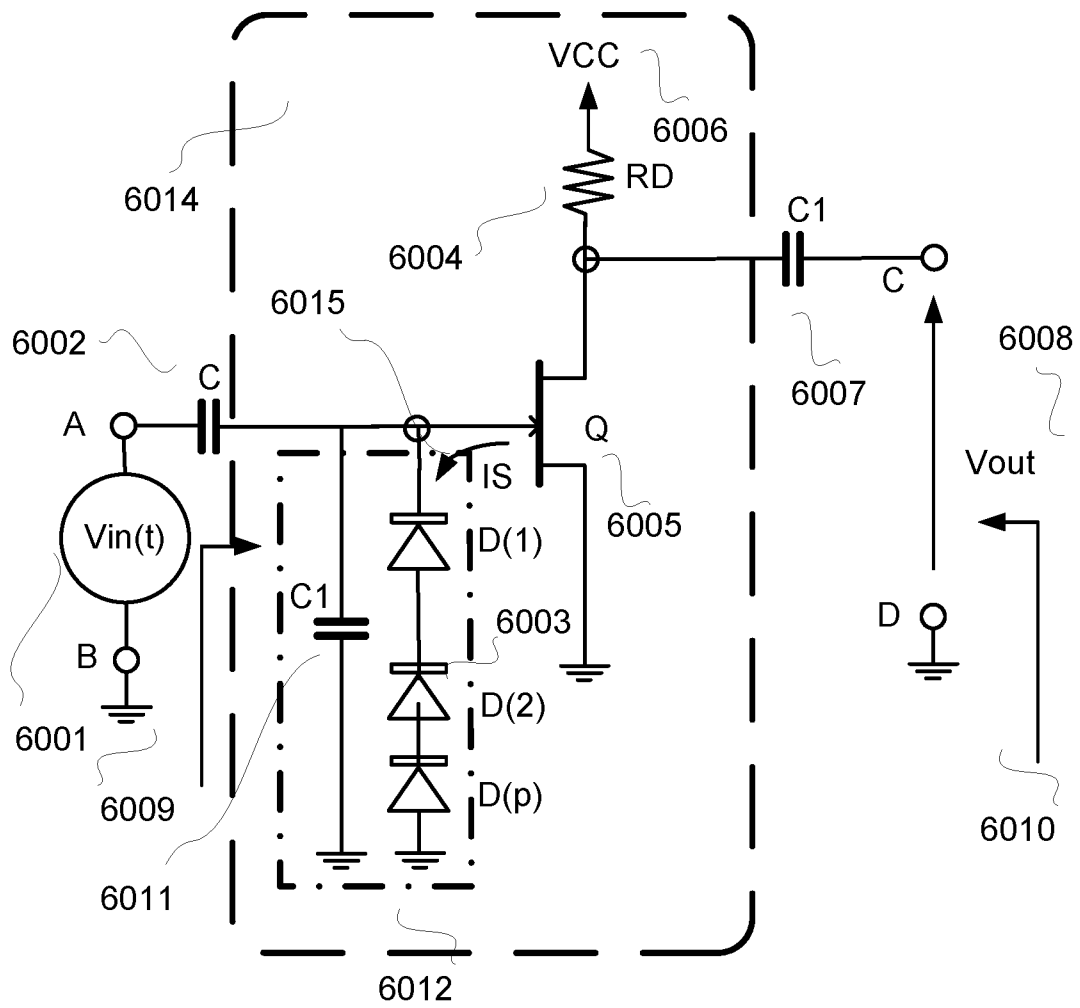


FIG. 7

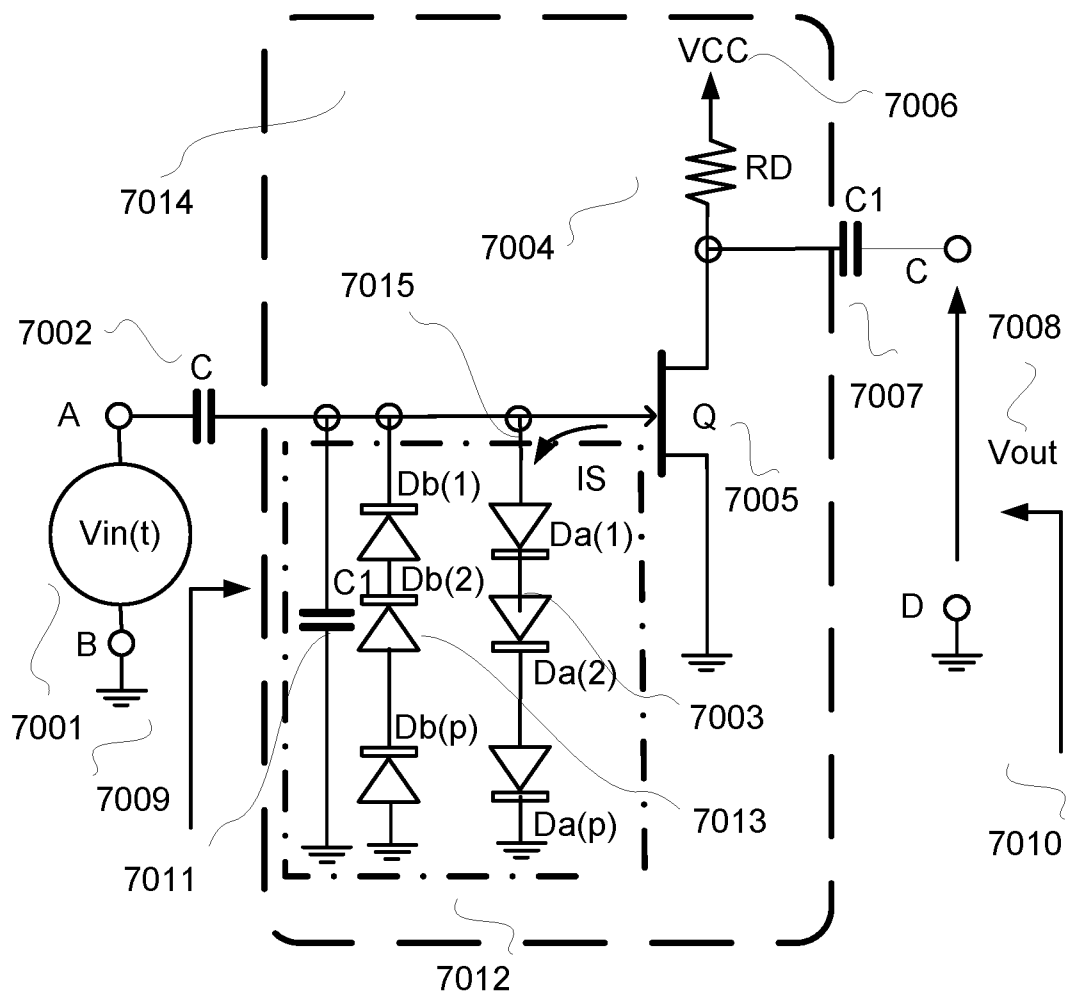


FIG. 8

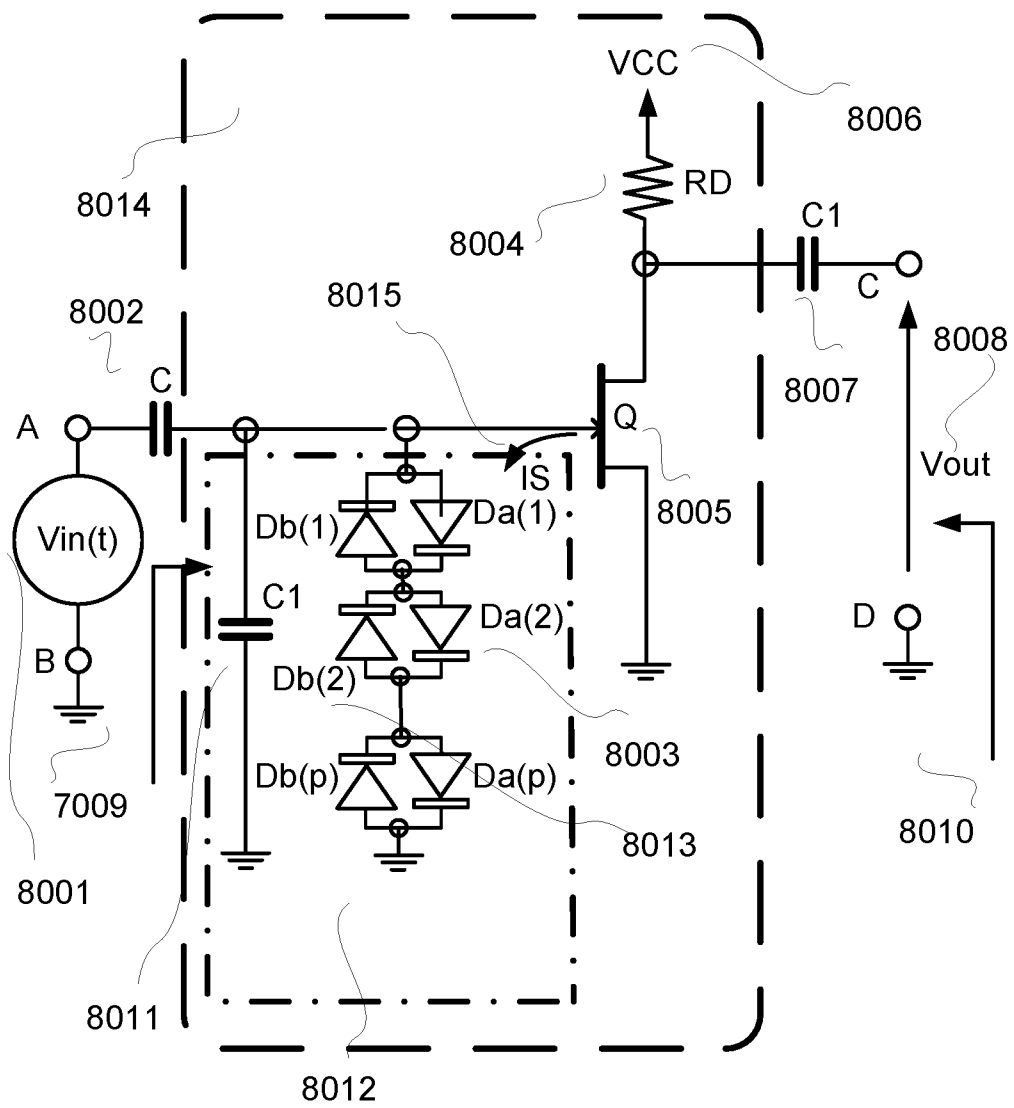


FIG. 9

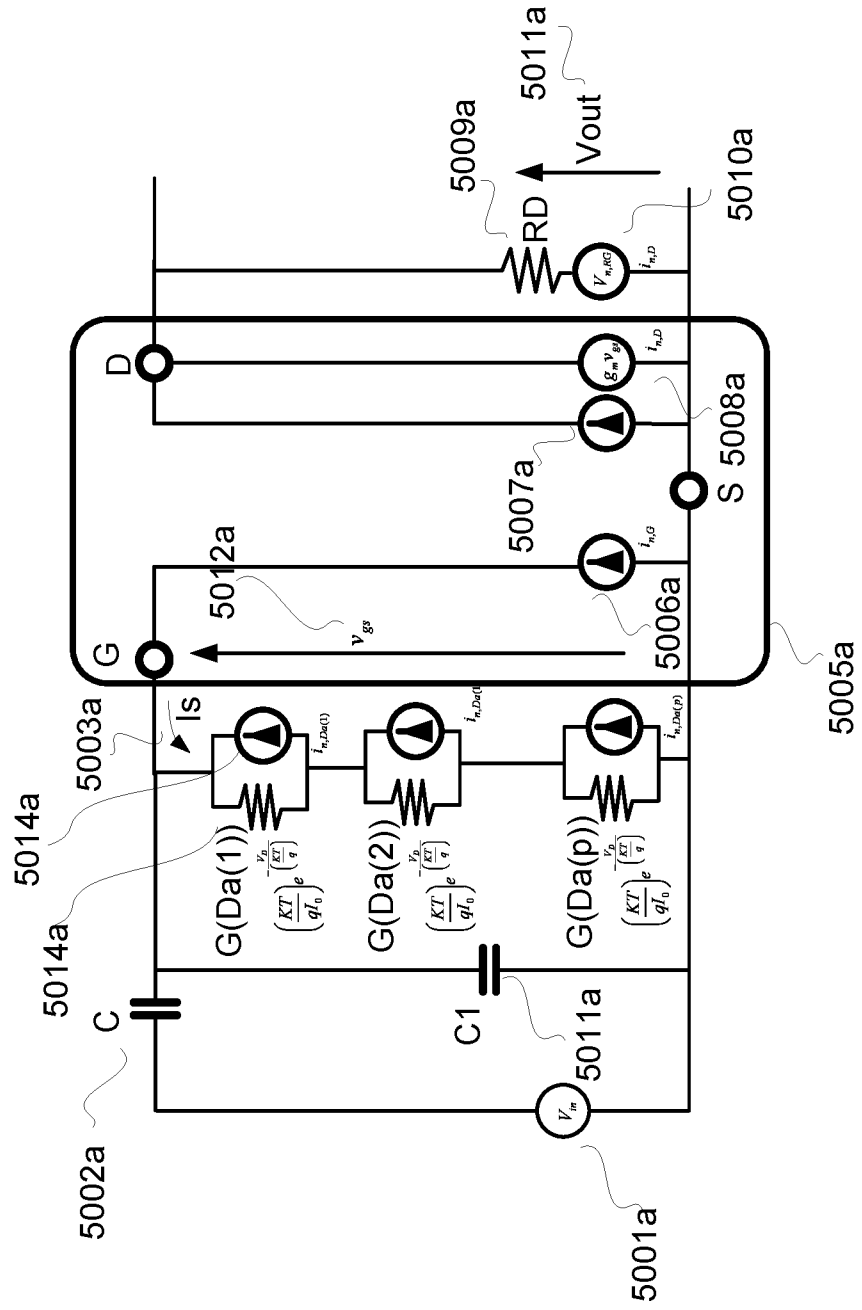


FIG. 10

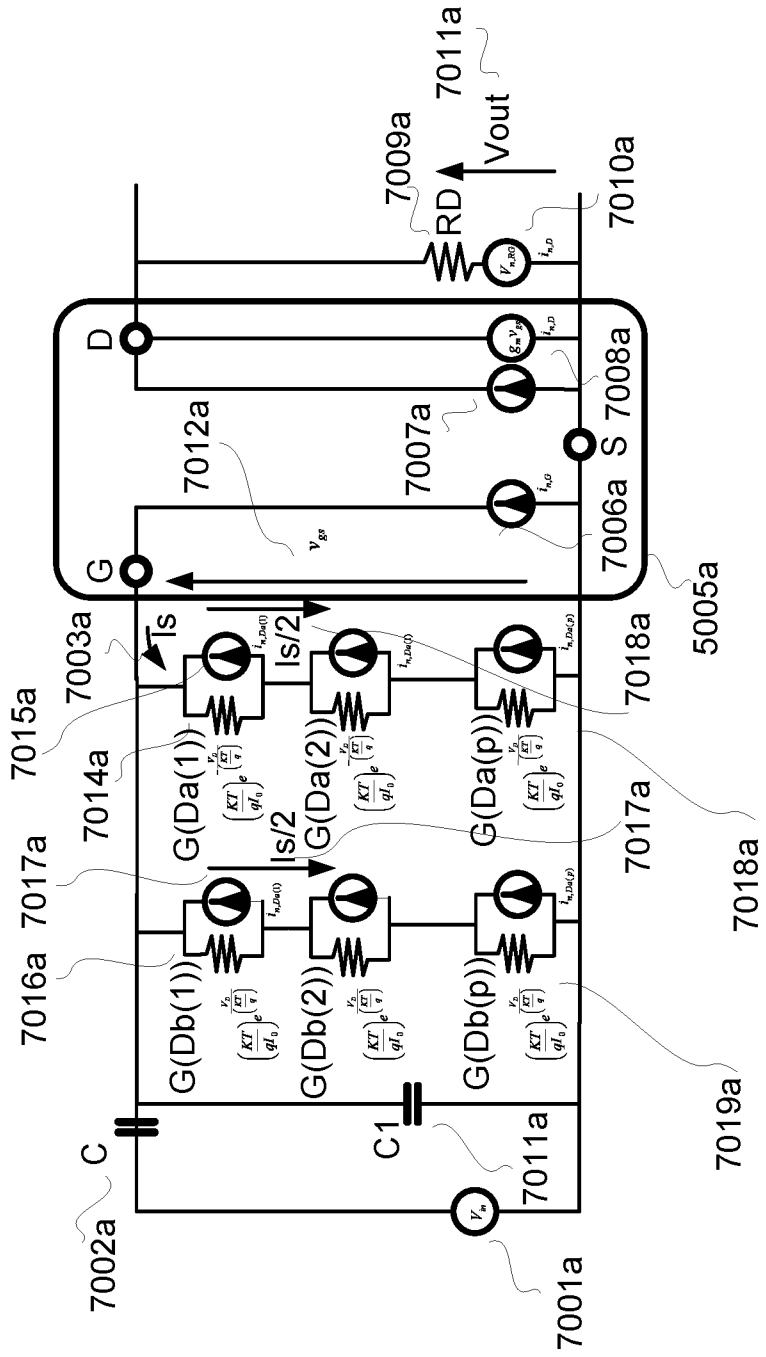


FIG. 11

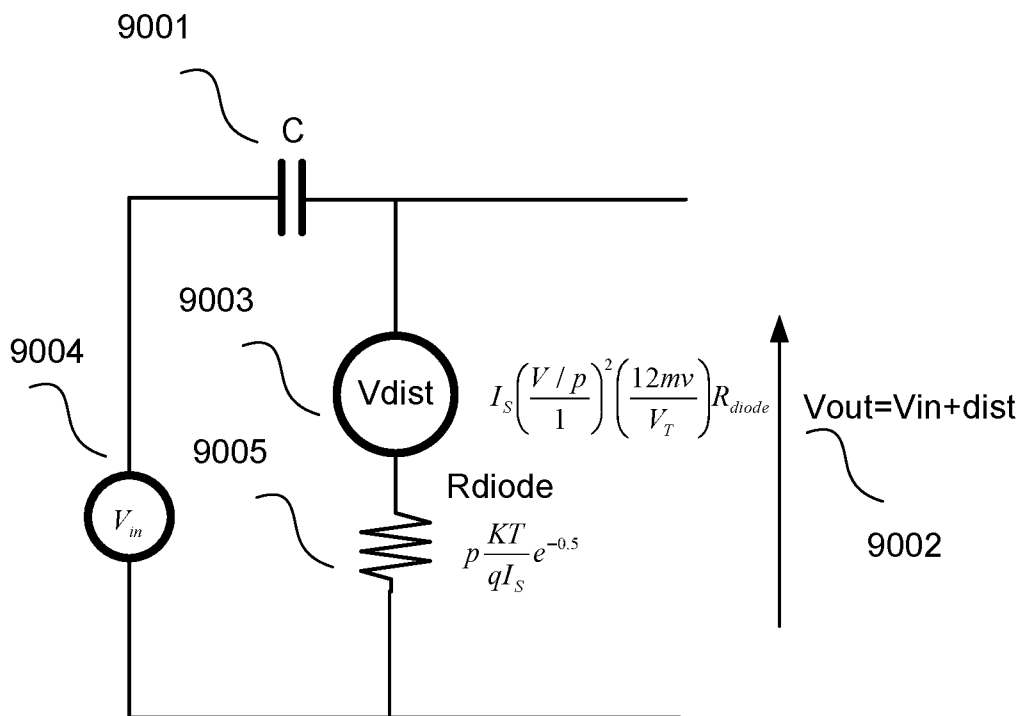


FIG. 12

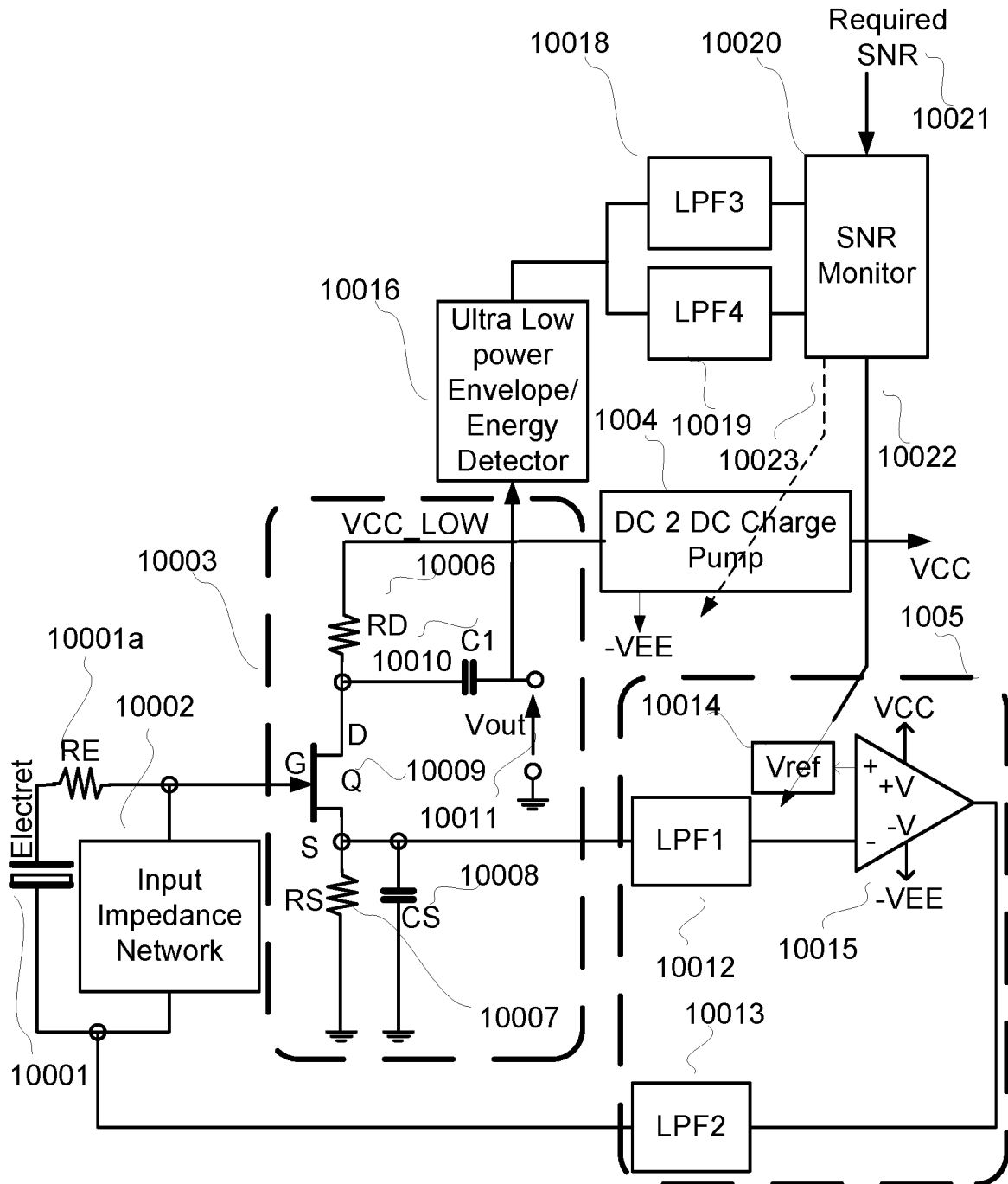


FIG. 13

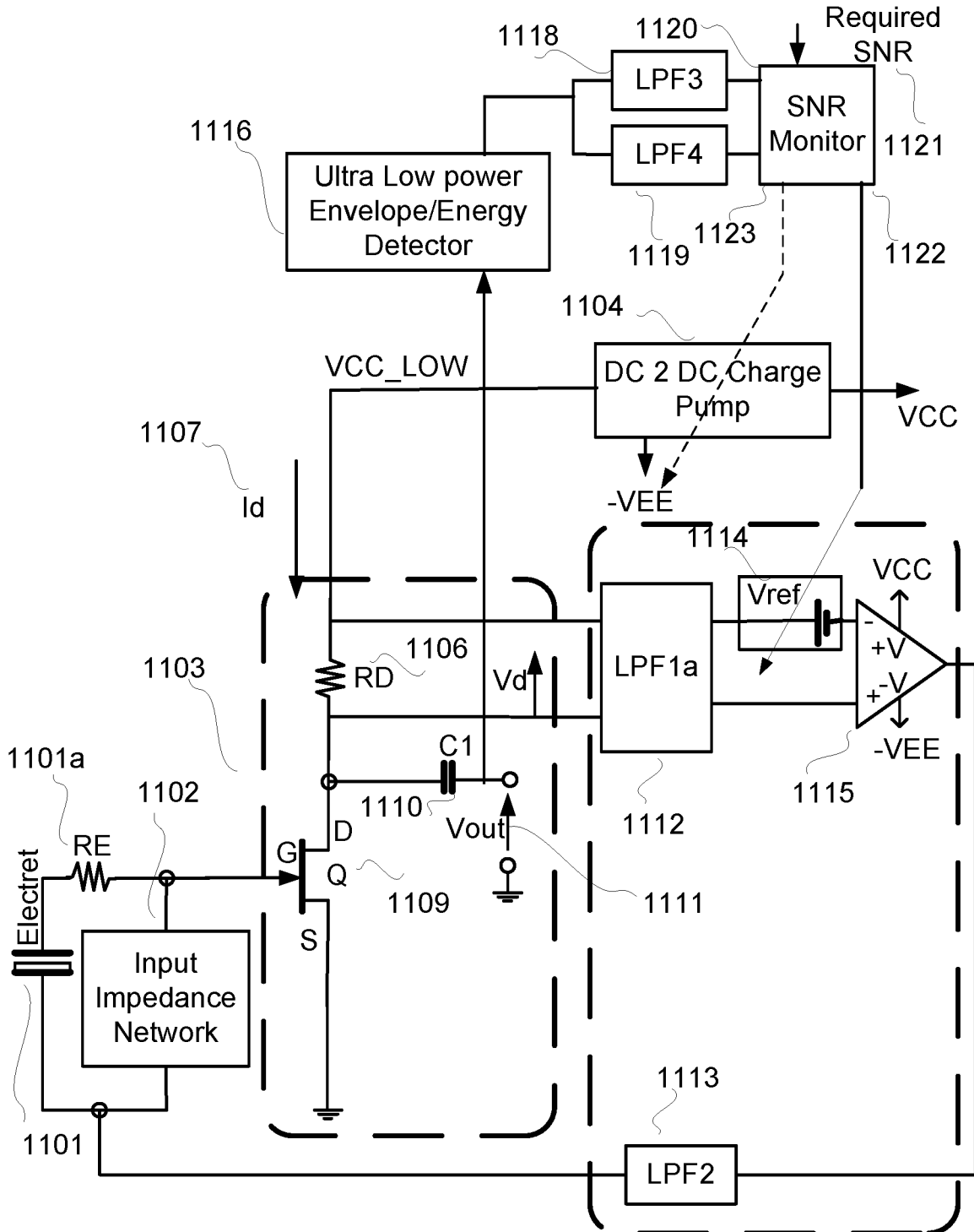


FIG. 14

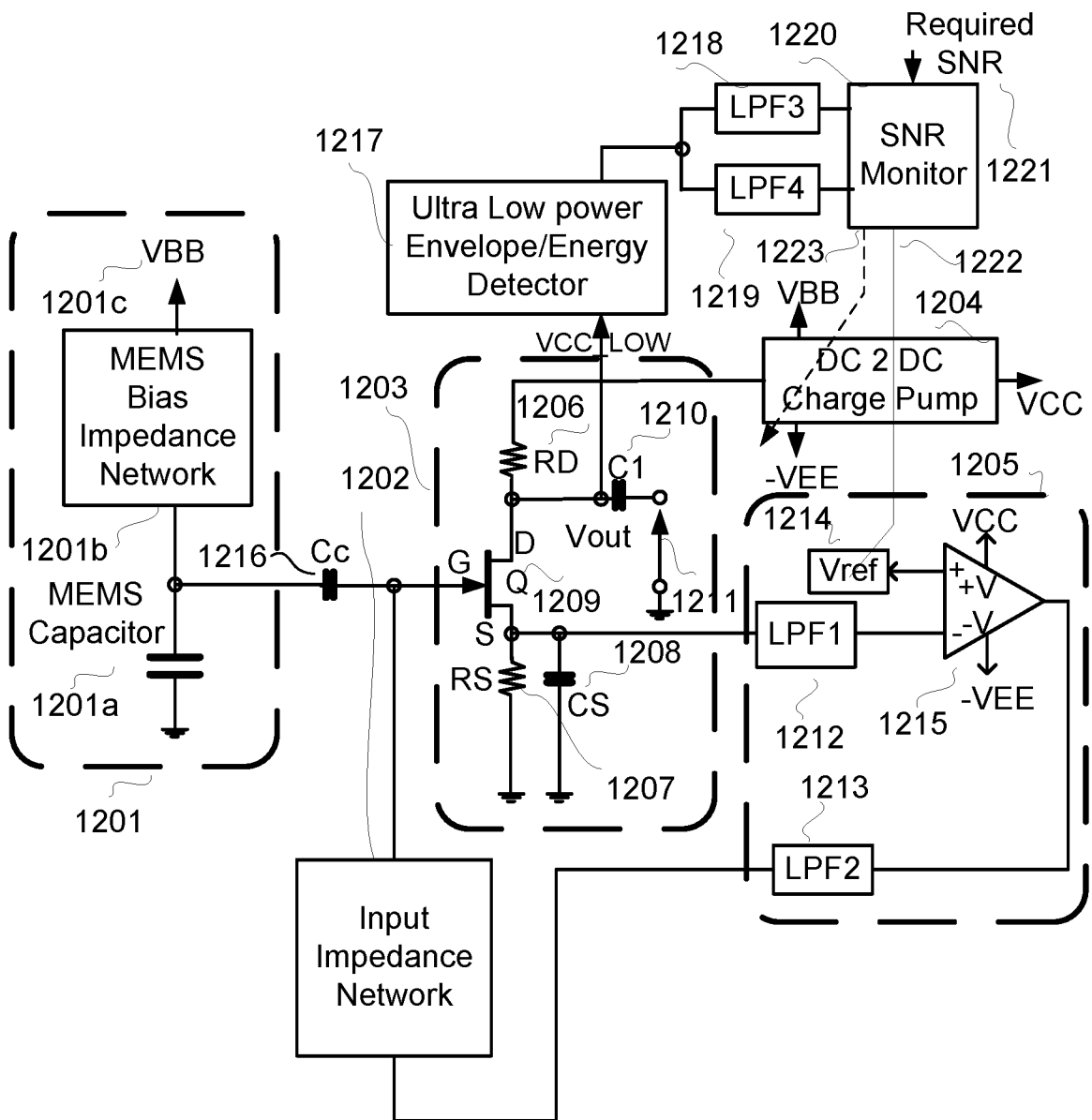


FIG. 16

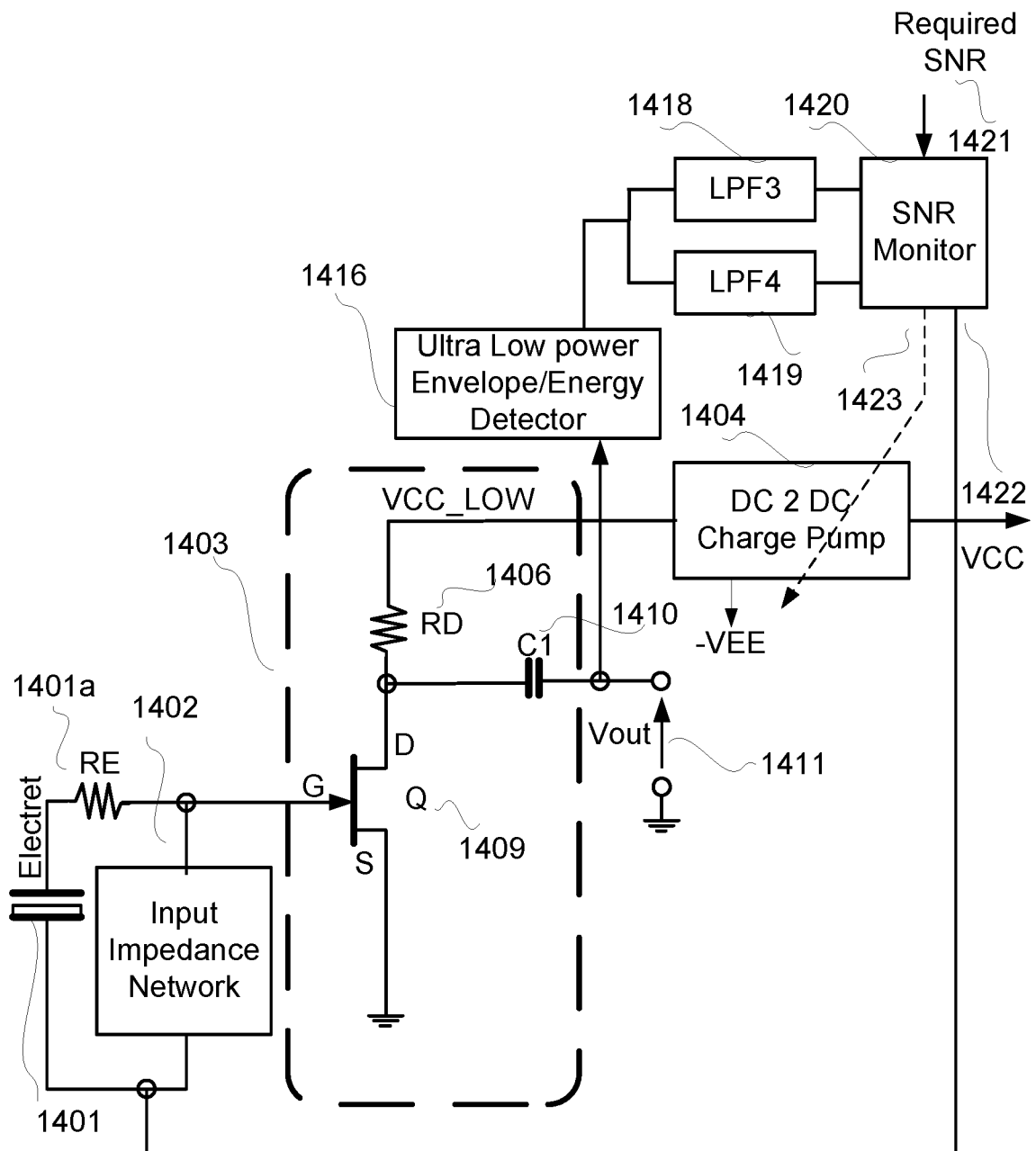


FIG. 17

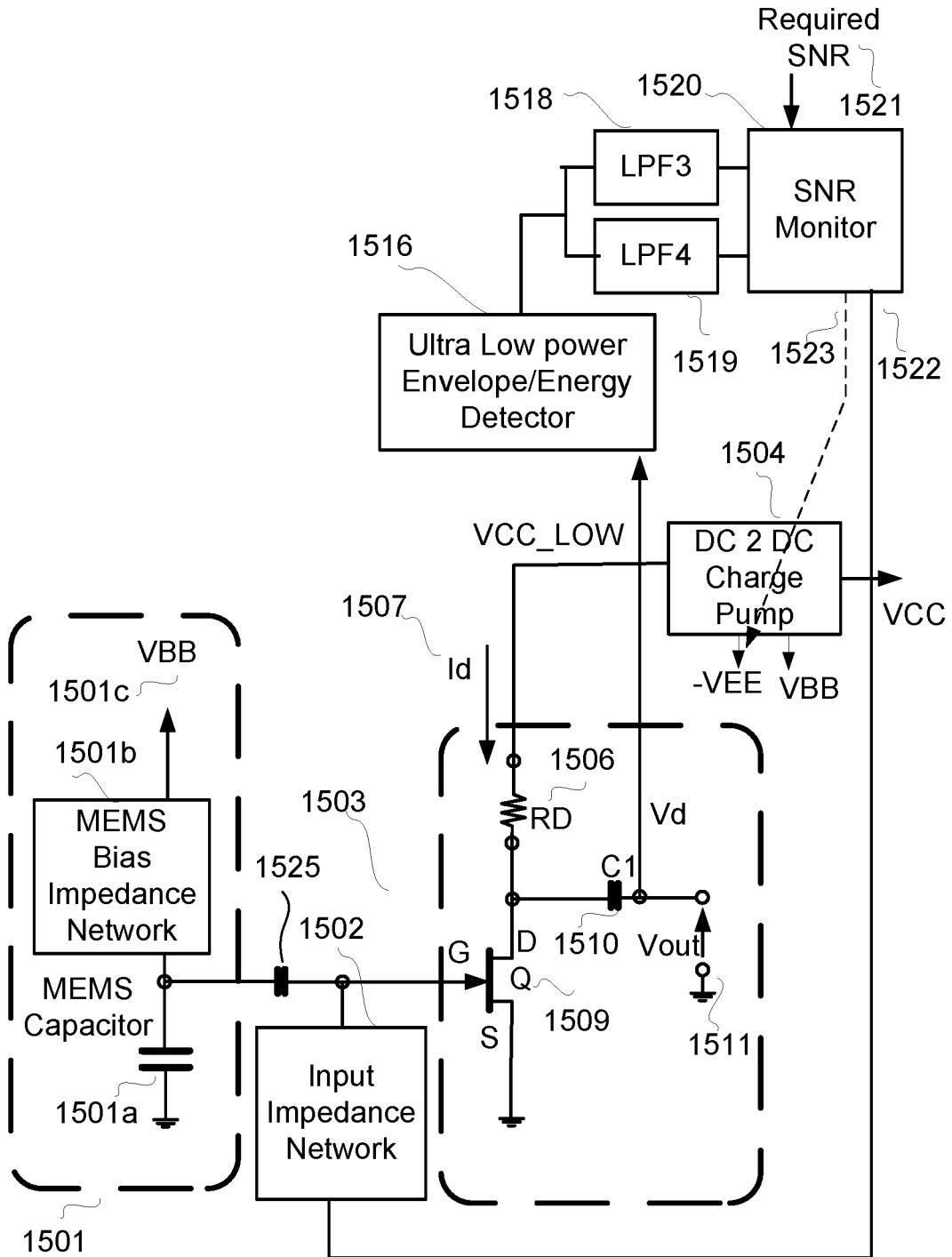


FIG. 18

