Single-ended to differential LNA

Fig. 3

Abstract: An amplifier (300) for converting a single-ended input signal to a differential output signal. The amplifier (300) comprises a first transistor (301), a second transistor (302), a third transistor (303) and a fourth transistor (304). The first transistor (301), configured in common-source or common-emitter mode, receives the single-ended input signal and generates a first part of the differential output signal. The second transistor (302), also configured in common-source or common-emitter mode, generates a second part of the differential output signal. The third and fourth transistor (303,304) are capacitively cross-coupled. The amplifier (300) further comprises inductive degeneration such that a source or emitter of the first transistor (301) is connected to a first inductor (321) and a source or emitter of the second transistor (302) is connected to a second inductor (322).
A LOW NOISE AMPLIFIER CIRCUIT

TECHNICAL FIELD

Embodiments herein relate to an amplifier. In particular, they relate to a low noise amplifier for converting a single-ended input signal to a differential output signal in a wireless communication device.

BACKGROUND

Transceivers, which in general comprise transmitters and receivers, employed in wireless communication devices, e.g. modern cellular phones, are usually highly integrated with most of the transceiver functions integrated on a Radio Frequency Integrated Circuit (RFIC). Highly integrated RFIC reduces phone’s Printed Circuit Board (PCB) area, complexity and power consumption, while lowering cost of components. In addition, cellular receivers used in high-end mobile phones and laptops need to operate at multiple frequency bands and the cellular receivers have to support several wireless standards such as Global System for Mobile Communications (GSM), Wideband Code Division Multiple Access (WCDMA), and Long Term Evolution (LTE) etc.

As each reception frequency band usually needs its own pre-selection filter between an antenna and the RFIC, the number of receiver inputs of the RFIC is basically determined by the number of bands needed to be supported. In practice, state-of-the-art RFICs may have as many as 10 to 30 receiver inputs. Moreover, as differential signal processing is considered to be more insensitive and robust against common-mode disturbances and interferences, often differential inputs are employed for receiver RFICs. Naturally, a corresponding first stage of the RFIC receiver, usually a Low-Noise Amplifier (LNA), is also implemented as a differential-input, differential-output amplifier. Unfortunately, as each differential LNA needs two input package pins, the number of RFIC package pins consumed by the receiver inputs will increase largely assuming that a large number of frequency bands needs to be supported. For instance, with 20 differential receiver inputs, altogether 40 package pins for the receiver inputs are needed in the RFIC. In addition, routing 20 differential Radio Frequency (RF) traces on PCB between the RFIC and a Front-End Module (FEM) containing pre-selection filters etc. becomes very challenging. For this reason, it would be very beneficial to have an LNA with a single-
ended input so as to lower the number of RFIC package pins needed for the receiver. In addition, this would simplify the PCB routing between the FEM and RFIC, and also lower the PCB area and footprint needed for the corresponding routing. On the other hand, due to electrical performance reasons it is very beneficial to implement a down-conversion mixer following the LNA in the receiver downstream as a double-balanced circuit, so the LNA needs to have a differential output. As a result, a single-ended-to-differential LNA is needed.

The single-ended-to-differential amplifier may be implemented by using a single-ended amplifier, i.e. an amplifier with single-ended input and output, followed by a passive or active balun circuit, which converts a single-ended output signal of the amplifier to a differential signal. Unfortunately, single-ended amplifiers are very sensitive to poorly modeled ground and supply parasitics, such as parasitic inductances, which may degrade amplifier gain, input matching, Noise Figure (NF) etc. and in some extreme cases may cause circuit oscillation. As very accurate modeling of ground and supply parasitics is needed for the single-ended amplifier design, there is also a risk of penalty in time-to-market due to a longer design cycle. Moreover, in a product containing the RFIC, customers or another subcontractors may design the PCB, therefore it would be beneficial to use LNAs that are less sensitive to PCB parasitics, e.g. supply and ground inductances. Finally, unavoidable ground and supply parasitic loops may also act as a victim loop for magnetic coupling of undesirable spurious signals.

Usually, a passive balun circuit is implemented as an inductive transformer. However, a passive balun circuit or transformer circuit used at the amplifier output has usually lower quality factor than a corresponding differential inductor, which leads to power consumption penalty. Moreover, active balun circuits degrade performance of a receiver by introducing noise and nonlinearity while also increasing power consumption of the receiver.

It is also possible to realize a single-ended-to-differential amplifier by employing a balun circuit followed by a differential amplifier, i.e. an amplifier with balanced or differential input and output. The balun circuit converts a single-ended input signal to a differential signal for the differential amplifier. A conventional balun circuit may be implemented either as an on- or off-chip inductive transformer. However, as the loss of the balun circuit is very critical regarding the receiver NF, the balun circuit is usually implemented as an off-chip component with high Quality factor (Q-factor) and low loss.
Unfortunately, since each RFIC receiver input needs its own balun circuit and external balun circuits are almost as expensive as pre-selection filters, the solution is not attractive due to high cost and a large PCB area is consumed.

US 6366171 discloses a single-ended-to-differential LNA which can be integrated on silicon, but in this technique, a compensation circuit is needed to improve the differential signal phase imbalance. In addition, the auxiliary branch needed to generate the differential output signal generates substantial noise and nonlinearity.

In US 7646250 and CHOI, J. et al., A Low Noise and Low Power RF Front-End for 5.8-GHz DSRC Receiver in 0.13 µm CMOS, Journal of Semiconductor Technology and Science, Vol.11, No.1, March, 2011, single-to-differential signal converters with similar topology which can provide well-balanced output currents in response to a single-ended input voltage are disclosed. The topology is shown in Figure 1, where the single-to-differential converter comprises a first transistor $M_1$ and a second transistor $M_2$, each configured as a common-source amplifier. Further, a capacitive cross-coupled transistor pair $M_3$ and $M_4$ is coupled to outputs of the first and second transistors $M_1$ and $M_2$. $Z_L$ is an LC-resonator circuit coupled at the output of the converter. Unfortunately, since this circuit has capacitive or imaginary input impedance, its input impedance cannot be matched to a real impedance, such as 50 Ω, even with off-chip matching networks. As a result, the single-ended-to-differential converter shown in Figure 1 cannot be used as an LNA in a wireless receiver as shown in Figure 2 and described below, in which the LNA input impedance needs to be matched to a characteristic impedance, usually 50 Ω, of a band-pass filter preceding the LNA.

In the wireless receiver shown in Figure 2, an RF filter, or band pass filter, is needed to perform pre-selection of a received RF band. Without the RF filter, the linearity requirements of the receiver would be overwhelming and impractical. On the other hand, if the terminating impedance of the RF filter differs significantly from the specified characteristic impedance, it will cause large ripple and loss in the pass-band of the RF filter and worsen the transition band of the RF filter. Such large losses need to be avoided because they can, for example, lead to penalties in receiver NF and sensitivity. As a result, it is very important that the LNA presents sufficiently accurate terminating impedance for the RF filter.
SUMMARY

Therefore, a first object of embodiments herein is to provide a single-ended-to-differential amplifier with improved performance.

According to a first aspect of embodiments herein, the object is achieved by an amplifier for converting a single-ended input signal to a differential output signal. The amplifier according to embodiments herein comprises a first transistor, configured in common-source or common-emitter mode, to receive the single-ended input signal and generate a first part of the differential output signal. The amplifier further comprises a second transistor, configured in common-source or common-emitter mode, to generate a second part of the differential output signal. The amplifier further comprises a third transistor and a fourth transistor which are cross-coupled and connected to the first and second transistors in the following way:

- a drain or collector of the first transistor is coupled to a gate or base of the fourth transistor via a first capacitor;
- a drain or collector of the second transistor is coupled to a gate or base of the third transistor via a second capacitor; and
- the drain or collector of the first transistor is connected to a source or emitter of the third transistor, the drain or collector of the second transistor is connected to a source or emitter of the fourth transistor.

Further, the drain or collector of the first transistor is coupled to a gate or base of the second transistor directly or via a third capacitor.

The amplifier further comprises a degenerating inductance such that a source or emitter of the first transistor is connected to a first inductor and a source or emitter of the second transistor is connected to a second inductor.

A second object of embodiments herein is to provide a multiband receiver with improved performance.

According to an aspect of embodiments herein, this object is achieved by a receiver for operating at multiple frequency bands. The receiver comprises one or more radio-frequency filters configured to receive a single-ended input signal and to generate a single-ended output signal. The receiver further comprises one or more amplifiers
according to embodiments herein configured to convert a single-ended input signal, being the single-ended output signal generated from the radio-frequency filter, to a differential output signal. Further, input impedances of the one or more amplifiers are configured to match output impedances of the one or more radio frequency filters at operating frequencies respectively.

According to another aspect of embodiments herein, this object is achieved by a method in a receiver for operating at multiple frequency bands. The method comprises receiving in one or more radio-frequency filters single-ended input signals and generating single-ended output signals. The method further comprises receiving the generated single-ended output signals in one or more amplifiers according embodiments herein and converting the received single-ended signals to differential output signals in the one or more amplifiers. Further, input impedances of the one or more amplifiers are configured to match output impedances of the one or more radio frequency filters at operating frequencies respectively.

The amplifier according to embodiments herein has several advantages. First, since the amplifier comprises a first transistor which is an inductively degenerated common-source or common-emitter transistor, together with an input matching circuit, it can provide a well-defined and well-regulated input impedance. Second, since the amplifier can provide a well-defined and well-regulated input impedance, its input impedance may be designed to match a characteristic impedance of an RF filter, then the amplifier is suitable for using as a low noise amplifier in a receiver in a wireless communication device. Third, since the amplifier comprises a third transistor and a fourth transistor which are cross-coupled and connected to the first and second transistors, the amplifier can provide a well-balanced differential output signal. In addition, thanks to the cross-coupled the third and fourth transistors, the noise and nonlinearity due to the second transistor in the amplifier are cancelled at the well-balanced differential output signal. As a result, the second transistor has negligible effect on the entire amplifier noise and linearity performance.

Thus, embodiments herein provide a single-ended-to-differential amplifier with improved performance on input impedance matching, noise and linearity. Further, embodiments herein also provide a multiband receiver with improved performance as a result of using the amplifier according to embodiments herein as a low noise amplifier in
the receiver. Thanks to the improved performance on the input impedance matching, noise and nonlinearity of the amplifier, the entire receiver performance on, e.g. noise and linearity are improved.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Examples of embodiments herein are described in more detail with reference to attached drawings in which:

Figure 1 is a schematic diagram illustrating a single-ended-to-differential amplifier with capacitive cross-coupled transistor pair according to prior art.
Figure 2 is a schematic diagram illustrating a direct conversion receiver with a single-ended-to-differential LNA according to prior art.
Figure 3 is a schematic diagram illustrating a single-ended-to-differential amplifier according to embodiments herein.
Figure 4 is a schematic diagram illustrating an analysis model for the single-ended-to-differential amplifier shown in Figure 3.
Figure 5 is a block diagram illustrating a wireless communication device in which embodiments herein may be implemented.
Figure 6 is a flowchart depicting a method in a receiver according to embodiments herein.

DETAILED DESCRIPTION

Nowadays most receivers in wireless communication devices are based on direct conversion or zero Intermediate Frequency (zero-IF) architectures, because these receiver topologies allow a very high level of integration and low cost. Zero-IF receivers also permit efficient integration of multimode, multiband receivers.

A simplified block diagram of a direct conversion receiver 200 with a single-ended-to-differential LNA 210 is shown in Figure 2. An antenna 220 feeds a received RF analog signal to a RF filter 230 that performs pre-selection of received RF bands and passes on a selected RF analog signal. The LNA 210 amplifies the selected RF analog signal and drives down-conversion mixers 240, mixers for short, which down-convert the amplified RF analog signal. The down-converted analog signal is filtered and amplified in low-pass filters and gain stages of Analog Baseband (ABB) 250 and then converted to a digital
signal in Analog-to-Digital Converters (ADC) 260. As shown in Figure 2, the selected RF signal at the LNA 210 input is single-ended but the remaining signal processing before the ADC 260 is carried out with differential signals.

The mixers 240 utilized in an integrated direct conversion receiver are practically always based either on single- or double-balanced circuit topologies. If a mixer operates with a differential Local Oscillator (LO) signal and a single-ended RF signal, it is called single-balanced. However, if a mixer accommodates both differential RF and LO signals, it is called double-balanced.

Double-balanced mixers generate less even-order distortion and provide better port-to-port isolation than their single-balanced counterparts. In addition, single-balanced topologies are more susceptible to noise in the LO signal. For these reasons, double-balanced mixer topologies are preferred and the LNA 210 needs to provide differential drive signals for the double-balanced mixer, as shown in Figure 2. Embodiments herein is to provide LNA circuits that improve the performance of the receiver 200.

According to embodiments herein, a single-ended-to differential amplifier 300 for converting a single-ended input signal to a differential output signal is shown in Figure 3. Figure 3 is a simplified schematic, where all biasing details are omitted. The amplifier 300 may be used as the LNA 210 in the receiver in Figure 2.

As shown in Figure 3, the amplifier 300 comprises a first transistor 301, M₁, a second transistor 302, M₂, a third transistor 303, M₃, and a fourth transistor 304, M₄. Although transistors shown in Figure 3 are Metal-Oxide-Semiconductor (MOS) transistors with terminal names of gate, drain and source, it is also possible to use other types of transistor, for example, Bipolar Junction Transistors (BJT) with corresponding terminal names of base, collector and emitter.

The first transistor 301, configured in common-source or common-emitter mode, receives the single-ended input signal and generates a first part of the differential output signal, i.e. the output current \( i_{o_{+}} \). The second transistor 302, also configured in common-source or common-emitter mode, generates a second part of the differential output signal, i.e. the output current \( i_{o_{-}} \). The third and fourth transistors 303,304 are capacitively cross-coupled and connected to the first and second transistors 301,302.

Further, as shown in Figure 3, detailed connections of the first, second, third and fourth transistors 301,302,303,304 are: a drain or collector of the first transistor 301 is coupled to a gate or base of the fourth transistor 304 via a first capacitor 311, C₁; a drain or collector of the second transistor 302 is coupled to a gate or base of the third transistor...
303 via a second capacitor 312, C₂; further, the drain or collector of the first transistor 301 is coupled to a gate or base of the second transistor 302 via a third capacitor 313, C₃; and furthermore the drain or collector of the first transistor 301 is connected to a source or emitter of the third transistor 303, the drain or collector of the second transistor 302 is connected to a source or emitter of the fourth transistor 304.

According to some embodiments, the third capacitor C₃ may be replaced with a short circuit. In that case the gate or base of the second transistor 302 is directly connected to the drain or collector of the first transistor 301.

The amplifier 300 further comprises inductive degeneration such that a source or emitter of the first transistor 301 is connected to a first inductor 321, Lₛ₁, and a source or emitter of the second transistor 302 is connected to a second inductor 322, Lₛ₂. 

According to some embodiments, degeneration inductors 321 and 322, i.e. Lₛ₁ and Lₛ₂, may also be implemented with a single differential inductor. Then, the amplifier 300 comprises a differential degenerating inductance such that the source or emitter of the first transistor 301 is connected to a first terminal of the differential inductor and the source or emitter of the second transistor 302 is connected to a second terminal of the differential inductor. Depending on the differential inductor topology, a middle access terminal of the differential inductor may be connected to a ground.

The amplifier 300 further comprises a matching circuit 330. The gate or base of the first transistor 301 is coupled to the single-ended input signal through the matching circuit 330. In Figure 3, Z₆ represents a parasitic ground impedance, ideally Z₆ = 0 Ω. The matching circuit 330 is usually implemented with off-chip high-Quality (high-Q) passive components. Most often, one or two passive components are sufficient to match the amplifier input impedance at the frequency of interest to the impedance of an RF filter, e.g. 50 Ω. The matching circuit 330 may comprise, for instance, starting from the gate of the first transistor 301, a series inductance and a parallel capacitance between the amplifier 300 input terminal, i.e. the terminal named Vᵢ and the ground. In Figure 3, the first, second and third capacitors 311, 312, 313, i.e. C₁, C₂, and C₃ are assumed to act as short-circuits at the operation frequency of interest.

At the frequency of interest, the input matching circuit 330 together with the first transistor 301, which is the inductively degenerated common-source transistor M₁, matches the amplifier 300 input impedance to the characteristic impedance of the RF filter 230. The first transistor 301 also amplifies the input voltage Vᵢ across the gate-source of
the first transistor 301. In the following, the first transistor 301, \( M_1 \) converts the amplified version of the input voltage \( V_{in} \) or its gate-source voltage \( V_{gs1} \) to a first part of the differential output current \( i_{out1} \). The second transistor 302, which is the common-source transistor \( M_2 \), is responsible for converting its gate-source voltage \( V_{gs2} \) to a second part of, i.e. the complementary of the differential output current \( i_{out2} \). Moreover, thanks to the cross-coupled third and fourth transistors 303,304, i.e. \( M_3 \) and \( M_4 \), the output currents \( i_{out3} \) and \( i_{out4} \) are well-balanced.

As a summary, the amplifier 300 being a single-ended-to-differential amplifier, converts the input signal, the voltage \( v_{in} \) applied via the input matching network 330 to the gate or base of the first transistor 301, \( M_1 \) to a differential output signal, i.e. the output current \( i_{out} = i_{out+} - i_{out-} \), where \( i_{out+} = i_{out-} \), available at the drains or collectors of the cross-coupled third and fourth transistors 303, 304, \( M_3 \) and \( M_4 \). At the output of the amplifier 300, the differential output current may be converted to a differential output voltage \( v_{out} = Z_L \cdot i_{out} \) by a load impedance \( Z_L \) if needed.

Now, detailed operations of the single-ended-to-differential converting in the amplifier 300 are described. By inspection of the amplifier 300 in Figure 3, the output currents can be written as

\[
i_{out+} = g_{m3} (v_2 - v_1) \quad (1)
\]

\[
i_{out-} = g_{m4} (v_1 - v_2) \quad (2)
\]

Where, \( v_1 \) and \( v_2 \) are voltages at nodes 1 and 2, and \( g_{m3}, g_{m4} \) are transconductances of the third transistor \( M_3 \) and the fourth transistor \( M_4 \) respectively. By choosing \( g_{m3} = g_{m4} \)

\[
i_{out-} = g_m (v_1 - v_2) = g_{m3} (v_2 - v_1) = -i_{out+} \quad (3)
\]

Thus well-balanced output currents are obtained.

At a frequency \( f_o \) of interest, an input impedance \( Z_{in} \) of the amplifier 300 is designed to match the characteristic RF pre-selection filter impedance \( R_s \), also called as a source resistance, usually \( R_s = 50\Omega \).
\[ Z_w(\omega_0) = R_s \quad (4) \]

Where \( 0 = 2rf_0 \). In addition, at the operation frequency of \( f_0 \), while impedance matched, i.e. the input impedance of the amplifier 300 is matched to the source resistance, or condition in Equation (4) is fulfilled, the magnitude of the differential output current can be approximated as

\[ |i_{OUT}(\omega_0)| = |i_{OUT-} - i_{OUT+}| = 2|g_m|v_{GS1}| = 2g_mQv_{IN} \quad (5) \]

where \( g_m \) is the transconductance of the first transistor \( M_1 \), \( v_{GS1} \) is the gate-source voltage of the first transistor \( M_1 \), and \( Q \) is a quality factor, Q-factor, of the input matching circuit 330 and is expressed as

\[ Q = \left| \frac{v_{GS1}(\omega_0)}{v_{IN}} \right| = \left| \frac{v_{GS1}(\omega_0)}{v_{IN}} \right| \quad (6) \]

Accordingly, the equivalent transconductance of the amplifier 300 is given as

\[ G_m = \frac{|i_{OUT}(\omega_0)|}{v_{IN}} = 2g_mQ \quad (7) \]

It can be seen that Equation (7) describes how the single-ended input voltage \( v_{IN} \) is converted to a differential output current \( i_{OUT} \) and the conversion gain in terms of transconductance is \( 2g_mQ \).

Also, when impedance matched at the frequency of interest, an input current magnitude of the amplifier 300 is expressed as

\[ \left| i_{IN}(\omega_0) \right| = \frac{v_{IN}}{Z_{IN}(\omega_0)} = \frac{v_{IN}}{R_s} \quad (8) \]

Thus, the amplifier 300 output current given by (5) is written as

\[ v_{OUT+}(-\omega_0) = 2g_mQv_{IN} = 2g_mQ \left| i_{IN}(-\omega_0) \right| \quad (9) \]

Thus, a current gain of the amplifier 300 at impedance match is given as

\[ \left| i_{OUT}(\omega_0) \right| = 2g_mQR_s \quad (10) \]

In practice, \( 2g_mQR_s \) - 1 and thus

\[ \left| i_{OUT}(\omega_0) \right| \gg \left| i_{IN}(\omega_0) \right| \quad (11) \]

Using the approximation expressed in Equation (11) at impedance match, the Kirchhoff's current law for node 3 can be written as
\[ v_{3^{\text{GND}}} \approx i_{\text{OUT}^+} + i_{\text{OUT}^-}, \]  

(12)

Where, \( v_3 \) is a voltage across the parasitic ground impedance \( Z_{\text{GND}} \). Since

\[ i_{\text{OUT}^+} = -i_{\text{OUT}^-}, \] thus

\[ v_3 Z_{\text{GND}}^{-1} \approx i_{\text{OUT}^+} + i_{\text{OUT}^-} \approx 0 \]  

(13)

and therefore

\[ v_3 \approx 0 \]  

(14)

Thus, the voltage across the parasitic ground impedance \( Z_{\text{GND}} \) is close to zero. In other words, practically no current flows through \( Z_{\text{GND}} \) at the operation frequency \( f_0 \). The residual RF current that flows thorough the parasitic ground impedance \( Z_{\text{GND}} \) in the single-ended-to-differential amplifier 300 is due to the input current expressed in Equation (8). Compared to the current that flows via ground impedance in a truly single-ended inductively degenerated common-source amplifier, the parasitic ground RF current in the single-ended-to-differential amplifier 300 according to embodiments herein is a factor of \( 2 g_{m1} Q_R \) smaller, i.e. the current gain expressed in Equation (10). As a result, in the single-ended-to-differential amplifier 300, the parasitic ground-impedance has only a minor effect, for example, on the equivalent transconductance, input matching and input impedance. This is beneficial, because inaccurately modeled Integrated Circuit (IC) package ground pins etc., will now have an ignorable effect on performance of the amplifier 300. As a result, the amplifier 300 according to embodiments herein may lower time-to-market due to an enhanced design cycle, as discussed above.

In the amplifier 300 herein, noise and nonlinearity due to the second transistor \( M2 \) are cancelled at the output current. Figure 4 shows an analyze model of the amplifier 300, the same reference numbers used in Figure 3 are used in Figure 4 for the same components. As shown in Figure 4, the noise or weak nonlinearity due to the second transistor \( M2 \) is represented by a current source of \( i_{n2} \). Again, \( Z_{\text{GND}} \) represents a parasitic ground impedance and \( R_s \) is source resistance, usually \( R_s = 50 \Omega \).

To analyze the output current \( i_{\text{OUT}^+} \) due to \( i_{n2} \), the amplifier 300 input is connected to ground via the source resistor \( R_s \). Now, the output currents are given by

\[ i_{\text{OUT}^+} = S m_3 (V_2 - V_1) = S m_1 V_{GS1} \]  

(15)

\[ i_{\text{OUT}^-} = i_{n2} + S m_2 V_{GS2} = g_m A (V_1 - V_2) \]  

(16)
Here, \( v_1 \) and \( v_2 \) are voltages at nodes 1 and 2, \( v_{GS1} \) and \( v_{GS2} \) are gate-source voltages of \( M_1 \) and \( M_2 \), and \( g_m \) is transconductance of transistor \( i \), \( M_j \), where \( i=1,2,3,4 \). Moreover, the Kirchhoff's current law for node 3 can be written as

\[
v_{3}\overset{\text{GND}}{=} i_{OUT\_+} - i_{OUT\_} = S_{M} \left( v_2 - v_1 + v_1 - v_2 \right) = 0 \tag{17}
\]

where equations (15) and (16) have been used and \( g_m = g_m \). Thus, again it is found that \( v_3 = 0 \) and thus \( i_{OUT\_} = 0 \), which implies that \( v_1 = v_2 \), since

\[
i_{OUT\_+} = g_m \left( v_2 - v_1 \right) = 0 \tag{18}
\]

As a result, also \( i_{OUT\_-} = 0 \) according equation (16). Accordingly, the amplifier 300 output current shows no component due to noise or weak nonlinearity of the second transistor \( M_2 \) in the auxiliary branch. This is a clear advantage of the single-ended-to-differential amplifier 300 according to embodiments herein.

As discussed in the background, by employing a single-ended input LNA in a receiver of a wireless communication device, the number of package pins needed for the RFIC can be lowered and the PCB routing between the FEM and RFIC can be simplified. Accordingly, the PCB area and footprint can be reduced. As a result, lower cost and bills-of-material (BOM) can be achieved. The amplifier 300 according to embodiments herein has a single-ended input, therefore the amplifier 300 achieves above advantages.

In addition, the amplifier 300 according to embodiments herein minimizes signal currents at frequencies of interest both at the ground node of the inductively degenerated transistors, such as the first and second transistors \( M_1 \) and \( M_2 \), and at supply node. Accordingly, the effect of the non-ideal ground and supply impedances on conversion gain, input impedance, noise figure of the amplifier 300 etc. are minimized. Consequently, use of the amplifier 300 can lower time-to-market due to the enhanced design cycle.

The amplifier 300 according to embodiments herein converts the single-ended input signal to a differential output signal. The single-ended-to-differential conversion is performed in such a way, that it has minimal effect on the amplifier noise or linearity performance. This is due to the fact that the noise and nonlinearity due to the second or auxiliary branch of the amplifier 300 needed to generate the complementary output signal are cancelled at the differential output signal. Thus the amplifier 300 according to
embodiments herein is suitable for using as an LNA in a receiver of a wireless communication device, as shown in Figure 5, since its input impedance can be accurately matched to a characteristic impedance of an RF pre-selection filter. As shown in Figure 5, the wireless communication device 500 comprises a Receiver 510, wherein the amplifier 300 may be implemented. The wireless communication device 500 further comprises a Transmitter 520, a Memory 530 and a Processing unit 540. Moreover, the amplifier 300 may be integrated on the same RFIC with rest of the Receiver 510 and it requires no expensive off-chip inductive balun circuits at the input of the amplifier 300 and no integrated balun circuits at the output of the amplifier 300.

The amplifier 300 according to embodiments herein is also suited for multiband receivers, since the single-ended-to-differential conversion itself is wideband while the amplifier 300 input impedance can be configured to match the RF filter output impedance at frequencies of interest. According some embodiments, a multiband receiver for operating at multiple frequency bands may comprise one or more radio-frequency filters configured to receive a single-ended input signal and to generate a single-ended output signal. The multiband receiver may further comprise one or more amplifiers 300 according to embodiments herein for converting a single-ended input signal, being the single-ended output signal generated from the radio-frequency filter, to a differential output signal.

Further, input impedances of the one or more amplifiers 300 are configured to match output impedances of the one or more radio frequency filters at operating frequencies respectively.

Corresponding embodiments of a method in a receiver for operating at multiple frequency bands will now be described with reference to Figure 6. As mentioned above, the receiver comprises one or more radio-frequency filters and one or more amplifiers 300. The method comprises following actions:

Action 601
The one or more radio-frequency filters receive a single-ended input signal.

Action 602
The one or more radio-frequency filters generate a single-ended output signal.

Action 603
The one or more amplifiers 300 receive the generated single-ended output signal.

Action 604
The one or more amplifiers 300 convert the received single-ended output signal to a differential output signal.

Those skilled in the art will understand that although the amplifier 300 is described with N-channel Metal-Oxide-Semiconductor (NMOS) devices, the amplifier 300 may comprise any other types of devices or transistors, such as Bipolar Junction Transistors (BJT), P-channel MOS (PMOS) devices, Complementary MOS (CMOS) devices etc. When using the word "comprise" or "comprising" it shall be interpreted as non-limiting, i.e. meaning "consist at least of".

The embodiments herein are not limited to the above described preferred embodiments. Various alternatives, modifications and equivalents may be used. Therefore, the above embodiments should not be taken as limiting the scope of the invention, which is defined by the appending claims.
CLAIMS

1. An amplifier (300) for converting a single-ended input signal to a differential output signal, the amplifier (300) comprising:
   a first transistor (301), configured in common-source or common-emitter mode, to receive the single-ended input signal and generate a first part of the differential output signal;
   a second transistor (302), configured in common-source or common-emitter mode, to generate a second part of the differential output signal;
   a third transistor (303) and a fourth transistor (304), and wherein the third transistor (303) and forth transistor (304) are cross-coupled and connected to the first and second transistors (301,302) such that:
      a drain or collector of the first transistor (301) is coupled to a gate or base of the fourth transistor (304) via a first capacitor (311);
      a drain or collector of the second transistor (302) is coupled to a gate or base of the third transistor (303) via a second capacitor (312); and
      the drain or collector of the first transistor (301) is connected to a source or emitter of the third transistor (303), the drain or collector of the second transistor (302) is connected to a source or emitter of the fourth transistor (304); and further
      the drain or collector of the first transistor (301) is coupled to a gate or base of the second transistor (302) directly or via a third capacitor (313);
      a source or emitter of the first transistor (301) is connected to a first inductor (321) and a source or emitter of the second transistor (302) is connected to a second inductor (322).

2. The amplifier (300) according to claim 1, wherein the amplifier (300) further comprises a matching circuit (330), and wherein a gate or base of the first transistor (301) is coupled to the single-ended input signal through the matching circuit (330).

3. The amplifier (300) according to any of the claims 1-2, wherein the first and second inductors (321,322) comprise a single differential inductor.
4. The amplifier (300) according to any of the claims 1-3, wherein an input impedance of the amplifier (300) is configured to match an output impedance of a radio frequency filter.

5. The amplifier (300) according to any of the claims 1-4, wherein the first and second inductors (321, 322) are coupled to ground via a parasitic impedance (340).

6. A wireless communication device (500) comprising one or more amplifiers (300) according to any of the claims 1-5.

7. A receiver (510) for operating at multiple frequency bands, the receiver comprising:
   one or more radio-frequency filters configured to receive a single-ended input signal and to generate a single-ended output signal;
   one or more amplifiers (300) according to any of the claims 1-5 configured to convert a single-ended input signal, being the single-ended output signal generated from the radio-frequency filter, to a differential output signal; and wherein
   input impedances of the one or more amplifiers (300) are configured to match output impedances of the one or more radio frequency filters at operating frequencies respectively.

8. A method in a receiver (510) for operating at multiple frequency bands, the method comprising:
   receiving (601) in one or more radio-frequency filters, a single-ended input signal,
   generating (602) in the one or more radio-frequency filters, a single-ended output signal;
   receiving (603) the generated single-ended output signal in one or more amplifiers (300) according to any of the claims 1-5;
   converting (604) the received single-ended output signal to a differential output signal in the one or more amplifiers (300) according to any of the claims 1-5, wherein input impedances of the one or more amplifiers (300) are configured to match output impedances of the one or more radio frequency filters at operating frequencies respectively.
Fig. 1 Prior art
Single-ended to differential LNA

Matching circuit

$V_{IN}$

$Z_{GND}$
Fig. 5

Processing unit 540
Memory 530
Receiver 510
LNA 300
Transmitter 520
Transceiver

Wireless communication device 500
601. Receives in one or more radio-frequency filters single-ended input signal

602. Generates in the one or more radio-frequency filters single-ended output signal

603. Receives the generated single-ended output signal in one or more amplifiers according to embodiments herein

604. Converts received single-ended output signal to differential output signal in the one or more amplifiers

Fig. 6
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03F3/193 H03F1/22 H03F1/26

ADD.

According to International Patent Classification (IPC) or both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H03B H03H H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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</tr>
</thead>
</table>

Further documents are listed in the continuation of Box C.

X See patent family annex.

* Special categories of cited documents:

"X" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or one which may establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search
29 April 2015

Date of mailing of the international search report
08/05/2015

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<table>
<thead>
<tr>
<th>Category</th>
<th>Citation</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2008199611 A</td>
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<tr>
<td></td>
<td></td>
<td>KR 20080074336 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 2008191807 A1</td>
</tr>
<tr>
<td>US 6366171 B1</td>
<td>02-04-2002</td>
<td>NONE</td>
</tr>
</tbody>
</table>

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