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[Continued on next page]

(54) Title: TO CALIBRATE AN APPARATUS TO RECEIVE DATA SIGNALS

(57) Abstract: A method to calibrate an apparatus to receive data signals in which a clock signal is received from a low voltage differential signaling (LVDS) line. A plurality of data signals are received from a plurality of low voltage differential signaling (LVDS) lines according to a predetermined fixed calibration sequence. The apparatus is calibrated using the received clock signal and the plurality of received data signals to account for differences in latency between the low voltage differential signaling (LVDS) lines.

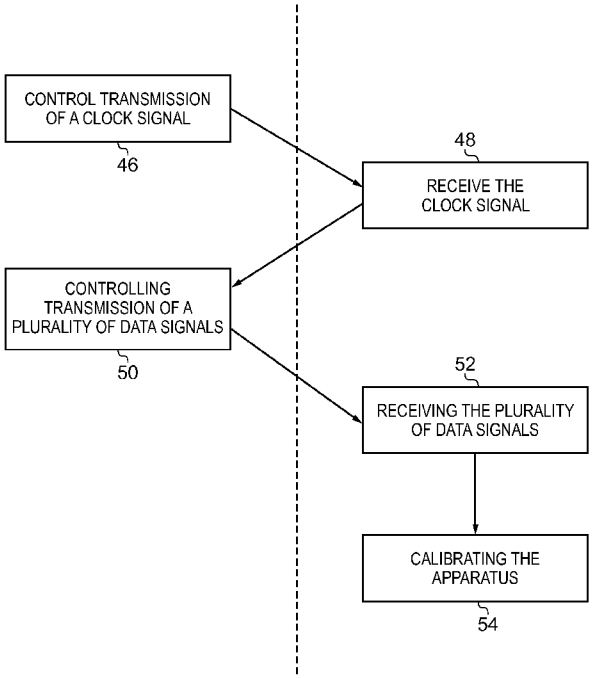


FIG. 2

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TITLE

To calibrate an apparatus to receive data signals

BACKGROUND

Apparatus, such as computing devices and displays, may be connected to one another via at least one wired connection. The wired connection may include at least one low voltage differential signaling (LVDS) line.

Low voltage differential signaling (LVDS) lines usually include a pair of cables that are relatively inexpensive (the cables may comprise copper) and are able to operate at relatively low power and at relatively high speeds (for example, 650 Mbit/s or greater).

BRIEF DESCRIPTION

Reference will now be made by way of example only to the accompanying drawings in which:

Fig. 1 illustrates a schematic diagram of a communication system according to an example;

Fig. 2 illustrates a flow diagram of a method according to an example; and

Fig. 3 illustrates a flow diagram of another method according to an example.

DETAILED DESCRIPTION

As used herein, the terms 'connected' and 'coupled' include operationally connected and coupled and may any number or combination of intervening elements (including no intervening elements).

Fig. 1 illustrates a schematic diagram of a communication system 10 including a first apparatus 12 and a second apparatus 14 coupled to one another via a wired connection 16.

The first apparatus 12 may be any suitable electronic device for transmitting data to the second apparatus 14. For example, the first apparatus 12 may be a computing device such as a desktop computer. The first apparatus 12 includes at least a first controller 18 and a transmitter 20. In some examples, the first apparatus 12 may be a module. As used herein, 'module' refers to a unit or apparatus that excludes certain parts/components that would be added by an end manufacturer or a user.

The implementation of the first controller 18 can be in hardware alone (for example, a circuit, a processor, etc.), have certain aspects in software including firmware alone or can be a combination of hardware and software (including firmware).

The first controller 18 may be implemented using instructions that enable hardware functionality, for example, by using executable computer program instructions 26 in a general-purpose or special-purpose processor 22 that may be stored on a computer readable storage medium 24 (disk, memory etc) to be executed by such a processor 22.

The processor 22 is configured to read from and write to the memory 24. The processor 22 may also comprise an output interface via which data and/or commands are output by the processor 22 and an input interface via which data and/or commands are input to the processor 22.

The memory 24 stores a computer program 26 comprising computer program instructions that control the operation of the first apparatus 12 when loaded into the processor 22. The computer program instructions 26 provide the

logic and routines that enables the first apparatus 12 to perform the methods illustrated in Figs. 2 and 3 and described in the following paragraphs. The processor 22 by reading the memory 24 is able to load and execute the computer program 26.

The computer program 26 may arrive at the first apparatus 12 via any suitable delivery mechanism 28. The delivery mechanism 28 may be, for example, a non-transitory computer-readable storage medium, a computer program product, a memory device, a record medium such as a compact disc read-only memory (CD-ROM) or digital versatile disc (DVD), an article of manufacture that tangibly embodies the computer program 28. The delivery mechanism 28 may be a signal configured to reliably transfer the computer program 28. The first apparatus 12 may propagate or transmit the computer program 26 as a computer data signal.

The transmitter 20 is arranged to transmit a clock signal via a first low voltage differential signal line 30, a data signal via a second low voltage differential signal line 32, and a data signal via a third low voltage differential signal line 34. The controller 18 is arranged to control the transmitter 20 to transmit the clock signal and the data signals.

The second apparatus 14 may be any suitable electronic device for receiving data from the first apparatus 12. For example, the second apparatus 14 may be a display device such as a liquid crystal display or a light emitting diode display. The second apparatus 14 includes at least a second controller 36 and a receiver 38. In some examples, the second apparatus 14 may be a module. As used herein, 'module' refers to a unit or apparatus that excludes certain parts/components that would be added by an end manufacturer or a user.

The implementation of the second controller 36 can be in hardware alone (for example, a circuit, a processor, etc.), have certain aspects in software

including firmware alone or can be a combination of hardware and software (including firmware).

The second controller 36 may be implemented using instructions that enable hardware functionality, for example, by using executable computer program instructions 44 in a general-purpose or special-purpose processor 40 that may be stored on a computer readable storage medium 42 (disk, memory etc) to be executed by such a processor 40.

The processor 40 is configured to read from and write to the memory 42. The processor 40 may also comprise an output interface via which data and/or commands are output by the processor 40 and an input interface via which data and/or commands are input to the processor 40.

The memory 42 stores a computer program 44 comprising computer program instructions that control the operation of the second apparatus 14 when loaded into the processor 40. The computer program instructions 44 provide the logic and routines that enables the second apparatus 14 to perform the methods illustrated in Figs. 2 and 3 and described in the following paragraphs. The processor 40 by reading the memory 42 is able to load and execute the computer program 44. The computer program 44 may arrive at the second apparatus 14 via the delivery mechanism 28. The second apparatus 14 may propagate or transmit the computer program 44 as a computer data signal.

The receiver 38 is arranged to receive the clock signal via the first low voltage differential signal line 30, a data signal via the second low voltage differential signal line 32, and a data signal via the third low voltage differential signal line 34. The controller 36 is arranged to receive the clock signal and data signals from the receiver 38.

The wired connection 16 is arranged to connect the transmitter 20 of the first apparatus 12 to the receiver 38 of the second apparatus 14. The wired

connection 16 includes the first low voltage differential signal line 30, the second low voltage differential signal line 32 and the third low voltage differential signal line 34. In other examples, the wired connection 16 may include any number of low voltage differential signal lines. The low voltage differential signaling (LVDS) lines 30, 32, 34 are unidirectional (in other words, the clock and data signals are transmitted from the first apparatus 12 to the second apparatus 14).

The operation of the communication system 10 is described in the following paragraphs with reference to Figs. 2 and 3.

Fig. 2 illustrates a flow diagram of a method according to an example. The left hand side column represents the blocks performed at the first apparatus 12, and the right hand side column represents the blocks performed at the second apparatus 14.

At block 46, the controller 18 controls the transmission of a clock signal via the low voltage differential signaling (LVDS) line 30.

At block 48, the controller 36 receives the clock signal from the low voltage differential signaling (LVDS) line 30.

At block 50, the controller 18 controls the transmission of a plurality of data signals via a plurality of low voltage differential signaling (LVDS) lines (the second low voltage differential signaling line 32 and the third low voltage differential signaling line 34 in this example) according to a predetermined fixed calibration sequence.

The calibration sequence is 'fixed' in that the calibration sequence may not change between calibrations. The calibration sequence is 'predetermined' in that the plurality of data signals are known to the first apparatus 12 and to the second apparatus 14 prior to the calibration sequence being performed.

At block 52, the controller 36 receives the plurality of data signals from the plurality of low voltage differential signaling (LVDS) lines (the second low voltage differential signaling line 32 and the third low voltage differential signaling line 34 in this example) according to the predetermined fixed calibration sequence. The plurality of data signals (which may also be referred to as calibration words) may use balanced words (that is, an equal number of '0' and '1') that may allow DC-coupling techniques.

At block 54, the controller 36 calibrates the second apparatus 14 using the received clock signal and the plurality of received data signals to account for differences in latency between the low voltage differential signaling (LVDS) lines (namely, the second low voltage differential signaling line 32 and the third low voltage differential signaling line 34 in this example).

Fig. 3 illustrates a flow diagram of another method according to an example. Similarly to Fig. 2, the left hand side column represents the blocks performed at the first apparatus 12, and the right hand side column represents the blocks performed at the second apparatus 14.

At block 56, the first controller 18 initiates calibration of the second apparatus 14 by controlling the transmitter 20 to not transmit a clock signal to the second apparatus 14 via the first low voltage differential signaling (LVDS) line 30 for a predetermined period of time. For example, the first controller 18 may control the transmitter 20 to not transmit a clock signal to the second apparatus 14 for a time period of 40 clock cycles.

At the end of the predetermined period of time, the first controller 18 controls the transmission of a clock signal via the first low voltage differential signaling (LVDS) line 30. The frequency of the clock signal may be less than the frequency of the plurality of data signals transmitted across the second and third low voltage differential signaling lines 32 and 34. For example, the clock

signal may have frequency that is eight times less than the frequency of the data signals.

At block 58, the second controller 36 controls initiation of the calibration of the second apparatus 14 in response to not receiving the clock signal for the predetermined period of time. Subsequently, the second controller 36 detects the clock signal and may determine whether the clock signal has an adequate frequency (for example, the second controller 36 may determine whether the clock signal has a predetermined frequency). If the frequency of the cock signal is inadequate, the second controller 36 continues to detect the clock signal. If the frequency of the clock signal is adequate, the second controller 36 then receives the clock signal from the first low voltage differential signaling (LVDS) line 30.

At block 60, the first controller 18 controls the transmitter 20 to transmit a first predetermined data signal via the second and third low voltage differential signaling lines 32 and 34. For example, the first controller 18 may control the transmitter 20 to transmit 1000 'b00110011' sequences via the second and third low voltage differential signaling lines 32 and 34.

At block 62, the second controller 36 detects the first predetermined data signal using the detected clock signal. For example, the second controller 36 may multiply the incoming clock signal so that the frequency of the clock signal and the data signals are the same (for example, the clock signal may be multiplied by eight) and uses the result to sample incoming data signals. The second controller 36 and the receiver 38 are not aligned to the incoming clock signal, but regardless of the clock to bit alignment, due to the 2 bit 0/1 sequence, the second controller 36 and receiver 38 are able to detect the different data states.

At block 64, the first controller 18 controls the transmitter 20 to transmit a second predetermined data signal via the second and third low voltage

differential signaling lines 32 and 34. For example, the first controller 18 may control the transmitter to transmit 20000 'b01010101' sequences via the second and third low voltage differential signaling lines 32 and 34.

At block 66, the second controller 36 performs clock phase alignment with the received second predetermined data signal. For example, the second controller 36 may modify the clock signal to 8 different phases and may then test for the 'b01010101' sequence in each tested phase. For one phase, the second controller 36 determines that the data is not sampled correctly and then selects a phase for the clock signal for that low voltage differential signaling line that is the opposite to the phase where the data is not sampled correctly. Alternatively, the second controller 36 may select the phase for the clock signal for that low voltage differential signaling line that has the most accurate sampling of the data. The selected clock phase for each low voltage differential signaling line may be stored in the memory 42. The second controller 36 may use the stored selected clock phase for a low voltage differential signaling line when receiving data on that low voltage differential signaling line.

At block 68, the first controller 18 controls the transmitter 20 to transmit a third predetermined data signal via the second and third low voltage differential signaling lines 32 and 34. For example, the first controller 18 may control the transmitter 20 to transmit 800 'b11001001' signals.

At block 70, the second controller 36 performs word alignment using the received third predetermined data signal. For example, the second controller 36 may shift the received third predetermined data signal incrementally by 1 bit until the received byte matches the 'b11001001' pattern. For each low voltage differential signaling line, the second controller 36 may store the shift value that provided the match in the memory 42. The second controller 36 may use the stored shift value for a low voltage differential signaling line when receiving data on that low voltage differential signaling line.

Subsequent to block 70, the first and second apparatus 12, 14 are advantageously synchronized to one another due to the calibration of the low voltage differential signaling lines 32, 34, and application data may flow from the first apparatus 12 to the second apparatus 14. The second controller 36 and the receiver 40 may wait for a data signal having a value different to 'b11001001' to identify the beginning of the flow of application data.

Subsequent to the communication system 10 being calibrated, data may be encoded using a pseudo-random binary sequence (PRBS). This may be advantageous in that electromagnetic energy produced by the communication system 10 is distributed more evenly in different frequencies. Additionally, this may also advantageously maintain a balance between '0' and '1' that allows the communication system 10 to use DC coupling techniques.

The apparatus and methods described in the preceding paragraphs may provide several advantages. Firstly, since the low voltage differential signaling lines are calibrated independently of one another and to a common clock signal, the calibration accounts for differences in latency between the low voltage differential signaling (LVDS) lines. Consequently, the low voltage differential signaling lines may be relatively fast and provide data speeds of 1Gbit/s per line.

Secondly, the communication system 10 may have a low electromagnetic compatibility emission profile due to the relatively low clock signal frequency (relative to the frequency of the data signals).

Thirdly, the communication system 10 may be scalable since the appropriate number of low voltage differential signaling lines and the frequency of the clock signal may be selected to provide an optimum implementation.

Fourthly, the communication system 10 may be relatively low cost since the first and second apparatus 12, 14 may be provided by field programmable gate arrays (FPGAs) and the wired connection may be provided by a HDMI cable, a mini HDMI cable, a DVI cable, or a USB cable. Consequently, the communication system 10 may enable a multi-gigabit wired connection that has a relatively low cost.

The blocks illustrated in the Figs. 2 and 3 may represent steps in a method and/or sections of code in the computer programs 26 and 44. The illustration of a particular order to the blocks does not necessarily imply that there is a required or preferred order for the blocks and the order and arrangement of the block may be varied in some examples. Furthermore, it may be possible for some blocks to be omitted in some examples.

Although examples have been described in the preceding paragraphs, it should be appreciated that modifications to the examples given can be made without departing from the scope as claimed. For example, the patterns for the first, second and third predetermined data signals may be different in other examples. Additionally, the first, second and third predetermined data signals may be identical to one another and have the same pattern (for example, the pattern may be 8'b01110001 (0x71)). In other words, a single predetermined data signal may be used in the predetermined fixed calibration sequence.

Although the processors 22, 40 are illustrated as single components, they may be implemented as one or more separate components some or all of which may be integrated/removable.

Although the memories 26, 42 are illustrated as single components, they may be implemented as one or more separate components some or all of which may be integrated/removable and/or may provide permanent/semi-permanent/ dynamic/cached storage.

References to 'computer-readable storage medium', 'computer program product', 'tangibly embodied computer program' etc. or a 'controller', 'computer', 'processor' etc. should be understood to encompass not only computers having different architectures such as single /multi- processor architectures and sequential (Von Neumann)/parallel architectures but also specialized circuits such as field-programmable gate arrays (FPGA), application specific circuits (ASIC), signal processing devices and other processing circuitry. References to computer program, instructions, code etc. should be understood to encompass software for a programmable processor or firmware such as, for example, the programmable content of a hardware device whether instructions for a processor, or configuration settings for a fixed-function device, gate array or programmable logic device etc.

Features described in the preceding description may be used in combinations other than the combinations explicitly described.

Although functions have been described with reference to certain features, those functions may be performable by other features whether described or not.

Although features have been described with reference to certain examples, those features may also be present in other examples whether described or not.

Whilst endeavoring in the foregoing specification to draw attention to those features believed to be of particular importance it should be understood that the Applicant claims protection in respect of any patentable feature or combination of features hereinbefore referred to and/or shown in the drawings whether or not particular emphasis has been placed thereon.

I/we claim:

CLAIMS

1. A method to calibrate an apparatus to receive data signals, the method comprising:

receiving a clock signal from a low voltage differential signaling (LVDS) line;

receiving a plurality of data signals from a plurality of low voltage differential signaling (LVDS) lines according to a predetermined fixed calibration sequence; and

calibrating the apparatus using the received clock signal and the plurality of received data signals to account for differences in latency between the low voltage differential signaling (LVDS) lines.

2. A method as claimed in claim 1, wherein the frequency of the clock signal is less than the frequency of the plurality of data signals.

3. A method as claimed in claim 1, wherein the low voltage differential signaling (LVDS) lines are unidirectional.

4. A method as claimed in claim 1, further comprising controlling initiation of the calibration of the apparatus in response to not receiving a clock signal for a predetermined period of time.

5. A method as claimed in claim 1, further comprising detecting the clock signal and determining whether the clock signal has a predetermined frequency.

6. A method as claimed in claim 5, further comprising detecting a first predetermined data signal using the detected clock signal.

7. A method as claimed in claim 1, further comprising performing clock phase alignment with a received second predetermined data signal.

8. A method as claimed in claim 1, further comprising performing word alignment using a received third predetermined data signal.

9. A method to calibrate an apparatus to receive data signals, the method comprising:

controlling transmission of a clock signal via a low voltage differential signaling (LVDS) line;

controlling transmission of a plurality of data signals via a plurality of low voltage differential signaling (LVDS) lines according to a predetermined fixed calibration sequence to calibrate an apparatus to account for differences in latency between the low voltage differential signaling (LVDS) lines.

10. A method as claimed in claim 9, further comprising initiating calibration of the apparatus by not transmitting a clock signal to the apparatus via the low voltage differential signaling (LVDS) line for a predetermined period of time.

11. Apparatus comprising:

a controller to:

receive a clock signal from a low voltage differential signaling (LVDS) line;

receive a plurality of data signals from a plurality of low voltage differential signaling (LVDS) lines according to a predetermined fixed calibration sequence; and

calibrate the apparatus using the received clock signal and the plurality of received data signals to account for differences in latency between the low voltage differential signaling (LVDS) lines.

12. Apparatus as claimed in claim 11, wherein the low voltage differential signaling (LVDS) lines are unidirectional.

13. Apparatus as claimed in claim 11, wherein the controller is to control initiation of the calibration of the apparatus in response to not receiving a clock signal for a predetermined period of time.

14. Apparatus as claimed in claim 11, wherein the controller is to perform clock phase alignment with a received second predetermined data signal.

15. Apparatus method as claimed in claim 1, wherein the controller is to perform word alignment using a received third predetermined data signal.

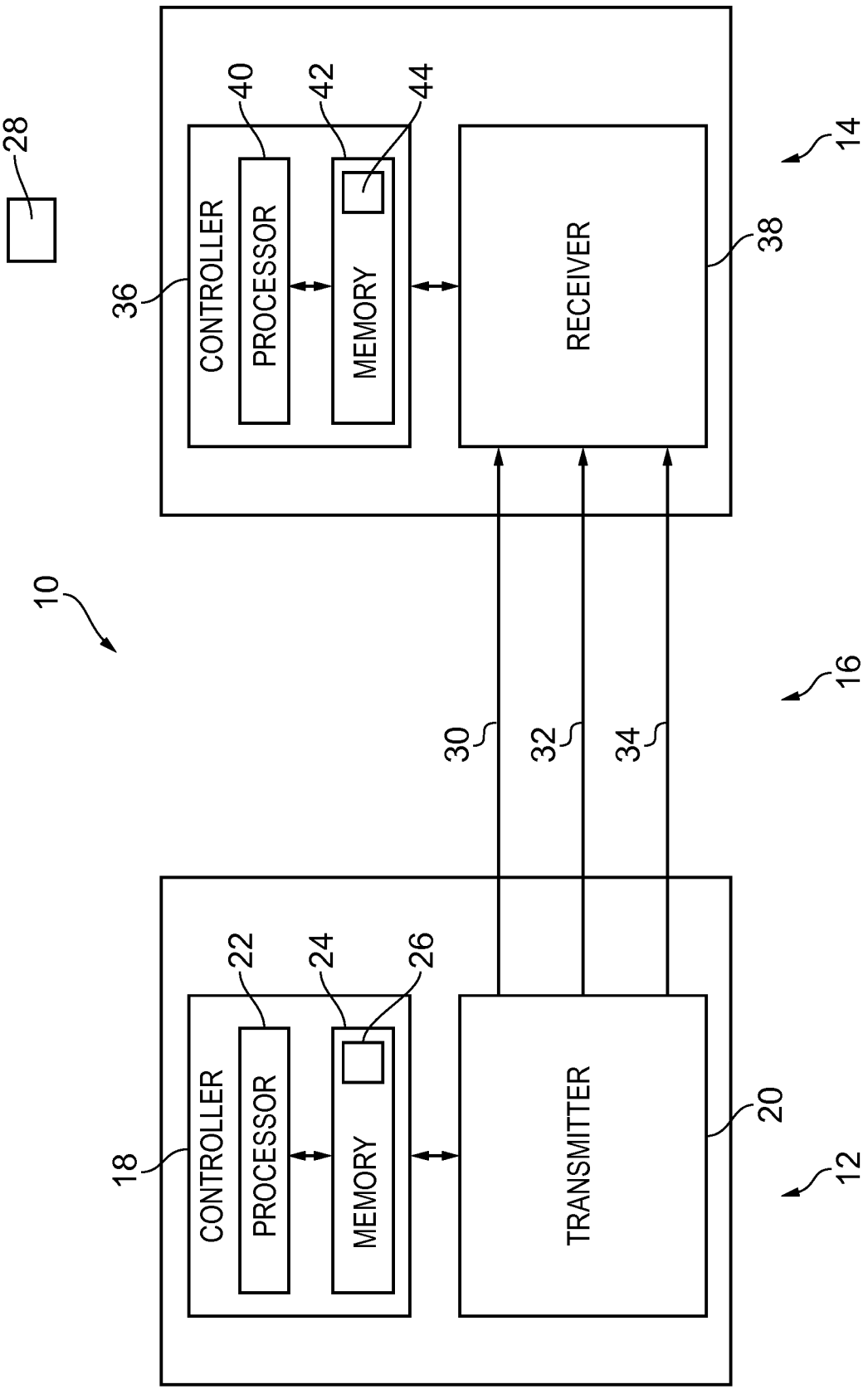

28
40
42
44
14
CONTROLLER
PROCESSOR
MEMORY
RECEIVER
36
38
10
16
30
32
34
22
24
26
18
CONTROLLER
PROCESSOR
MEMORY
TRANSMITTER
20
12

FIG. 1

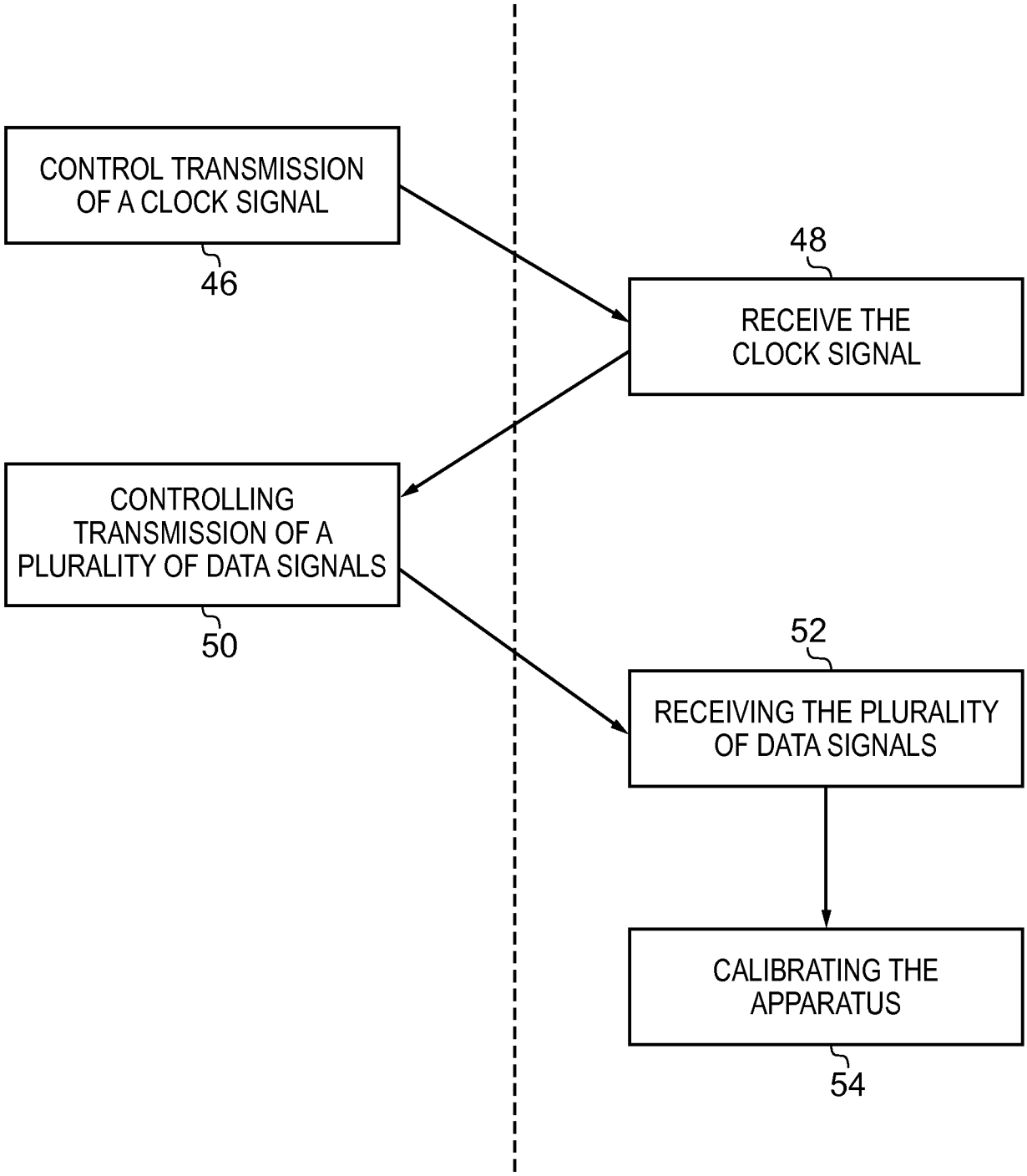

CONTROL TRANSMISSION OF A CLOCK SIGNAL
46
48
RECEIVE THE CLOCK SIGNAL
CONTROLLING TRANSMISSION OF A PLURALITY OF DATA SIGNALS
50
52
RECEIVING THE PLURALITY OF DATA SIGNALS
CALIBRATING THE APPARATUS
54

FIG. 2

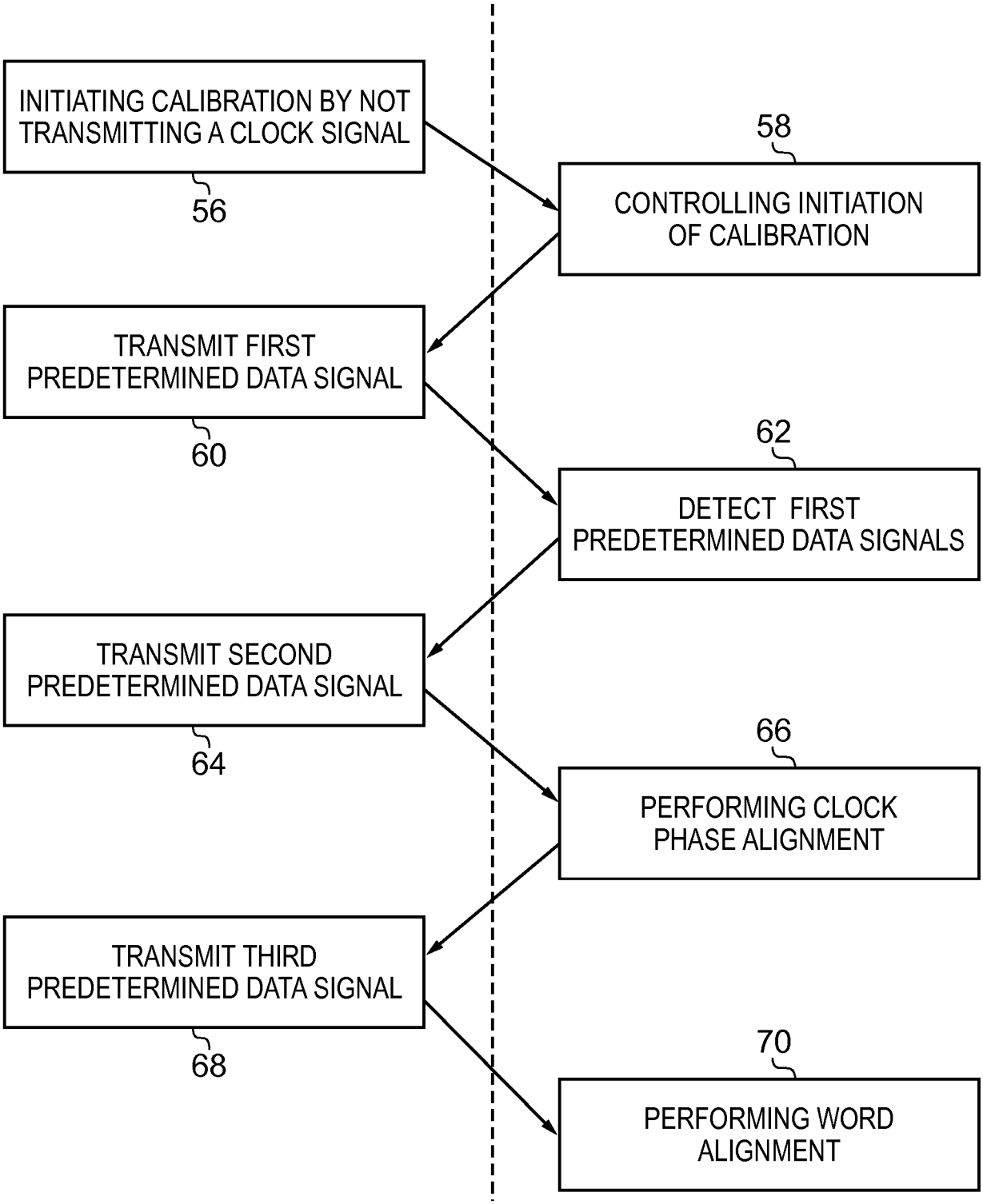

INITIATING CALIBRATION BY NOT TRANSMITTING A CLOCK SIGNAL
56
58
CONTROLLING INITIATION OF CALIBRATION
TRANSMIT FIRST PREDETERMINED DATA SIGNAL
60
62
DETECT FIRST PREDETERMINED DATA SIGNALS
TRANSMIT SECOND PREDETERMINED DATA SIGNAL
64
66
PERFORMING CLOCK PHASE ALIGNMENT
TRANSMIT THIRD PREDETERMINED DATA SIGNAL
68
70
PERFORMING WORD ALIGNMENT

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/061698

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F13/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/141335 A1 (STARK DONALD C [US]) 30 June 2005 (2005-06-30) paragraph [0025] paragraph [0035] figure 4 figures 5A,5B -----	1-15
A	US 2008/120457 A1 (GILLINGHAM PETER [CA] ET AL) 22 May 2008 (2008-05-22) figure 10B ----- -/--	1-15

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 January 2015	05/02/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Braccini, Guido

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/061698

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	"IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI);IEEE Std 1596.3-1996", IEEE STANDARD, IEEE, PISCATAWAY, NJ, USA, 1 January 1996 (1996-01-01), page i, XP017602994, ISBN: 978-1-55937-746-1 page 5 -----	1-15

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2014/061698

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