

FORM 1
REGULATION 9

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952-1973

APPLICATION FOR A PATENT

628154

We INTERNATIONAL CONTROL AUTOMATION FINANCE S.A.

of Ville de Luxembourg, 16 Rue des Bains, LUXEMBOURG

hereby apply for the grant of a Patent for an invention entitled:

FREQUENCY SHIFT KEYING MODULATION AND DEMODULATION FOR SERIAL
COMMUNICATION ON A CURRENT LOOP

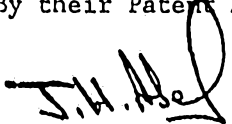
which is described in the accompanying complete specification. This
Application is a Convention Application and is based on the
Application numbered: 337,006 for a Patent or similar protection
made in U.S.A. on 12 April 1989.

Our address for service is:

GRIFFITH HACK & CO
71 YORK STREET
SYDNEY NSW 2000

DATED this 11th day of April 1990

INTERNATIONAL CONTROL AUTOMATION FINANCE S.A.
By their Patent Attorney



GRIFFITH HACK & CO

TO: THE COMMISSIONER OF PATENTS
COMMONWEALTH OF AUSTRALIA

5014214 11/04/90

7442A:rk

PATENTS ACT 1952 (AS AMENDED)

DECLARATION IN SUPPORT OF AN APPLICATION FOR A PATENT

(Name of applicant) In support of an Application made by: International Control Automation Finance S.A.

(Title) for a patent for an invention entitled: FREQUENCY SHIFT KEYING MODULATION AND DEMODULATION FOR SERIAL COMMUNICATION ON A CURRENT LOOP

(Full name of signatory) I, Michael L. Hoelter
(Address of signatory) of 117 Millsaps Place
Kenner, La 70065

do solemnly and sincerely declare as follows:

1. I am authorised by the above mentioned applicant for the patent to make this Declaration on its behalf.

(Insert details of inventor/s)

2. The name and address of each actual inventor of the invention is as follows:
Edward Bastijanic and Joseph C. Nemer
of 7064 Bristlewood Drive, Concord, OHIO 44077, U.S.A. and
1262 Lander Road, Mayfield Heights, OHIO 44124, U.S.A., respectively

(Insert details of assignment, etc.)

and the fact(s) upon which the applicant is entitled to make this application are as follows:
INTERNATIONAL CONTROL AUTOMATION FINANCE S.A.,
the Applicant, is the Assignee of the invention from BABCOCK & WILCOX TRACEY POWER, INC; BABCOCK & WILCOX TRACEY POWER, INC. is the Assignee of the invention from THE BABCOCK & WILCOX COMPANY; and THE BABCOCK & WILCOX COMPANY is the Assignee of the invention from the actual inventors.

Delete paragraphs and 4 or non-convention application)

3. The basic application(s) as defined by Section 141 of the Act was(were) made as follows:
Country U.S.A. on . . . 12 April 1989
in the name(s) Edward Bastijanic and Joseph C. Nemer
and in on
in the name(s)
and in on
in the name(s)

4. The basic application(s) referred to in the preceding paragraph of this Declaration was(were) the first application(s) made in a Convention country in respect of the invention the subject of this application.

(Place and date of signing)

Declared at New Orleans this 23rd day of October- 1990

Signed: [Signature]
Position: Patent Attorney

(12) PATENT ABRIDGMENT (11) Document No. AU-B-53170/90
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 628154

- (54) Title
FREQUENCY SHIFT KEYING MODULATION AND DEMODULATION FOR SERIAL COMMUNICATION ON A CURRENT LOOP
- (51)⁵ International Patent Classification(s)
H04L 012/42 H04L 027/12 H04L 027/14
- (21) Application No. : **53170/90** (22) Application Date : **11.04.90**
- (30) Priority Data
- (31) Number (32) Date (33) Country
337006 12.04.89 US UNITED STATES OF AMERICA
- (43) Publication Date : **18.10.90**
- (44) Publication Date of Accepted Application : **10.09.92**
- (71) Applicant(s)
INTERNATIONAL CONTROL AUTOMATION FINANCE S.A.
- (72) Inventor(s)
EDWARD BASTIJANIC; JOSEPH C. NEMER
- (74) Attorney or Agent
GRIFFITH HACK & CO. , GPO Box 4164, SYDNEY NSW 2001
- (57) Claim

1. A 4 to 20 mA D.C. current loop arrangement having a frequency shift keying oscillating signal superimposed thereon to permit reliable on-line communication between low power devices normally using 4 - 20 mA D.C. current value comprising:

a power supply for producing 4 to 20 mA D.C. current;

a current loop connected to said power supply for carrying said current;

modulating means for producing frequency shift keying oscillating signals including a digitally controlled oscillator having a low level capacitor selectively chargeable and discharging at a first rate and at a second rate corresponding to first and second frequency shift keying frequencies respectively; and

transformer means for connecting said modulating means to said current loop while isolating same from said oscillator to superimpose said frequency shift keying frequencies on said 4 to 20 mA D.C. current to permit on-

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line communication of said frequency shift keying
frequencies onto said current loop to low power devices
therein.

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

Form 10

620154

COMPLETE SPECIFICATION

FOR OFFICE USE

Short Title:

Int. Cl.:

Application Number:
Lodged:

Complete Specification-Lodged:
Accepted:
Lapsed:
Published:

Priority:

Related Art:

TO BE COMPLETED BY APPLICANT

Name of Applicant: INTERNATIONAL CONTROL AUTOMATION
FINANCE S.A.

Address of Applicant: Ville de Luxembourg, 16 Rue des Bains,
LUXEMBOURG

Actual Inventor: Edward Bastijanic and Joseph C. Nemer

Address for Service: GRIFFITH HACK & CO
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SYDNEY NSW 2000

Complete Specification for the invention entitled:

FREQUENCY SHIFT KEYING MODULATION AND
DEMODULATION FOR SERIAL COMMUNICATION ON A
CURRENT LOOP

The following statement is a full description of this
invention, including the best method of performing it
known to us:-

21302-H:GOS:RK

7442A:rk

- 1A

FREQUENCY SHIFT KEYING MODULATION AND
DEMULATION FOR SERIAL COMMUNICATION ON
A CURRENT LOOP

TECHNICAL FIELD

5 The present invention relates, in general, to modulation and demodulation techniques and, more particularly, to a frequency shift keying modulation and demodulation technique on a current loop.

BACKGROUND ART

10 Frequency Shift Keying (FSK) is a form of frequency modulation commonly used in low-speed modems in which the two
15 states of the signal are transmitted at two separate frequencies. A 1 is transmitted by a predefined signal frequency (space frequency) and a 0 is transmitted by another predefined
20 signal frequency (mark frequency). In noisy environments, it has been found that FSK has more noise immunity than other forms of modulation, such as amplitude modulation or phase modulation. In power limited devices, such as loop transmitters and battery
25 powered devices, the use of FSK for on-line communication between the transmitter and another device typically requires a substantial amount of power due to the numerous circuit elements required to decode and encode the FSK signals. In order to minimize power usage, modulation techniques not utilizing frequency shift keying have been developed, such as that employed in U.S. Patent No. 4,607,247 (Sterling, Jr., et al).

 Because of the foregoing, it has become desirable to develop a frequency shift keying modulation system and demodulation system which minimizes overall power usage and hardware requirements.

SUMMARY OF THE INVENTION

According to the present invention there is provided a 4 to 20 mA D.C. current loop arrangement having a frequency shift keying oscillating signal superimposed thereon to permit reliable on-line communication between low power devices normally using 4-20 mA D.C. current value comprising:

a power supply for producing 4 to 20 mA D.C. current;

10 a current loop connected to said power supply for carrying said current;

modulating means for producing frequency shift keying oscillating signals including a digitally controlled oscillator having a low level capacitor selectively chargeable and discharging at a first rate and at a second rate corresponding to first and second frequency shift keying frequencies respectively; and

transformer means for connecting said modulating means to said current loop while isolating same from said oscillator to superimpose said frequency shift keying frequencies on said 4 to 20 mA D.C. current to permit on-line communication of said frequency shift keying frequencies onto said current loop to low power devices



therein.

Preferably the current loop arrangement further includes means for demodulating a modulated signal on said current loop, said demodulating means producing
5 frequency shift keying pulses representative of said modulated signal.

Also preferably said demodulating means further includes comparator means connected to said digitally controlled oscillator in a phase-locked loop arrangement.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic drawing of the frequency shift keying modulation system of the present invention.

Figure 2 illustrates waveforms at various points within the modulation system shown in Figure 1.

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Figure 3 is a schematic drawing of the frequency shift keying demodulation system of the present invention.

Figure 4 illustrates waveforms at various points within the demodulation system shown in Figure 3.



DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings where the illustrations are for the purpose of describing the preferred embodiment of the present invention and are not intended to limit the invention hereto, Figure 1 is a schematic diagram of the frequency shift keying modulation system 10 of the present invention. The system 10 is comprised of a transmitting interface device 12, a digitally controlled oscillator 14, a power supply 16 powering a current loop 18, and a circuit 20 interconnecting the digitally controlled oscillator 14 and the current loop 18.

The interface device 12 is commonly referred to as an RS-232, or the like, and is properly referred to as an Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange. The interface device 12 generates a supply voltage V_s for one of the two possible signal states (space frequency) and a 0 output voltage for the other signal state (mark frequency). The output of the interface device 12 is connected to an input to an OR gate 30 within the digitally controlled oscillator 14. The other input to the OR gate 30 is connected at point B to one side of a resistor 32 and to the input to an inverter 34. The output of the OR gate 30 is connected to a resistor 36 which is connected to the other side of resistor 32 at point A. The output of inverter 34 is connected at point C to the input to an inverter 38 and to one side of a resistor 40. The other side of resistor 40 is connected to resistors 32 and 36 at point A. A capacitor 42 is connected from point A to the output of inverter 38 (point D). The output of inverter 38, which represents the output of the digitally controlled oscillator 14, is connected to the input to an inverter 44. The output of inverter 44 is connected to a series combination of a resistor 46 and a capacitor 48 which is connected to one side of a transformer 50 which is grounded. The



other side of the transformer 50 is connected across the current loop 18 via a resistor 52 and a capacitor 54. The current loop 18 includes a resistor 56 and is connected to the output of the power supply 16 that can typically draw a minimum of 4 mA to a maximum of 20 mA.

Operationally, the output voltage of the interface device 12 controls the frequency of the digitally controlled oscillator 14. Referring to Figure 2, the output of the interface device 12 is shown as waveform F. The other waveforms shown in Figure 2 represent the voltages at various points within the modulation system 10 and correspond with the letters shown on Figure 1. With respect to waveform F, presence of a supply voltage V_s at the output of the interface device 12 results in the digitally controlled oscillator 14 producing a predefined upper signal frequency (space frequency), whereas \emptyset voltage at the output of the interface device 12 results in the oscillator 14 producing a predefined lower signal frequency (mark frequency). When a supply voltage V_s exists at point F, the OR gate 30 acts as an inverter for the signal at point B. The presence of a voltage at point B, as shown in Figure 2 (point a), causes the voltages at points E and C to be 0 and the voltage at point D to be the supply voltage V_s . Inasmuch as OR gate 30 and inverter 34 have high input impedances, a negligible current flows through resistor 32 and the voltages at points A and B are substantially equal to the supply voltage V_s . As capacitor 42 starts charging from point D through resistors 40 and 36 to points C and E, respectively, the voltage at point A starts decreasing from the supply voltage V_s toward 0 volts. When points B and A reach the maximum input voltage for a logic zero trip point (VIL) of the OR gate 30 and inverter 34, these devices switch causing the voltages at points C and E to increase to the supply voltage V_s which, in turn, causes the voltage at points B, A and D to



become 0. When point D becomes 0 volts, capacitor 42 starts discharging through resistors 40 and 36, causing the voltage at point B to start increasing from 0 volts towards the supply voltage V_s . When point B reaches the minimum input voltage for logic one trip point (V_{IH}) of OR gate 30 and inverter 34, these devices switch causing the voltage at points C and E to become 0 and the voltage at points B, A and D to become the supply voltage V_s . Since points E and C are equal at all times, the charging and discharging time of capacitor 42 is proportional to the parallel combination of resistors 40 and 36. Oscillations continue at the rate of charging and discharging of capacitor 42, which represents the predefined upper signal frequency (space frequency), until the input voltage at point F changes.

When the output of the interface device 12 is 0 volts (Figure 2, point d), then OR gate 30 acts as a non-inverting buffer for the voltage at point B resulting in the output at point E equalling the input at point B. This condition causes points C and E to be of opposite potential at all times. When this occurs, the charging and discharging time of capacitor 42 will be proportional to the ratio of the resistance of resistor 40 to the sum of the resistance of resistors 40 and 36. This results in the capacitor 42 charging and discharging at a slower rate which, in turn, causes oscillations to be produced at a predefined lower frequency (mark frequency). Thus, the digitally controlled oscillator 14 produces an output at point D at a predefined upper signal frequency when the input at point F is equal to the supply voltage V_s and produces a predefined lower signal frequency when the input at point F is 0 volts.

The output of the digitally controlled oscillator 14 drives the transformer 50 via the inverter 44, resistor 46 and capacitor 48. The transformer 50 is used to isolate the oscillator 14 from



the current loop 18. The signal at point H in Figure 1 is reflected to point I by means of the transformer 50 and is AC coupled to the current loop 18 through resistor 52 and capacitor 54. The transformer 50 prevents any DC current from the current loop from being transmitted to the digitally controlled oscillator 14, and vice versa. This permits on-line communication on the current loop 18 without disturbing the 4 to 20 mA DC current present thereon.

10 Referring now to Figure 3, a schematic diagram of a
frequency shift keying demodulation system 60 of the present
invention is illustrated. Those components which are similar to
the components utilized within the modulation system 10 carry
similar reference numerals and will not be discussed in further
15 detail. The demodulation system 60 includes a demodulator 62, a
current 64 interconnecting the demodulator 62 with the current
loop 18, a digitally controlled oscillator 14, and a receiving
interface device 66. The current 64 interconnects the current
loop 18 with the demodulator 62 by means of a transformer 68
20 having one side connected across the current loop 18 via a
resistor 70 and a capacitor 72. The other side of the
transformer 68 is connected to ground and to a band-pass filter
74 whose output is connected to one input to an OR gate 76. The
other input to the OR gate 76 is connected to the output of the
25 inverter 38 within the digitally controlled oscillator 14. The
output of the OR gate 76 is connected to an input to the OR gate
30 within the oscillator 14 and to a resistor 78 which is
connected to one side of a resistor 80 and to ground via a
capacitor 82. The other side of resistor 80 is connected to an
30 input to an OR gate 84 and to the output of same via a resistor
86. The other input to OR gate 84 is connected to ground. The
output of OR gate 84 is connected to the receiving interface
device 66, which can be a RS-232, or the like.



As in the previous discussion, the waveforms at selected points on Figure 3 are shown in Figure 4. Operationally, a frequency shift keying signal on the current loop 18 is transmitted through the capacitor 72, resistor 70 and transformer 68 to the band-pass filter 74. The AC coupling of the transformer 68 prevents any DC current from the current loop 18 from passing to the demodulator 62. The band-pass filter 74 rejects any signal outside the frequency shift keying band. The output of filter 74, shown in Figure 4 as waveform C, is a digital representation of the filtered frequency shift keying signal.

The system comprised of the digitally controlled oscillator 14 and the OR gate 76 is a form of a phase-locked loop. The signals at points B and C are compared by the OR gate 76 producing an output at point A which is transmitted back to the digitally controlled oscillator 14 to adjust its frequency so as to be the same as the input frequency at point C. In order to accomplish the foregoing, the duty cycle of the digitally controlled oscillator 14 varies with the input frequency. A low input frequency produces an oscillator duty cycle less than 50% whereas a high input frequency produces an oscillator duty cycle greater than 50%.

The signal at point D is the average of the signal produced at point A filtered by the RC circuit comprised of resistor 78 and capacitor 82. OR gate 84 acts as a voltage comparator, i.e., if the voltage at point D is above $V_{cc}/2$, then the voltage at point F goes high (Figure 4-waveform F). However, if the voltage of point D is less than $V_{cc}/2$, then the voltage at point F goes low. In essence, the voltage at point F is the digital representation of the frequency shift keying signal and can be transmitted to any data terminal equipment (not shown) by the interface device 66. Resistors 86 and 80 introduce a hysteresis to OR gate 84 to reduce any jitter when a level transition occurs.



The major advantages of the modulation system 10 and the demodulation system 60 are the low power requirements of these systems. Such low power requirements can be attributed to the reduced number of components required within the systems, the use of CMOS chips where appropriate and the low unit values for the capacitors utilized. These systems are also frequency stable under wide variations in power supply voltage because the input trip points (VIH and VIL) of the gates are proportional to the power supply voltage. The foregoing advantages permit reliable on-line communication between the low power devices using the same current loop that carries the 4 to 20 mA DC without effecting the DC current value.

Certain modifications and improvements will occur to those skilled in the art upon reading the foregoing. It should be understood that all such modification and improvements have been deleted herein for the sake of conciseness and readability, but are properly within the scope of the following claims.



THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A 4 to 20 mA D.C. current loop arrangement having a frequency shift keying oscillating signal superimposed thereon to permit reliable on-line
5 communication between low power devices normally using 4 - 20 mA D.C. current value comprising:

a power supply for producing 4 to 20 mA D.C. current;

a current loop connected to said power supply for
10 carrying said current;

modulating means for producing frequency shift keying oscillating signals including a digitally controlled oscillator having a low level capacitor selectively chargeable and discharging at a first rate
15 and at a second rate corresponding to first and second frequency shift keying frequencies respectively; and

transformer means for connecting said modulating means to said current loop while isolating same from said oscillator to superimpose said frequency shift keying
20 frequencies on said 4 to 20 mA D.C. current to permit on-line communication of said frequency shift keying frequencies onto said current loop to low power devices therein.

2. The current loop arrangement as defined in claim
25 1 further including means for demodulating a modulated signal on said current loop, said demodulating means producing frequency shift keying pulses representative of said modulated signal.

3. The current loop arrangement as defined in claim
30 2 wherein said demodulating means further includes comparator means connected to said digitally controlled oscillator in a phase-locked loop arrangement.

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4. A current loop arrangement substantially as herein described according to the accompanying drawings.

Dated this 23rd day of June 1992

INTERNATIONAL CONTROL AUTOMATION FINANCE S.A.

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By their Patent Attorneys

GRIFFITH HACK & CO

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FIG. 1

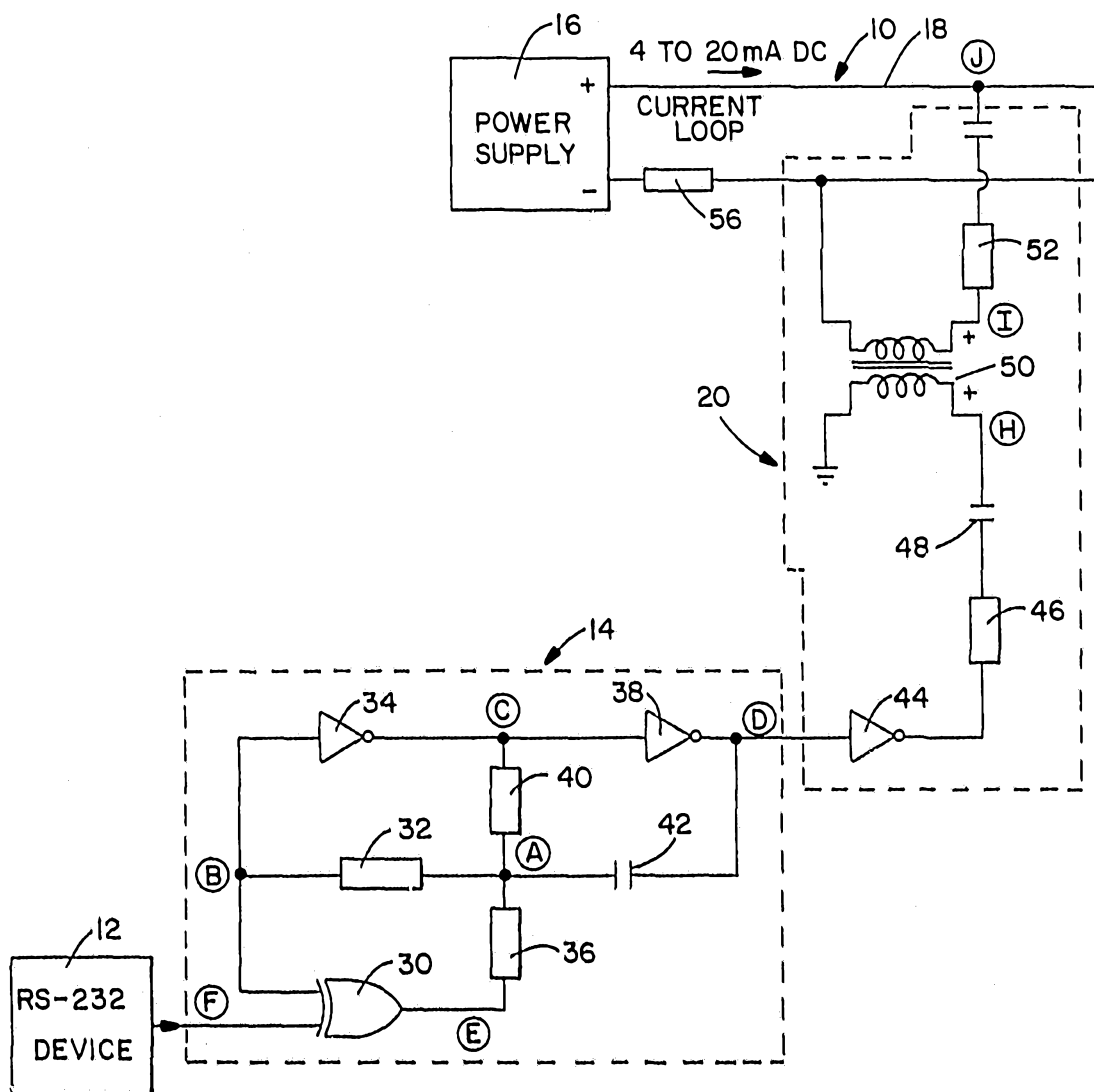
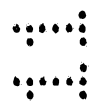
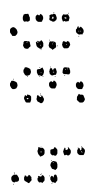
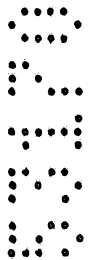
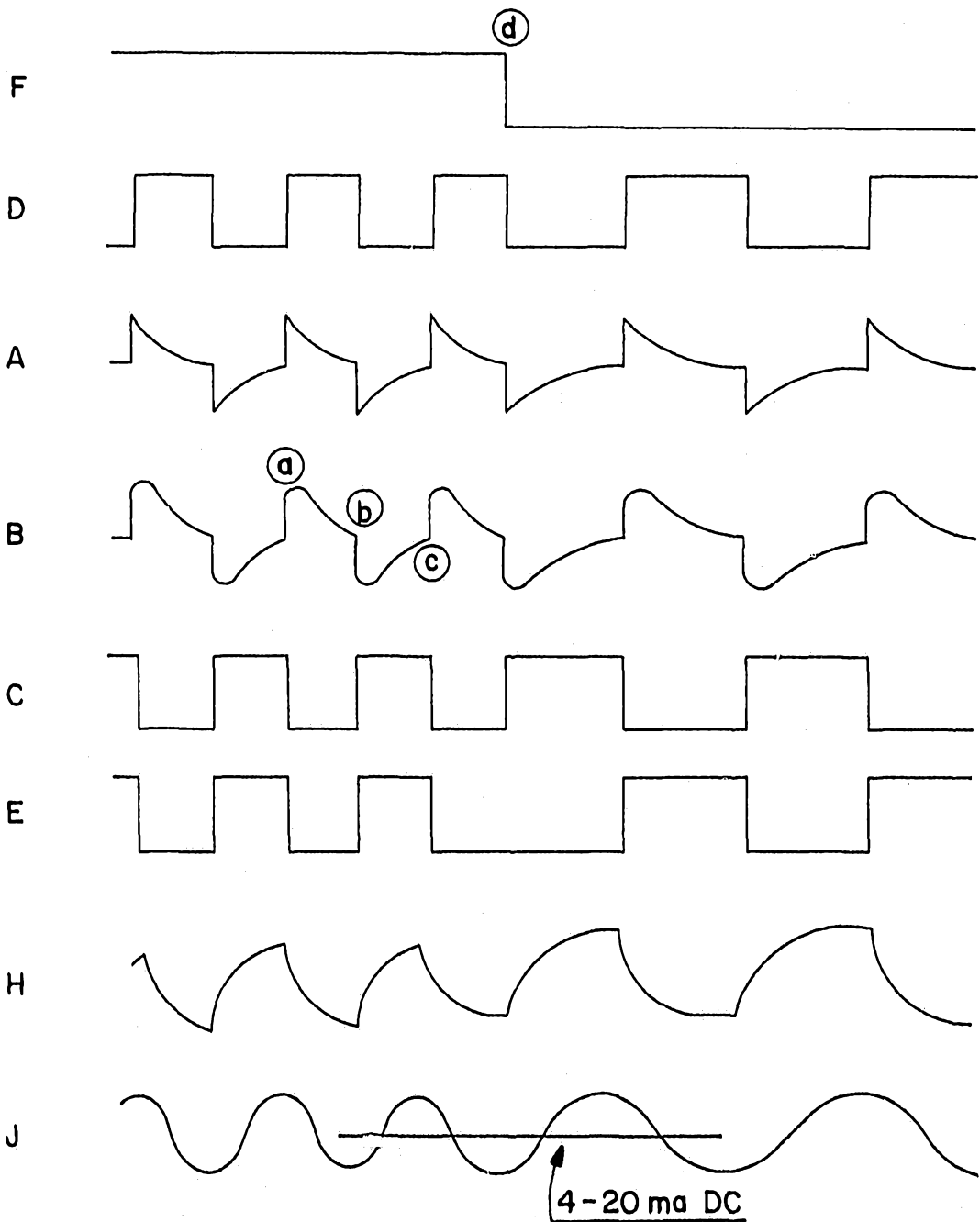


FIG. 2



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FIG. 3

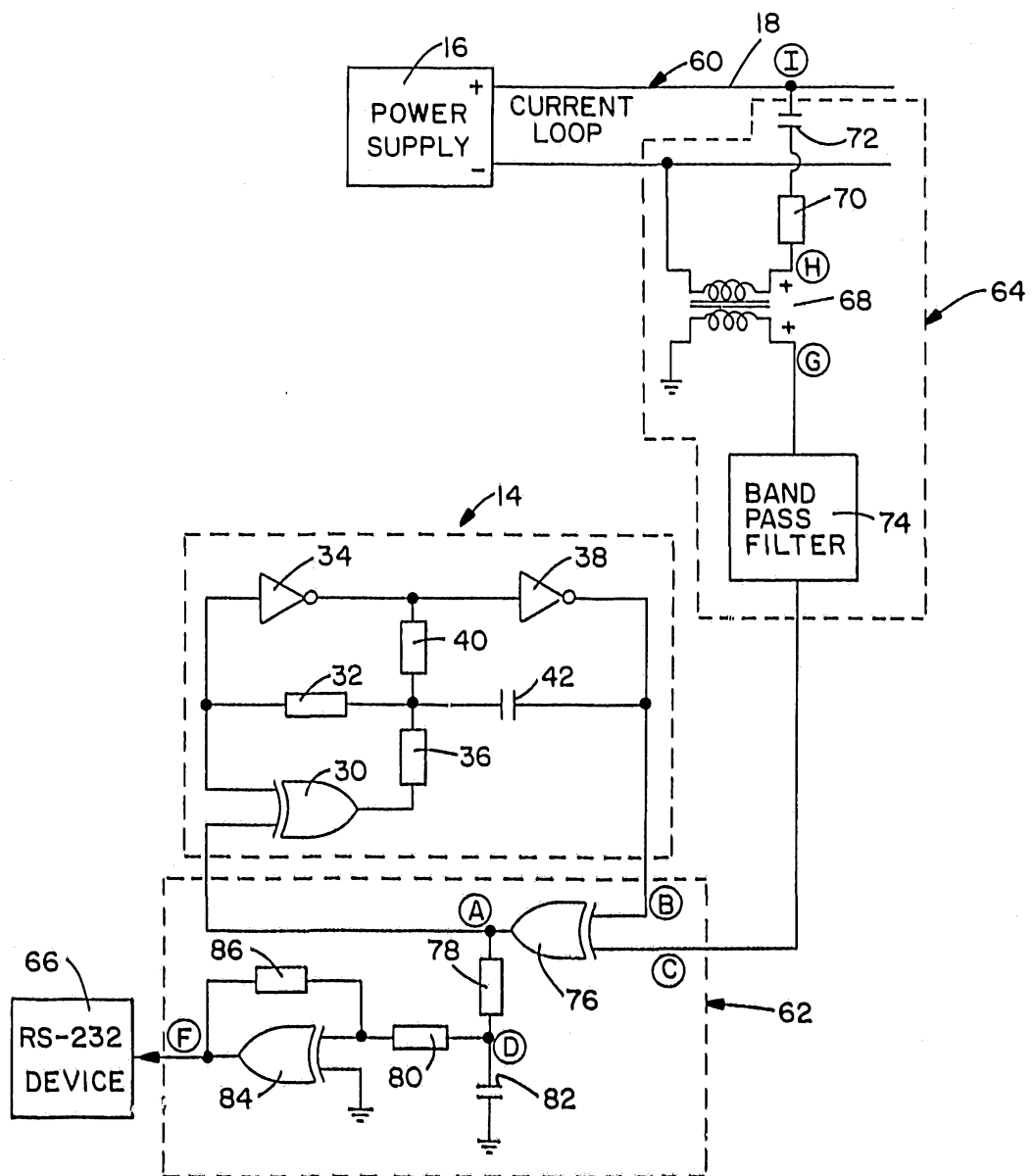


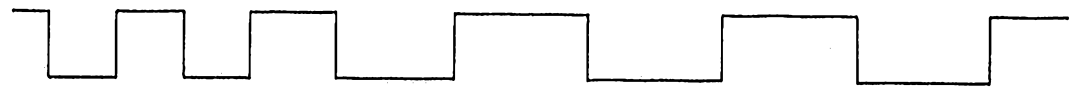
FIG. 4



G
I



C



B



A



D



F

