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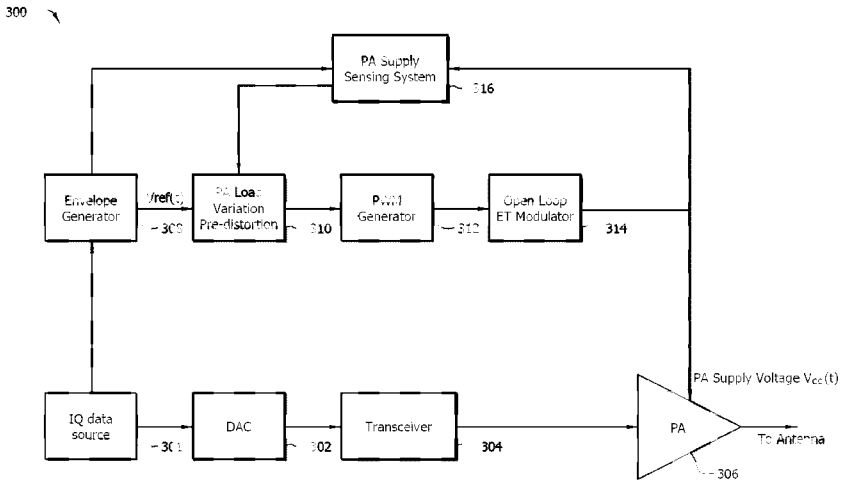


FIG. 3

(57) Abstract: An apparatus for providing envelope tracking (ET), comprising: a power amplifier (PA) load variation pre-distortion, and an open loop ET modulator operatively coupled to the PA load variation pre-distortion, wherein the PA load variation pre-distortion is configured to determine a load variation at a PA supply voltage path based on an envelope signal generated from an input signal received by a PA, and use the load variation in a digital domain to generate a pre-distortion compensation signal that attempts to correct the envelope signal such that the PA supply voltage matches the envelope signal, and wherein the open loop ET modulator is configured to generate a PA supply voltage on the PA supply voltage path using the pre-distortion compensation signal.

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A METHOD AND APPARATUS FOR ENVELOPE TRACKING

TECHNICAL FIELD

[0001] The present invention relates to a power supply control technology, and, in particular embodiments, to a method and apparatus for envelope tracking.

BACKGROUND

[0002] A transmitter's overall efficiency within a wireless terminal, such as a cellular phone, is a key metric in determining the operating time or talk time for the wireless terminal. The wireless terminal comprises a power amplifier (PA) that consumes a sizeable amount of current when transmitting signals at relatively high output power levels. One method to reduce the PA current consumption and/or improve PA efficiency is to modulate the supply voltage for the PA. For instance, the supply voltage can be modulated using an envelope tracking (ET) system that dynamically adjusts the supply voltage for the PA based on the PA's input signal level. Rather than applying the wireless terminal's battery voltage directly to the PA's supply voltage, the wireless terminal's battery is typically connected to an ET modulator, and the output of the ET modulator is connected to the PA supply voltage pin. The ET modulator can reduce the PA's supply voltage when the PA input signal level is relatively low and increase the PA's supply voltage when the PA input signal level is relatively high. Thus, the ET modulator improves the efficiency in providing the PA's supply voltage by reducing unnecessary headroom.

[0003] One of the challenges for implementing an ET system within a wireless terminal is managing the PA load variations seen by the ET modulator. Typically, the ET modulator can experience PA loads that substantially fluctuate depending on the PA's power. For example, when the PA outputs relatively low power, the PA consumes relatively low current causing the impedance on the PA's supply voltage line to be relatively high. Conversely, when the PA outputs relatively high power, the PA consumes relatively high current causing the impedance on the PA's supply voltage line to be relatively low. To accurately track the varying PA loads, a closed loop ET modulator may implement a feedback loop that tracks the PA load and adjusts the PA's supply voltage accordingly. Unfortunately, the feedback loop utilized by the closed

loop ET modulator can often cause stability issues that affect the overall performance of the ET system.

[0004] As an alternative, an ET system may utilize an open loop ET modulator to mitigate the stability issues that arise from the feedback loop within a closed loop ET modulator. In contrast to a closed loop ET modulator, the open loop ET modulator may not implement a feedback path to detect the varying PA loads. Unfortunately, without a feedback path, the PA load variations may cause the open loop ET modulator to yield varying voltage reference inputs that produce an overall system degradation of the wireless terminal. To alleviate this problem, the open loop ET modulator may need to be configured to digitally pre-distort the PA load variation. However, for the pre-distortion to be effective, the open loop ET modulator may need to obtain accurate information about the imperfections between the open loop ET modulator and the PA's supply. For instance, the open loop ET modulator may need to obtain information about the PA load variations under dynamic signal excitation (e.g. Long Term Evolution (LTE)), as well as the inductor-capacitor (LC) filter response information.

SUMMARY

[0005] In one embodiment, the disclosure includes an apparatus for providing ET, comprising a memory, and a processor coupled to the memory, wherein the memory includes instructions that when executed by the processor cause the apparatus to perform the following: determine a nonlinear PA current load for a PA using a reference voltage signal, filter the nonlinear PA current load to obtain an error correction signal, and add the error correction signal to the reference voltage signal to generate a pre-distortion compensation signal, wherein the reference voltage signal corresponds to an input for a PA, and wherein the error correction signal corresponds to a mismatch between the reference voltage signal and a PA supply voltage.

[0006] In another embodiment, the disclosure includes an apparatus for providing ET, comprising a PA load variation pre-distortion and an open loop ET modulator operatively coupled to the PA load variation pre-distortion, wherein the PA load variation pre-distortion is configured to: determine a load variation at a PA supply voltage path based on an input signal received by a PA, and generate a pre-distortion compensation signal using the load variation, and wherein the open loop ET modulator is configured to generate a PA supply voltage on the PA supply voltage path using the pre-distortion compensation signal.

[0007] In yet another embodiment, the disclosure includes a method for implementing ET, comprising receiving an envelope signal, obtaining a PA's nonlinear load characterization, generating an error correction signal based on the PA's nonlinear load characterization, adding the error correction signal to the envelope signal to generate the pre-distortion compensation signal, and transmitting the pre-distortion compensation signal for pulse-width-modulation generation, wherein the error correction signal is based on a mismatch between the envelope signal and a PA supply voltage.

[0008] These and other features will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of this disclosure, reference is now made to the following brief description, taken in connection with the accompanying drawings and detailed description, wherein like reference numerals represent like parts.

[0010] FIG. 1 is a schematic diagram of an embodiment of an open loop ET modulator system.

[0011] FIG. 2 illustrates a plot for the impact of PA load variation on the ET modulator's frequency response.

[0012] FIG. 3 is a schematic diagram of an embodiment of an open loop ET modulator system where embodiments of the present disclosure may operate.

[0013] FIG. 4 is a schematic diagram of an embodiment of an open loop ET modulator system configured with dynamic sensing during factory calibration.

[0014] FIG. 5 is a schematic diagram of an embodiment of a PA load variation pre-distortion.

[0015] FIG. 6 is a schematic diagram of an embodiment of a PA load variation pre-distortion during factory calibration.

[0016] FIG. 7 is a schematic diagram of an embodiment of an open loop ET modulator system with a PA load variation pre-distortion.

[0017] FIG. 8 is a schematic diagram of an embodiment of a PA load variation pre-distortion.

[0018] FIG. 9 is a flowchart of an embodiment of a method to update one or more component parameters for a PA load variation pre-distortion during factory calibration.

[0019] FIG. 10 is a flowchart of an embodiment of a method for a PA load variation pre-distortion prior to pulse-width-modulation (PWM) generation.

[0020] FIG. 11 is a schematic diagram of an embodiment of a wireless terminal.

DETAILED DESCRIPTION

[0021] It should be understood at the outset that, although an illustrative implementation of one or more embodiments are provided below, the disclosed systems, apparatuses, and/or methods may be implemented using any number of techniques, whether currently known or in existence. The disclosure should in no way be limited to the illustrative implementations, drawings, and techniques illustrated below, including the exemplary designs and implementations illustrated and described herein, but may be modified within the scope of the appended claims along with their full scope of equivalents. While certain aspects of conventional technologies have been discussed to facilitate the present disclosure, applicants in no way disclaim these technical aspects, and it is contemplated that the present disclosure may encompass one or more of the conventional technical aspects discussed herein.

[0022] FIG. 1 is a schematic diagram of an embodiment of an open loop ET modulator system 100. The open loop ET modulator system 100 may comprise a PWM generator 102, an open loop ET modulator 104, and an ET PA 106. The PWM generator 102 may receive an input reference supply voltage signal Vref(t) and perform pulse-width-modulation on the reference supply voltage signal Vref(t) to generate digital pulses that represent the desired reference supply voltage signal Vref(t). The reference supply voltage signal Vref(t) may be in-phase/quadrature (IQ) data that has undergone envelope processing. The PWM generator 102 outputs and feeds the digital pulses into the open loop ET modulator 104. Within the open loop ET modulator 104, the ET switching power stage 108 initially receives the digital pulses and may modify the switching frequency to generate a required current. The ET switching power stage 108 may also be configured to reduce switching losses. The LC filter 110 may receive the modified digital pulses from the ET switching power stage 108 and filter the modified digital pulses to remove clock spurs and other high frequency impairments before outputting the modified digital pulses as the PA supply voltage.

[0023] The open loop ET modulator 104 is configured to replicate the reference supply voltage signal Vref(t) as the PA supply voltage (e.g. integrated circuit (IC) power supply voltage

(t) (Vcc(t))). When the RF input of the PA is relatively low, the PA draws a relatively small amount of current, which typically means the PA load looking in from the PA supply voltage is relatively large. Conversely, when the RF input of the PA is relatively high, the PA draws a relatively large amount of current, which typically means the load looking in from the PA supply voltage is relatively small. Thus, variations in the PA supply load may impact the frequency response of the LC filter 110 and the accuracy of matching the PA supply voltage Vcc(t) with the reference supply voltage signal Vref(t).

[0024] FIG. 2 illustrates a plot 200 for the impact of PA load variation on the ET modulator's frequency response. The impedance load (Zload) from the PA and experienced by the open loop ET modulator may be a function of the RF envelope signal and the PA supply voltage Vcc(t). The PA load variation may cause nonlinearity and/or peaking or drooping in the LC filter frequency response. In plot 200, the Amplitude axis (e.g. y-axis) represents the LC filter frequency response while the x-axis represents frequency. Plot 200 further depicts three different Zload curves 202, 204, and 206 that demonstrate how the LC filter frequency response changes when the Zload changes. Specifically, Zload curve 202 represents when the actual PA load experienced by the ET modulator is relatively smaller than an optimal PA load configured for the open loop ET modulator; Zload curve 204 represents when the actual PA load experienced by the open loop ET modulator is about equal to the optimal PA load configured for the open loop ET modulator; and Zload curve 206 represents when the actual PA load experienced by the open loop ET modulator is relatively greater than the optimal PA load configured for the open loop ET modulator.

[0025] In FIG. 2, the Zload curve 202 illustrates that the LC filter's frequency response is over damped, which means that the open loop ET modulator outputs only the lower frequency portion of the envelope signal. In contrast, Zload curve 206 depicts that the LC filter's frequency response is under damped, which means the higher frequency content of the envelope signal is amplified excessively by the open loop ET modulator. Thus, both the under damped and over damped scenarios may cause an overall performance degradation because of the inaccurate tracking of the PA load. Typically, to minimize performance degradation, open loop ET modulators may be designed with low pass and LC filter parameters that produce over damping and under damping at relatively moderate levels. In other words, without a method to accurately track PA load variations, a design tradeoff may be employed for the open loop ET modulators in

order to balance the stability of the system (e.g. under damped case) and the performance of the system (e.g. over damped case).

[0026] Disclosed herein are at least one method, apparatus, and system that implements a PA load variation pre-distortion to manage varying PA loads for an open loop ET modulator system. In one embodiment, the PA load variation pre-distortion may dynamically sense the PA supply voltage Vcc(t) via a PA supply sensing system during factory calibration. The sensed PA supply voltage Vcc(t) may be compared to the reference supply voltage Vref(t) in order to update and/or determine a PA load variation pre-distortion using a factory calibration adaptation algorithm. To prevent stability issues, the PA supply sensing system may operate during factory calibration and may not be operational during the open loop ET modulator system's normal mode of operation. During the normal mode of operation (e.g. transmission of RF signals via the wireless transmitter) and/or non-factory calibration use, the open loop ET modulator may use the PA load variation pre-distortion obtained during factory calibration to output the desired PA supply voltage Vcc(t) under nominal conditions and varying processes. Specifically, the PA load variation pre-distortion may be configured to produce a pre-distortion compensation signal that attempts to match the reference supply voltages Vref(t) to the PA supply voltages Vcc(t).

[0027] FIG. 3 is a schematic diagram of an embodiment of an open loop ET modulator system 300 where embodiments of the present disclosure may operate. In one embodiment, the open loop ET modulator system 300 may be found within any wireless terminal configured to transmit RF signals. The open loop ET modulator system 300 may comprise an IQ data source 301, a digital-to-analog converter (DAC) 302, a transceiver 304, a PA 306, an envelope generator 308, a PA load variation pre-distortion 310, a PWM generator 312, an open loop ET modulator 314, and a PA supply sensing system 316. The open loop ET modulator system 300 may be sub-divided into a signal path and envelope path during the normal mode of operation. The DAC 302, transceiver 304, and PA 306 may be part of the signal path, and the envelope path may comprise the envelope generator 308, PA load variation pre-distortion 310, PWM generator 312, and open loop ET modulator 314. The signal path may generate the RF signal used for transmission via a wireless terminal's transmitter (e.g. RF signal outputted via an antenna), and the envelope path may provide ET functionality to generate a PA supply voltage Vcc(t) that substantially matches the reference supply voltage Vref(t). As shown in FIG. 3, the signal path

and envelope path may merge at the PA 306, which may be any amplifying device that generates the amplified RF signal.

[0028] FIG. 3 illustrates that the signal path may obtain the modulated IQ data from an IQ data source 301. The IQ data source 301 may be any device configured to convert digital data outputted from the baseband to I and Q components. Components I and Q data may be eventually converted separately by local oscillators to the desired RF carrier frequency within the signal path. In the signal path shown in FIG. 3, the IQ data source 301 may forward the IQ data to DAC 302 to convert the IQ data (e.g. a digital signal) to a baseband analog signal. The DAC 302 may be any device used to convert digital signals into analog signals. Afterwards, the DAC 302 may output the baseband analog signal to the transceiver 304, which may be any device used to convert the baseband analog signal to an RF signal. For example, the transceiver 304 may comprise a transmitter, a receiver, a low pass filter, and an RF variable gain amplifier (VGA). The transceiver 304 may output the RF signal and send (e.g. transmit) the RF signal to the PA 306 in order to amplify the RF signal to an appropriate level. The PA 306 outputs the amplified RF signal that is eventually transmitted via the antenna of the wireless terminal. Persons of ordinary skill in the art are aware that signal path may include additional components (e.g. filter, delay components, amplifiers, etc.) used to convert and process digital data into an amplified RF signal for wireless transmission. The use and discussion of the signal path in FIG. 3 is only an example to facilitate ease of description and explanation.

[0029] The envelope path may comprise an open loop ET modulator 314. In contrast to a closed loop ET modulator, the open loop ET modulator 314 may not comprise an analog feedback path to track varying PA loads. Typically, the analog feedback path returns the PA supply voltage Vcc(t) as an input to the closed loop ET modulator in order to match the reference supply voltage Vref(t) and PA supply voltage Vcc(t). Thus, the analog feedback path for a closed loop ET modulator may provide current sensing. Without an analog feedback path, the open loop ET modulator 314 and open loop ET modulator system 300 may not suffer from stability issues caused by the analog feedback path. Moreover, an error amplifier (e.g. class "AB" error amplifier) that suppresses residual impairments (e.g. stability issues) caused by the feedback path may not be used within the open loop ET modulator 314. As such, the open loop ET modulator 314 may provide current savings when compared to a closed loop ET modulator. FIG. 3 also illustrates that the envelope path may be implemented in the digital domain, and thus does not include a DAC and/or

a reconstruction filter (RCF) generally found within an envelope path that comprises an analog closed loop ET modulator.

[0030] The envelope path may generate a dynamic PA supply voltage Vcc(t) that corresponds to the amplitude or "envelope" of the RF signal generated in the signal path. The envelope generator 308 may receive the IQ data and generate an envelope signal in response to the IQ data. In other words, the voltage levels (e.g. about zero volts (V)) for the envelope signal may be determined from the voltage range (e.g. about one to two V) of the IQ data. Persons of ordinary skill in the art are aware that a variety of methods may be used to implement an envelope generator 308 that processes IQ data. Afterwards, the envelop generator 308 may forward the envelope signal to a PA load variation pre-distortion 310.

[0031] The PA load variation pre-distortion 310 may be configured to correct the envelope signal such that PA supply voltage Vcc(t) outputted by the open loop ET modulator 314 substantially matches the reference supply voltage Vref(t) received from the envelope generator 308. The PA load variation pre-distortion 310 may model the nonlinear load current of PA 306 in the digital domain to prevent distortion of the PA supply voltage Vcc(t) caused by the PA's 306 nonlinear load impedance. To correct the envelope signal, the PA load variation pre-distortion 310 may add an error correction signal to the envelope signal prior to PWM conversion to form a pre-distortion compensation signal. In one embodiment, to produce the error correction signal, the PA load variation pre-distortion 310 may obtain the PA nonlinear load characterization during factory calibration via the PA supply sensing system 316. The PA load variation pre-distortion 310 may also be configured to implement up sampling and/or down sampling to improve the accuracy of the load pre-distortion filters within the PA load variation pre-distortion 310. By determining the error correction signal and applying it to the envelope signal, the PA load variation pre-distortion 310 may minimize the nonlinear load impact on the LC filter within the open loop ET modulator 314. As such, the PA load variation pre-distortion 310 may compensate for impairments due to nonlinear, time-varying load impedance for the open loop ET modulator system 300.

[0032] The PA load variation pre-distortion 310 may subsequently output the pre-distortion compensation signal to the PWM generator 312. The PWM generator 312 may be configured to perform a PWM on the compensated envelope signal to create a pulse wave that conforms to the compensated envelope signal. In other words, the PWM generator 312 may improve signal linearity by performing signal modulation in the digital domain where the widths of the pulses

correspond to specific data values of the compensated envelope signal. The PWM generator 312 may then forward the outputted digital PWM signal to the open loop ET modulator 314. The open loop ET modular 314 may use the digital PWM signal and battery voltage to generate the PA supply voltage Vcc(t). The PA supply voltage signal Vcc(t) is then fed into PA 306 to provide the supply voltage for PA 306 that corresponds to the RF signal from the signal path. The open loop ET modulator 314 and PA load variation pre-distortion 310 will be discussed in more detail in FIGS. 4 and 5.

[0033] FIG. 3 also illustrates that the open loop ET modulator system 300 may comprise a PA supply sensing system 316. The PA supply sensing system 316 may be operational during factory calibration, but not during the normal mode of operation of the ET modulator system 300. The PA supply sensing system 316 may be part of the sensing path that compares reference supply voltage Vref(t) to the PA supply voltage Vcc(t) (e.g. using signal to noise ratio (SNR)) and updates parameters (e.g. filter parameters) within the PA load variation pre-distortion 310 during factory calibration. The open loop ET modulator system 300 may not implement the PA supply sensing system 316 during normal mode of operations and/or non-factory calibration operations. During factory calibration, the reference supply voltage Vref(t) may be set or generated using LTE (e.g. LTE-band 20), Wideband Code Division Multiple Access (WCDMA), and/or other types of stimulus signals (e.g. sinusoidal-based wave) generated on-chip. The PA supply sensing system 316 may sense the PA supply voltage Vcc(t) and determine the difference between the reference supply voltage Vref(t) and the PA supply voltage Vcc(t). After the comparison, the PA supply sensing system 316 may update parameters within the PA load variation pre-distribution 310 to improve the SNR and/or other equivalent metrics between the reference supply voltage Vref(t) and the PA supply voltage Vcc(t), in order to match the voltage levels for the reference supply voltage Vref(t) and the PA supply voltage Vcc(t). The PA supply sensing system 316 will be discussed in more detail below.

[0034] FIG. 4 is a schematic diagram of an embodiment of an open loop ET modulator system 400 configured with dynamic sensing during factory calibration. The open loop ET modulator system 400 comprises a PA load variation pre-distortion 402, a PWM generator 404, an open loop ET modulator 409, an Rx RF path component 410, a delay component 422, an ET PA 424, and a PA supply sensing system 426. The open loop ET modulator 409 may comprise an ET power stage 406 and an LC filter 408, and the PA supply sensing system 426 may comprise a

switch 412, a multiplexer 414, an Rx intermediate frequency (IF) path component 416, an Rx analog-to-digital converter (ADC) 418, and a factory calibration adaptation algorithm module 420. Under the normal mode of operation (e.g. transmission of RF signals via the wireless transmitter) and/or non-factory calibration use, the PWM generator 404 may receive the IQ data and function substantially similar to the PWM generator 312 discussed in FIG. 3. Afterwards, the ET power stage 406 may receive the envelope signal from the PWM generator 404. The ET power stage 406 may comprise one or more power stages that modify the switching frequency of the PWM signal and generate the required current. The ET power stage 406 may then forward the PWM signal to the LC filter 408. The LC filter 408 may comprise one or more lower order and/or higher order filters (e.g. two poles and/or six poles) that modify the PWM signal by removing clock spurs and other high frequency impairments before feeding the signal as the actual PA supply voltage Vcc(t). The LC filter 408 may comprise one or more low pass filters that drive the PA supply voltage Vcc(t).

[0035] The sensing path may comprise the PA supply sensing system 426, which is substantially similar to the PA supply sensing system 316 discussed in FIG. 3. As shown in FIG. 4, the PA supply current I(Vcc(t), Vin(t)) is a function of the PA supply voltage Vcc(t) and the PA input Vin(t). In one embodiment, the PA supply sensing system 426 may comprise an Rx IF path component 416, Rx ADC 418, and the factory calibration adaptation algorithm module 420. During the normal mode of operation, the multiplexer 414 switches to the Rx RF path component 410 to receive wireless data (e.g. RF signals) from the antenna. The Rx RF path component 410 may comprise a low noise amplifier (LNA) and a mixer to receive and process RF signals. The sensing path may not be operational during the normal mode of operation (e.g. transmitting and receiving RF signals for wireless communication) to avoid stability issues. During factory calibration (e.g. not transmitting and receiving RF signals for wireless communication), the open loop ET modulator system 400 may sense the actual PA supply voltage Vcc(t) via the PA supply sensing system 426. The PA supply sensing system 426 may be operational to implement Vcc(t) sensing when the multiplexer 414 switches from the Rx RF path component 410 to the PA supply voltage path. The PA supply sensing system 426 may provide an error signal and/or other information that can be used to update parameters within the PA load variation pre-distortion 402. The PA supply sensing system 426 may continue to be operational during factory calibration until the PA supply voltage Vcc(t) substantially matches (e.g. within a tolerance range) the reference

supply voltage Vref(t) under nominal conditions and varying processes. Additionally, the PA supply sensing system 426 may not perform RF down-conversions (e.g. RF signal converted to a lower IF signal) typically found within an analog feedback path for closed loop ET modulators.

[0036] In one embodiment, a switch 412 may be connected to one of the multiplexer's 414 inputs and to the PA supply voltage path. When the switch 412 is in an "off" state (e.g. not connected or open circuit) the impedance between the multiplexer's 414 input and the PA supply voltage path may be configured with a relatively high impedance to prevent impacting the efficiency of the open loop ET modulator system 400. Switch 412 may be implemented to isolate the PA supply voltage path from the PA supply sensing system 426 during normal mode of operation. In another embodiment, the PA supply sensing system 426 may not comprise a switch 412 and may use only the multiplexer 414 to switch to the PA supply sensing system 426 during factory calibration.

[0037] After multiplexer 414 switches to the PA supply path (e.g. switch is an "on" state), the sensed PA supply voltage Vcc(t) is sent to the Rx IF path component 416. The Rx IF path component 416 may perform filtering (e.g. resistor–capacitor (RC) filtering and/or second order filtering) and/or other signal processing on the PA supply voltage Vcc(t) to remove clock spurs and other signal impairments. The Rx ADC 418 may convert the analog PA supply voltage Vcc(t) to a digital PA supply voltage Vcc(t) and provide (e.g. transmit) the digital PA supply voltage Vcc(t) to the factory calibration adaptation algorithm module 420.

[0038] The factory calibration adaptation algorithm module 420 may also receive the reference supply voltage Vref(t) as an input from the delay component 422. The delay component 422 may be any type of delay and/or buffering circuit. The delay component 422 may be configured to provide a long enough delay such that the reference supply voltage Vref(t) arrives at the factory calibration adaption algorithm module 420 about the same time as the digital PA supply voltage Vcc(t). The factory calibration adaptation algorithm module 420 may compare the reference supply voltage Vref(t) with the digital PA supply voltage Vcc(t) and produce an error signal based on the comparison. In one embodiment, the factory calibration adaptation algorithm module 420 may perform the comparison using the SNR of the reference supply voltage Vref(t) and the digital PA supply voltage Vcc(t). The error signal may be outputted to the PA load variation pre-distortion 402 in order to update different attributes within the PA load variation pre-distortion 402. The factory calibration adaptation algorithm module

420 may use any adaptation algorithm well known in the art, such as the Least Square algorithm and/or the recursive Least Square algorithm. The PA load variation pre-distortion 402 will be discussed in more detail below.

[0039] FIG. 5 is a schematic diagram of an embodiment of a PA load variation pre-distortion 500. The PA load variation pre-distortion 500 may comprise an RF PA nonlinear current model 502 and a digital linear filter 504. The RF PA nonlinear current model 502 may receive a reference supply voltage Vref(t) signal and use the reference supply voltage Vref(t) to generate the nonlinear PA current. The RF PA nonlinear current model 502 may implement digital interpolation filters and Lagrange interpolation to obtain the nonlinear PA current. The RF PA nonlinear current model 502 may be computed at a relatively high data rate to improve accuracy. Afterwards, the RF PA nonlinear current model 502 outputs the nonlinear PA current.

[0040] The nonlinear PA current may subsequently be received by a digital linear filter 504, which may convert the nonlinear PA current to a voltage signal. As shown in FIG. 5, the digital linear filter 504 may receive filter component parameter values 503. In one embodiment, the filter component parameter values 503 may be determined during factory calibration. After the digital linear filter 504 filters and converts the nonlinear PA current to a voltage signal, the voltage signal may be sent to an adder 506 to be combined with the reference supply voltage Vref(t) signal to form the pre-distortion compensation signal. FIGS. 6-8 provide a more detailed embodiment of the PA load variation pre-distortion 500.

[0041] FIG. 6 is a schematic diagram of an embodiment of a PA load variation pre-distortion 600 during factory calibration. The PA load variation pre-distortion 600 may rely on accurate knowledge of the LC filter response as well as a digital look-up table (LUT) dependent on the dynamic behavior of the PA supply load when stimulated with an IQ signal similar to the one experienced during normal mode of operation (e.g. LTE). Without implementing a feedback sensing of the PA supply voltage during factory calibration, a mismatch may occur between the PA load variation pre-distortion 600 and the actual LC filter response. Moreover, a mismatch between the digital LUT and the actual dynamic PA supply voltage behavior may negatively impact the accuracy of the pre-distortion of the open loop ET modulator.

[0042] To overcome the potential mismatch, the reference supply voltage Vref(t) and PA supply voltage Vcc(t) may be compared to generate an error signal Error(t). FIG. 6 illustrates that the Rx ADC 604 outputs the sensed PA supply voltage Vcc(t) as a digital signal, and the delay

component 602 sends the reference supply voltage Vref(t) to a comparator 618a. Comparator 618a may be implemented using the factory calibration adaptation algorithm module 420 described in FIG. 4. The Rx ADC converter 604 and delay component 602 may be substantially similar to the Rx ADC converter 418 and delay component 422 in FIG. 4, respectively. In one embodiment, the factory calibration adaptation algorithm module may perform the comparison and provide the error signal Error(t) based on the SNR to the PA load variation pre-distortion 600. The error signal Error(t) may update component parameters within the PA load variation pre-distortion 600 that are used to minimize the SNR between the reference supply voltage Vref(t) and the sensed PA supply voltage Vcc(t). For example, the adaptation algorithm may use a Least Square algorithm to update the parameters that correspond to the H(z) filter 610, B(z) filters 612a and 612b, LUT 614, and F(z) filter 620.

[0043] After providing the updated component parameters, the PA load variation pre-distortion 600 may produce an error correction signal that corrects for the SNR difference. The PA load variation pre-distortion 600 may comprise an up sample component 606, a pre-emphasis filter 608, an H(z) filter 610, B(z) filters 612a and 612b, LUT 614, multiplier 616, comparator 618b, F(z) filter 620, a down sample component 622, and Vbattery limiter 624. The up sample component 606 may receive the reference supply voltage Vref(t) signal and increase the sampling rate of the reference supply voltage Vref(t) signal by an appropriate factor (e.g. about five). The sample component 606 may then output the up-sampled reference supply voltage Vref(t) signal to the pre-emphasis filter 608 to filter out any drooping, attenuation distortion, saturation and/or other signal distortions within the up-sampled reference supply voltage Vref(t) signal. The pre-emphasis filter 608 may be used to improve the overall SNR.

[0044] The pre-emphasis filter 608 may then output the reference supply voltage Vref(t) to a B(z) filter 612a and an H(z) filter 610. The H(z) filter 610 may represent the digital synthesis of the LC filter within the open loop ET modulator (e.g. LC filter 408 in FIG. 4). The H(z) filter 610 may perform a z transformation of the up-sampled reference supply voltage Vref(t) signal, and may have filtering characteristics based on the transfer function H(z). In another embodiment, the H(z) filter 610 may have filtering characteristics based on the transfer function H(s) when the filtering is implemented in the Laplace domain. The B(z) filters 612a and 612b may be a digital synthesis of a low pass filter that attenuates the out-of-band signals from the F(z) filter 620 and the in-band signals from the pre-emphasis filter 608. The B(z) filters 612a and 612b may be used to

limit the voltage output for a pre-distortion compensation signal. For example, the B(z) filter 612 may be a second order Butterworth filter used to limit the voltage output for the pre-distortion compensation signal.

[0045] After the H(z) filter 610 processes the reference supply voltage Vref(t) signal, the H(z) filter 610 outputs a voltage value "Vr." The voltage value "Vr" may be sent to LUT 614 and multiplier 616. LUT 614 may be a table that stores the dynamic behavior of the PA supply load. The PA supply load data stored with LUT 614 may be updated from the sensing path during the factory calibration process (e.g. using Error(t) value). LUT 614 may receive the voltage value "Vr" and use the voltage value "Vr" to perform a look up within the table and match the voltage value "Vr" with a corresponding current value. After the look up, LUT 614 may return the corresponding current value and output the current value to comparator 618b.

[0046] Multiplier 616 may receive the voltage value "Vr" and multiply the voltage value "Vr" with the value "1/R." "R" may represent the desired varying load experienced by the LC filter within the open loop ET modulator. The multiplier 616 may also output a current value, which may be the same or different from the current outputted from LUT 614. The output of the multiplier 616 is subsequently sent to comparator 618b to determine the difference of the current values sent from multiplier 616 and LUT 614. Based on the two input current values, comparator 618b may determine the correction current "Ir." In other words, current "Ir" may represent the residual or the undesired nonlinear current error. "Ir" may be represented by equation 1 shown below:

$$Ir(Vcc(t), Vin(t)) = I(Vcc(t), Vin(t)) - Vcc(t)/R \quad (1)$$

Vcc(t) and Vin(t) may represent the PA supply voltage and the PA input signal, respectively. Ir (Vcc(t), Vin(t)) may represent the residual nonlinear current error, while I(Vcc(t), Vin(t)) may represent the actual nonlinear current. Both Ir(Vcc(t), Vin(t)) and I(Vcc(t), Vin(t)) may be a function of Vcc(t) and Vin(t). In one embodiment, the RF PA nonlinear current model 502 shown in FIG. 5 may comprise the up sample component 606, a pre-emphasis filter 608, an H(z) filter 610, LUT 614, multiplier 616, and comparator 618b to generate the nonlinear PA current (e.g. "Ir").

[0047] Afterwards, comparator 618b outputs the correction current "Ir" signal to the F(z) filter 620. The F(z) filter 620 may be a high pass filter that receives the current "Ir" and converts the current "Ir" back into a voltage signal. As such, the F(z) filter 620 may be the digital pre-distortion filter that determines the correction voltage signal. In one embodiment, the F(z) filter's 620 transfer

function may be represented as an finite impulse response (FIR) (e.g. $a_1(1-z^{-1}) + a_2(1-z^{-1})^3$). In another embodiment, the F(z) filter 620 (Laplace equivalent is F(s)) may be represented as an infinite impulse response (IIR). The F(z) filter 620 may then output the correction voltage signal to the B(z) filter 612b, which band limits the correction voltage signal to form the error correction signal. The B(z) filter 612b outputs the error correction signal to the adder 626, which adds the error correction signal to the signal received from B(z) 612a (e.g. the reference supply voltage Vref(t) signal) to form the pre-distortion compensation signal. The adder 626 may forward the pre-distortion compensation signal to the down-sample component 622 to decrease the sampling rate by a desired factor (e.g. about a factor of 5). Afterwards, the pre-distortion compensation signal may enter the Vbattery limiter 624 to limit the voltage ranges of the pre-distortion compensation signal to the battery voltage ranges. In one embodiment, the digital linear filter 504 shown in FIG. 5 may comprise the F(z) filter 620 and B(z) filter 612b to generate the error correction signal.

[0048] In one embodiment, the parameter updates for error signal Error(t) may be obtained by determining coefficients for the H(s) and F(s) filtering parameters (Z domain equivalents are H(z) and F(z), respectively). Assuming that PA load variation pre-distortion is turned off during normal operation, and thus the reference supply voltage Vref(t) is outputted to the ET PWM generator, the PA supply voltage Vcc(t) may be expressed with equation 2:

$$Vcc(t)=\sum_{k=0}^{N} b_k \frac{d^k Vref(t)}{dt^k} - \sum_{k=1}^{M} a_k \frac{d^k Vcc(t)}{dt^k} - \sum_{k=1}^{L} c_k \frac{d^k Ir\left(Vcc(t), Vin(t)\right)}{dt^k} \quad (2)$$

Additionally, "Ir," which may represent the error correction current in the Laplace domain (e.g. Ir (s)), may be expressed with equation 3:

$$Ir(s) = Laplace\ \{Ir(Vcc(t), Vin(t))\} \quad (3)$$

Alternatively, equation 3 may be implemented in the Z domain. Equation 2, which is represented in the time domain, may then be converted to the Laplace domain to form equation 4 shown below:

$$Vcc(s)=\sum_{k=0}^{N} b_k s^k Vref(s) - \sum_{k=1}^{M} a_k s^k Vcc(s) - \sum_{k=1}^{L} c_k s^k Ir(s) \quad (4)$$

Equation 4 may then be modified to form equation 5 and 6, which is shown below:

$$Vcc(s)= Vref(s)\left[\frac{\sum_{k=0}^{N} b_k s^k}{1+\sum_{k=1}^{M} a_k s^k}\right] - Ir(s)\left[\frac{\sum_{k=1}^{L} c_k s^k}{1+\sum_{k=0}^{N} b_k s^k}\right]\left[\frac{\sum_{k=0}^{N} b_k s^k}{1+\sum_{k=1}^{M} a_k s^k}\right] \quad (5)$$

$$Vcc(s) = Vref(s)H(s) - Ir(s)F(s)H(s) \quad (6)$$

Thus, equation 6 can be used to determine the transfer function H(s) and F(s),(e.g.. the coefficients a1…aM, b0…bN, and c1…cL) such that the left side of equations 6 is close in the SNR sense to the right side of equation 6. In other words, equation 6 is used to minimize the frequency domain error signal Error(s), which is effectively minimizing the time domain error signal Error(t)). A system of equations Ax=b using a Least Squares approach may be used to obtain the coefficients, a1…aM, b0…bN, and c1…cL. Table 1 is an example of the matrix format using Ax =b to solve for the different coefficients:

$$\begin{bmatrix} Vref(s_1) & s_1 Vref(s_1) \dots s_1^N Vref(s_1) & s_1 Vcc(s_1) \dots s_1^M Vcc(s_1) & Ir(s_1) \dots s_1^L Ir(s_1) \\ Vref(s_2) & s_2 Vref(s_2) \dots s_2^N Vref(s_2) & s_2 Vcc(s_2) \dots s_2^M Vcc(s_2) & Ir(s_2) \dots s_2^L Ir(s_2) \\ \vdots & \vdots & \vdots & \\ Vref(s_K) & s_K Vref(s_K) \dots s_K^N Vref(s_K^n) & s_K Vcc(s_K) \dots s_K^M Vcc(s_K) & s_K Ir(s_K) \dots s_K^L Ir(s_K) \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ \vdots \\ b_N \\ a_1 \\ a_2 \\ \vdots \\ a_M \\ c_1 \\ c_2 \\ \vdots \\ c_L \end{bmatrix} = \begin{bmatrix} Vcc(s_1) \\ Vcc(s_2) \\ Vcc(s_3) \\ \vdots \\ Vcc(s_K) \end{bmatrix}$$

Table 1

[0049] FIG. 7 is a schematic diagram of an embodiment of an open loop ET modulator system 700 with a PA load variation pre-distortion 722. The IQ data source 702, envelope generator 718, transceiver 714, and PA 716 may be substantially similar to the IQ data source 301, envelop generator 308, transceiver 304, and PA 306 as described in FIG. 3, respectively. The PWM generator 746, open loop ET modulator 748, ET power stage 750, and LC filter 760 may be substantially similar to the PWM generator 404, open loop ET modulator 409, ET power stage 406, and LC filter 408 in FIG. 4, respectively. The pre-emphasis filter 724, up sample component 726, H(z) filter 728, B(z) filters 730a and 730b, multiplier 734, comparator 736, F(z) filter 738, adder 740, down sample component 742 and Vbattery limiter 744 are substantially similar to pre-

emphasis filter 608, up sample component 606, H(z) filter 610, B(z) filters 612a and 612b, multiplier 616, comparator 618b, F(z) filter 620, adder 626, down sample component 622 and Vbattery limiter 624 as described in FIG. 6, respectively.

[0050] The PA load variation pre-distortion 722 may be similar to the PA load variation pre-distortion 600 as described in FIG. 6 except that the pre-emphasis filter 724 is located before the up sample component 726 in reference to the signal input and a PA load data two dimensional (2-D) LUT 732 may be used to perform the look up function. As shown in FIG. 7, the PA load data 2-D LUT 732 may receive and perform the look up using the voltage signal "Vr" input and the IQ data from the IQ data source 702. After the look up, the PA load data 2-D LUT 732 may output a current value based on the anticipated PA supply load.

[0051] The open loop ET modulator system 700 may also comprise a time alignment 704, an amplitude modulation (AM) pre-distortion LUT 720, a phase modulation (PM) pre-distortion LUT 706, a delay component 710 to align the input signal for the PA with H(z) and B(z) processing, a delay component 708 to align the input signals for the PA Load Data 2-D LUT 232, and a DAC and RCF component 712. The time alignment 704 and delay component 710 may align the RF signal from the signal path with the corresponding PA supply voltage Vcc(t). The DAC and RCF component 712 may perform a digital-to-analog conversion of the IQ data and implement an RCF to smooth out the converted analog signal. The AM pre-distortion LUT 720 may be used to estimate the amplitude-to-amplitude distortion caused by the PA 716 and the PM pre-distortion LUT 706 may be used to estimate the amplitude-to-phase distortion caused by the PA 716. Persons of ordinary skill in the art are aware that a variety of implementations and/or methods may be used to implement the AM pre-distortion LUT 720 and the PM pre-distortion LUT 706.

[0052] FIG. 8 is a schematic diagram of an embodiment of a PA load variation pre-distortion 800. The a H(z) filter 802, the multiplier 804, PA Load Data 2-D LUT 806, the comparator 808, up sample component 810, F(z) filter 812, a down sample component 814, an adder 816, and a B(z) filter 818 within the PA load variation pre-distortion 800 are substantially similar to H(z) filter 728, multiplier 734, PA Load Data 2-D LUT 732, comparator 736, up sample component 726, F(z) filter 738, down sample component 742, adder 740, and B(z) filter 730a and 730b as described in FIG. 7, respectively. As shown in FIG. 8, the up sample component 810 may be placed after generating "Ir," and the down sample component 814 may be placed before adding the error

correction signal and the reference supply voltage Vref(t). Moreover, the B(z) filter 818 may be placed after generating the pre-distortion compensation signal.

[0053] FIG. 9 is a flowchart of an embodiment of a method 900 to update one or more component parameters for a PA load variation pre-distortion during factory calibration. Method 900 may be implemented within the PA supply sensing system 426 and/or the factory calibration adaptation algorithm module 420 discussed in FIG. 4. Method 900 may start at block 902 and receive a known reference supply voltage Vref(t) for a PA. Recall that during factory calibration, the reference supply voltage Vref(t) may be an IQ signal similar to the one experienced during normal mode of operation (e.g. LTE). Method 900 may then proceed to block 904 and sense the PA supply voltage Vcc(t) for the PA. In one embodiment, the PA supply voltage Vcc(t) may be a digital signal. Afterwards, method 900 continues to block 906 and compares the PA supply voltage Vcc(t) with the reference supply voltage Vref(t). Additionally, the comparison may be based on the SNR of the PA supply voltage Vcc(t) and the reference supply voltage Vref(t).

[0054] Method 900 may move to block 908 and determine the error signal Error(t) between the PA supply voltage Vcc(t) and the reference supply voltage Vref(t). Recall that the Least square algorithm and Ax=b matrix format (e.g. Table 1) may be used to determine the optimal H(s) and F(s) that minimize the error signal Error(t). Due to the complexity, the system of equations Ax=b is typically solved iteratively using Least Mean Square adaptive techniques in which the error signal Error(t) is used to iteratively update H(s) and F(s) (or effectively H(z) and F(z)). In another embodiment, the pre-calculated H(z) and F(z) coefficients representing the LC filter with the LC component variations (e.g. +/-10%) can be stored and one set of coefficients is used during each iteration. Method 900 continues to block 910 and determines whether the error signal Error(t) is within a set tolerance range. If the error signal Error(t) is within a set tolerance range, then method 900 ends. On the other hand, if the error signal Error(t) is outside a set tolerance range (e.g. not within the set tolerance range), then method 900 may move to block 912. At block 912, method 900 may provide the error signal Error(t) to update one or more component parameters (e.g. H(z) and F(z)) for the PA load pre-distortion. Afterwards, method 900 returns back to block 902.

[0055] FIG. 10 is a flowchart of an embodiment of a method 1000 for a PA load variation pre-distortion prior to PWM generation. Method 1000 may be implemented within the PA load variation pre-distortion 402, 500, 600, 722, and 800 as discussed in FIGS. 4-8. Method 1000 may start at block 1002 and receive a reference supply voltage Vref(t) for a PA. Method 1000

may start at block 1002 and receive a reference supply voltage Vref(t) for a PA. After generating the nonlinear PA current, method 1000 may proceed to block 1006 and filter the nonlinear PA current to obtain the error correction signal. At block 1006, method 1000 may filter the nonlinear PA current to convert it into a voltage signal. Method 1000 may move to block 1008 and add the correction signal to the reference supply voltage Vref(t) signal to generate the pre-distortion compensation signal. Afterwards, method 1000 may move to block 1010 and transmit the pre-distortion compensation signal for PWM generation.

[0056] FIG. 11 is a schematic diagram of an embodiment of a wireless terminal 1100, which may comprise any of the following: the open loop ET modulator system 300 and 400, the open loop ET modulator 314, 409, and 748, the PA load variation pre-distortion 500, 600, 722, and 800, and the PA supply sensing system 316 and 426. Wireless terminal 1100 may comprise a two-way wireless communication device having voice and/or data communication capabilities. In some aspects, voice communication capabilities are optional. The wireless terminal 1100 generally has the capability to communicate with other computer systems on the Internet and/or other networks. Depending on the exact functionality provided, the wireless terminal 1100 may be referred to as a data messaging device, a tablet computer, a two-way pager, a wireless e-mail device, a cellular telephone with data messaging capabilities, a wireless Internet appliance, a wireless device, a smart phone, a mobile device, or a data communication device, as examples. At least some of the features/methods described in the disclosure. For example, the open loop ET modulator system 300 and 400, the open loop ET modulator 314, 409, and 748, the PA load variation pre-distortion 500, 600, 722, and 800, and the PA supply sensing system 316 and 426 may be implemented in the wireless terminal 1100.

[0057] Wireless terminal 1100 may comprise a processor 1120 (which may be referred to as a central processor unit or CPU) that may be in communication with memory devices including secondary storage 1121, read only memory (ROM) 1122, and random access memory (RAM) 1123. The processor 1120 may be implemented as one or more general-purpose CPU chips, one or more cores (e.g. a multi-core processor), or may be part of one or more application specific integrated circuits (ASICs) and/or digital signal processors (DSPs). The processor 1120 may also be configured to perform computations as described in equations 1-6 and matrix calculations shown in Table 1.

[0058] The secondary storage 1121 may be comprised of one or more solid state drives and/or disk drives which may be used for non-volatile storage of data and as an over-flow data storage device if RAM 1123 is not large enough to hold all working data. Secondary storage 1121 may be used to store programs that are loaded into RAM 1123 when such programs are selected for execution. The ROM 1122 may be used to store instructions and perhaps data that are read during program execution. ROM 1122 may be a non-volatile memory device and may have a small memory capacity relative to the larger memory capacity of secondary storage 1121. The RAM 1123 may be used to store volatile data and perhaps to store instructions. Access to both ROM 1122 and RAM 1123 may be faster than to secondary storage 1121. The RAM 1123, ROM 1122, and/or the secondary storage 1121 may be used to store data within the LUT 614, the PA Load Data 2-D LUT 732, and/or implement the factory adaptation algorithm module 420, methods 900, and 1000.

[0059] Wireless terminal 1100 may be any device that communicates data (e.g., packets) wirelessly with a network. The wireless terminal 1100 may comprise a receiver 1112, which may be configured for receiving data, packets, or frames from other components. The receiver 1112 may be coupled to the processor 1120, which may be configured to process the data and determine to which components the data is to be sent. The wireless terminal 1100 may also comprise a transmitter (Tx) 1132 coupled to the processor 1120 and configured for transmitting data, packets, or frames to other components. The receiver 1112 and transmitter 1132 may be coupled to an antenna 1130, which may be configured to receive and transmit wireless signals (e.g. RF signals).

[0060] The wireless terminal 1100 may also comprise a device display 1140 coupled to the processor 1120, for displaying output thereof to a user. The device display 1140 may comprise a light-emitting diode (LED) display, a Color Super Twisted Nematic (CSTN) display, a thin film transistor (TFT) display, a thin film diode (TFD) display, an organic LED (OLED) display, an active-matrix OLED display, or any other display screen. The device display 1140 may display in color or monochrome and may be equipped with a touch sensor based on resistive and/or capacitive technologies.

[0061] The wireless terminal 1100 may further comprise input devices 1141 coupled to the processor 1120, which may allow a user to input commands to the wireless terminal 1100. In the case that the device display 1140 comprises a touch sensor, the device display 1140 may also be

considered an input device 1141. In addition to and/or in the alternative, an input device 1141 may comprise a mouse, trackball, built-in keyboard, external keyboard, and/or any other device that a user may employ to interact with the wireless terminal 1100. The wireless terminal 1100 may further comprise sensors 1150 coupled to the processor 1120. Sensors 1150 may detect and/or measure conditions in and/or around the wireless terminal 1100 at a specified time and transmit related sensor input and/or data to processor 1120.

[0062] It is understood that by programming and/or loading executable instructions onto the wireless terminal 1100, at least one of the receiver 1112, processor 1120, secondary storage 1121, ROM 1122, RAM 1123, antenna 1130, transmitter 1132, input device 1141, device display 1140, and/or sensors 1150, are changed, transforming the wireless terminal 1100 in part into a particular machine or apparatus, e.g., a multi-core forwarding architecture, having the novel functionality taught by the present disclosure. It is fundamental to the electrical engineering and software engineering arts that functionality that can be implemented by loading executable software into a computer can be converted to a hardware implementation by well-known design rules. Decisions between implementing a concept in software versus hardware typically hinge on considerations of stability of the design and numbers of units to be produced rather than any issues involved in translating from the software domain to the hardware domain. Generally, a design that is still subject to frequent change may be preferred to be implemented in software, because re-spinning a hardware implementation is more expensive than re-spinning a software design. Generally, a design that is stable that will be produced in large volume may be preferred to be implemented in hardware. For example, in an ASIC, because for large production runs the hardware implementation may be less expensive than the software implementation. Often a design may be developed and tested in a software form and later transformed, by well-known design rules, to an equivalent hardware implementation in an application specific integrated circuit that hardwires the instructions of the software. In the same manner as a machine controlled by a new ASIC is a particular machine or apparatus, likewise a computer that has been programmed and/or loaded with executable instructions may be viewed as a particular machine or apparatus.

[0063] At least one embodiment is disclosed and variations, combinations, and/or modifications of the embodiment(s) and/or features of the embodiment(s) made by a person having ordinary skill in the art are within the scope of the disclosure. Alternative embodiments

that result from combining, integrating, and/or omitting features of the embodiment(s) are also within the scope of the disclosure. Where numerical ranges or limitations are expressly stated, such express ranges or limitations should be understood to include iterative ranges or limitations of like magnitude falling within the expressly stated ranges or limitations (e.g., from about 1 to about 10 includes, 2, 3, 4, etc.; greater than 0.10 includes 0.11, 0.12, 0.13, etc.). For example, whenever a numerical range with a lower limit, R_l, and an upper limit, R_u, is disclosed, any number falling within the range is specifically disclosed. In particular, the following numbers within the range are specifically disclosed: $R = R_l + k * (R_u - R_l)$, wherein k is a variable ranging from 1 percent to 100 percent with a 1 percent increment, i.e., k is 1 percent, 2 percent, 3 percent, 4 percent, 5 percent, ..., 70 percent, 71 percent, 72 percent, ..., 95 percent, 96 percent, 97 percent, 98 percent, 99 percent, or 100 percent. Moreover, any numerical range defined by two R numbers as defined in the above is also specifically disclosed. The use of the term about means $\pm$10% of the subsequent number, unless otherwise stated. Use of the term "optionally" with respect to any element of a claim means that the element is required, or alternatively, the element is not required, both alternatives being within the scope of the claim. Use of broader terms such as comprises, includes, and having should be understood to provide support for narrower terms such as consisting of, consisting essentially of, and comprised substantially of. Accordingly, the scope of protection is not limited by the description set out above but is defined by the claims that follow, that scope including all equivalents of the subject matter of the claims. Each and every claim is incorporated as further disclosure into the specification and the claims are embodiment(s) of the present disclosure. The discussion of a reference in the disclosure is not an admission that it is prior art, especially any reference that has a publication date after the priority date of this application. The disclosure of all patents, patent applications, and publications cited in the disclosure are hereby incorporated by reference, to the extent that they provide exemplary, procedural, or other details supplementary to the disclosure.

[0064] While several embodiments have been provided in the present disclosure, it may be understood that the disclosed systems and methods might be embodied in many other specific forms without departing from the spirit or scope of the present disclosure. The present examples are to be considered as illustrative and not restrictive, and the intention is not to be limited to the details given herein. For example, the various elements or components may be combined or integrated in another system or certain features may be omitted, or not implemented.

[0065] In addition, techniques, systems, subsystems, and methods described and illustrated in the various embodiments as discrete or separate may be combined or integrated with other systems, modules, techniques, or methods without departing from the scope of the present disclosure. Other items shown or discussed as coupled or directly coupled or communicating with each other may be indirectly coupled or communicating through some interface, device, or intermediate component whether electrically, mechanically, or otherwise. Other examples of changes, substitutions, and alterations are ascertainable by one skilled in the art and may be made without departing from the spirit and scope disclosed herein.

CLAIMS

What is claimed is:

1. An apparatus for providing envelope tracking (ET), comprising:

a memory; and

a processor coupled to the memory, wherein the memory includes instructions that when executed by the processor cause the apparatus to perform the following:

apply a reference voltage signal to model a nonlinear power amplifier (PA) current for a PA in a digital domain , wherein the reference voltage signal is an envelope signal corresponding to an input for the PA;

filter the nonlinear PA current to obtain an error correction signal in the digital domain; and

add the error correction signal to the reference voltage signal to generate a pre-distortion compensation signal in the digital domain,

wherein the error correction signal is based on a mismatch between the reference voltage signal and a PA supply voltage.

2. The apparatus of claim 1, wherein the instructions executed by the processor further cause the apparatus to generate the PA supply voltage using the pre-distortion compensation signal.

3. The apparatus of claim 1, wherein the mismatch between the reference voltage signal and a PA supply voltage is caused by a varying load experienced at the PA's supply voltage path; wherein the instructions executed by the processor further cause the apparatus to store the varying load experienced at the PA's supply voltage path.

4. The apparatus of any one of claims 1 to 3, wherein applying a reference voltage signal to model a nonlinear power amplifier (PA) current for a PA in a digital domain comprises applying the reference voltage signal to model the nonlinear PA current for the PA in the digital domain using a radio frequency (RF) PA nonlinear current model comprising a pre-emphasis filter.

5. The apparatus of any one of claims 1 to 4, wherein filtering the nonlinear PA current comprises applying a digital pre-distortion filter that converts the nonlinear PA current to a voltage signal.

6. The apparatus of claim 5, wherein the instructions executed by the processor further cause the apparatus to apply a low pass filter to the voltage signal to obtain the error correction signal.

7. The apparatus of any one of claims 1 to 6, wherein the PA supply voltage is not generated using an analog feedback loop that senses the PA supply voltage.

8. An apparatus for providing envelope tracking (ET), comprising:

a power amplifier (PA) load variation pre-distortion; and

an open loop ET modulator operatively coupled to the PA load variation pre-distortion,

wherein the PA load variation pre-distortion is configured to:

determine a load variation at a PA supply voltage path based on an envelope signal generated from an input signal received by a PA; and

use the load variation in a digital domain to generate a pre-distortion compensation signal that attempts to correct the envelope signal such that the PA supply voltage matches the envelope signal, and

wherein the open loop ET modulator is configured to generate a PA supply voltage on the PA supply voltage path using the pre-distortion compensation signal.

9. The apparatus of claim 8, wherein the PA load variation pre-distortion is further configured to compare the envelope signal with the input signal to determine an error correction signal and add the error correction signal to the envelope signal to generate a pre-distortion compensation signal.

10. The apparatus of claim 8 or 9, wherein generating the PA supply voltage within the open loop ET modulator is implemented in the digital domain.

11. The apparatus of any one of claims 8 to 10, wherein the open loop ET modulator is not configured to track the load variation for the PA supply voltage path.

12. A method for implementing envelope tracking (ET), comprising:

receiving an envelope signal;

obtaining a power amplifier (PA)'s nonlinear load characterization;

generating an error correction signal based on the PA's nonlinear load characterization;

adding the error correction signal to the envelope signal to generate the pre-distortion compensation signal; and

transmitting the pre-distortion compensation signal for pulse-width-modulation generation,

wherein the error correction signal is based on a mismatch between the envelope signal and a PA supply voltage.

13 The method of claim 12, further comprising performing an ET modulation on the pre-distortion compensation signal to generate the PA supply voltage.

14. The method of claim 13 wherein the ET Modulation and generating the pre-distortion compensation signal are performed in the digital domain.

15. The method of any one of claims 12 to 14, further comprising determining a nonlinear load current based on the received envelope signal and filtering the nonlinear load current to obtain the error correction signal.

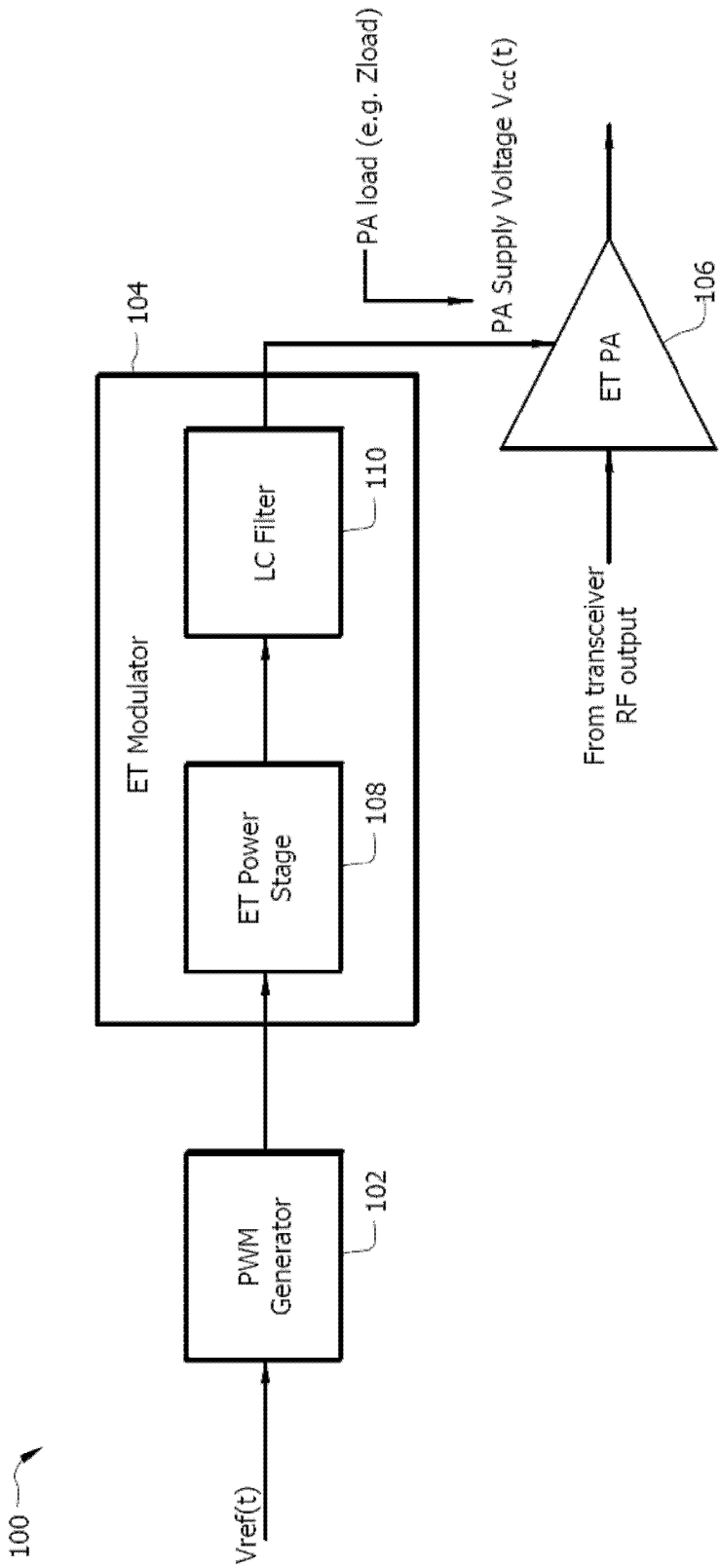

100
Vref(t)
PWM Generator
102
ET Power Stage
108
LC Filter
110
ET Modulator
104
PA load (e.g. Zload)
PA Supply Voltage Vcc(t)
ET PA
106
From transceiver RF output

FIG. 1

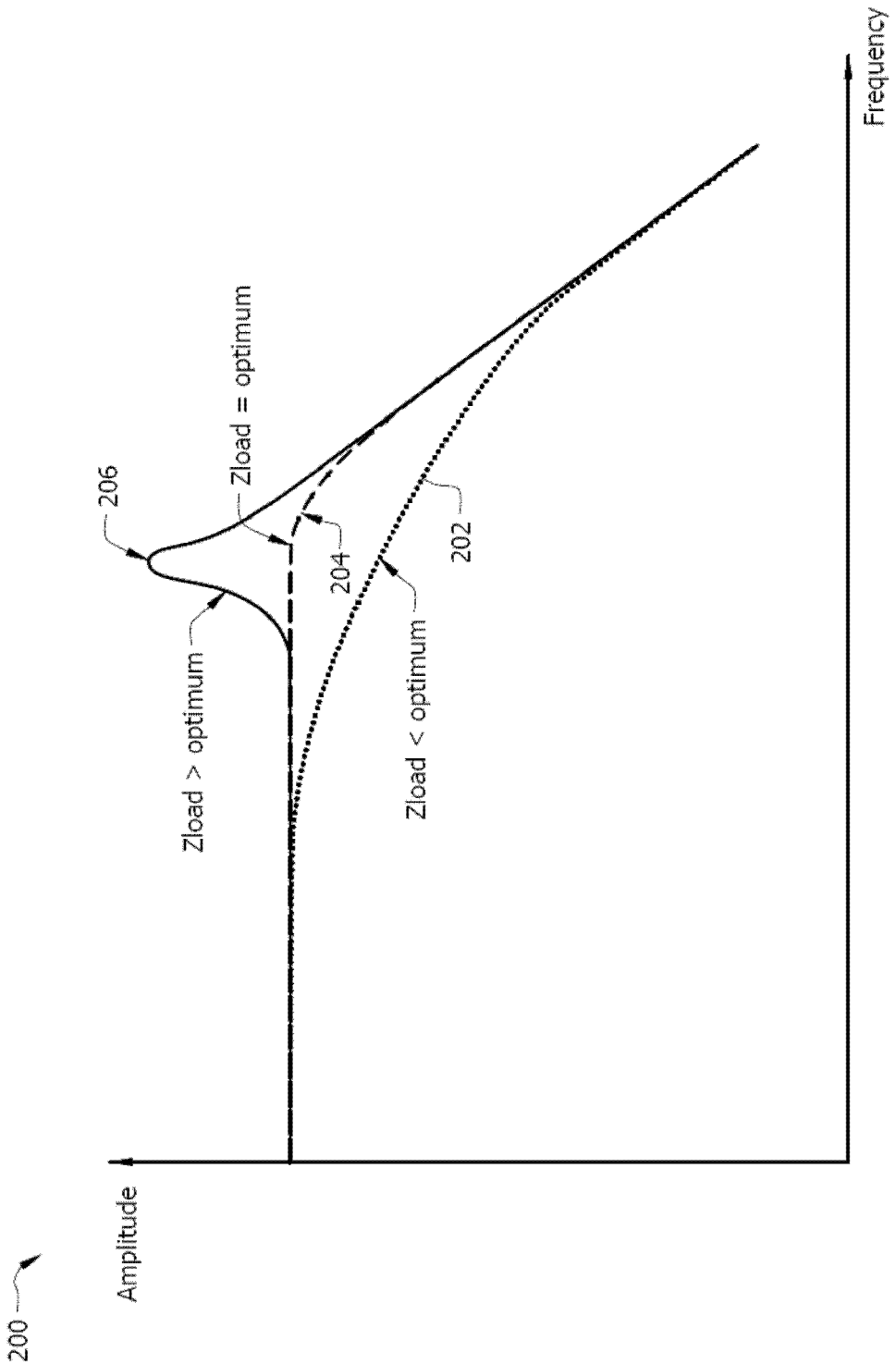

200
Amplitude
Frequency
206
Zload = optimum
204
202
Zload > optimum
Zload < optimum

FIG. 2

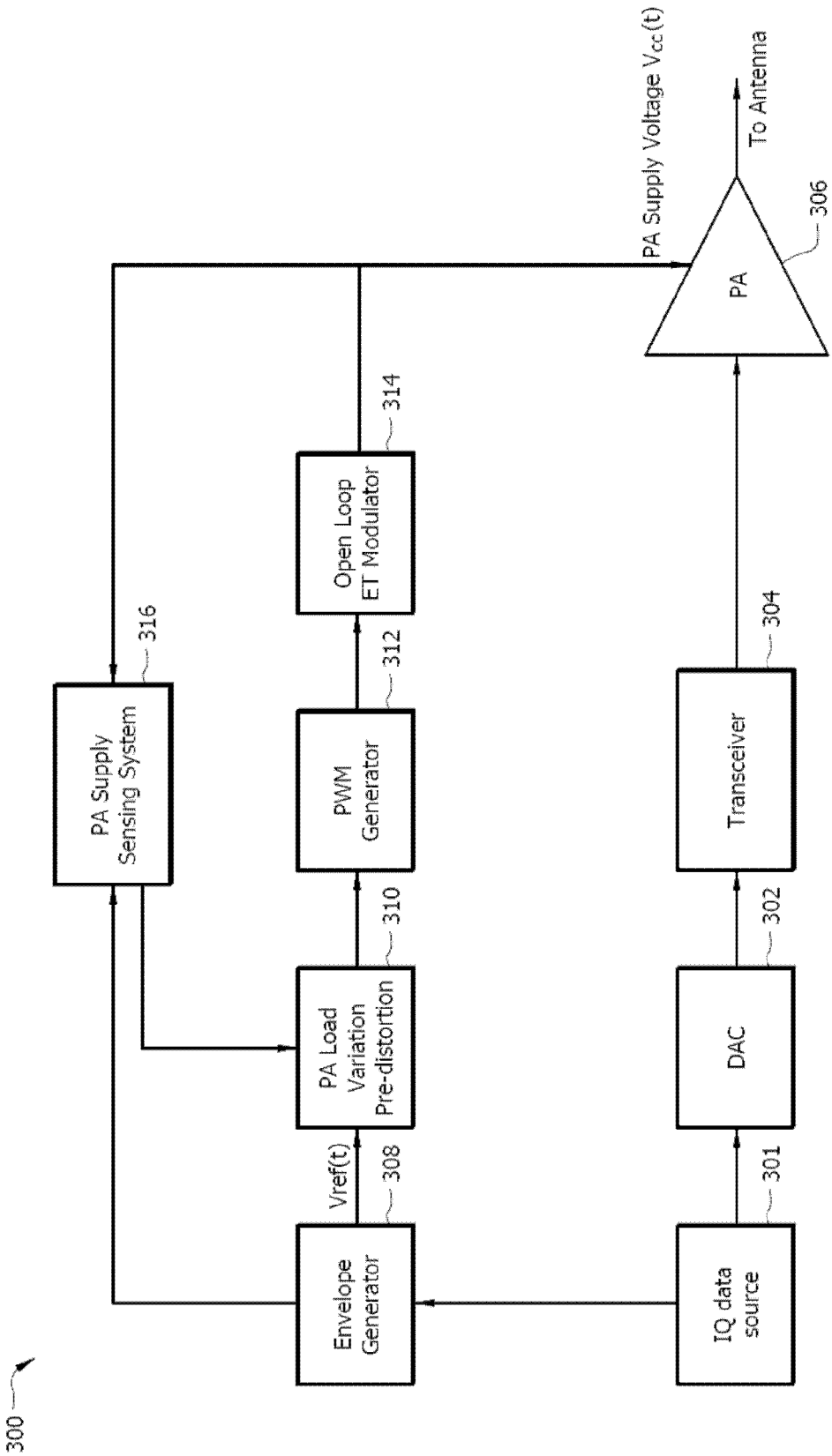

300
IQ data source
301
Envelope Generator
308
Vref(t)
DAC
302
PA Load Variation Pre-distortion
310
Transceiver
304
PWM Generator
312
PA Supply Sensing System
316
Open Loop ET Modulator
314
PA
306
PA Supply Voltage Vcc(t)
To Antenna

FIG. 3

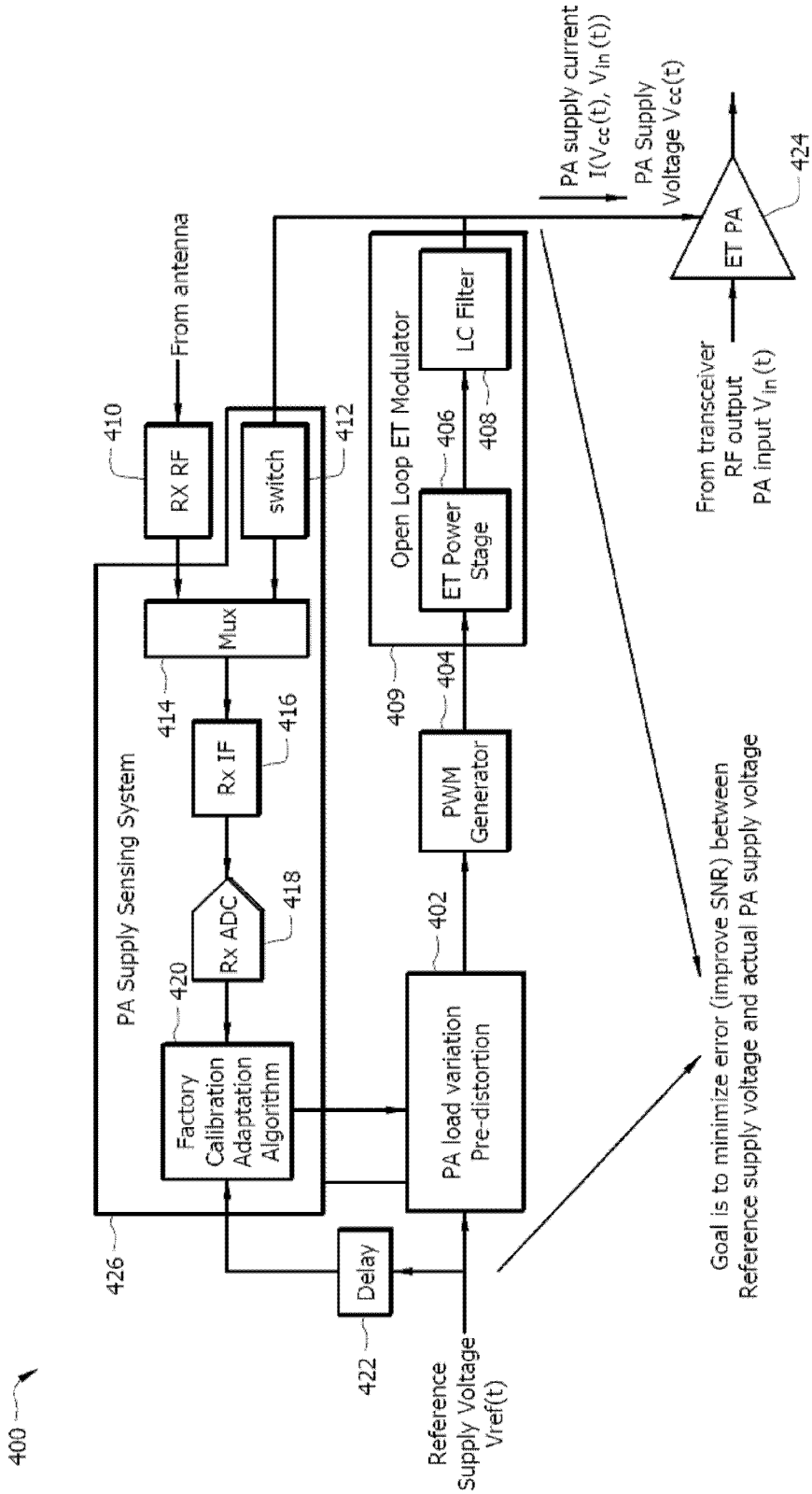

400
Reference Supply Voltage Vref(t)
422
Delay
426
PA Supply Sensing System
420
Factory Calibration Adaptation Algorithm
Rx ADC
418
Rx IF
416
414
Mux
410
RX RF
From antenna
412
switch
402
PA load variation Pre-distortion
404
PWM Generator
409
Open Loop ET Modulator
406
ET Power Stage
408
LC Filter
424
ET PA
From transceiver RF output PA input Vin(t)
PA Supply Voltage Vcc(t)
PA supply current I(Vcc(t), Vin(t))
Goal is to minimize error (improve SNR) between Reference supply voltage and actual PA supply voltage

FIG. 4

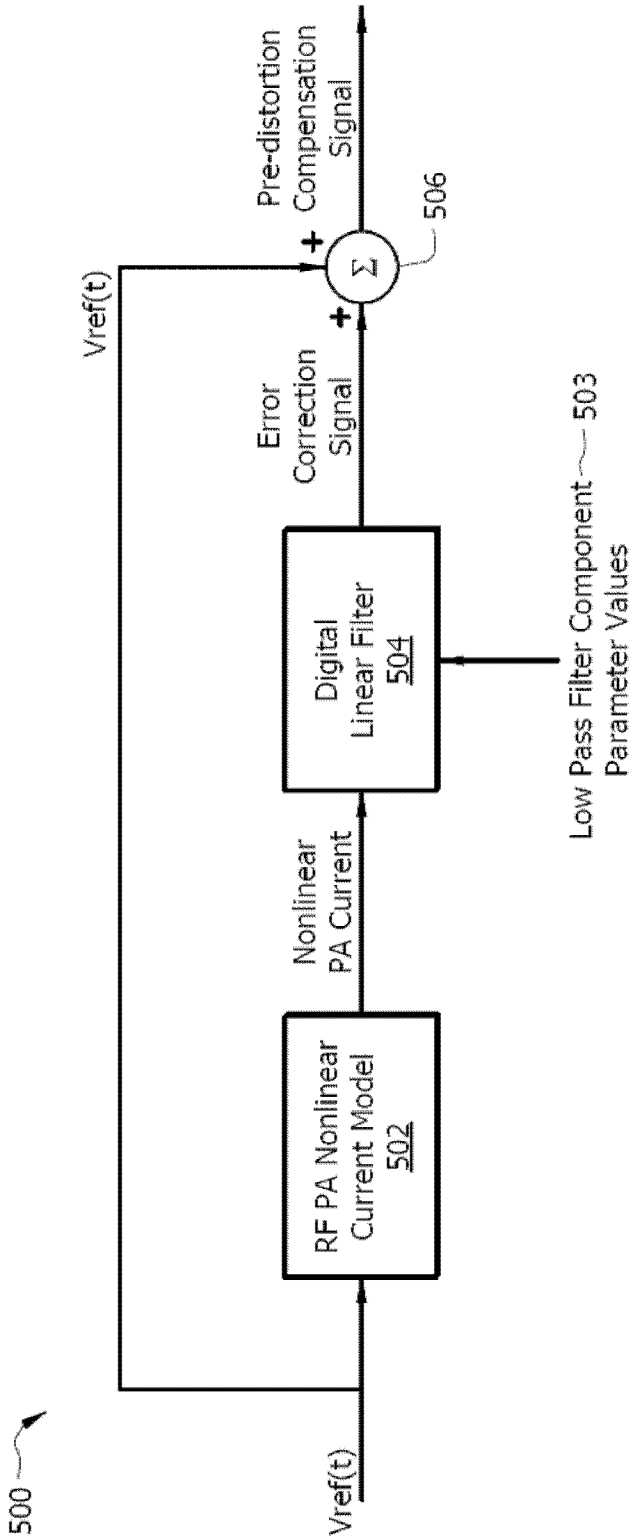

500
Vref(t)
Vref(t)
RF PA Nonlinear Current Model 502
Nonlinear PA Current
Digital Linear Filter 504
Low Pass Filter Component Parameter Values
503
Error Correction Signal
+
+
Σ
506
Pre-distortion Compensation Signal

FIG. 5

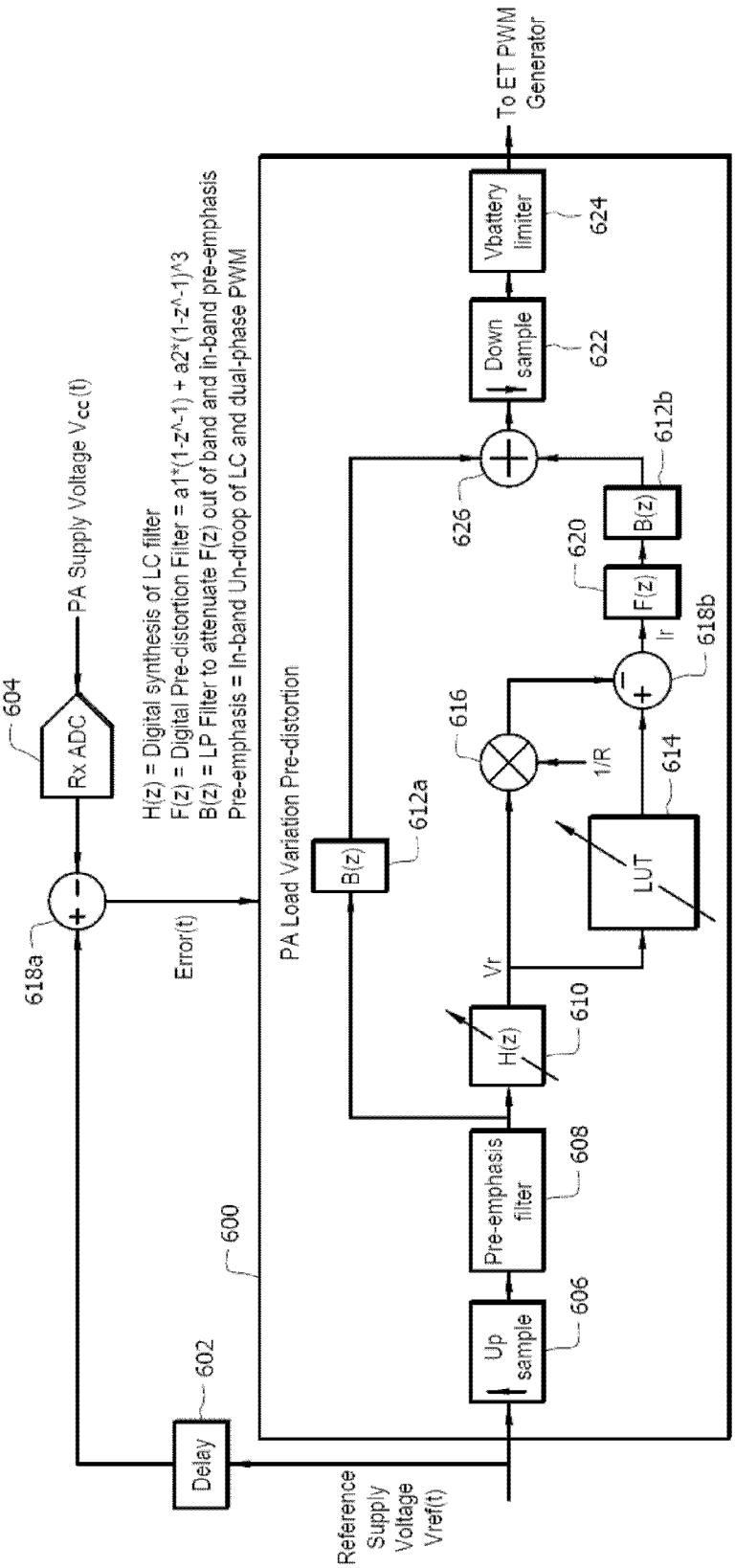

To ET PWM Generator
Vbattery limiter
624
Down sample
622
626
612b
B(z)
620
F(z)
618b
Ir
1/R
616
614
LUT
612a
B(z)
Vr
H(z)
610
Pre-emphasis filter
608
Up sample
606
600
602
Delay
Reference Supply Voltage Vref(t)
PA Load Variation Pre-distortion
Error(t)
618a
604
Rx ADC
PA Supply Voltage Vcc(t)
H(z) = Digital synthesis of LC filter
F(z) = Digital Pre-distortion Filter = a1*(1-z^-1) + a2*(1-z^-1)^3
B(z) = LP Filter to attenuate F(z) out of band and in-band pre-emphasis
Pre-emphasis = In-band Un-droop of LC and dual-phase PWM

FIG. 6

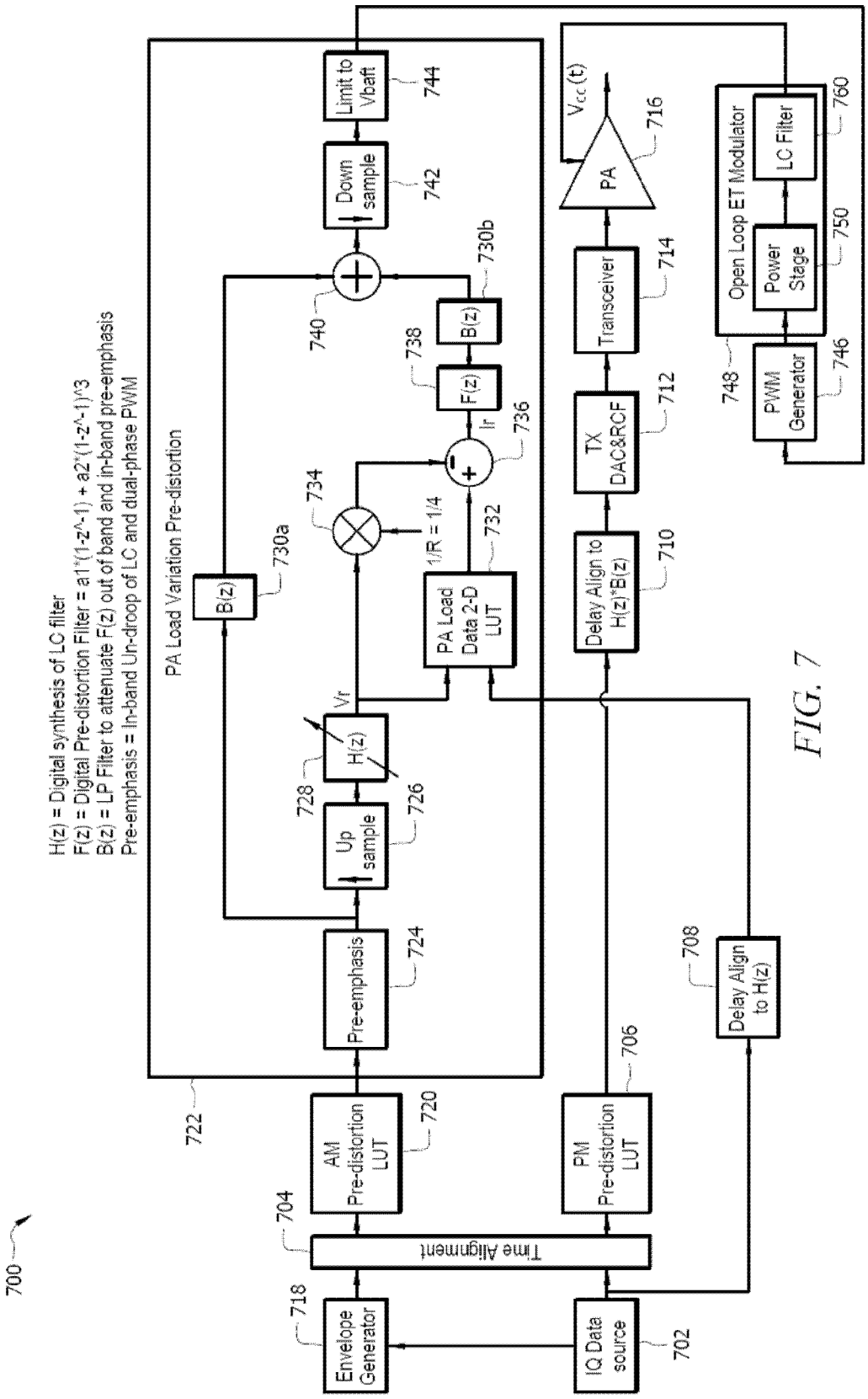

H(z) = Digital synthesis of LC filter
F(z) = Digital Pre-distortion Filter = a1*(1-z^-1) + a2*(1-z^-1)^3
B(z) = LP Filter to attenuate F(z) out of band and in-band pre-emphasis
Pre-emphasis = In-band Un-droop of LC and dual-phase PWM
700
PA Load Variation Pre-distortion
722
IQ Data source
702
Envelope Generator
718
Time Alignment
704
AM Pre-distortion LUT
720
PM Pre-distortion LUT
706
Delay Align to H(z)
708
Pre-emphasis
724
Up sample
726
H(z)
728
Vr
B(z)
730a
PA Load Data 2-D LUT
732
1/R = 1/4
734
Ir
736
F(z)
738
B(z)
730b
740
Down sample
742
Limit to Vbatt
744
Delay Align to H(z)*B(z)
710
TX DAC&RCF
712
Transceiver
714
PA
716
Vcc(t)
PWM Generator
746
748
Power Stage
750
LC Filter
760
Open Loop ET Modulator

FIG. 7

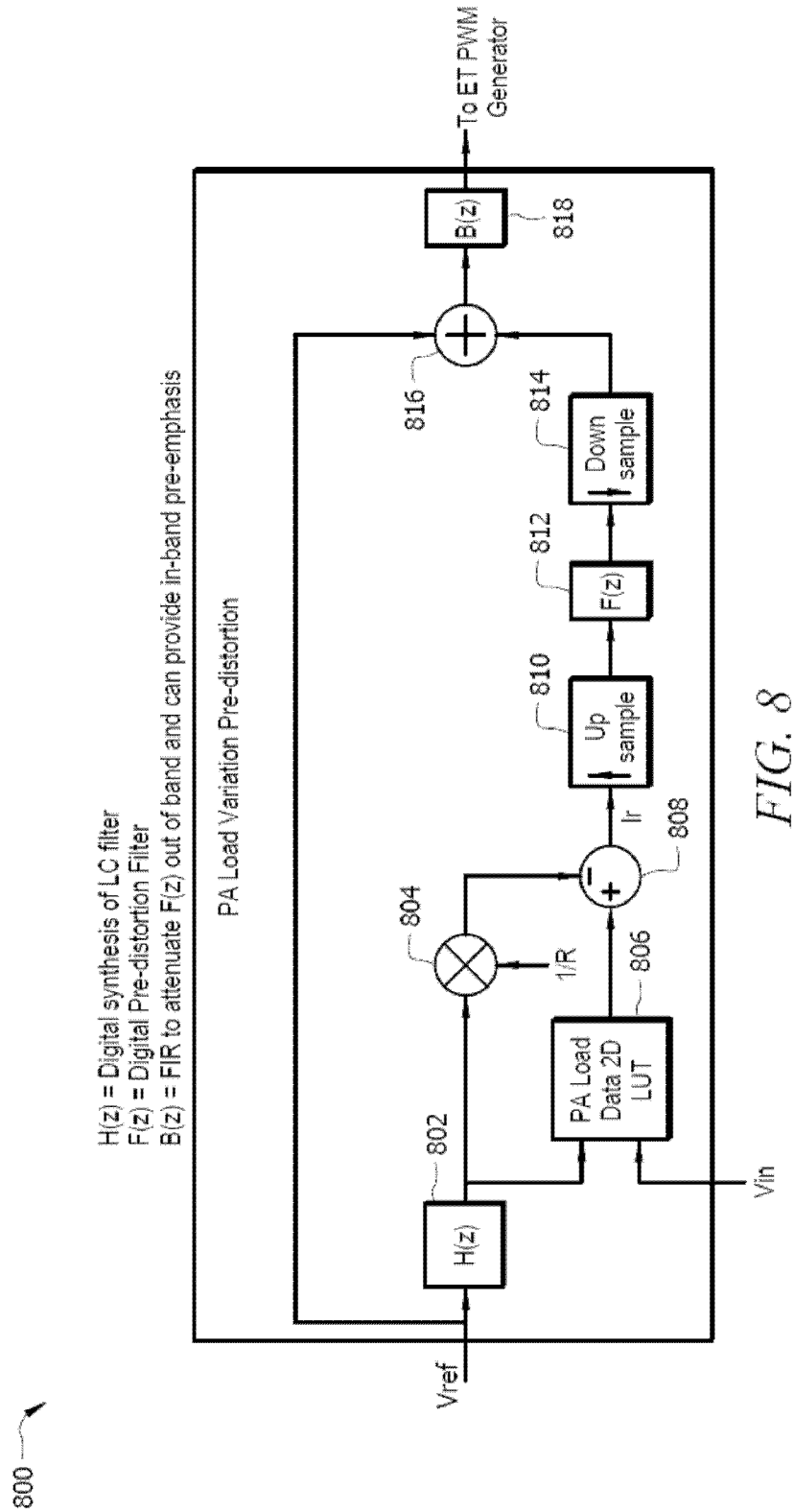

800
H(z) = Digital synthesis of LC filter
F(z) = Digital Pre-distortion Filter
B(z) = FIR to attenuate F(z) out of band and can provide in-band pre-emphasis
PA Load Variation Pre-distortion
Vref
H(z)
802
804
1/R
PA Load Data 2D LUT
806
Vin
808
Ir
Up sample
810
F(z)
812
Down sample
814
816
B(z)
818
To ET PWM Generator

FIG. 8

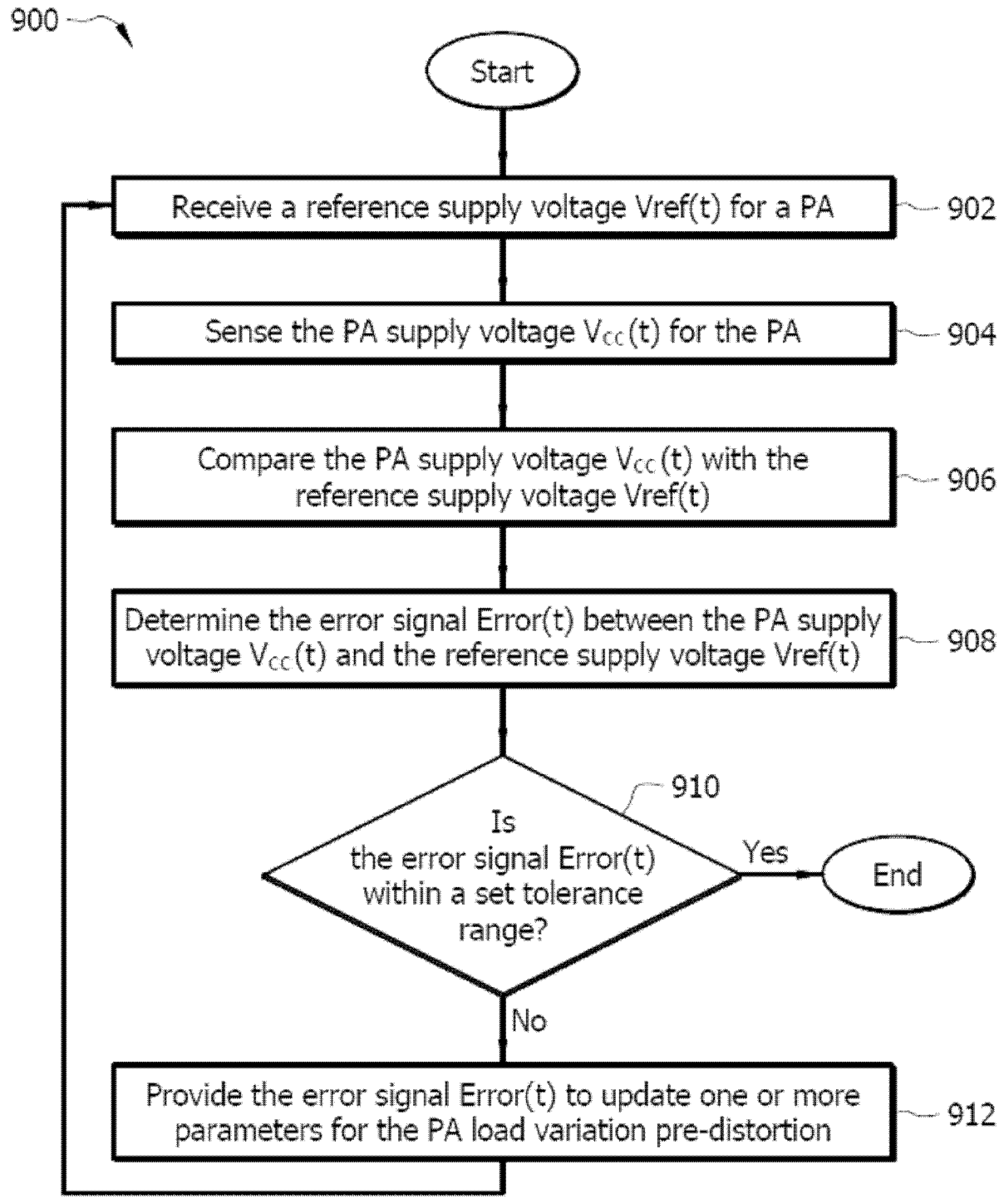

900
Start
Receive a reference supply voltage Vref(t) for a PA
902
Sense the PA supply voltage $V_{CC}(t)$ for the PA
904
Compare the PA supply voltage $V_{CC}(t)$ with the reference supply voltage Vref(t)
906
Determine the error signal Error(t) between the PA supply voltage $V_{CC}(t)$ and the reference supply voltage Vref(t)
908
910
Is the error signal Error(t) within a set tolerance range?
Yes
End
No
Provide the error signal Error(t) to update one or more parameters for the PA load variation pre-distortion
912

FIG. 9

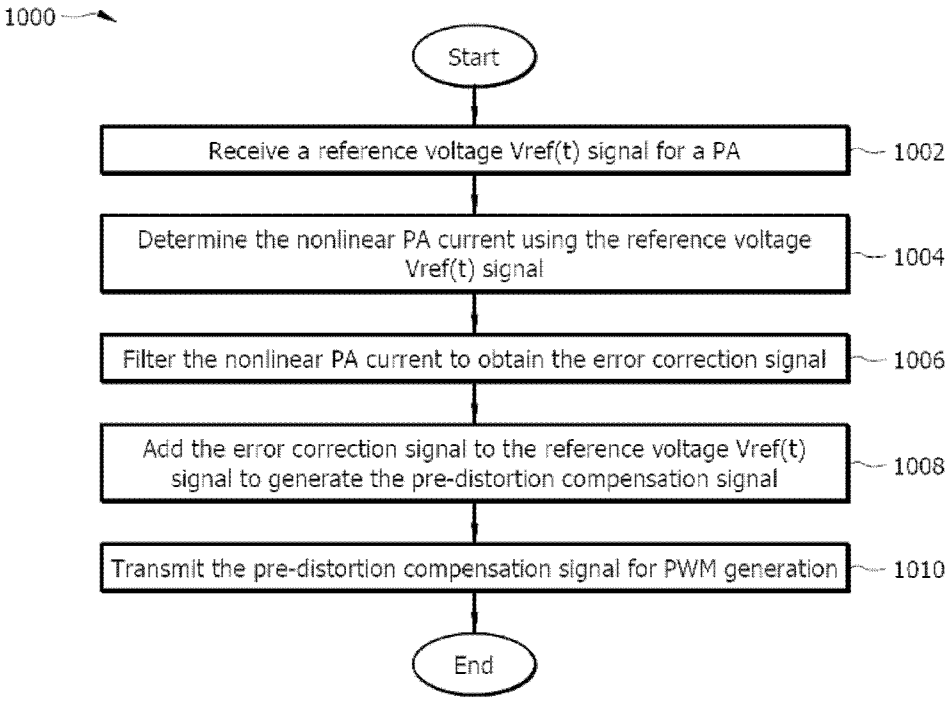

1000
Start
Receive a reference voltage Vref(t) signal for a PA
1002
Determine the nonlinear PA current using the reference voltage Vref(t) signal
1004
Filter the nonlinear PA current to obtain the error correction signal
1006
Add the error correction signal to the reference voltage Vref(t) signal to generate the pre-distortion compensation signal
1008
Transmit the pre-distortion compensation signal for PWM generation
1010
End

FIG. 10

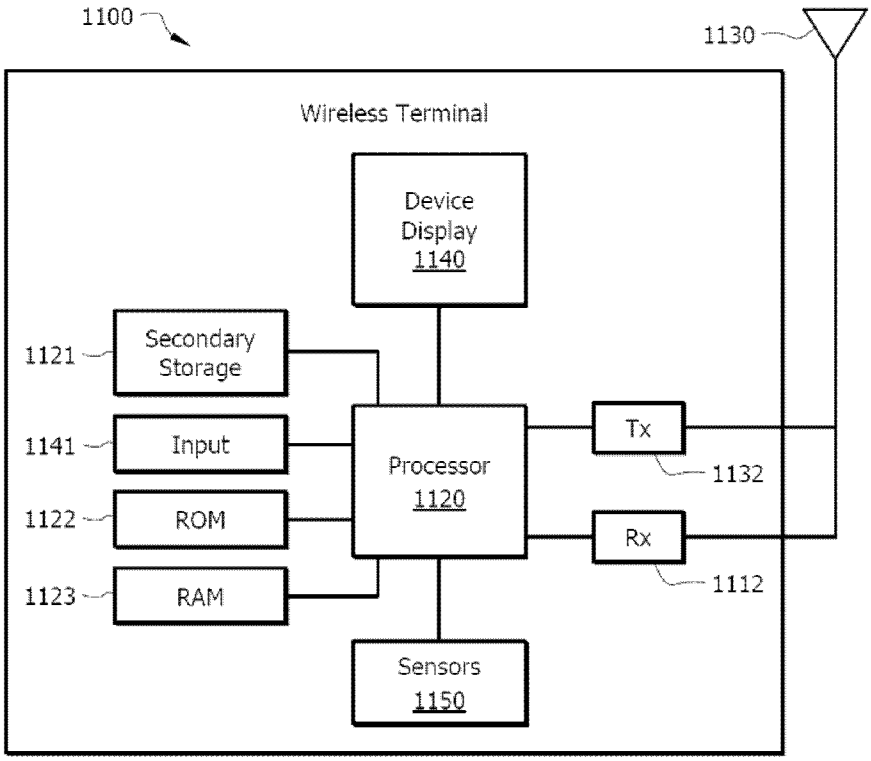

1100
1130
Wireless Terminal
Device Display 1140
1121
Secondary Storage
1141
Input
1122
ROM
1123
RAM
Processor 1120
Tx
1132
Rx
1112
Sensors 1150

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2014/092822

A. CLASSIFICATION OF SUBJECT MATTER

H03F 3/20 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F,G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,WPI,EPODOC: envelope, tracking, ET, power amplifier, PA, reference voltage, current, filter, error correction, compensation, nonlinear, mismatch, compare

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011273235 A1 (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 10 November 2011 (2011-11-10) description, paragraphs [0012]-[0017]	1-15
A	CN 101872208 A (ZTE CORPORATION) 27 October 2010 (2010-10-27) the whole document	1-15
A	CN 101207366 A (HUAWEI TECHNOLOGIES CO., LTD.) 25 June 2008 (2008-06-25) the whole document	1-15

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2015	**10 March 2015**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA(ISA/CN) **6,Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**KOU,Limin**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)61648278**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2014/092822

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2011273235 A1	10 November 2011	None	
CN 101872208 A	27 October 2010	WO 2011160329 A1	29 December 2011
CN 101207366 A	25 June 2008	US 2010253426 A1	07 October 2010
		WO 2009082922 A1	09 July 2009