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Hooghordel

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[54] **ERASING CIRCUIT FOR USE IN A DISPLAY TUBE PROVIDED WITH A STORAGE SCREEN**

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[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** ..... **307/246,** 307/247 A, 307/202, 307/268, 307/262, 315/12, 328/123, 340/173 CR

[51] **Int. Cl.** **H03k 17/00,** H01j 29/41

[58] **Field of Search** ..... 328/123, 124; 315/8.5, 8.6, 12; 340/173 CR; 307/202, 246, 247 A, 268, 262

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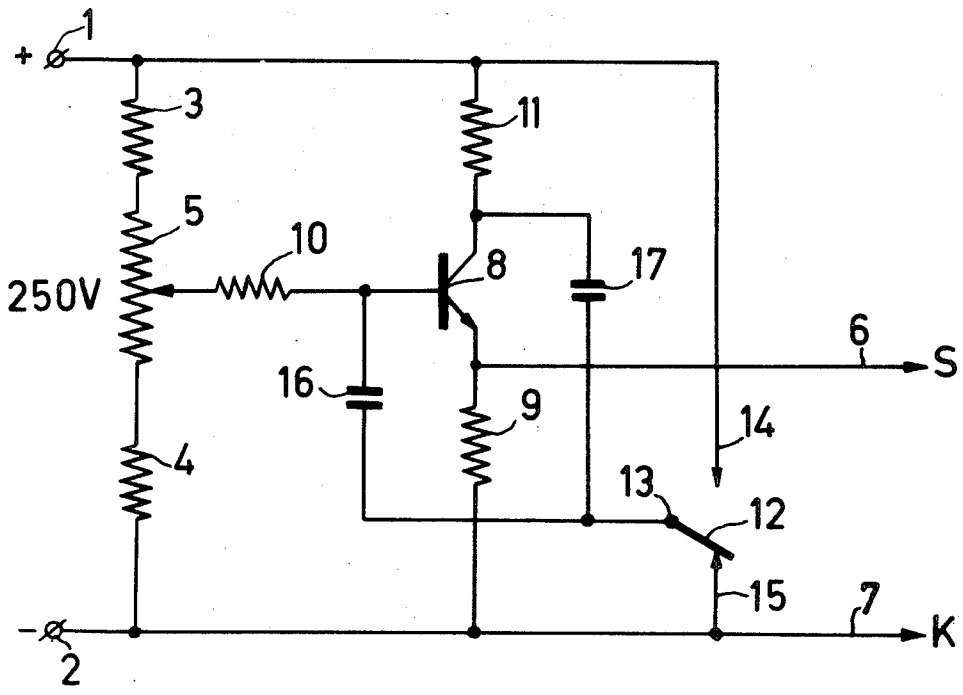
Primary Examiner—Stanley D. Miller, Jr.
Attorney—Frank R. Trifari

[57] **ABSTRACT**

To erase the information on a storage screen of a display tube there must be applied to the tube sudden potential variations which may have values of several hundreds of volts. By using a low-voltage transistor in emitter-follower connection in conjunction with transistor protective means and an appropriate RC time determination both the normal bias voltage and the sudden high-voltage potential variations may be applied to the tube.

This erasing circuit may be used in storage oscilloscopes.

5 Claims, 4 Drawing Figures



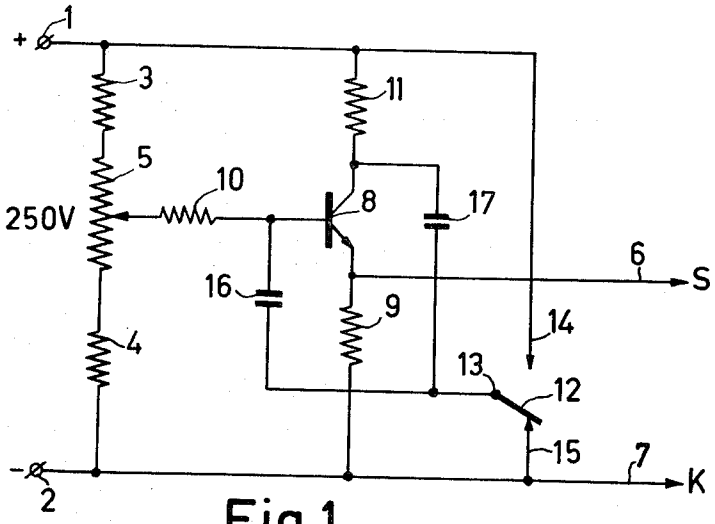

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Fig.1

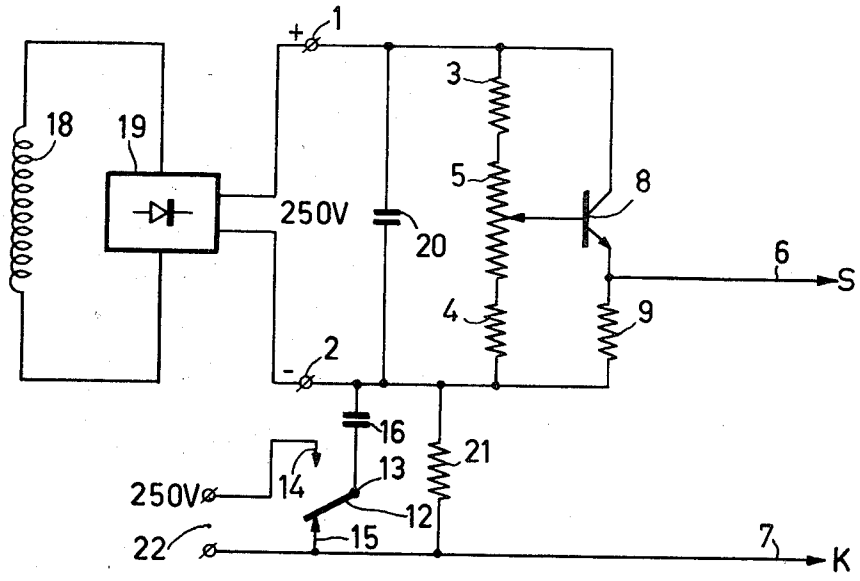
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Fig.2

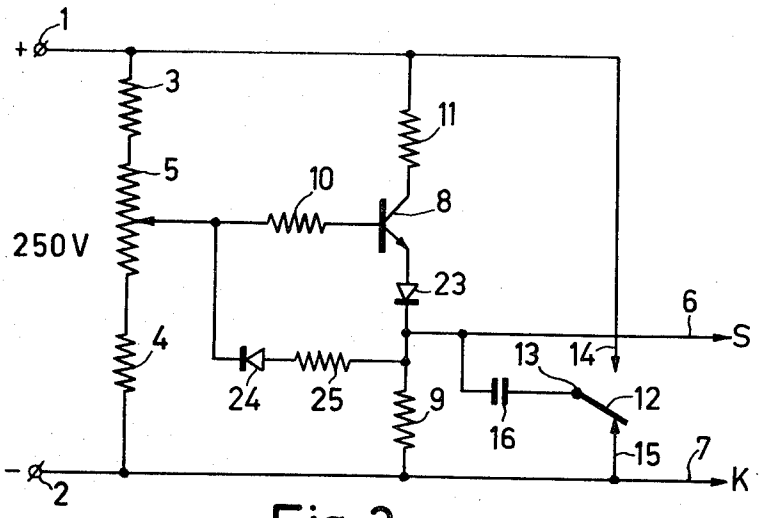
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Fig. 3

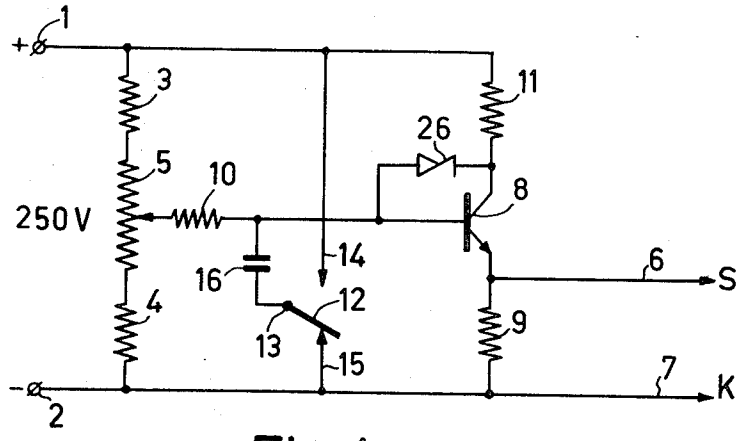
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Fig. 4

ERASING CIRCUIT FOR USE IN A DISPLAY TUBE PROVIDED WITH A STORAGE SCREEN

The invention relates to an erasing circuit for use in a display tube provided with a storage screen, which circuit comprises a direct-voltage supply source connected between the storage screen and the cathode circuit for storing information on the screen and a first capacitor one electrode of which is connected to a square-wave voltage supply source, the co-operation of the capacitor and of resistors producing an erasing voltage which is the differential of the square-wave voltage and is superposed on the voltage from the direct-voltage supply source and which erases the information on the screen.

It is known to use cathode ray tubes to display electric information. By deflecting an electron beam emitted from a cathode charges may locally be stored on a display screen or the screen may be caused to emit light. In general, in oscilloscope and television technology display tubes are used which have a display screen which emits light only when the electron beam strikes the screen, and in some cases a screen exhibiting afterglow is used. However, if the oscillogram or the information is to be stored for a prolonged period of time and hence the screen must exhibit after-flow for a very long period, a given type of storage screen may be used in conjunction with a special tube construction.

A tube of such type may be provided with a writing gun, i.e., a system which provides the controllable writing beam, at least one holding gun capable of emitting a uniform stream of electrons to the entire screen, and a special screen comprising a glass plate which is coated with a thin conductive layer which in turn is coated with a dielectric layer of, for example, a phosphor.

Depending upon the energy which the electrons have when striking the phosphor layer the secondary emission factor of the layer is smaller or greater than unity. This energy depends not only on the voltage between the cathodes and the conductive layer but also, owing to the insulating properties of the dielectric layer, on the charge present on the layer. If the emission factor is less than unity, a negative charge is collected on the screen which is supplied from the continuously spraying holding guns, and the layer assumes cathode potential. The screen is dark, no light is emitted and hence information may be written in. For this purpose the writing gun provides a beam of high-energy electrons, for its cathode is at a high negative potential of several thousands of volts relative to the screen. At the points of impact on the screen the emission factor is greater than unity, so that a positive charge builds up.

At these points the phosphor emits light, so that the oscillogram or the information becomes visible.

The positive charge attracts stray electrons which are given an energy such that the emission factor still remains greater than unity, so that after the collapse of the writing beam the information remains visible. Thus, a store in produced.

To clear this store the local charge differences must be equalized or the charges must be discharged.

It is known to use an erasing circuit for this purpose. One of the effects of the known erasing circuit is that the correct bias voltage between the spraying cathode and the conductive layer on the screen is adjusted and maintained. For this purpose a tube circuit is used which represents a direct voltage supply having a low

internal resistance and is generally referred to as cathode follower.

The anode of the tube used is connected to a supply source of a voltage of about 500 Volts, its grid is connected through a resistor to a voltage divider having a range between 150 V and 250 V, and its cathode is connected through a resistor to the common lead to which the spraying cathode also is connected and on the other hand to the conductive layer on the screen.

To enable the image on the screen to be erased the screen must be brought to a high positive potential for a given time so that the emission factor for the entire dielectric layer becomes greater than unity and hence the entire layer is given a positive charge and the entire screen emits light: equalization of the charge, after which this charge is removed, and a negative charge is applied to the layer in that the conductive layer is temporarily brought to a low potential or to zero potential relative to the spraying cathode.

The sudden positive- and negative-going voltage variations which may be superimposed on the bias voltage must be of sufficient duration to equalize the entire screen in respect of charges. For present-day storage tubes this time must be of the order of from 50 to 150 milliseconds.

The known circuit uses sudden voltage variations which decrease exponentially and are obtainable by differentiating a square-wave voltage via a capacitance-resistance network. For this purpose one electrode of a capacitor is connected to the grid of the tube and the other electrode is connected to a change-over switch which has a rest position, in which it establishes a connection to the common line, and an operative position, in which it etablishes a connection to a potential of, say, +250 V. The combination of the various resistors included in the grid circuit and the capacitor produces an RC time of a duration sufficient for the erasing process.

By changing over the switch to the operative position a sudden voltage variation of + 250 V is produced at the grid and hence at the cathode and at the screen. This voltage exponentially decreases to the initial screen bias voltage.

By returning the switch to the rest position a negative-going voltage variation is produced.

Because of the tendency to reduce the size, the weight and the power dissipation of apparatus semiconductor elements will be employed at all points where their use is possible. Furthermore endeavors should be made to reduce the cost of the apparatus.

A disadvantage of the known erasing circuit consists in the use of a tube, which is comparatively bulky, and together with its high voltage and filament-current supply devices is heavy and dissipates a considerable amount of power.

Substituting a transistor for the tube does not remove all these disadvantages: it still requires a high-voltage supply and the cost of such a high-voltage transistor is considerable.

The erasing circuit according to the invention obviates all these difficulties. Only one cheap low-voltage transistor is required, and the supply voltage may be halved, for example from 500 V to 250 V.

For this purpose an erasing circuit according to the invention is characterized in that the direct-voltage supply source includes an emitter follower circuit the emitter circuit of which is connected between the stor-

age screen and the cathode circuit and which includes at least one transistor the maximum permissible collector-emitter voltage of which is smaller than the sum of the direct voltage and the peak value of the erasing voltage. Means are provided to protect the emitter follower circuit against excessive voltages, while the point of the circuit to which the other electrode of the first capacitor is connected is chosen so that the resistors together with the capacitor and in conjunction with the said means provide the appropriate time constants.

The various embodiments of the invention are based on the recognition that sudden voltage variations are obtainable by superposition on the bias direct voltage, without an amplifier element being required to be driven through the entire peak-to-peak voltage range, by capacitive coupling, the amplifier element being switched off, being saturated or retaining a constant voltage and hence being protected against excessive voltages.

It should be borne in mind that the positive-going and the negative-going sudden voltage variations must be associated with a given RC time constant to enable adequate erasure. The time constants are to be determined for both polarities having regard to the protecting means, the adjusting resistors and the one fixed capacitor.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

FIG. 1 shows schematically an erasing circuit according to the invention in which the collector-emitter voltage remain substantially constant,

FIG. 2 shows such a circuit using a series arrangement,

FIG. 3 shows a circuit using blocking diodes and time-constant matching, and

FIG. 4 shows a circuit using collector-base protection.

Referring now to FIG. 1, a 250 V supply source is connected to terminals 1 and 2 of the erasing circuit, in which this voltage is converted to the bias voltage of from 130 V to 230 V by means of a voltage divider comprising resistors 3 and 4 and a potentiometer 5.

To obtain an adjustable direct-voltage supply source having a low internal resistance a screen S of a display tube, not shown, is connected through a lead 6 to the emitter circuit of an emitter follower to which is also connected, through a lead 7, a cathode circuit K of the display tube.

The emitter follower comprises a transistor 8 having an emitter resistor 9 and is biased, via a resistor 10 connected to the base, by means of the slider of the potentiometer 5. The collector is connected through a collector resistor 11 to the positive terminal 1, while the emitter is connected through an emitter resistor 9 and the lead 7 to the negative terminal 2. The transistor 8 is of the *npn* type.

The positive-going and negative-going sudden voltage variations used for erasing are produced by means of a change-over switch 12 which acts as a square-wave voltage supply source. For this purpose a rest contact 15 is connected to the lead 7, a make contact 14 is connected to the terminal 1 and the switch-over contact 13 is capacitively coupled to the emitter follower. The 250 V pulses are produced via a capacitor 16 connected between the base of the transistor 8 and the switch-over contact 13 and decay exponentially owing to the provision of a base equivalent resistance comprising the resistors of the voltage divider 3, 4 and 5, the base resistor 10 and the input resistance of the transistor circuit. The peak-to-peak value of the sudden voltage variations is substantially 500 V. The transistor 8 has a maximum permissible collector-emitter voltage of, for example, 180 V. To protect the transistor a capacitor 17 is connected between the switch-over contact 13 and the collector of the transistor 8. The time constant of the base circuit, which constant is determined by the capacitor 16 and the base equivalent resistance, is made equal to, or slightly greater than, the time constant of the collector circuit. This latter constant is determined by the capacitor 17 connected in parallel with the collector resistor 11, the emitter resistor 9 and the screen load. Thus there are produced at the three electrodes of the transistor equal sudden voltage variations which decay exponentially at a substantially identical rate. Consequently, the voltages between the said electrodes remain constant and there is no risk of the transistor limit voltages being exceeded.

In the circuit diagram shown in FIG. 2 elements corresponding to those of FIG. 1 are designated by the same reference numerals. In this circuit, however, the direct-voltage supply source is floating, because the emitter follower circuit is fed from a separate winding 18 of a supply transformer, for example of a DC-AC inverter of a line voltage transformer, through a rectifying circuit 19 which may also act as a voltage stabilizer. The terminal 2 and hence the common lead of the emitter follower circuit are separate from the lead 7 to the cathode K but are connected to it through a small resistor 21.

The change-over switch 12 is fed from a separate source 22 of 250 V, the rest contact 15 being connected to the lead 7 and the make contact 14 being connected to the + 250 V terminal. The switch-over contact 13 is connected via the capacitor 16 to the emitter follower circuit, or strictly speaking to the said common lead thereof.

When the switch 12 is thrown over, the desired erasing voltages are produced across the resistor 21, the RC time constant being determined by the capacitor 16 and the resistor 21. These sudden voltage variations are in series with the screen bias voltage as measured across the emitter resistor 9. The resistor 21 is given a small value because, seen from the display tube, it increases the internal resistance of the direct-voltage source. Since because of the series arrangement the erasing current to the display tube must pass through the emitter follower circuit, it is ensured that this current cannot produce a voltage drop which might damage the transistor by giving the supply part a low internal resistance, for example by means of a buffer capacitor 20. The current drive of the transistor 8 has a magnitude such that the transistor is not cut off and the erasing current is permissible as a modulation of its bias current.

In the circuit shown in FIG. 3 the sudden voltage variation obtained by means of the switch 12 and the capacitor 16 is directly set up at the lead 6 to the screen S.

For the negative-going pulse the capacitor 16 and the switch 12 form a load of the emitter follower. The latter will deliver a large current so that the transistor 8 is driven into saturation by the provision of the base resistor 10, the voltage divider 3, 4 and 5 and the collector

resistor 11. In this circuit, the equivalent resistor used for determining the RC time must be constituted by the parallel arrangement of the said resistors with the emitter resistor 9 and the screen load.

The positive-going pulse causes a diode 23 included between the emitter of the transistor 8 and the emitter current to cut off, so that the transistor is shielded against the high voltage. Since the RC time for this pulse must be of the same order as for the negative-going pulse, a parallel path is provided in the form of a resistor 25 and a diode 24 which ensures that the value of the resistor 25 is equal to the parallel resistance of the resistors 10 and 11.

In the circuit shown in FIG. 4 one electrode of the capacitor 16 is connected between the base resistor 10 and the transistor 8.

When the positive-going pulse appears the emitter follower follows the input voltage, but by the larger current it is driven into saturation owing to the collector resistor 11. As a result, a diode 26 connected between the base and the collector will be biassed in the forward direction, so that no high voltages are applied to the transistor electrodes. With respect to the RC time, account must be taken of the parallel arrangement of the resistor 10 with the voltage divider 3, 4 and 5 and further of the resistor 11, the resistor 9 and the screen load.

The negative-going pulse is also passed by the emitter follower, causing the collector-emitter voltage of the transistor to rise to a value at which the diode 26 will break down in the reverse direction. This breakdown voltage is such that the maximum permissible voltages across the transistor are not exceeded. The diode 26 may be a Zener diode of a particular type.

In the circuit shown in FIG. 4 it is desirable for the RC time for negative-going and positive-going sudden voltage variations to be mainly determined by the resistor 10 and the voltage divider 3, 4 and 5. Owing to the parallel connection of the resistors 11 and 9 and the screen load the time thus obtained for the positive-going voltage variation will be slightly shorter than that obtained for the negative-going variation, which at the beginning of the pulse has the same RC time as long as the diode 26 is operated in the breakdown direction.

It has been found, however, that writing on the screen by means of the positive-going voltage pulse is not as critical as erasure by means of the negative-going pulse, so that the proportions of the circuit must be matched to the latter erasing stage.

What is claimed is:

1. An erasing circuit for use in a display tube provided with a storage screen and a cathode circuit, comprising a DC voltage source, a potentiometer connected in parallel with the DC voltage source, a transistor having a base, an emitter and a collector, means connecting the potentiometer to the base of the transistor, a resistor, means connecting the emitter of the transistor to the DC voltage source through the resistor, means connecting the cathode circuit of the display tube to the side of the DC voltage supply connected to the emitter of the transistor, means connecting the collector of the transistor to a side of the DC voltage supply remote from the emitter of the transistor, a square wave voltage supply, a capacitor, means connecting the square wave voltage supply to the base of the transistor through the capacitor, whereby the capacitor and the potentiometer provide a circuit for applying the differential of the square wave to the base of the transistor thereby superimposing the differential of the square wave voltage on the potential from the DC voltage source, the maximum permissible collector-emitter voltage of the transistor being smaller than the sum of the direct voltage from the DC voltage source and the peak value of the differentiated square wave, means connected to the collector of the transistor for protecting the transistor against excessive voltages, and means connecting the emitter of the transistor to the storage screen of the display tube.

2. An erasing circuit as claimed in claim 1, wherein the capacitor is directly connected to the base of the transistor, wherein the means connecting the collector of the transistor to the DC voltage supply comprises a resistor, and wherein the protection means comprises a second capacitor having one electrode connected to the collector of the transistor and having the other electrode connected to the square wave voltage supply, the time constant of the first capacitor and the associated resistors being at least equal to the time constant of the second capacitor and the parallel combination of the emitter circuit equivalent resistors and the resistor connected between the collector and the DC voltage source.

3. An erasing circuit as claimed in claim 1, wherein the means connecting the cathode circuit of the display tube to the DC supply comprises a second resistor, wherein the square wave voltage source is connected to the base of the transistor through the capacitor and the potentiometer, and wherein the means for protecting the transistor comprises a low internal resistance of the DC voltage source.

4. An erasing circuit as claimed in claim 1, wherein the protection means comprises a second resistor connecting the emitter of the transistor to the DC voltage source, a third resistor connecting the base of the transistor to the potentiometer, a diode connecting the emitter of the transistor to the first resistor and having a low resistance conduction path in the direction of conduction through the emitter of the transistor, a fourth resistor, a second diode connected in series with the fourth resistor, means connecting the side of the diode remote from the fourth resistor to the side of the third resistor remote from the base of the transistor, and means connecting the side of the fourth resistor remote from the diode to the side of the first diode remote from the emitter of the transistor.

5. An erasing circuit as claimed in claim 1, wherein the protection means comprises a second resistor connecting the collector of the transistor to the DC voltage source, a diode connected in parallel with the base-collector path of the transistor, the diode having the same forward direction of conduction as the base-collector diode of the transistor and having a reverse breakdown voltage below the maximum permissable base-collector voltage of the transistor, the means connecting the base of the transistor to the potentiometer comprising a third resistor, and wherein the side of the capacitor remote from the square wave voltage supply is connected to the side of the third resistor remote from the potentiometer.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,751,688 Dated August 7, 1973

Inventor(s) RIJK HOOGHORDEL

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

IN THE TITLE PAGE

"[75] Inventor: Rojk Hooghordel, Emmasingel, Eindhoven, Netherlands "

should read

--[75] Inventor: Rijk Hoohordel, Emmasingel, Eindhoven, Netherlands --;

IN THE SPECIFICATION

Col. 1, line 25, "after-flow" should be --after--glow--;

Col. 2, line 34, "etablishes" should be --establishes--;

Signed and sealed this 20th day of November 1973.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

RENE D. TEGTMEYER
Acting Commissioner of Patents

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(5/64)

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