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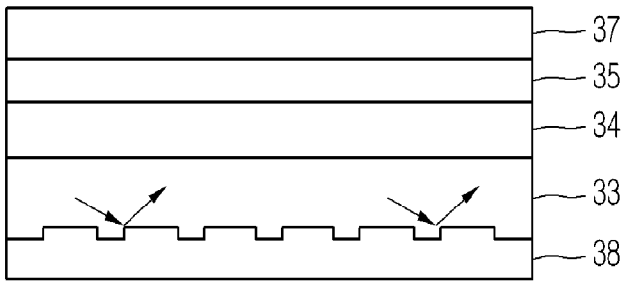
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(54) **Title:** SEMICONDUCTOR LIGHT EMITTING DEVICE AND FABRICATION METHOD THEREOF



(57) **Abstract:** A semiconductor light emitting device includes a first semiconductor layer having a bottom surface with uneven patterns, an active layer formed on the first semiconductor layer, a second semiconductor layer formed on the active layer, a second electrode formed on the second semiconductor layer, and a first electrode formed under the first semiconductor layer.

WO 2007/013757 A1

Description

SEMICONDUCTOR LIGHT EMITTING DEVICE AND FABRICATION METHOD THEREOF

Technical Field

[1] The present invention relates to a semiconductor light emitting device and a fabrication method thereof.

Background Art

[2] In general, a semiconductor light emitting device, for example, a light emitting diode, has a stack structure in which an n-type semiconductor layer, a light emitting region, and a p-type semiconductor layer are stacked on a substrate. An electrode is formed on the p-type semiconductor layer and the n-type semiconductor layer. As an electron injected from the semiconductor layer recombines a hole, light is generated from the light emitting region. The light generated from the light emitting region is emitted from a light-transmittable electrode on the p-type semiconductor layer or from the substrate. Here, the light-transmittable electrode on an almost entire surface of the p-type semiconductor layer is a light-transmittable electrode formed of a thin metal layer or a transparent conductive layer.

[3] The color (i.e., wavelength) of light emitted from the light emitting diode is determined depending on a semiconductor material used to manufacture the light emitting diode. This is because the wavelength of the emitted light corresponds to a band gap of the semiconductor material, which is defined as an energy difference between electrons in the valence band and electrons in the conduction band.

[4] Fig. 1 is an exemplary schematic view showing a structure of a related art semiconductor light emitting device.

[5] As shown in Fig. 1, the related semiconductor light emitting device includes a substrate 11, a buffer layer 12, an n-type cladding layer 13, an active layer 14, a p-type cladding layer 15, a p-type contact layer 16, a p-type electrode 17, and an n-type electrode 18.

[6] Because the stack structure of the semiconductor light emitting device is controlled at the atomic level, substrate processing is performed to provide the substrate with flatness of a mirror surface. Thus, the semiconductor layers 12, 13 and 15, the active layer 14, and the electrodes 17 and 18 are stacked on the substrate 11 parallel to one another.

[7] The semiconductor layer has a great refractive index, and a waveguide is constructed by a surface of the p-type cladding layer 15, and a surface of the substrate 11. Accordingly, when light is incident upon a surface of the p-type electrode 17 or a

surface of the substrate 11 at a predetermined critical angle or greater, the incident light is reflected by an interface between the p-type electrode 17 and the p-type cladding layer 15, or by the surface of the substrate 11, and propagates through the inside of the stack structure of the semiconductor layers in a horizontal direction. During such propagation, light is confined within the waveguide and may be lost. For this reason, external quantum efficiency cannot be achieved as much as expected.

[8] As one method to eliminate aforementioned defections and improve the external quantum efficiency, a semiconductor light emitting device as illustrated in Fig. 2 has been proposed. Fig. 2 is a schematic view showing a different example of the related art semiconductor light emitting device.

[9] As shown in Fig. 2, the improved semiconductor light emitting device includes a substrate 21, a buffer layer 22, an n-type cladding layer 23, an active layer 24, an p-type cladding layer 25, a p-type contact layer 26, a p-type electrode 27, and an n-type electrode 28.

[10] As compared to the related art semiconductor light emitting device illustrated in Fig. 1, the substrate 21 of the improved semiconductor light emitting device has a top surface with uneven patterns. The buffer layer 22 is formed on the uneven surface of the substrate 21, and the n-type cladding layer 23 is stacked thereon.

[11] In the semiconductor light emitting device having the flat substrate illustrated in Fig. 1, when light propagates in the semiconductor layer in the horizontal direction, a portion of the light is absorbed into the semiconductor layer or the electrode, which causes attenuation of light coming out of the semiconductor layer.

[12] In comparison, as for the improved semiconductor light emitting device illustrated in Fig. 2, light propagating in the horizontal direction is scattered or diffracted. Thus, light can be efficiently emitted from the upper semiconductor layers 22, 23, 24 and 25 or from the lower substrate 21, contributing to improving the external quantum efficiency.

[13] In the case of the improved semiconductor light emitting device illustrated in Fig. 2, injected carriers move on surfaces and interfaces, thereby generating electrical conductivity. A high drive voltage applied within a predetermined area for the light emission allows a large amount of injected carriers (electrons) to flow. Here, a current flows through a thin layer of the n-type cladding layer 23 located under the n-type electrode 28. A current density-concentrated region is located closely to the n-type electrode 28.

[14] In this region, current crowding occurs, which makes the current density relatively high. When such a region where the current distribution is concentrated is generated, a temperature drastically increases. Then, generated heat lowers the light emitting efficiency, and consequently, reliability of a device is reduced in the long run.

[15] Also, the proximity of the two electrodes makes the semiconductor light emitting device vulnerable to static electricity. Because the substrate is an insulating substrate, thermal dissipation is not improved even if a heat sink is attached to the substrate.

[16] Therefore, research is made on a semiconductor light emitting device that can improve the external quantum efficiency and the thermal dissipation.

Disclosure of Invention

Technical Problem

[17] The present invention provides a semiconductor light emitting device and a fabrication method thereof that can improve external quantum efficiency and thermal dissipation.

Technical Solution

[18] The present invention provides a semiconductor light emitting device. The semiconductor light emitting device includes a first semiconductor layer having a bottom surface with uneven patterns; an active layer formed on the first semiconductor layer; a second semiconductor layer formed on the active layer; a second electrode formed on the second semiconductor layer; and a first electrode formed under the first semiconductor layer.

[19] The present invention provides a method for fabricating a semiconductor light emitting device, the method includes forming a first semiconductor layer on a substrate; forming an active layer on the first semiconductor layer; forming a second semiconductor layer on the active layer; removing the substrate; forming uneven patterns on the first semiconductor layer; and forming a first electrode on the first semiconductor layer, and forming a second electrode on the second semiconductor layer.

Advantageous Effects

[20] According to the present invention, external quantum efficiency and thermal dissipation may be improved.

Brief Description of the Drawings

[21] Fig. 1 is a schematic view showing one example of a structure of a related art semiconductor light emitting device;

[22] Fig. 2 is a schematic view showing another example of a structure of the related art semiconductor light emitting device;

[23] Fig. 3 is a schematic view showing a structure of a semiconductor light emitting device according to the present invention;

[24] Figs. 4 to 11 are views illustrating a process of fabricating the semiconductor light emitting device according to the present invention; and

[25] Fig. 12 is a schematic view showing another structure of the semiconductor light

emitting device according to the present invention.

Mode for the Invention

[26] It will be understood that when a substrate, a layer (film), a region, a pattern, or a structure are referred to as being "on/above/over/upper" or "down/below/under/lower" another substrate, layer, region, pad or pattern, they can directly contact the other substrate, layer, region, pad or pattern, or intervening layers, regions, pads, patterns or structures may also be present. The meaning must be understood based on the technical concept of the present invention.

[27] An embodiment of the present invention will now be described in detail with reference to accompanying drawings.

[28] Fig. 3 is a schematic view showing a structure of a semiconductor light emitting device according to the present invention.

[29] As illustrated in Fig. 3, the semiconductor light emitting device according to the present invention includes an n-type cladding layer 33 having a bottom surface with uneven patterns, an active layer 34 formed on the n-type cladding layer 33, and a p-type cladding layer 35 formed on the active layer 34.

[30] The semiconductor light emitting device according to the present invention may further include a p-type electrode 37 formed on the p-type cladding layer 35, and an n-type electrode 38 formed under the n-type cladding layer 33. A p-type contact layer 36 may be further formed between the p-type cladding layer 35 and the p-type electrode 37.

[31] The n-type cladding layer 33 may be an n-GaN cladding layer, and the p-type cladding layer 35 may be a p-GaN cladding layer. The active layer 34 may have a single quantum well structure or a multi-quantum well structure.

[32] The uneven patterns of the n-type cladding layer 33 may be formed at regular intervals or at different intervals. The n-type electrode 38 may be formed over the entire uneven surface of the n-type cladding layer 33.

[33] The semiconductor light emitting device having such a stack structure according to the present invention has a vertical structure in which the n-type electrode 38 and the p-type electrode 37 are formed at lower and upper parts of the device, respectively. Accordingly, the concentration of the current density near the n-type electrode, which is a problem of a related art planar structure, may be prevented.

[34] That is, in the semiconductor light emitting device according to the present invention, the p-type electrode 37 and the n-type electrode 38 are stacked parallel at upper and lower parts. Accordingly, the current density is not concentrated in a specific region, but may be evenly distributed over an entire region corresponding to the n-type electrode 38. In this manner, the current crowding is prevented from

occurring at a specific portion of the n-type electrode 38, thereby preventing a drastic increase in temperature at this specific region.

[35] Also, because the two electrodes are placed at a sufficient distance therebetween in the semiconductor light emitting device according to the present invention, the device has a property that is proof against the static electricity. The thermal dissipation of the semiconductor light emitting device may also be improved by, for example, attaching the device to a heat sink.

[36] In addition, in the semiconductor light emitting device according to the present invention, light propagating in the horizontal direction is scattered or diffracted in the region where the uneven patterns of the n-type cladding layer 33 are formed. Therefore, the external quantum efficiency can be greatly improved.

[37] Then, a process of fabricating the semiconductor light emitting device according to the present invention having such a structure will now be described with reference to Figs. 4 to 11. Figs. 4 to 11 are views for describing the process of fabricating the semiconductor light emitting device according to the present invention.

[38] In the method for fabricating the semiconductor light emitting device according to the present invention, as illustrated in Fig. 4, a buffer layer 32, an n-type cladding layer 33, an active layer 34, and a p-type cladding layer 35 are stacked on a substrate 31. The buffer layer 32 may be excluded, but is formed as one of methods to improve characteristics of the semiconductor layer. The n-type cladding layer 33 may be an n-GaN cladding layer, and the p-type cladding layer 35 may be a p-GaN cladding layer.

[39] Then, as illustrated in Fig. 5, the substrate 31 is removed from the resulting structure. The substrate 31 may be separated and removed by a laser lift-off method. In the laser lift-off method, an eximer laser may be used to separate and remove the substrate 31.

[40] As illustrated in Figs.6 and 7, the buffer layer 32 is removed to expose the n-type cladding layer 33. Chemical mechanical polishing or etching may be performed to remove the buffer layer 32 and expose the n-type cladding layer 33.

[41] As illustrated in Fig. 8, a photoresist layer 41 is formed on the n-type cladding layer 33, and patterning is performed thereon. Then, the patterned photoresist layer 41 is etched to form uneven patterns 43 in the n-type cladding layer 33. The uneven patterns 43 of the n-type cladding layer 33 may be formed at regular intervals or different intervals.

[42] Then, the photoresist layer 41 is removed. As illustrated in Fig. 10, an n-type electrode 38 is formed on the n-type cladding layer 33 where the uneven patterns are formed, and a p-type electrode 37 is formed on the p-type cladding layer 35. The n-type electrode 38 may be formed over the entire surface of the n-type cladding layer 33, and the p-type electrode 37 may be formed over the entire surface of the p-type

cladding layer 35. Preferably, one of the n-type electrode 38 and the p-type electrode 37 formed over the entire surfaces is formed as a transparent electrode. As illustrated in Fig. 3, a p-type contact layer 36 may be further formed between the p-type cladding layer 35 and the p-type electrode 37.

[43] As illustrated in Fig. 11, in the semiconductor light emitting device fabricated in the aforementioned manner, light propagating in the horizontal direction is scattered or diffracted in the region of the n-type cladding layer 33 where the uneven patterns 43 are formed. Accordingly, the external quantum efficiency of the semiconductor light emitting device according to the present invention can be improved to a great extent.

[44] Also, in the semiconductor light emitting device according to the present invention, the p-type electrode 37 and the n-type electrode 38 are stacked parallel at the upper and lower parts thereof. Thus, the current density is not concentrated in a specific region, but is evenly distributed over the entire region corresponding to the n-type electrode 38. Accordingly, the current crowding is prevented from occurring at a specific portion of the n-type electrode 38, so that a drastic increase in temperature in the specific region can be prevented from occurring.

[45] In addition, because the two electrodes are placed at a sufficient distance therebetween in the semiconductor light emitting device according to the present invention, the device can be proof against the static electricity. The thermal dissipation property of the semiconductor light emitting device may also be improved through a method of attaching the device to a heat sink or the like.

[46] Although in the present embodiment, the case where the buffer layer 32 is removed to expose the n-type cladding layer 33 is described, the buffer layer 32 may not be completely removed. That is, as shown in Fig. 12, uneven patterns may be formed in both the buffer layer 42 and the n-type cladding layer 33 through etching, and the n-type electrode 38 may be formed thereon. The buffer layer 32 may be formed of a conductive material. Fig. 12 is a schematic view showing another structure of the semiconductor light emitting device according to the present invention.

[47] In the present embodiment, the uneven patterns are formed in the n-type cladding layer 35, and the n-type electrode 38 is formed on the surface where the uneven patterns are formed. However, the present invention is not limited thereto, and such uneven patterns may be formed in the p-type cladding layer 35.

[48] In the present embodiment, the semiconductor light emitting device of a p-n junction structure is described as an example, in which the p-type semiconductor layer is formed at an upper part and the n-type semiconductor layer is formed at a lower part. However, the semiconductor light emitting device may have an n-p-n junction structure where an n-type semiconductor layer is further formed on the p-type semiconductor layer. The n-p-n junction structure means that a first electrode layer and a

second electrode layer are all formed as n-type semiconductor layers, and a p-type semiconductor layer is formed therebetween. A first electrode is formed on the first electrode layer, the n-type semiconductor layer, and the second electrode is formed on the second electrode layer, the n-type semiconductor layer.

Industrial Applicability

[49] According to the semiconductor light emitting device and the fabrication method thereof, the external quantum efficiency and the thermal dissipation can be improved.

Claims

[1] A semiconductor light emitting device comprising:
a first semiconductor layer having a bottom surface with uneven patterns;
an active layer formed on the first semiconductor layer;
a second semiconductor layer formed on the active layer;
a second electrode formed on the second semiconductor layer; and
a first electrode formed under the first semiconductor layer.

[2] The semiconductor light emitting device according to claim 1, wherein the first semiconductor layer is an n-type semiconductor layer, and the second semiconductor layer is a p-type semiconductor layer.

[3] The semiconductor light emitting device according to claim 1, wherein the uneven patterns of the first semiconductor layer are formed at regular intervals.

[4] The semiconductor light emitting device according to claim 1, wherein the uneven patterns of the first semiconductor layer are formed at different intervals.

[5] The semiconductor light emitting device according to claim 1, wherein at least the first electrode is formed over the entire surface of the first semiconductor layer, or at least the second electrode is formed over the entire surface of the second semiconductor layer.

[6] The semiconductor light emitting device according to claim 1, wherein at least one of the first and second electrode is a transparent electrode.

[7] The semiconductor light emitting device according to claim 1, further comprising a third semiconductor layer formed between the second semiconductor layer and the second electrode.

[8] The semiconductor light emitting device according to claim 7, wherein the first and third semiconductor layers are n-type semiconductor layers, and the second semiconductor layer is a p-type semiconductor layer.

[9] The semiconductor light emitting device according to claim 1, further comprising a buffer layer formed between a convex portion of the uneven patterns of the first semiconductor layer and the first electrode.

[10] A method for fabricating a semiconductor light emitting device, the method comprising:
forming a first semiconductor layer on a substrate;
forming an active layer on the first semiconductor layer;
forming a second semiconductor layer on the active layer;
removing the substrate;
forming uneven patterns in the first semiconductor layer; and
forming a first electrode on the first semiconductor layer, and forming a second

electrode on the second semiconductor layer.

[11] The method according to claim 10, wherein the first semiconductor layer is an n-type semiconductor layer, and the second semiconductor layer is a p-type semiconductor layer.

[12] The method according to claim 10, wherein the uneven patterns of the first semiconductor layer are formed at regular intervals.

[13] The method according to claim 10, wherein the uneven patterns of the first semiconductor layer are formed at different intervals.

[14] The method according to claim 10, wherein at least the first electrode is formed over the entire surface of the first semiconductor layer, or at least the second electrode is formed over the entire surface of the second semiconductor layer.

[15] The method according to claim 10, wherein the removing of the substrate comprises separating and removing the substrate using a laser lift-off method.

[16] The method according to claim 15, wherein the laser lift-off method uses an eximer laser.

[17] The method according to claim 10, wherein the forming of the uneven patterns in the first semiconductor layer comprises:
forming a photoresist layer on the first semiconductor layer and patterning the photoresist layer;
performing etching on the patterned photoresist layer to form uneven patterns in the first semiconductor layer; and
removing the photoresist layer.

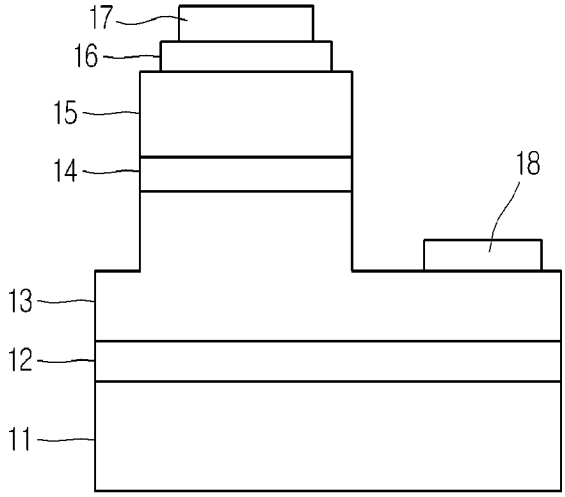
[18] The method according to claim 10, further comprising, before the forming of the first semiconductor layer on the substrate, forming a buffer layer on the substrate.

[19] The method according to claim 18, further comprising, after the removing of the substrate, removing the buffer layer to expose the first semiconductor layer.

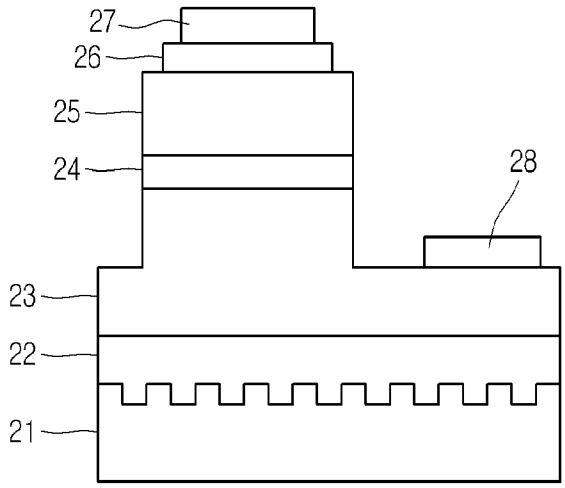
[20] The method according to claim 19, wherein the removing of the buffer layer comprises removing the buffer layer using one of chemical mechanical polishing and etching.

[21] The method according to claim 18, further comprising, after the removing of the substrate, etching the buffer layer and the first semiconductor layer to form uneven patterns in the first semiconductor layer, wherein the buffer layer is formed on a convex portion of the uneven patterns of the first semiconductor layer.

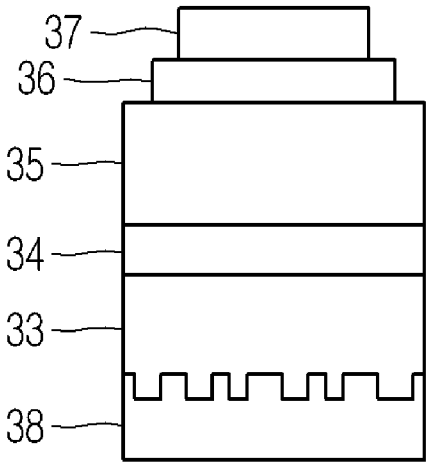
[Fig. 1]



[Fig. 2]



[Fig. 3]



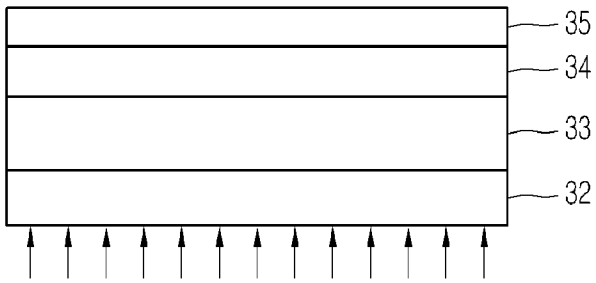
[Fig. 4]



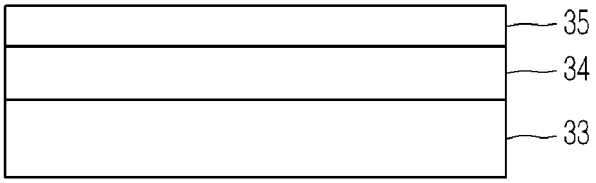
[Fig. 5]



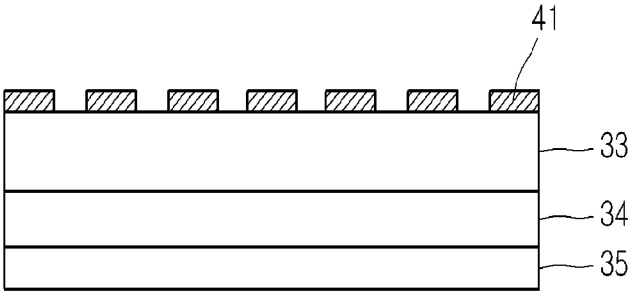
[Fig. 6]



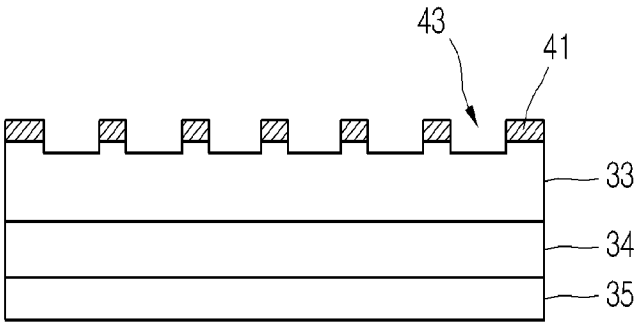
[Fig. 7]



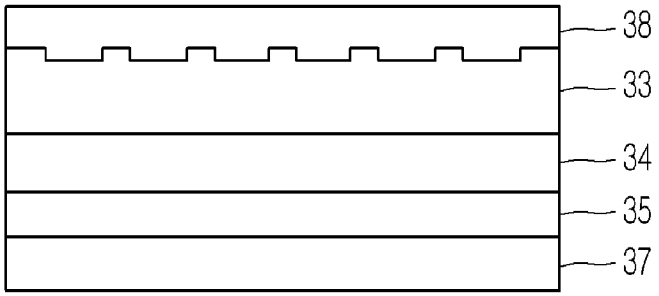
[Fig. 8]



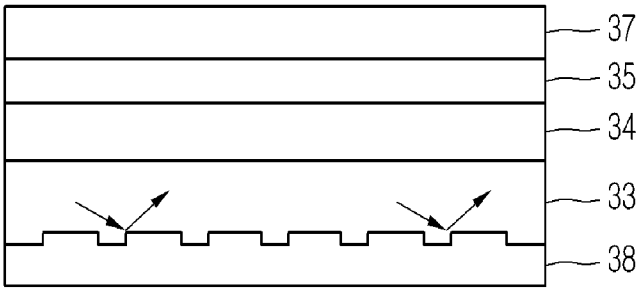
[Fig. 9]



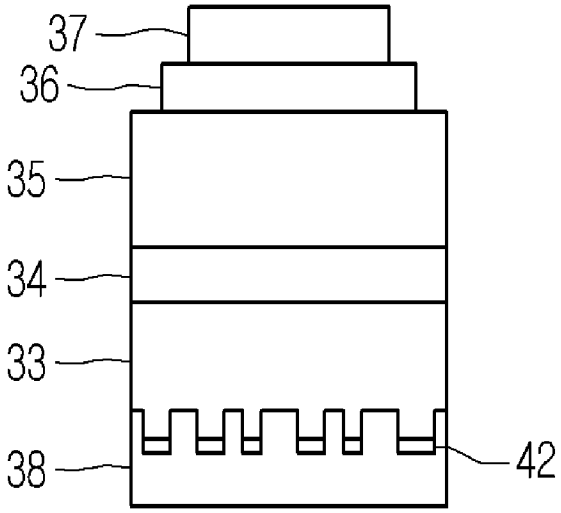
[Fig. 10]



[Fig. 11]



[Fig. 12]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/002916

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 8 H01L 33/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975.
Utility models and applications for Utility models since 1975.
Japanese Utility Models and applications for inventions since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)
eKIPASS(KIPO internal) "LED, light emitting", "uneven, rough, protrude, wave"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US2005082546A1 (JEONGWOOK LEE et al) 21 APRIL 2005 See Abstract, Figure 3A-3C, [35]-[39] of specification	1-6, 9 10-21
Y A	US 6825056 B2 (KOJI ASAKAWA et al) 30 NOVEMBER .2004 See Figure 1, column 6 line 25-column 7 line 22	1-6, 9 10-21
Y A	JP1999-274568A(HEWLETT PACKARD CO) 08 OCTOBER 1999 See Figure 1, [11]-[31] of specification	6 1-21
A	JP2000-196152A (TOSHIBA CORP) 14 JULY 2000 See Figure 6, 8-9, claim 1	1-21
A	US2003/222263 A1 (HONG K.CHOI) 04 DECEMBER 2003 See Abstract, Figure 2, [23]-[27] of specification	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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20 NOVEMBER 2006 (20.11.2006)	**21 NOVEMBER 2006 (21.11.2006)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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