United States Patent [19]

Colucci et al.

[11] **3,805,246**

[45] **Apr. 16, 1974**

[54] **CODED ACCESS DEVICE**

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[22] Filed: **May 8, 1972**

[21] Appl. No.: **250,970**

[52] **U.S. Cl.** **340/172.5,** 340/149, 340/164, 317/134, 235/61.7

[51] **Int. Cl.** **G05b 1/00,** H04g 3/02

[58] **Field of Search** ..... 340/172.5, 149 A, 164, 340/164 A, 164 B, 174 SD, 274, 276; 328/190–191, 48; 317/134; 235/61.7

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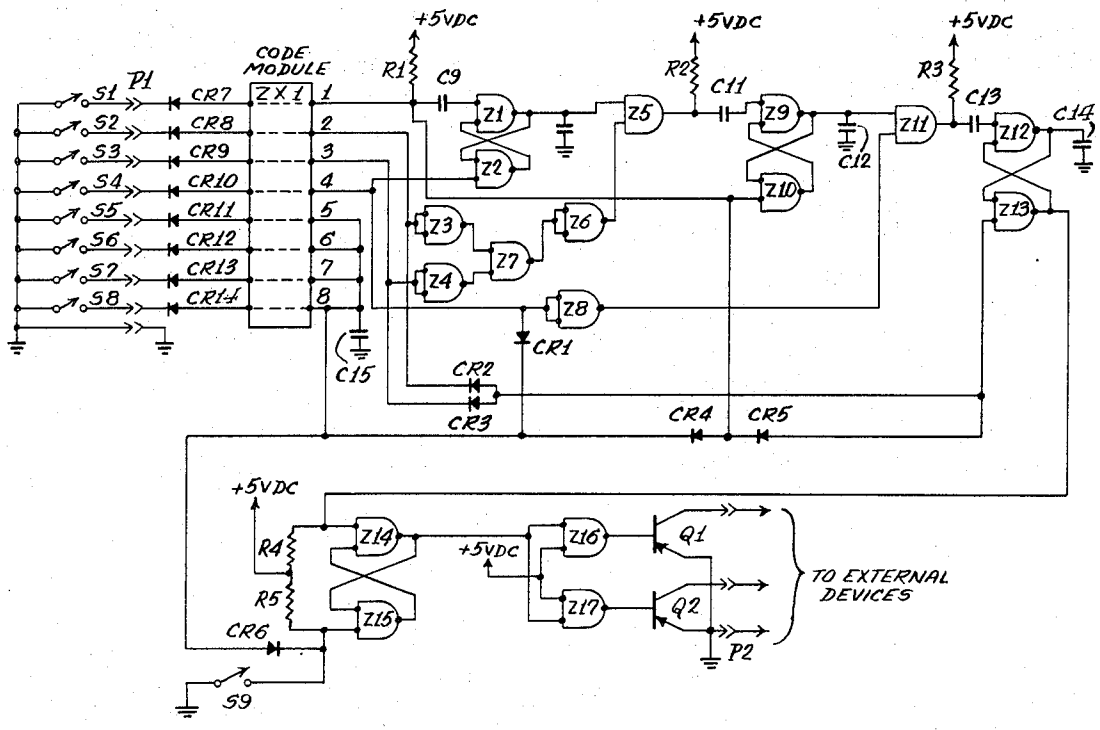
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Attorney, Agent, or Firm—Gary, Juettner, Pigott & Cullinan

[57] **ABSTRACT**

An electrical lock mechanism includes a series of sequentially connected memory storage elements, such as flip-flops, terminating in one or more electrical and/or electromechanical devices that control an external function. Entries into the circuit are made from a plurality of remote switches or switching devices connected to interlocks or logic elements, such as nand gates, that are connected between adjacent memory storage elements. Entry to the circuit through the interlocks in a single predetermined sequence allows for the setting of successive memory elements; the memory elements serve to nullify any progress through the sequence if an incorrect entry is made. An exchangeable code module between the switches and the circuit allows for the changing of switch combinations. The predetermined code may require the correct selection of single switches in a particular sequence, as well as simultaneous entries from a plurality of switches. Several circuits may be connected in series, such that a plurality of individuals having knowledge of their respective portion of the sequence are required to effect the proper combinations. A simple circuit allows for about 50,000 possible combinations, and several million possible combinations may be easily attained.

11 Claims, 8 Drawing Figures



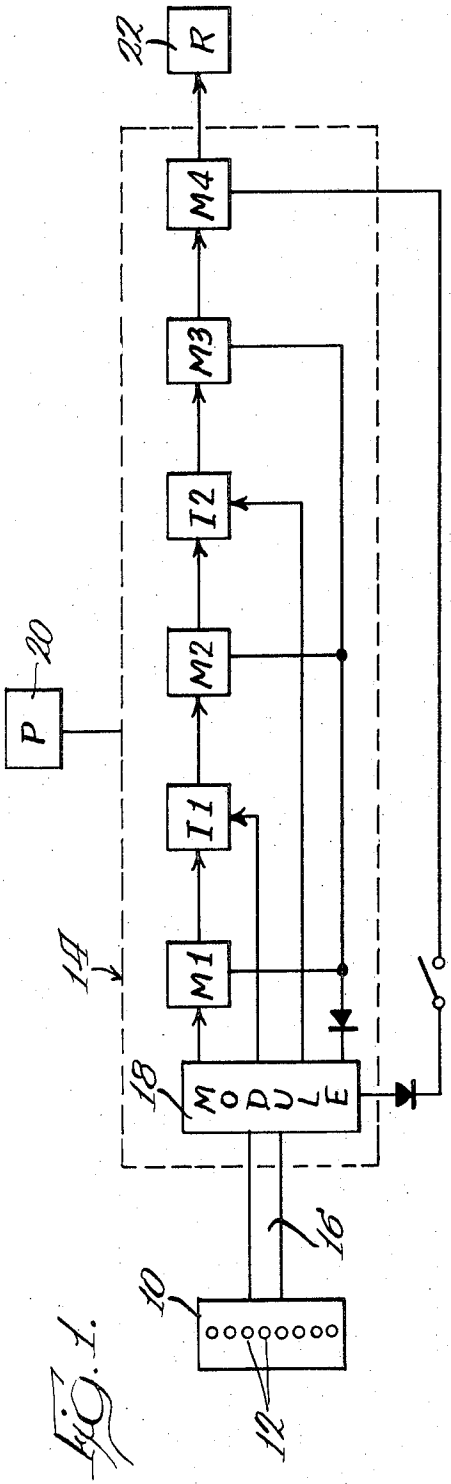


FIG. 1.

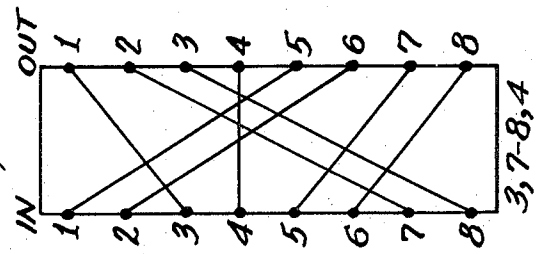


FIG. 5.

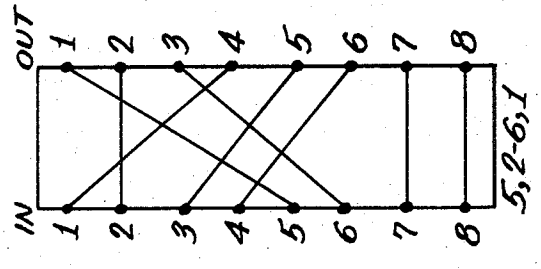


FIG. 4.

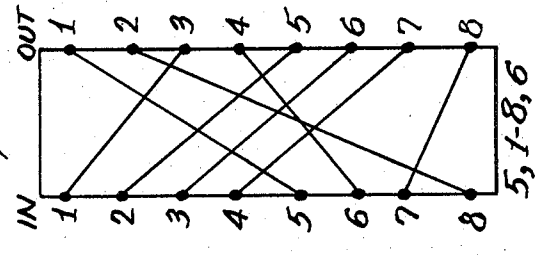


FIG. 3.

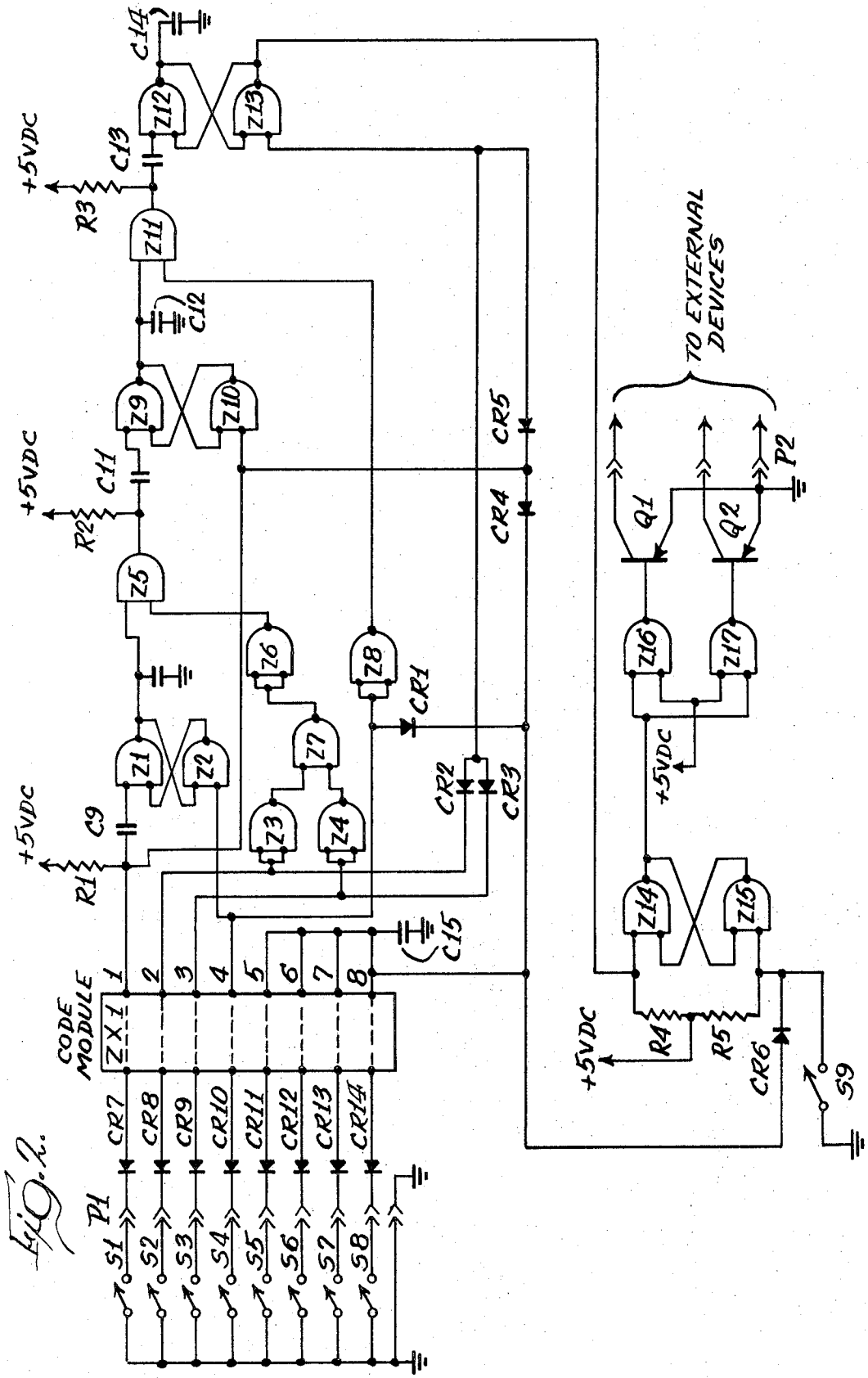

+5VDC
R1
C9
R2
C11
R3
C13
C14
C12
C15
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
Z11
Z12
Z13
Z14
Z15
Z16
Z17
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
CODE MODULE
ZX1
1
2
3
4
5
6
7
8
P1
S1
S2
S3
S4
S5
S6
S7
S8
S9
R4
R5
Q1
Q2
P2
TO EXTERNAL DEVICES

Fig. 2.

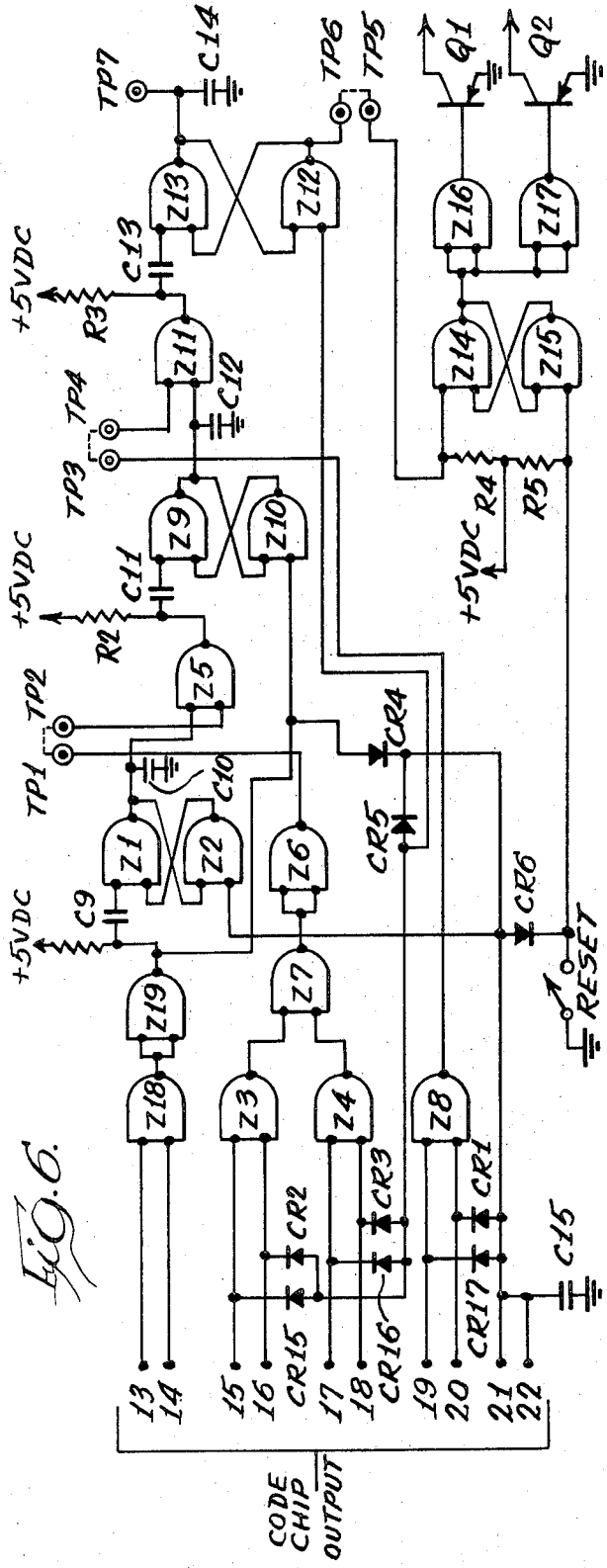


FIG. 6.

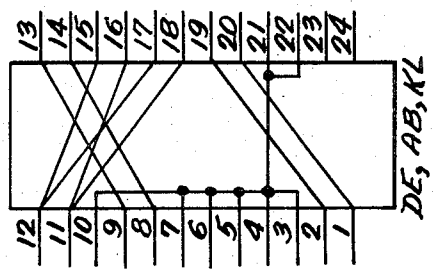


FIG. 8.

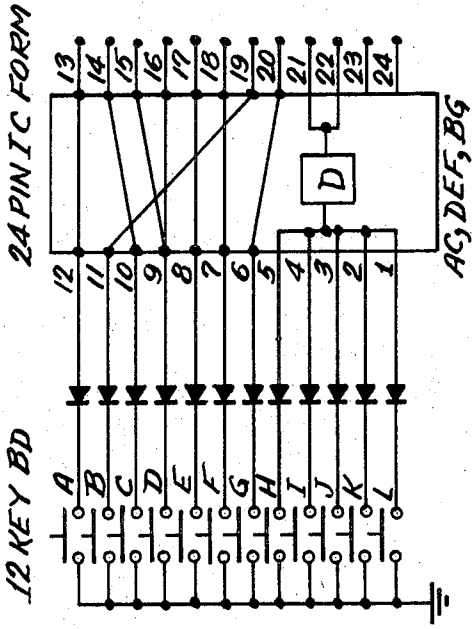


FIG. 7.

CODED ACCESS DEVICE

BACKGROUND OF THE INVENTION

This invention relates to coded access devices and more particularly to a maximum security electrical lock mechanism having a large number and variation of possible combinations.

The security or lock mechanisms available today range from the simple to the complex. The simple devices tend to be unreliable and easily tampered with or bypassed, whereas the more complex devices may be extremely bulky and expensive. Most coded access devices have a limited number of combinations, and the combinations may be difficult to change.

An example of a coded actuating device is a mechanical combination lock, which requires the rotation of a dial to a plurality of correct positions in a predetermined sequence in order to actuate a latch or bolt mechanism. The mechanical arrangement employed is highly complex, especially in locks having a large number of possible combinations. An additional drawback is the known ability to determine the proper combination by surreptitious means.

Another example of a coded actuating device is a plurality of electrical switches that must be actuated in a particular sequence to operate a latch or similar mechanism. Many electrical devices, however, may be subjected to tampering at the switches with electrical probes, and others allow access to the circuit, which may be shorted or bypassed upon examination.

The patent to Tellerman, U.S. Pat. No. 3,242,388, illustrates one type of coded actuating device having charge transfer capacitors that are arranged to prevent actuation if an improper entry is made. This and other similar devices, however, do not have variable code combinations, the number of possible switches is limited, and the switches carry current and therefore require armor or other protection, all of which features are undesirable in a device of this nature.

SUMMARY OF THE INVENTION

The present invention overcomes the problems stated above and provides an improved coded access device, which allows the use of an integrated logic circuit in an extremely compact arrangement. The circuit generally comprises a connected sequence of memory elements having logic or interlock elements connected between adjacent memory elements. In order to transmit a pulse through the circuit and thereby actuate an electrical or electromechanical device, entries must be made in a predetermined sequence from one or more switches through successive logic devices, which in turn set a successive memory element. An improper entry causes all memory devices to be reset, and provision is made to deter unauthorized tampering with the circuit as well as discovery of the circuit code combination through the switches. The combination or code of the device may be changed very easily by means of an exchangeable code module located in the circuit. The device has a large number of applications, and the circuit cannot be bypassed, shorted or easily damaged if properly installed. Unlike prior art devices, the switches do not carry current but instead supply information by which the circuit is activated.

The Drawings

FIG. **1** is a diagram of the components of the coded actuating device of the present invention;

FIG. **2** is a schematic view of the complete circuit of the present invention;

FIGS. **3, 4** and **5** are schematic views of various code modules that may be employed in the circuit shown in FIG. **2**;

FIG. **6** is a schematic view of the circuit of another embodiment of the present invention; and

FIGS. **7** and **8** are schematic views of code modules that may be employed in the circuit shown in FIG. **6**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to FIG. **1**, the coded actuating device generally comprises some type of a switching device such as a switch box **10** having a plurality of normally open switch buttons **12** located in any convenient fashion thereon so as to be easily accessible. The switch box **10** is preferably located in a spaced relationship from the circuit, generally indicated at **14**, and is connected thereto by an electrical cable **16** containing a plurality of separate wires. Any number of switch buttons **12** may be provided in the box **10**, but the preferred number is between four to **12** in the specific arrangement shown.

One side of each of the switches is connected to a separate wire in the cable **16**, with the other side of the switches being connected to ground. The other end of the cable terminates inside the circuit **14** and is connected to a code module **18**. It will be understood that several of the switches **12** may serve as dummy switches and therefore are connected only to the reset circuit. In this manner, the number of possible sequential combinations of switches is greatly increased without incorporating corresponding complications into the circuit.

The code module **18** is removable and serves to intermingle the lines between the switch box and the main circuit, such that the order of the lines leaving the module is different from the order or identity of the incoming lines. In general, the module **18** may comprise any mating electrical connection, but as shown, comprises a plurality of terminals connected to the wires in the cable **16**. A second group of terminals are provided in a spaced relationship from the first group and are connected either to a secondary reset circuit or to an operational line of the main circuit. Examples of such modules are shown in FIGS. **3, 4** and **5**, and it will be recognized that the opposing groups of lugs may be electrically connected in an extremely large number of combinations, such that the correct or predetermined access code may be conveniently and easily changed on the switch box without disrupting the wiring in the circuit.

The main circuit **14** and the contained module **18** are preferably located in a secure area, or the area to which access is only gained by knowledge of the correct code, while the switch box **10** is located outside of the secure area. This feature effectively prevents access to the circuit or code module by unauthorized persons. As will be hereafter more fully explained, no information concerning the circuit or code module may be gained by tampering with the switches **12** or cable **16**, since the switches do not carry current, and since the primary

key to the circuit is determined by the code module and by the circuit itself.

The components making up the bulk of the circuit are preferably miniaturized integrated circuit logic elements of the type commonly found in computers and powered by any convenient source of DC or rectified current, indicated at **20.** A plurality of memory elements, indicated at **M1, M2, M3** and **M4** in FIG. **1** are connected in sequence with the first element being connected through the code module **18** to one or more of the switches **12.** Each memory element may comprise any combination of known components that may be activated between two different states, which for the purposes of convenience, will be called set and reset states. As will be hereinafter described, the memory elements are preferably in the form of one bit storage circuits or flip-flops capable of storing a single variable and remembering the most recent input state, although other equivalent bistable or resettable devices may be employed, such as latching type relays, read only memories and fluidic logic devices.

The first memory element **M1** is switched to a set state by means of a correct entry from the switch box **10,** which creates a pulse on the set input of the element and makes possible the setting of the next subsequent memory element. Other switches are connected to the reset input of the memory element, thereby canceling progress in the circuit when an incorrect switch is activated, since the resetting of any memory element resets all successive memory elements.

At least one truth type interlock or logic device, such as **I1** and **I2** is located between adjacent pairs of memory devices and may be in the form of a nand gate. The inputs of the interlocks are connected to respective other switches **12** through the module **18.** The interlocks function to combine signals into one DC level and to prevent transmission of a signal pulse between the memory elements or to the next successive memory element unless entries from the switches are made in the predetermined correct sequence, i.e., the sequence by which an information pulse is transmitted first to **I1** and then to **I2,** thereby setting **M2, M3** and **M4.**

The final memory device in the sequence, in this case **M4,** is connected to any desired electrical or electromechanical or mechanical device **22** which is to be activated upon receipt of a pulse through **M4.** Memory element **M4** is directly activated by **M3,** and **M4** serves to activate the external device until being reset.

The simplified circuit shown also includes means for resetting the memory devices in the event that a switch is activated out of sequence or in the event that the switch is not connected to the main circuit. For this purpose, a secondary circuit **15** is provided and extends from the code module **18** to the reset input of each memory device. The switches connected to the set input of a particular memory device or interlock-memory are also connected to the reset inputs of the other memory devices. The extra switches which are not connected to the set input circuit and are not a part of the combination are connected to the reset input of all memory devices. In this manner, activation of any one of the extra switches or any one of the combination switches out of sequence will cause resetting of the memory device, and any progress in the sequence will be totally eliminated. Memory **M4** or all of the memory elements may be connected to normally open grounded switch **17** or the like, which may serve as a manual resetting device to clear the circuit.

From the foregoing, it may be understood that one and only one correct entry can be made to the primary circuit for any step in the sequence; any other entry will reset the entire circuit. The integrity of the sequence is maintained by the interlocks, which require that the next preceding memory element be in a set state before the next following memory can be set.

The operation of the simplified version of the circuit shown in FIG. **1** will now be understood. Memory **M1** is first set by activating the correct switch in the switch box. A second switch is then activated, which if correct, matches the output of **M1** at **I1** and sets **M2.** Activation of the third correct switch matches the input of **I2,** and the output of **I2** sets **M3.** Memory **M3** is then able to latch **M4** in a set state, thereby allowing activation of R. Activation of any incorrect button in any step of the sequence resets the circuit completely, and the person seeking to gain access must start a new sequence.

The circuit of the present invention is shown in detail in FIG. **2.** The logic components of the circuit consist of dual input positive nand gates, **Z1** through **Z17,** the construction of which may take many well known forms. Although the use of nand gates is preferred and will be recited in connection with the present description, it will be obvious that the principles of the present invention are applicable to the utilization of other types of functionally complete logic elements, as well as equivalents such as fluidic devices and other logic or memory devices. The function of the positive nand gates is such that the single output is negative or zero if and only if both of the inputs are positive. All other possible combinations at the inputs will result in a positive output.

The memory elements may take many forms, but in the preferred embodiment, each are composed of a flip-flop, comprising a pair of cross wired nand gates, such as **Z1–Z2, Z9–Z10,** and **Z12–Z13.** The upper input and the output of one of the nand gates is connected in the primary circuit. The output of the second nand gate is cross wired to the upper input of the first nand gate and the output of the first nand gate is cross wired to the upper input of the second nand. The lower input of the second nand is connected to a secondary reset circuit. As is well known, the flip-flops operate between a set and reset state. For example, a negative pulse to the upper input sets the flip-flop **Z1–Z2** and imparts a positive state to the output; a negative pulse to the lower input of **Z2** resets the flip-flop and removes the positive state from the output. In this manner, when a reset signal is received on a flip-flop, the progress in the code sequence up to that component is eliminated, since subsequent set states are dependent upon the next preceding set state.

Each of the flip-flops is supplied with an input pulse, preferably by means of the time constant network indicated by **R1–C9, R2–C11** and **R3–C13,** the resistor being connected to a source of DC current Vcc, which in the present case is +5 volts, and the capacitors being connected in series between the switching device and the set input of the flip-flop. The networks serve to form a pulse of the correct potential and of sufficient width to set the flip-flop when a predetermined switch is activated. For example, the closing of switch **S1** grounds **R1** and removes the positive charge of **C9,**

thereby momentarily driving the upper or set input of Z1 negative for the duration required to set Z1–Z2.

The aforesaid flip-flops are connected sequentially as a portion of the main circuit. The set input of the first or leading flip-flop in the sequence is connected through its time constant network through the code module **18** to one of the switches, which for the sake of convenience, is shown as **S1**, although it may be seen that the code module may be cross-wired to allow connection to any one of the switches.

An interlock or logic device, which in this case consists of nand gates **Z5** and **Z11**, is connected in series between respective adjacent pairs of flip-flops in the primary circuit. The nand gates **Z5** and **Z11** limit progress through the sequence to a predetermined switch by requiring that matching positive inputs must be present to allow the next successive flip-flop to be set. Also, since the nand gates are responsive to the reset of an adjacent preceding flip-flop, the correct switch or switches must be activated in the correct sequence.

Shaping capacitors **C10, C12** and **C14** are connected in the primary circuit on the output side of the respective flip-flops. These capacitors help to maintain the required square pulse or wave form suitable for the logic components and may be omitted unless the environment of the circuit is liable to be subjected to outside electrical noise.

The external switches, indicated as **S1** through **S8**, are each grounded on one side and are individually connected on the other side through cable **P1** and through individual blocking devices, such as diodes **CR7** through **CR14**, to individual locations on the code module. The diodes are orientated to block current from the switches to the circuit and serve to protect the circuit from electrical tampering or probing. For the sake of simplicity, the code module is shown to be wired directly across between opposite terminals, such that **S1** through **S4** must be activated in sequence. If desired, the diodes **CR7** through **CR14** may be located on the other side of the code module in the circuit.

As mentioned, output **1** of the code module is connected to the set input of flip-flop **Z1–Z2**, and the output of said flip-flop is connected to one input of nand **Z5**. The second entry in the sequence is thus made to the other or lower input of **Z5**. For the second entry, means are provided to require the activation of two switches simultaneously before **Z5** is activated. For this purpose, module outputs **2** and **3** are connected together and to all of the inputs of respective nands **Z3** and **Z4**, and the outputs of **Z3** and **Z4** are connected to the respective inputs of a single nand **Z7**. The output of **Z7** is connected to both inputs of nand **Z6**, with its output connected to **Z5**. As described, the combination of **Z3–Z4** and **Z7** require that switches **S2** and **S3** be closed concurrently. Nand **Z6** serves as a signal inverter to match the **Z1–Z2** positive output. The matching positive entries to **Z5** ground time constant network **R2, C11**, thereby setting flip-flop **Z9–Z10**.

The final entry is made from code module output **4**, which is connected to nand **Z11** through the signal inverting nand **Z8**. The output of **Z11** grounds the time constant network **R3, C13**, thereby setting flip-flop **Z12–Z13**. The output of the flip-flop **Z12–Z13** is connected to the set input of flip-flop **Z14–Z15**, and the set output of said flip-flop is connected in parallel to respective inputs of two or more nands, such as **Z16** and **Z17**, which drive the base of respective switching transistors **Q1** and **Q2** connected to external devices. The inputs of **Z14–Z15** are stabilized by resistors **R4** and **R5**.

Means are provided to reset all but the final ones of the flip-flops in the sequence in the event that an incorrect entry is made from any of code module outputs **1** through **8** or in the event that the sequence of entries does not match the code. In the case of the outputs connected to the main circuit, a pulse through any of the first three outputs resets all out of sequence memory devices, and a pulse through the fourth or final output resets the first memory device.

In the embodiment shown, the remaining code module outputs **5** through **8** are connected to the reset circuit only, which comprises a discharge capacitor **C15** and a reset circuit comprising lines that lead to the reset inputs of all of the flip-flops in the unit except **Z14–Z15** and **Z16–Z17**. In addition, a manually operated grounded switch **S9** may be connected in the reset circuit to allow complete resetting of all memory elements at any time through **CR6**. It will be noted that all reset functions are connected to a common reset circuit comprised of **CR1**, through **CR6**, which serves as steering diodes to insure that the reset function of the various switches does not disrupt the sequence of the circuit. Thus, the first entry from the code module resets the second and third memory elements, the second entry resets only the third memory element, and the third entry resets the first element.

The function of the circuit will now be described in connection with the correct combination, which is in this case, the sequence of switches **1, 2–3**, and **4**. Depression of **S1** causes a pulse across the network of **R1, C9**, and drives the input of **Z1** negative momentarily, thereby setting flip-flop **Z1–Z2** and putting a positive voltage on the upper input of **Z5**. The output of **R1, C9** is also used as a reset signal to **Z9–Z10** flip-flop and through **CR5** to flip-flop **Z12–Z13** to insure that **S1** is the first switch used in the code entrance sequence.

Switches **S2** and **S3** are then depressed concurrently driving both inputs **Z3** and **Z4** to ground and thereby driving the inputs of **Z7** positive. The negative output of **Z7** is inverted by **Z6** to match the positive upper input of **Z5**. The output of **Z5** drives **R2, C11** network negative, thereby setting flip-flop **Z9–Z10** and imparting a plus voltage to **Z11**. Depression of **S2** and **S3** also resets flip-flop **Z12–Z13**.

The final entry is made by depressing **S4**, which through **Z8**, matches the other entry at **Z11**. The output of **Z11** drives the **R3, C13** network negative, thereby setting flip-flop **Z12–Z13**. Depression of **S4** also resets **Z1–Z2**.

The setting of flip-flop **Z12–Z13** also sets flip-flop **Z14–Z15**, which serves as a holding latch and operates through nands **Z16** and **Z17** to control the desired external function. The resistors **R4** and **R5** are stabilizing resistors on **Z14–Z15** to increase the signal to noise ratio.

FIGS. **3, 4** and **5** illustrate examples of code modules that may be employed in the circuit shown in FIG. **2**. As indicated, the correct code of the FIG. **3** module is **5, 1–8** and **6** in sequence, and the other combinations are as indicated in the Figures. In general, it may be seen that any combination of variables in the form *w, x–y, z* may be employed, merely by providing exchangeable code modules having the desired wiring be-

tween the input side and the output side of the code module.

FIG. 6 illustrates a modified and more versatile version of the circuit shown in FIG. 2 and includes means for increasing the possible number and type of combinations, as well as means for interconnecting a plurality of separate circuits. Except for the additions mentioned below, the FIG. 6 circuit is substantially identical to the FIG. 2 circuit and the identical portions will not be described in detail.

It will be seen that the circuit has been modified and expanded by making more inputs available at the entry side of the circuit and by adding logic elements prior to the first memory device. Since eight main circuit-connected module outputs are available, the switch box (FIG. 7) contains eight or more switches, with twelve switches being shown; four of the switches are therefore solely reset switches and are connected only to the reset circuit. The code module (FIG. 7) contains twelve in-line pairs of terminals with eight circuit outputs and four reset outputs.

In order to enable the first entry in the sequence to be variable between one or two switches, a pair of series connected nand gates Z18 and Z19 are connected to the input side of the first memory device or flip-flop Z1–Z2. The inputs of the first nand Z18 are connected to respective code module output terminals 13 and 14, and the output is connected to both inputs of Z19. The output of nand Z19 is, in turn, connected to the R1, C9 network and to the first flip-flop Z1–Z2. In this manner, the code module may be programmed to effect the first step of the sequence with either one or two concurrent switch operations. Terminals 13 and 14 may be connected to allow a single switch activation, or these terminals may be connected to two respective switches.

The same principle is also be employed with the inputs of nands Z3 and Z4. Instead of connecting the dual inputs of these nands together, the four inputs may be connected to four separate module outputs 15 through 18. This allows the choice of a one switch entry, as well as two, three and four concurrent switch entries. The inputs of the third entry nand Z8 are also connected to separate terminals 19 and 20, thereby allowing a veriable of one or two switches as the third step in the sequence. Diodes CR15, CR16 and CR17 are connected between the newly established module outputs 15, 17 and 19 and the reset circuit to insure full resetting capabilities.

From the foregoing, it will be understood that additional nand gates may be added at any of the entry points to the circuit. Also, additional memory devices may be added to the main circuit to extend the length of the sequence indefinitely. In the circuit shown in FIG. 6, two switch combinations are available for the first sequence, four for the second, and two for the third. FIG. 7 illustrates a 2–3–2 code in the form AC, DEF, BG, and FIG. 7 illustrates a 2–2–2 code in the form DE, AB, KL. The present invention therefore provides for any variable sequence of unlimited length, as well as any number of variable concurrent entries in any step of the sequence. The number of possible combinations in a single circuit are therefore virtually unlimited and may range from about 50,000 to several million or more.

The invention is also adaptable to the inclusion of a time delay mechanism, which penalizes the user by imposing a time limit within which the correct sequence must be entered after an incorrect entry is made. The time delay device, for example, may be incorporated into or connected to the reset only inputs of the code module, such as the device D shown in the module of FIG. 7.

The circuit of FIG. 6 also includes means for placing several coded circuits in combination, thereby allowing additional combinations, but more importantly, imposing a requirement that several individuals must cooperate to complete the code through the sequence. For this purpose, tie points, such as TP1 through TP7 may be provided in the circuit. The leads to the lower inputs of nands Z5 and Z11 are broken and terminate in TP1–TP2 and TP3–TP4, respectively. A tie point TP-7 is provided at the upper output of flip-flop Z13–Z14, and the line from said flip-flop is broken at TP5–TP6.

If only a single circuit is employed, TP1–TP2, TP3–TP4 and TP5–TP6 are shorted, and the circuit functions are hereinbefore described. If two circuits are connected in series, TP–7 from the circuit shown, may, for example, be connected to TP2 for a second circuit, with the other tie points in both circuits, except TP1–TP2 in the second circuit, being connected. Thus, each individual must insert the proper code into the combined circuits in the proper sequence. Such arrangements are especially useful under circumstances where the authority of more than one individual is required before a given function may be performed.

The invention described herein is extremely versatile and has a wide variety of applications. Typical applications include protection of access to an automobile, access to a computer or a computer program, access to or performing acts relating to functions or operations where a high degree of security is required, as well as any other applications where a lock mechanism or the actuation of any other security mechanism is required. The device may be constructed in an extremely compact form from inexpensive and presently available computer chips, power requirements are minimal, and the circuit is highly reliable.

As one example of the invention, the coded access device may be employed in an automobile, with the switch box being located in the passenger area, such as on the dashboard, and the circuit and code module being located under the hood. The output of the circuit could be connected to electromechanical devices which control the distributor and the hood lock.

It will be understood that the switching mechanism need not be located in close proximity to the circuit, and the code may be transmitted to the circuit from one or several remote points by any known means.

An important feature of this invention is that access is gained by the input of information, and the switches do not carry current. No advantage is gained by examining or tampering with the switch box or the line from the switch box to the code module. Whereas the shorting of the inputs of many electrical devices might bypass the coded circuit, the shorting of the external lines or switches of the present invention will cause the circuit to reset.

In view of the foregoing, it will be understood that many modifications and additions may be made to the circuit described herein without departing from the scope of the present invention. For example, it will be obvious that the mechanical switches may be replaced by any type of switching devices, and the switches may

be activated at their location or from any remote point, such as by means of cable, photoelectric cells, or by any other convenient means. The code module may include means for changing the combination automatically or manually, and a time delay mechanism may be included in the circuit to disconnect the circuit in the event that an attempt is made to reen through the possible combinations.

Having thus described the invention, what is claimed is:

1. A coded device for obtaining limited access to a given function comprising a plurality of memory means sequentially connected in a circuit for storing at least one variable having a set and a reset valve, the final one of the sequence of memory means controlling said function, information means for transmitting a plurality of separate elements of information into said circuit in a plurality of sequences including a predetermined code sequence, said information means comprising a plurality of individual switches grounded on one side, certain of said switches being responsive to active portions of said circuit when grounded, and interlock means in said circuit for controlling transmission of signals sequentially between said memory means and being responsive only to a predetermined sequence of information elements to set said memory means in sequence, at least one of said memory means having a reset valve nullifying access to said function upon feed in and out of sequence information elements.

2. The device according to claim **1** wherein said information means comprises a plurality of sources located remote from said circuit, and code means between said sources and said circuit for intermingling information from said sources to said circuit.

3. The device according to claim **2** wherein said code means comprises one of a number of exchangeable modules having different configurations for the intermingling of information.

4. The device of claim **1** wherein each of said memory means comprises a flip-flop and means for electrically setting each flip-flop upon receipt of information in the proper code.

5. The device of claim **4** wherein said interlock means comprises a nand gate between adjacent flip-flops.

6. The device according to claim **1** wherein said information means comprises a plurality of separate sources, and means connected ahead of at least one memory means for requiring concurrent entry of a plurality of said sources in the code sequence.

7. The device according to claim **1** wherein means are provided for combining a plurality of said circuits into one circuit having a plurality of interdependent access codes.

8. The device according to claim **1** wherein time delay means are provided for resetting the circuit upon failure of the correct predetermined code being established within a period of time dependent upon the transmission of an incorrect and out of sequence information element into said circuit.

9. A coded device for obtaining limited access to a given function comprising a series of memory elements each having set and reset inputs and a defined logic output, means for feeding information into said memory elements in a plurality of sequences comprising a plurality of switches grounded on one side and operative to set certain of said memory elements when grounded, and means responsive to one and only one of said sequences for channeling said information into said memory elements sequentially and to activate reset inputs of said memory elements other than those preceding the elements and those elements being set, the set input of at least one of said elements being dependent on the logic output of the next preceding logic element.

10. The device of claim **1** wherein current blocking means are provided between each of said switches and said circuit to prevent flow of current from said switches to said circuit.

11. The device of claim **10** wherein the potential at each of said blocking means is the same.

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