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Wheelwright

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[54] **MUSICAL INSTRUMENT WITH DIGITAL DATA HANDLING SYSTEM AND LIGHTING DISPLAY**

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[52] **U.S. Cl.** **84/464**

[51] **Int. Cl.** **A63j 17/00**

[58] **Field of Search** 84/1.01, 1.18, 464

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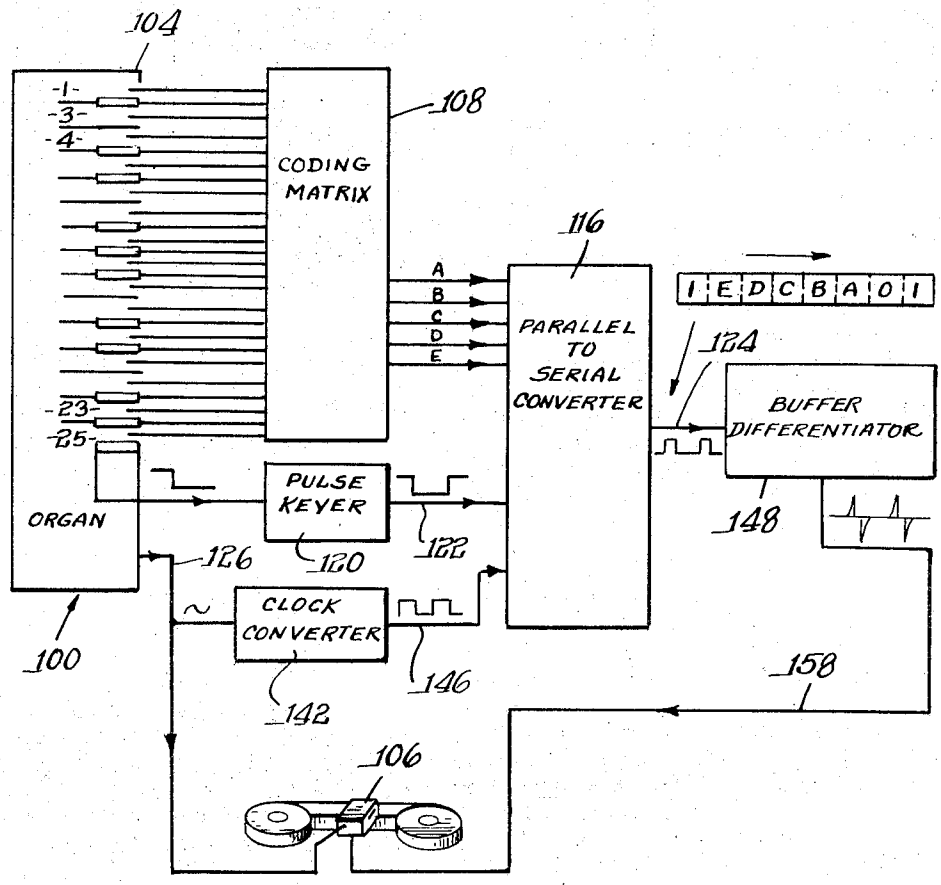
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[57] **ABSTRACT**

A data handling system has an arrangement in which input data may be recorded and/or displayed in analog form while at the same time the data is encoded in digital form on a storage or memory medium, such as magnetic tape. When the memory medium is operated for retrieval of the encoded data, the data is converted to one analog form for display while at the same time the originally recorded analog form may also be displayed, whereby two analog displays result. The system is described as embodied in an electronic organ and may be used as a teaching device wherein a series of electric lamps are mounted respectively above a series of organ keys. A key may be depressed causing the audio to be heard. At the same time audio is recorded along with data in digital coded form representing the key. Upon playback the audio is reproduced to constitute one analog form and the decoding circuitry causes the lamp associated with the key to be illuminated to provide the second analog form.

12 Claims, 12 Drawing Figures

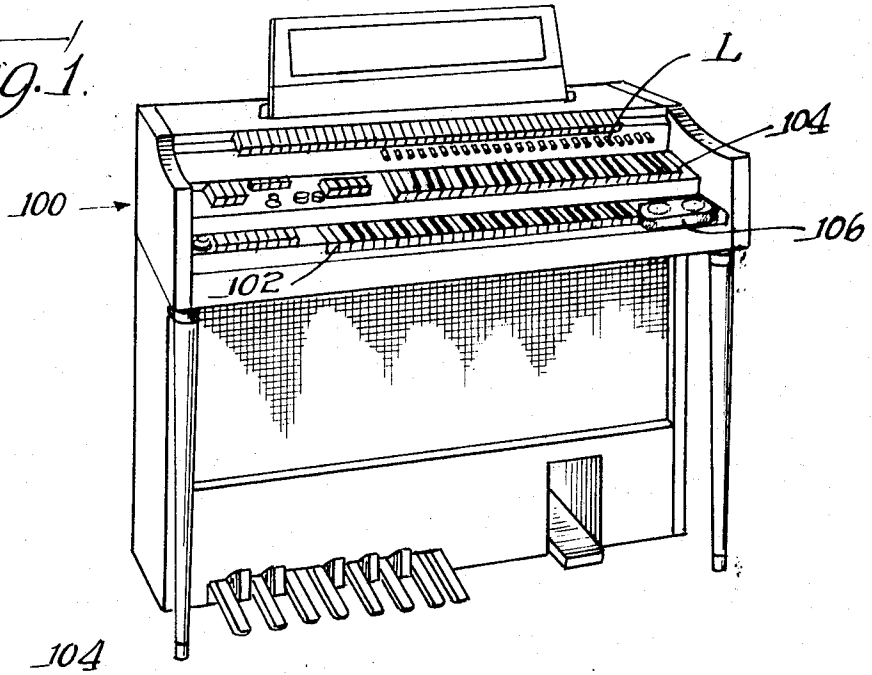


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SHEET 1 OF 9

Fig. 1.



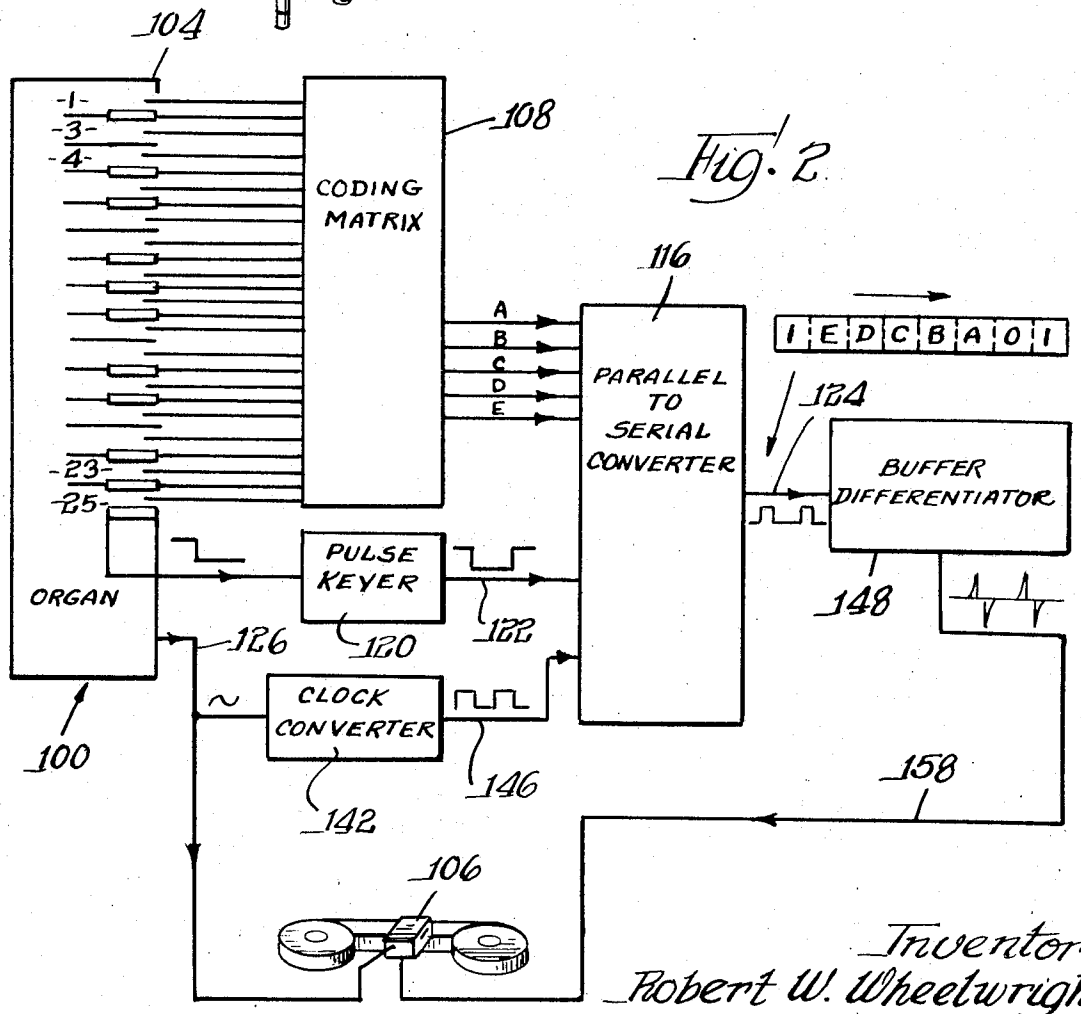


Fig. 2.

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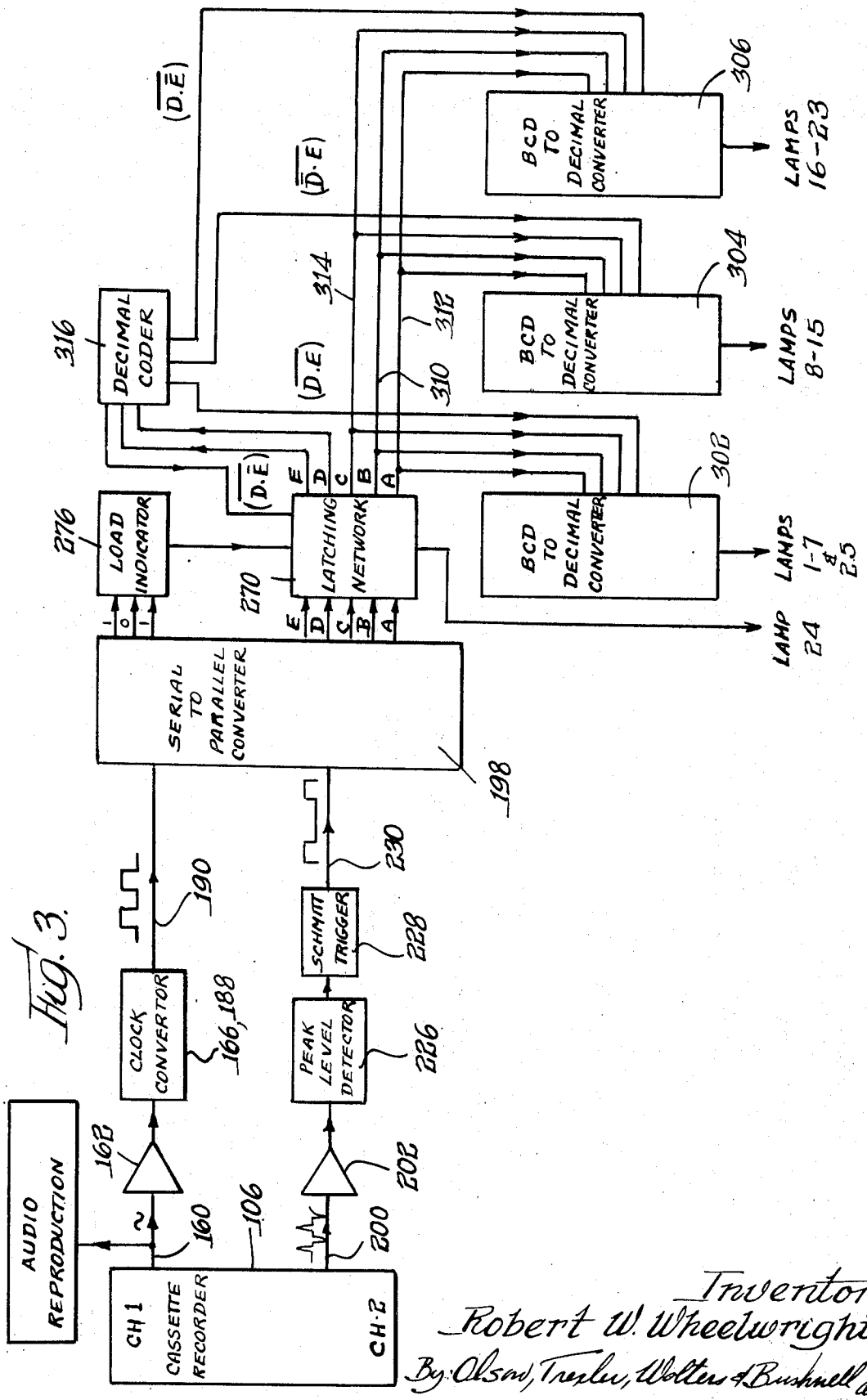


Fig. 3.

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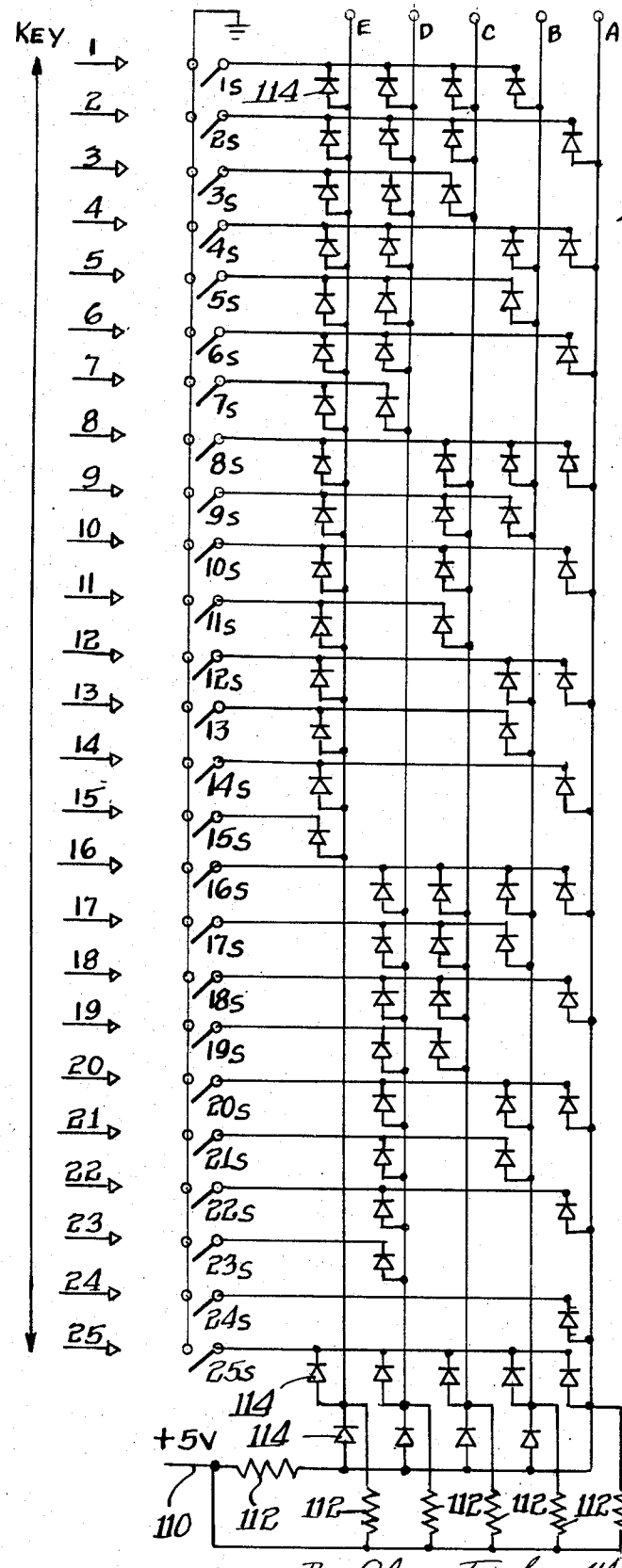


Fig. 4.

Fig. 5.

KEY NO.	E	D	C	B	A
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	0	0	0	0	0

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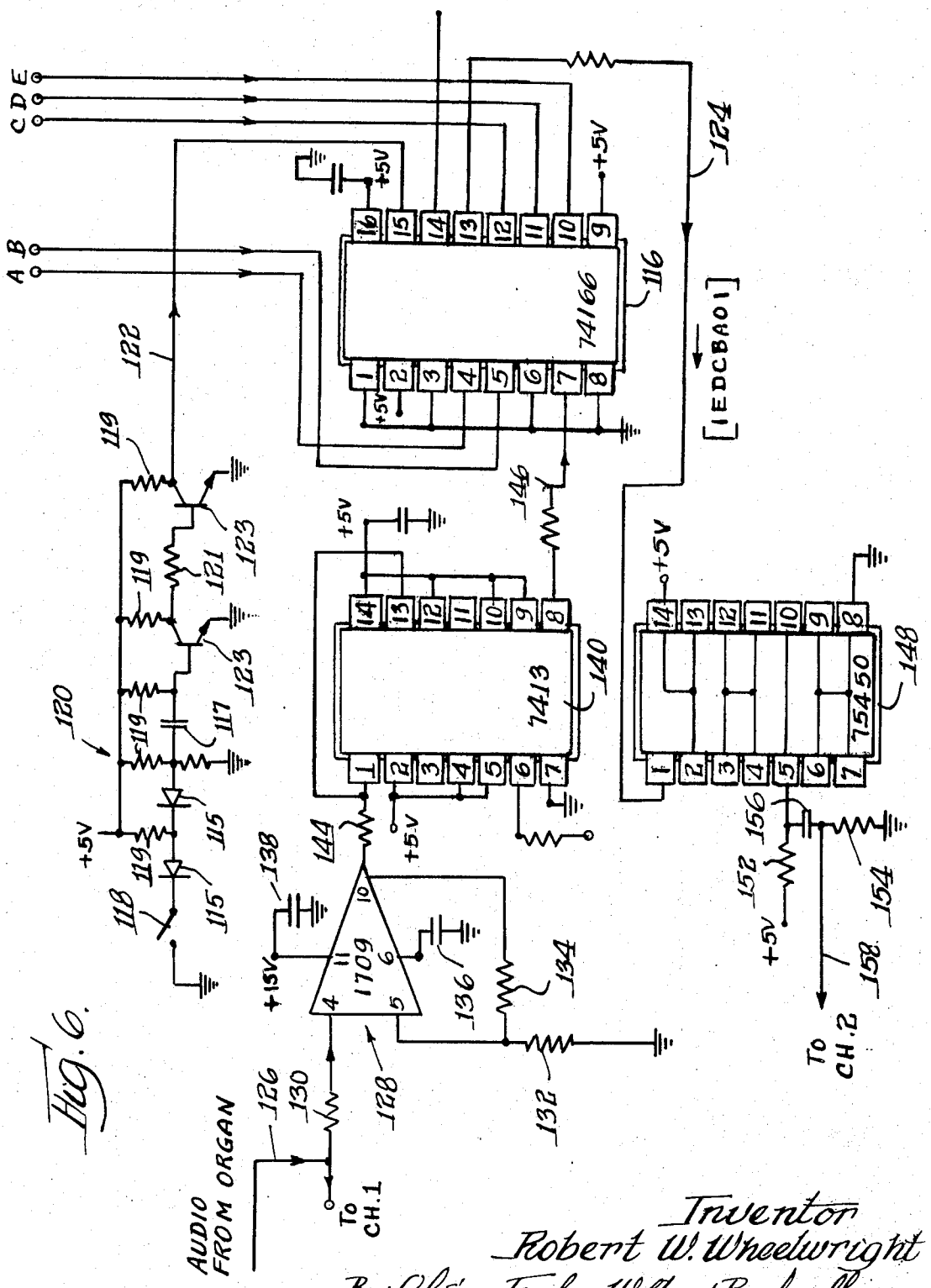


Fig. 6.

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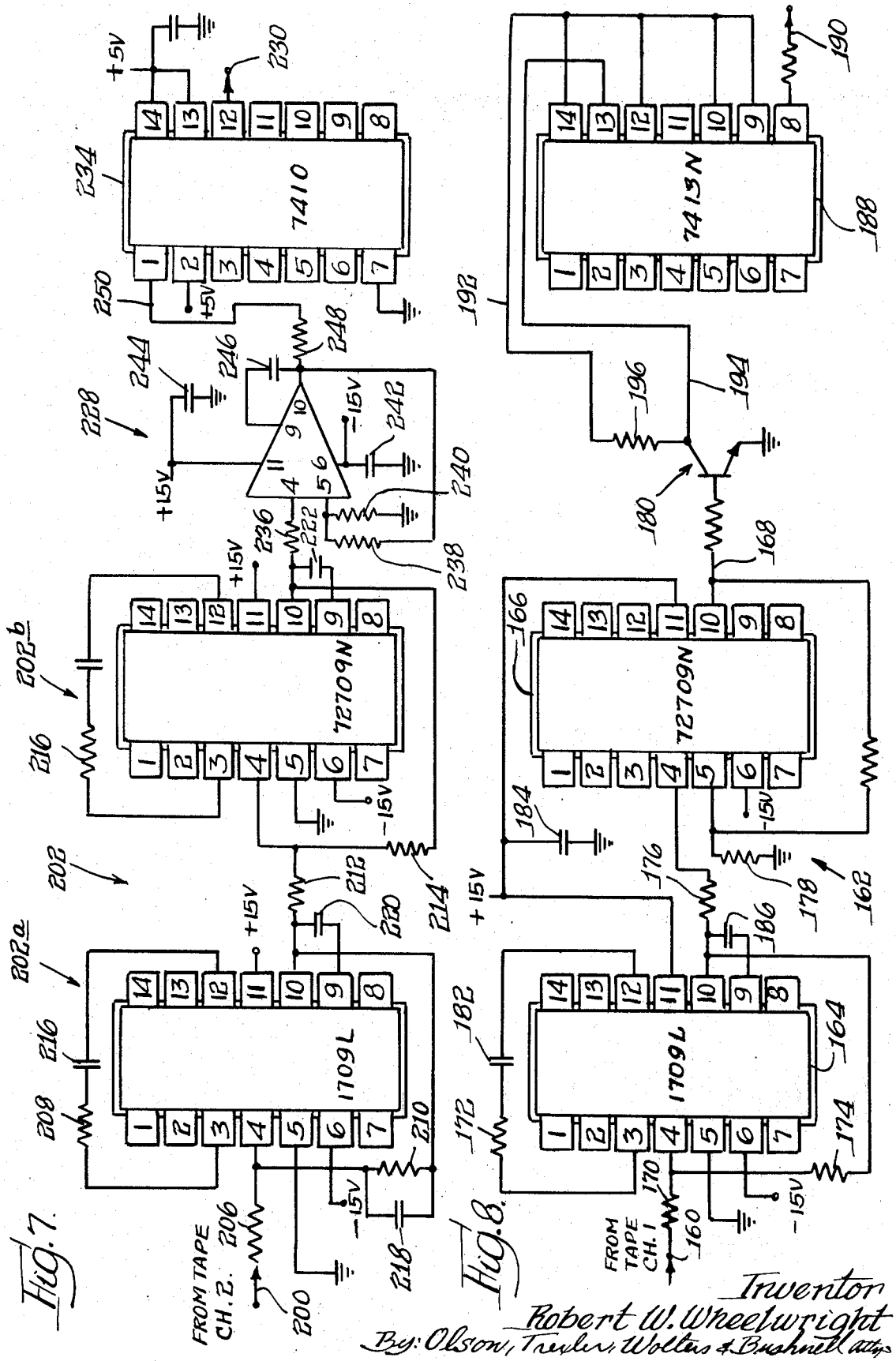


FIG. 7.

FIG. 8.

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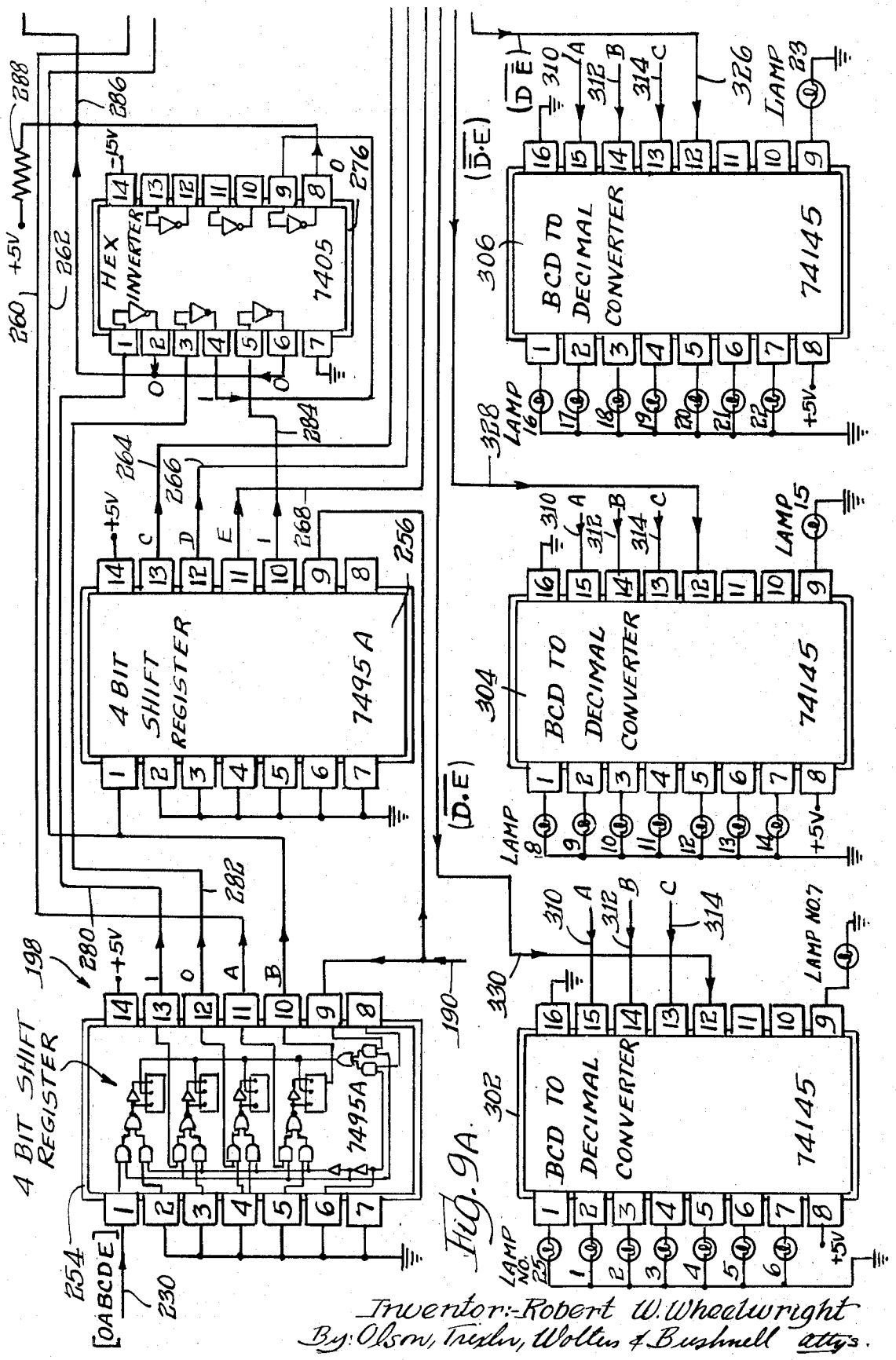


FIG. 9A.

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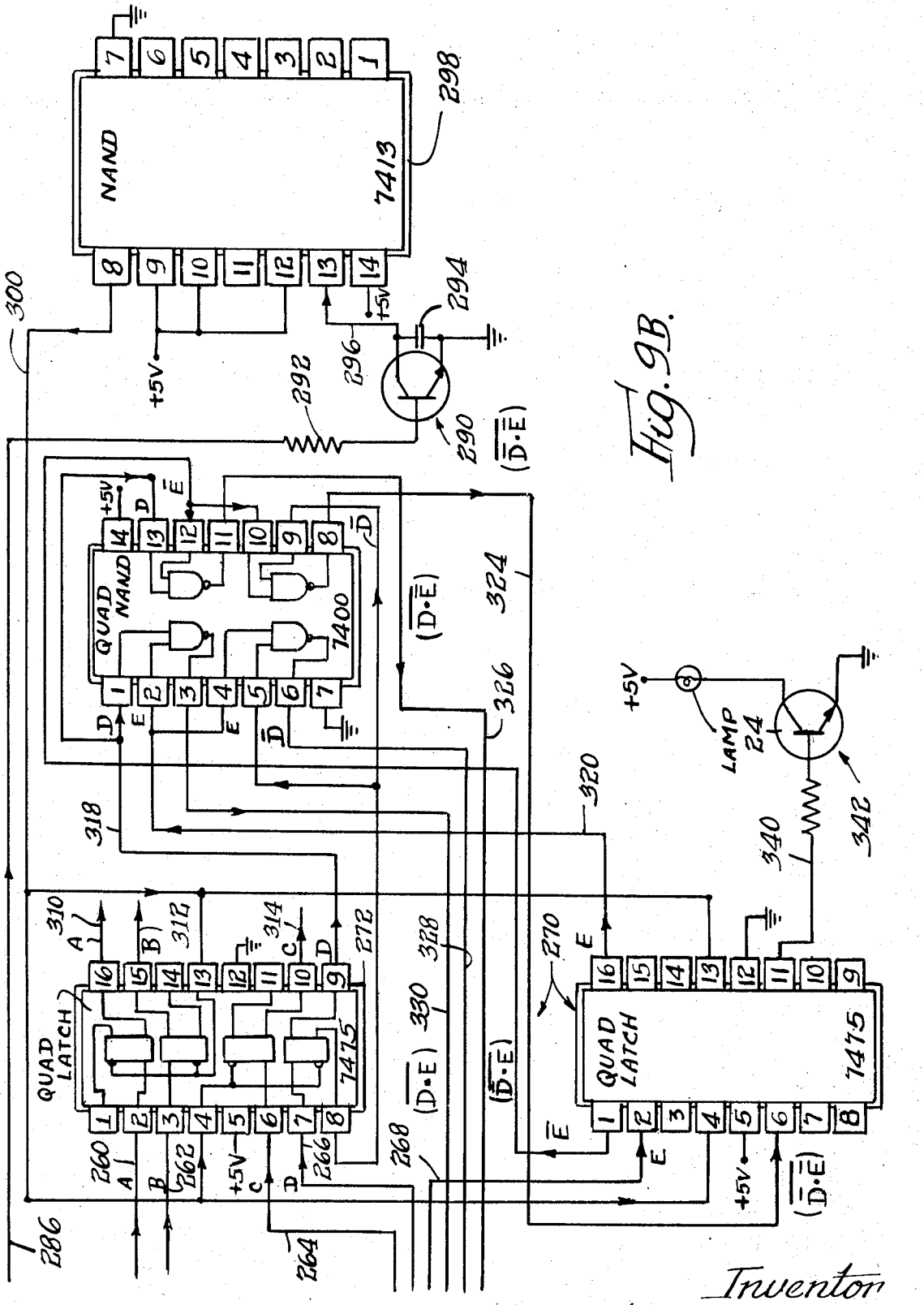


Fig. 9B.

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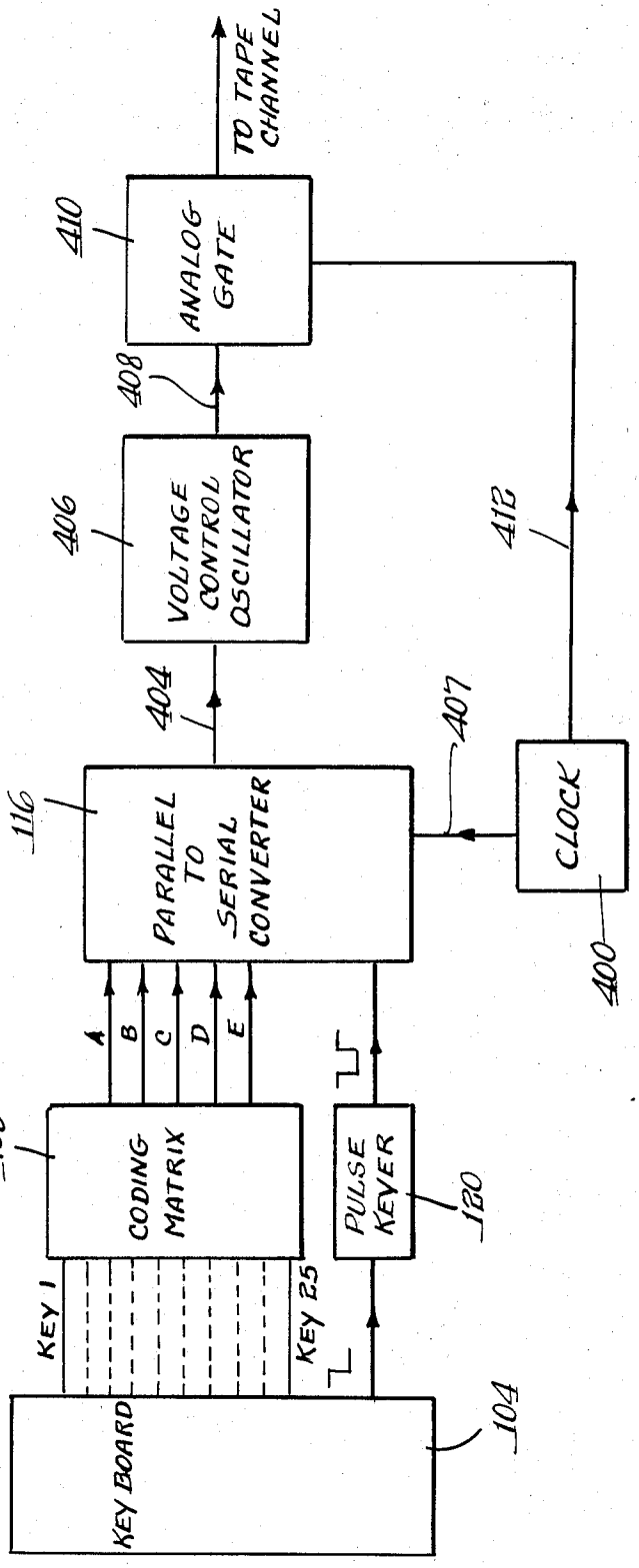


Fig. 10.

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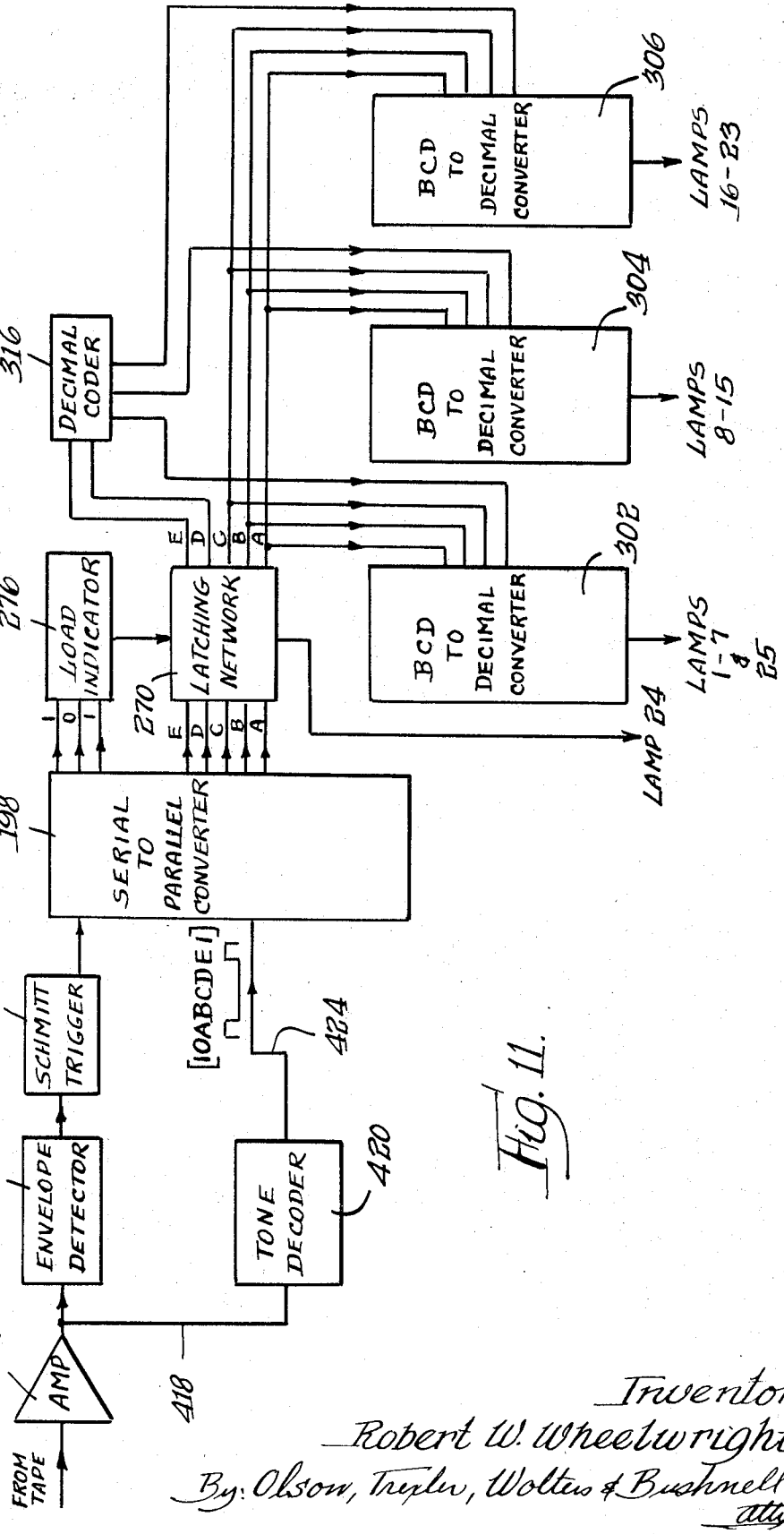


Fig. 11.

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MUSICAL INSTRUMENT WITH DIGITAL DATA HANDLING SYSTEM AND LIGHTING DISPLAY

This invention relates to a data handling system, more particularly to a system that utilizes digital control for the data.

It is an object of this invention to provide a system in which input data may be recorded and/or displayed in analog form while at the same time the data is encoded in digital form on a storage or memory medium. When the memory medium is operated for retrieval of the encoded data, the data may, by suitable circuitry, be converted from digital to analog form for display. At the same time the originally recorded analog form may also be displayed. Thus, the playback or retrieval may be in two analog forms for simultaneous reproduction. The preferred storage medium is a tape cassette.

It is a further object of the present invention to provide a system of the type stated which may be embodied in an audio-visual instruction arrangement for musical instruments, such as electronic organs.

In accordance with one form of the invention a light panel is mounted above a conventional organ keyboard. The panel may, by way of example, contain **25** lamps such that each lamp corresponds to one of **25** consecutive keys. A **25** note coding arrangement, corresponding to the respective keys, is used to record in digital coded form the output of a key while at the same time the audio tone for the key is simultaneously recorded. The coded data for the key and the audio tone are preferably recorded on a tape cassette that is used with a tape player/recorder built into the organ. One channel of the recorder is used to record the audio tone while the other channel is used to record the data that identifies the key. Both channels are used to effect decoding during playback since the channel containing the audio tone is utilized as a clock signal control. Also, when the tape cassette is played back, the audio tone is reproduced in the audio reproduction system of the organ. At the same time the lamp above the key corresponding to the audio tone is illuminated, the operation of the lamp being determined by the output of the decoding circuitry. This arrangement provides an effective audio and visual teaching device. Furthermore, since the signal from which the clock frequency is derived and the data identifying the key are recorded on separate channels of the tape, the playback speed of the cassette is not critical.

In another form of the invention for use in audio-visual organ instruction, a single channel tape cassette may be used. In such an arrangement, the digital code, in binary form, and its associated clock-control signals, are converted to certain audio tones corresponding to binary states 1 and 0. These frequencies are then modulated by a fixed clock frequency so that the composite signal is self-clocking. Thus, in a two channel cassette, one channel would be used for recording the data while the other channel would have unrestricted informational use.

Further objects of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings forming a part thereof.

In the drawings:

FIG. **1** is a perspective view of an organ embodying the present invention;

FIG. **2** is a block diagram of the coding system of the present invention;

FIG. **3** is a block diagram of the decoding system of the present invention;

FIG. **4** is a schematic of the coding matrix which forms part of the present invention;

FIG. **5** is a truth table for the coding matrix of FIG. **4**;

FIG. **6** is a schematic of the coding system of the present invention;

FIGS. **7** and **8** are schematics of the data and clock interface portions, respectively, of the decoding system;

FIGS. **9A** and **9B** taken together constitute a schematic of the logic portion of the decoding system;

FIG. **10** is a coding block diagram of a modified form of the present invention; and

FIG. **11** is a decoding block diagram for use with the coding arrangement of FIG. **10**.

Referring now in more detail to the drawing, and particularly to FIG. **1** thereof, there is shown an organ console **100** having keyboards **102, 104** and a tape recorder and playback unit **106** of a cassette type built into the organ at one end of the keyboard **102.** Above the upper keyboard **104** is a panel containing **25** lamps, collectively identified as L in FIG. **1.** Each lamp corresponds to one of **25** consecutive keys of the keyboard **104.** As will be seen later with reference to FIGS. **9A** and **9B,** these lamps may be illuminated in accordance with the decoding circuitry described herein. In FIG. **4** the keys are shown numbered **1** through **25,** and in FIG. **2** several of the keys are shown with their associated numbers, the remaining numbers being omitted so as not to obscure the figure. As will be seen hereafter, when a particular key is depressed, the audio tone for that key is recorded on one track of the recorder **106** and coded data representing that key will be recorded on another track of the recorder. The audio tone is also used to derive a clock signal in the coding. When the recorder is operated in the playback mode, the audio tone for that key will be reproduced in the sound system of the organ, and at the same time the lamp corresponding to that key, namely the lamp immediately above the key, will be illuminated. The keys may be depressed in any succession to produce a series of audio tones and a corresponding series of lamp illuminations. This will provide both an audio and a visual teaching device.

Referring now to FIGS. **4** and **5,** it will be seen that each key **1** through **25** is adapted to close its associated switch **1***s* through **25***s*, the switches forming part of a binary coding matrix **108.** As shown, the binary coding matrix **108** is powered from a suitable power supply at **110** through resistors **112** and to a number of diodes **114** that are interconnected with each other and with terminals of the respective switches **1***s*, **2***s*, **3***s*, etc., as is clearly shown in FIG. **4.** The output lines of the decoding matrix are identified as A, B, C, D and E, thereby to provide a five bit binary coded output from the coding matrix **108** each time one of the keys is depressed. The truth table of FIG. **5** shows the binary states of the outputs A, B, C, D, E for each key. These outputs A, B, C, D, E are also shown in FIGS. **2** and **6** and constitute input lines for transmitting data to a parallel-to-serial converter **116,** which is a synchronous, parallel-load, eight-bit shift register.

Each of the keys 1 through 25 is also operatively connected to a switch 118 shown in FIG. 6. Switch 118 forms a part of a pulse keyer 120, the circuit for which is shown in FIG. 6 and consists of diodes 115, 115, capacitor 117, resistors 119, 121 and resistance-coupled transistors 123, 123. Closing switch 118 causes a pulse to issue on conductor 122. This pulse keyer circuit 120 provides a control pulse for loading the binary code from the outputs A, B, C, D, E into the parallel-to-serial converter 116. Thus, the output from the pulse keyer 120 over conductor 122 is to the shift/load or gate input (terminal no. 15) of the converter 116.

The converter 116 is packaged as a standard type 74166 integrated circuit. A circuit of this type is commercially available and is, therefore, not described in detail. Furthermore, the standard type 74166 and the other integrated circuits hereinafter described are also identified by circuit numbers since such units are known in the art and are commercially available, for example from Texas Instruments, Inc., Dallas, Tex. The various numbered terminals appearing on the integrated circuits shown herein correspond to the standard terminal numberings on those units, the function of each of which is known and understood by those in the art.

Further with reference to FIG. 6, the data input lines A, B, C, D, E are connected to terminals numbered 4, 5, 12, 11, 10 of the converter 116, which are the parallel input terminals for the converter. Three additional data bits, which are used for control and error detection purposes in the decoding system, are added in the converter to the five binary bits ABCDE received from the coding matrix. These three additional data bits are added as states 1, 0, and 1 to input terminals numbered 2, 3 and 14 of converter 116.

The parallel data are loaded into the converter 116 upon receipt of a keying pulse over conductor 122. When clocked (as hereafter described) the serial data from the converter 116 will issue over conductor 124 that is connected to the serial output (terminal no. 13) of converter 116. The converter 116 operates to provide a serial output 10ABCDE1 on conductor 124, as shown in FIG. 2. The audio tone from the organ is transmitted over conductor 126 to channel no. 1 of the tape recorder and also to the inverting input (terminal no. 4) of an operational amplifier 128 through input resistance 130. This amplifier 128 is also an integrated circuit, type 1709 having operating characteristics which are a function of the external feedback components. Resistors 132, 134 and r.f. bypass capacitors 136, 138 are connected to the terminals indicated, resistor 134 being a feedback resistor. The amplifier 128 and circuit 140 constitute a clock converter 142 (FIG. 2). This clock converter processes the normal audio tone of the organ and converts it to a suitable clock signal for the converter 116 to regulate the width of its output pulses, which constitute the data bits. The output from the amplifier 128 through resistor 144 is connected to the input terminal of the circuit 140, which in the present example of the invention may be a type 7413 integrated circuit. This circuit 140 includes two NAND gates each with four inputs and an output. The output from the circuit 140 is sent over conductor 146 to the clock input terminal (no. 7) of the converter 116. The circuit to terminal no. 6 serves as a test point for the clock.

When a clock signal is sent over conductor 146, the data in the converter 116 will be sent out over conductor 124 in serial form, as aforesaid. To insure full data loading of the converter 116, the amplifier 128 is constructed so that the signal output from the circuit 140 will be delayed enough to complete the loading of the converter 116.

To preclude the likelihood recording of degraded data signals in the tape recorder cassette, the data signals are desirably sent to buffer/differentiator 148 which may take the form of a type 75450 integrated circuit with an output circuit consisting of resistors 152, 154 and capacitor 156. The differentiated output signal is sent over conductor 158 to channel no. 2 of the tape recorder 106. As seen in FIG. 2 the approximate shape of the wave form of the differentiated signal is shown adjacent to conductor 158. The wave forms associated with other conductors shown in the drawing herein are also illustrated.

As thus far described, the tape recorder 106 is turned on and set in the recording mode prior to depressing a selected organ key. When the selected key is depressed, the audio tone is recorded on channel no. 1 of the recorder and this audio tone is used for deriving the clock signal to converter 116. Switch 118 is also closed by the organ key which loads data from the coding matrix 108 into the converter under control of the signal from the pulse keyer 120. Data in serial form is sent from converter 116 through buffer/differentiator 148 and is recorded on tape channel no. 2 in serial form.

For playback, the recorder 106 is set in playback mode so that the stored signals may be sent to suitable decoding circuitry as shown in FIGS. 3, 7, 8, 9A and 9B to illuminate the lamp corresponding to the selected key.

Referring to FIGS. 3 and 8, the audio tone from channel no. 1 is sent over conductor 160 to the audio reproduction system of the organ. The audio signal is also sent to amplifier arrangement 162 comprising two general type 709 operational amplifiers 164, 166, namely, integrated circuits 1709L and 72709N, respectively, and a NAND gate circuit 188, which is a type 7413N integrated circuit. The inversion inputs and the outputs of the two amplifiers are at terminals 4 and 10 of each, the non-inverting input being at terminal no. 5 of each. The external feedback and other components consisting of resistors 170, 172, 174, 176, 178 and capacitors 182, 184, 186 are connected to the terminals indicated in the drawing. The second amplifier 166 serves as a Schmitt trigger.

The output at conductor 168 is sent through a transistor circuit 180 for driving the circuit 188 and operates as an additional Schmitt trigger to produce a square wave clock signal of correct rise and fall time characteristics on conductor 190 (see FIGS. 3 and 8). Thus, the clock converter of FIG. 3 may be considered as being made up of a portion of the circuit 166 and circuit 188. Signals for operating the circuit 188 are from conductors 192, 194 which are across resistor 196 in the transistor circuit 180. The transistor circuit 180 is a clipping/squaring stage. Conductor 192 maintains a signal on the input terminals numbered 9, 10, 12 and power supply terminal no. 14. When a signal is applied from conductor 192, the NAND gate conducts giving a pulse at output terminal no. 8 on conductor 190. Thus, the clock pulse on 190, which is derived from the

recorded audio tone from cassette, is sent to a serial-to-parallel converter **198** (FIGS. 3 and 9).

Referring to FIGS. 3 and 7, it is seen that the output data signals from channel no. 2 of the tape recorder **106** is over conductor **200**, and this signal is sent to the inverting input of amplifier arrangement **202**. The amplifier arrangement **202** includes two general type **709** operational amplifiers **202***a*, **202***b* comprised of integrated circuits, namely types 1709L and 72709N. The external components comprising resistors **206, 208, 210, 212, 214** and capacitors **216, 218, 220, 222** are connected in circuit and to the standard numbered terminals indicated in FIG. 7. Two amplifier circuits are used to provide adequate amplification and to return the signal to proper phase relationship. Resistor **208** and capacitor **216** are used for input lag compensation. Output lag is provided by capacitor **220**.

As seen in FIG. 3, the output from the amplifier arrangement **202** is sent to a peak level detector **226** which drives a Schmitt trigger **228**. Peak level detection is desired in order to detect the data stream and eliminate lower level extraneous signals. The peak level detector and Schmitt trigger process the data signals to a form in which they may be loaded via conductor **230** into the serial-to-parallel converter **198**.

The peak level detector **226** and Schmitt trigger circuit **228** are also shown in FIG. 7. The Schmitt trigger circuit **228** is type **1709** operational amplifier while circuit **234** is a type **7410** integrated circuit, which is a three input positive NAND gate. Circuit **228** has its inverting input connected through resistor **236**, the remaining components, namely resistors **238, 240** capacitors **242, 244, 246** being connected to the standard numbered terminals of circuit **228** as shown in FIG. 7. The threshold voltage of the circuit **228** is set by the feedback resistor **238** and the resistor **240** from terminal no. 5 to ground. The output terminal of circuit **228** is connected through resistor **248** and conductor **250** to the input of the NAND gate circuit **234**. The NAND gate circuit **234** provides a logic signal compatible with the input signal requirements of the hereinafter described shift registers **254, 256** of FIG. 9A. Thus, for block diagram purposes as in FIG. 3, circuit **232** may be considered as part of the Schmitt trigger **228**. From the foregoing it will be apparent that there are serial pulses on conductor **230** representing the data fed back from channel no. 2 of the tape recorder.

Referring now to FIG. 9A, it will be seen that the serial-to-parallel converter **198** utilizes two four-bit shift registers **254, 256** which may comprise two 7495A integrated circuits. However, a single eight bit shift register may be constructed for use as the converter **198**. In any event, the converter **198** as a whole must be capable of handling eight bits as this is the number of bits used in the code of the present example of the invention.

Conductor **230** is connected to the serial input terminal no. 1 of the register **254** while the conductor **190** is connected to one of the two clock terminals of each of the registers **254, 256** in accordance with the desired direction of bit shift. As the data are clocked into the shift registers **254, 256**, the data bits 10AB will appear on terminals numbered **13, 12, 11, 10** respectively of the register **254** while the data bits CDE1 will appear on terminals numbered **13, 12, 11, 10** respectively of the register **256**, all as clearly shown in FIG. 9A. The data will be in parallel form. To produce the CDE1 outputs from the second register **256** the output from terminal no. **10** of register **254** and containing the B bit is connected to the serial input terminal no. **1** of the register **256**.

It will be seen from FIGS. 9A and 9B that the data bits ABCDE are sent over conductors **260, 262, 264, 266, 268** to a latching network **270** (see also FIG. 3), which is, by way of example, made up of two bistable quad latches **272, 274**. Each latch circuit **272, 274** may be a type **7475** integrated circuit. The data bits ABCD are stored in the latch **272** while the data bit E is stored in the latch **274**.

Referring again to FIG. 9A and FIG. 3, it is noted that the control bits, namely the code bits 1, 0, 1 are sent to a load indicator **276** which, in the present embodiment, comprises a hex inverter made up of integrated circuit type **7405**. This load-indicator circuit **276** is utilized to determine the position of the information bits in the shift registers **254, 256**. When the shift registers are fully loaded with the eight bit code, the code bits 0, 1, 0 are sent over conductors **280, 282, 284** to terminals numbered **1, 3** and **5** of the circuit **276**. The logic states of those signals are inverted in the circuit **276** to produce logic 0 outputs from terminals numbered **2, 4** and **6** of circuit **276**. A logic state 1 output appears on terminal no. **4** and this is sent to terminal no. **9** to provide a state 0 output from terminal no. **8**. Consequently, when the shift registers **254, 256** are fully loaded, there will be a state 0 output on conductor **286**. At other times the conductor **286** is at a high state, as determined by the voltage drop across resistor **288**.

Referring to FIG. 9B, the signal on conductor **286** drives a transistorized pulse-stretching circuit **290** having input resistor **292** connected to the transistor base and capacitor **294** shunted from emitter to collector. The output signal from the circuit **290** on conductor **296** is sent to a NAND gate circuit **298**, which may be a type 7413 integrated circuit. Such circuit contains a NAND gate arrangement with four inputs; hence three of the inputs, as indicated at terminals numbered **9, 10** and **12** may be biased to a state 1. Thus, a signal on conductor **296** produces an output or clock signal from terminal no. **8** on conductor **300**, which signal is sent to the clock input terminals numbered **4** and **13** of the latches **272, 274**, thereby triggering the latches and releasing the data therefrom. In passing and with further reference to circuit **290** it should be noted that the inputs to the circuit **298**, and hence the input at terminal no. **13** thereof, is sufficiently above zero voltage to provide a power supply voltage for the transistor of the circuit **290**.

Still referring to FIGS. 3, 9A and 9B, three BCD to decimal converters **302, 304, 306** are used to convert the signals to decimal code for the purpose of illuminating the lamp that corresponds to the organ key that was depressed, as previously described. Since the converters **302, 304, 306** are controlled by a four bit parallel signal, it is necessary to modify the five bit code ABCDE to provide a compatible driving signal.

When the latches **272, 274** are clocked to release the data therein, the A, B and C data signals are sent out over conductors **310, 312, 314** (see FIG. 9B and again on FIG. 9A) to inputs of converters **302, 304, 306**. However, the D and E outputs from the latches **272, 274** are combined in a decimal coder **316**, which may be a quad NAND gate integrated circuit type 7400. The D output from the latch **272** to the coder **316** is

over conductor **318** while the E output from latch **274** is over conductor **320.** $\overline{D}$ sent from the terminal no. **8** of circuit **272** while $\overline{E}$ is sent from terminal no. **1** of circuit **274.** The D, $\overline{D}$, E, $\overline{E}$ outputs are combined in the quad NAND gate coder **316** to produce output signals on conductors **324, 326, 328, 330.** These signals constitute the fourth signals for the converters **302, 304, 306,** plus a signal that is sent back through one of the latches in the circuit **274** for operating lamp no. **24** (FIG. 9B). Thus, the combined D and E bits determine which converter **302, 304, 306,** or lamp no. **24** is activated. The states of ABC select the converter output and thus determine which lamp of the group is activated. For example, considering the signal on conductor **330,** $\overline{D \cdot E} = 0$ if and only if D = 1 and E = 1. Only then can the converter **302** be operated to illuminate any one of the lamps nos. **1** to **7** and **25,** as determined by the logic states of ABC. Likewise, converter **304** will be operated only if $\overline{D} = 1$ and E = 1. The groups of lamps will thus be activated in accordance with the following truth table:

$(\overline{D \cdot E})$	$(\overline{D \cdot E})$	$(\overline{D \cdot E})$	$(\overline{D \cdot E})$	Converter	Lamp Group
0	1	1	1	302	Nos. 1 to 7, 25
1	0	1	1	304	Nos. 8 to 15
1	1	0	1	306	Nos. 16 to 23
1	1	1	0		No. 24

As to lamp no. **24,** the output $(\overline{D \cdot E})$ over conductor **324** is sent through a latch of the circuit **274** to produce an output signal on conductor **340** to transistor stage **342** which acts as a switch for lamp no. **24.** It should be noted that with respect to the other lamps, they may be operated directly from the integrated circuits **302, 304, 306** since these have open collector configurations.

In the form of the invention shown in FIGS. **10** and **11,** the digital code and clock control signals may be recorded on a single tape channel so that with a two channel tape recorder, the system could provide one unrestricted information channel. The arrangement of FIGS. **10** and **11** utilizes a number of the components previously described, and like reference numerals in FIGS. **10** and **11** indicate like parts as described with reference to FIGS. **1–9B.** In essence, FIGS. **10** and **11** utilize a modulation-demodulation system that converts binary "ones" and "zeros" into selected audio tones. By way of example, the 1 could be represented by a 1,700Hz tone and the 0 by a 2,200Hz tone. These tones could be amplitude modulated by a fixed clock frequency whereby the composite envelope would in effect be self-clocking.

As shown in FIG. **10,** a clock signal generator **400** sends its output over conductor **402** to the parallel-to-serial converter **116,** and the output of the latter on conductor **404** is sent to a voltage-controlled oscillator **406.** Consequently, the output from the converter **116** contains the serial data gated by the clock pulses. The output from the voltage-controlled oscillator will consist of series of tone bursts of two different frequencies in accordance with the logic states of the signals on conductor **404.** These signals are sent to an analog gate **410** and the clock pulses from the clock generator **400** are also sent over conductor **412** to the analog gate **410.** In the analog gate **410,** the tone bursts of the two frequencies are, in effect, modulated by the clock pulses. This produces an envelope containing the clock signal and data tone signals. It is this envelope that is sent to the storage medium, such as one channel of the tape cassette recorder.

Referring now to FIG. **11** that shows the decoding arrangement, the signals from the tape channel are sent to an amplifier **414,** the output from which is sent to an envelope detector **416** and, over conductor **418,** to a tone decoder **420.** In the envelope detector, the clock signal "envelope" is demodulated and is used to drive a Schmitt trigger **422,** the latter being used for proper pulse timing and shaping of the clock signal for use with the logic in the serial-to-parallel converter **198.** In the tone decoder **420,** the signals of the two frequencies representing the two logic states of the data are converted and shaped to provide voltages corresponding to logic state 1 or state 0. This converts the data back into serial bit form for transmission over conductor **424** to the converter **198.** The remaining decoding functions are as previously described, as will be apparent from FIG. **11.**

If a multi-channel tape recorder or other multi-channel magnetic storage medium is used with the arrangement of FIGS. **10** and **11,** the audio tone for the particular organ key depressed can be recorded and played back from a second channel, or such second channel may be used for other instructional purposes.

The systems herein are monotonic in that only one note at a time can be played. However, the systems are adaptable for indicating chords. For example, a **12** bit code could be used in which four bits are for a chord, five bits for notes and three bits for loading information.

The invention is claimed as follows:

1. In a musical instrument having a keyboard, the keys of which are operable to produce selected audio tones, a series of electric lamps adjacent to the keyboard, each lamp corresponding to a key, first means operable responsive to actuation of a selected key for encoding data in digital form representing the selected key, a storage medium for said data, second means for processing the data from the first means and delivering the processed data to said storage medium, third means for retrieving said data from said storage medium, and fourth means for processing said retrieved data and delivering a signal to the lamp associated with the selected key.

2. In an instrument according to claim **1,** means for recording the audio tone for the selected key upon actuation thereof, and means for reproducing the audio tone upon retrieval of said data and actuation of said lamp by the signal delivered thereto.

3. In an instrument according to claim **1,** said first means including a binary coding matrix for coding the key-indicating data in para'lel bit form, and second means including a parallel-to-serial converter for converting said data to serial form, whereby the data is stored on said storage medium in serial form.

4. In an instrument according to claim **3** further including pulse generating means forming part of said first means and operable responsive to actuation of said selected key for enabling the loading of data into said parallel-to-serial converter.

5. In an instrument according to claim **4** further including means forming part of said first means and providing a signal derived from the audio tone for clocking the operation of said parallel-to-serial converter.

6. In an instrument according to claim 5 further including means for adding data bits of predetermined logic states in said converter to the data represented by the selected key whereby the data sent to said storage medium includes said added data bits.

7. In an instrument according to claim 1, fifth means forming part of said second means for adding additional bits to the data representing the key, and sixth means forming part of said third means for utilizing said additional bits as a control for the flow of the remaining bits to said fourth means.

8. In an instrument according to claim 7 further comprising a latching network also forming part of said fourth means and controlled by said sixth means such that the loading of said remaining bits in said latching network is ascertained by the presence of said additional bits in said sixth means.

9. In an instrument according to claim 7 further comprising a decimal coder also forming part of said fourth means for combining some of the data bits sent from said latching network, and BCD to decimal converter means also comprising part of said fourth means that receive data bits in parallel form from said latching network and said decimal coder for driving said lamp.

10. In an instrument according to claim 5 in which said storage means comprises a multi-channel magnetic tape in which the data is stored on one channel, and said audio tone is stored on the other channel.

11. In an instrument according to claim 4 including means for clocking said parallel-to-serial converter independently of said audio tone, the data and clock signal being recorded on a single channel of the storage medium.

12. In an instrument according to claim 11, said third means including means for detecting said clock signal from the data output from said storage medium.

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