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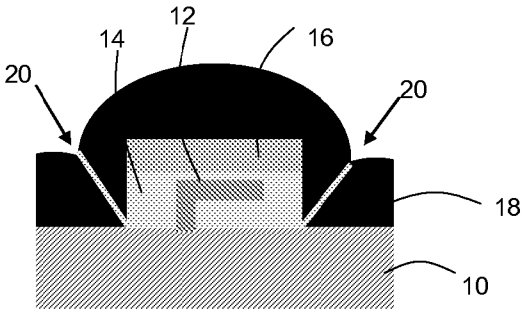


Fig. 1e

(57) Abstract: The present invention discloses a method of packaging a microscopic structure (12). The method comprises the steps of forming the microscopic structure (12) on a substrate (10); depositing a layer (14) of a thermally decomposable polymer over the substrate, thereby embedding the microscopic structure; patterning the deposited layer (14) such that the microscopic structure is embedded in a portion of the patterned layer, the side walls of said portion (14) forming a substantially right angle with the substrate (10); growing a capping layer (18) over the portion, wherein the substantially right angles cause the formation of at least one channel (20) from the portion (14) through the capping layer (18); and decomposing the polymer, whereby the decomposition products escape from the portion (14) through said channel (20). The present invention further discloses a device including a microscopic structure packaged in accordance with the above method.

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DESCRIPTION

MICROSCOPIC STRUCTURE PACKAGING METHOD AND DEVICE WITH PACKAGED MICROSCOPIC STRUCTURE

The present invention relates to a method of packaging a microscopic structure.

The present invention further related to a device comprising such a microscopic structure.

The ongoing miniaturization of feature sizes in semiconductor manufacturing processes has facilitated the formation of microscopic structures, i.e. structures that have feature sizes in the micron and submicron, e.g. nanometer domain, on substrates such as silicon substrates. A prime example of such a microscopic structure is a microelectromechanical system (MEMS) structure. Such structures are sometimes also referred to as micromachines.

MEMS structures can be used for a wide range of applications in different fields of technology, e.g. electronics, medicine, pharmacy and chemistry. Applications in the filed of electronics for instance include accelerometers, gyroscopes, sensors, and so on. The MEMS structures may be made from any suitable material, e.g. silicon, polymer, metals amongst others.

Typically, the MEMS structure requires a certain degree of translational freedom in order to perform its function. To this end, the MEMS structure is packaged such that the structure is located in a cavity. As mentioned in US2005/0095833 A1, such packaging techniques are typically applied at wafer level, e.g. by wafer bonding or encapsulate the MEMS structure using thin film techniques.

However, wafer-level packaging techniques are relatively cumbersome, i.e. processing intensive, and, as a consequence, very expensive. In fact, more

often than not, the packaging step in the manufacturing process of a microscopic device is the most expensive step in this process.

The present invention describes a wafer level packaging method using standard processing steps, which provides a less cumbersome method of packaging a microscopic structure on a substrate, thereby reducing the packaging cost and packaging size of such a structure

The present invention seeks to provide a device comprising such a packaged microscopic structure.

In accordance with a first aspect of the present invention, there is provided a method of packaging a microscopic structure, comprising forming the microscopic structure on a substrate; depositing a layer of a thermally decomposable polymer (TDP) over the substrate, thereby embedding the microscopic (MEMS) structure; patterning the deposited layer such that the microscopic structure is embedded in a portion of the patterned layer, the side walls of said portion having a substantially right angle with the substrate; growing a capping layer over the portion, wherein the substantially right angle causes the formation of at least one channel from the portion through the capping layer; and decomposing the polymer, whereby the decomposition products escape the portion through said channel.

The method of the invention describes a thin film technique to encapsulate a structure such as a MEMS structure, thereby reducing the packaging cost of such a structure because the use of special equipment for wafer level packaging using bonding is not required.

Instead, the microscopic structure is packaged early in the manufacturing process of a device comprising such a structure, which obviates the need for post-processing the completed device to form such a cavity protecting the microscopic structure. It has been found by the present inventors that when a TDP portion is patterned in such a manner that the side walls of the TDP portion form an angle of approximately 90° with the substrate, the subsequently formed

capping layer spontaneously forms a channel that more or less diagonally extends from such a side wall of the TDP portion through the capping layer. This channel may be used as a chimney to outgas the decomposition products when thermally decomposing the TDP.

At this point, it is noted that Höchst et al. in "Stable Thin Film Encapsulating of Acceleration Sensors using Polycrystalline Silicon as Sacrificial and Encapsulating Layer" in Sensors and Actuators, pages 355-361, A114 (2004) disclose the formation of a hole in a capping layer for making a cavity. However, this prior art method has the disadvantage that an additional mask is required to form the hole, thus adding to the cost of the packaging method.

It has been found that especially plasma-enhanced chemical vapor deposition (PE-CVD) formation of the capping layer promotes the spontaneous formation of such a channel. Preferably, the capping layer is formed of silicon oxide because this yields consistent channel formation. Alternatively, any other material may be used that can be deposited using CVD techniques. Examples of such materials include SiN, SiC and SiGe.

In an embodiment, the method further comprises sealing the channel following said decomposition step. This protects the microscopic structure from exposure to pollutants that may enter the cavity formed in the capping layer following the decomposition of the TDP. The channel may be sealed by the deposition of a further capping over the capping layer. The further capping layer may be another PECVD, CVD or LPCVD layer or a metal layer such as aluminum. In case of an aluminium further capping layer, this layer may be deposited using physical vapor deposition (PVD).

The method of the present invention preferably further comprises depositing an etch mask over the thermally decomposable polymer layer prior to said patterning step.

According to another aspect of the present invention, there is provided a device comprising a substrate carrying a microscopic structure and a capping layer, said capping layer comprising an embedded cavity including the microscopic structure; and a channel extending from said cavity through the

capping layer. Such a device manufactured by the method of the present invention is much cheaper to make than existing devices comprising embedded microscopic structures because the packaging of the microscopic structure can be achieved much more easily.

The device may comprise a further capping layer covering the capping layer, the further capping layer sealing the channel to protect the microscopic structure, e.g. a MEMS structure from exposure to an external environment.

Embodiments of the invention are described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:

Figs. 1a-g depict an embodiment of a method according to the present invention; and

Fig. 2 depicts a scanning electron microscope (SEM) image of a cavity formed by the method of the present invention.

It should be understood that the Figures are merely schematic and are not drawn to scale. It should also be understood that the same reference numerals are used throughout the Figures to indicate the same or similar parts.

In Fig. 1a a substrate 10 carrying a microscopic structure 12 is provided. In the remainder of this description, the microscopic structure 12 will be referred to as MEMS structure 12, but it will be appreciated that microscopic structure 12 may be any suitable microscopic structure, such as a structure in a microfluidic device. It is pointed out that the MEMS structure 12 may be formed on the substrate 10 in any suitable way using any suitable material. In addition, the substrate 10 may be any suitable substrate such as a silicon substrate. The specific embodiments of the substrate 10 and the MEMS structure 12 are not essential to the present invention.

In Fig. 1b, a layer 14 of a thermally decomposable polymer (TDP) is deposited over the substrate 10 and the MEMS structure 12 such that the MEMS structure 12 is fully covered by the TDP. Non-limiting examples of a suitable TDP include polynorbornenes, polymethoxymethacrylates. XP0733 marketed by

Rohm Haas™ is an example of such a material. The TDP material is sometimes also referred to as an unzipping material. The TDP layer may be deposited using any suitable deposition technique. It will be understood that the deposition technique should avoid damage to the MEMS structure 12. A non-limiting example of such a suitable technique is spin-coating.

Fig. 1c depicts an optional step in the packaging of the MEMS structure 12. In this optional step, a hard mask 16 is applied over the TDP layer 14, which may be applied using any suitable deposition technique. For instance, the hard mask may be HM2800 marketed by Rohm Haas™, which is an oxide material that may be applied over the TDP layer 14 by means of spin-coating. Alternative hard mask layers deposited in different ways may be equally feasible. An example of such an alternative is Black Diamond™, which is a low-k SiOC material marketed by Applied Materials®, and which may be deposited by CVD techniques. Other examples include SiC, SiGe and even metal layers. It will be appreciated that the hard mask will be subsequently patterned prior to patterning the TDP layer 14. This is not explicitly shown because this is a routine skill for the person skilled in the art.

In a next step depicted in Fig. 1d, the TDP layer 14 is patterned such that the TDP layer 14 is reduced to a portion in which the MEMS structure 12 is embedded. This patterning step may be preceded by a patterning of the hard mask 16 if present. The hard mask 16 may be removed using an etching step. The TDP layer 14 may be patterned using a further etching step. Table I gives a non-limiting example of an etch composition for these etching steps.

Table I

	Press [mT]	Power 27MHz [W]	Power 2MHz [W]	O_2 [Sccm]	Ar [Sccm]	CF_4 [Sccm]	N_2 [Sccm]	CH_3F [Sccm]	CH_2F_2 [Sccm]
Mask etch	100	400	150	5	200	65			5
TDP etch	80	700		10			500	2	

The etching steps were performed in an EXELAN chamber on a 2300 platform marketed by LAM™. In Table I, 'press' stands for the pressure inside the etching chamber, and 'power 27 MHz' and 'power 2MHz' stands for the respective frequencies of the power sources connected to the top and bottom electrodes inside the chamber.

In order to ensure the formation of an outgassing channel in the subsequent steps of the method, the formation of the portion of the TDP layer 14 must be well-controlled. For instance, care must be taken that angle θ doe not significantly deviate from a 90° value, because it has been found that a substantially right angle between the side walls of the portion and the substrate surface 10 is required. However, the value may deviate from around 90° depending on the chosen deposition settings in the PE-CVD process.

In addition, it is important that the dimensions of the TDP portion 14 are controlled, because an excessively large TDP portion 14 can reduce the stability of the cavity formed around the MEMS structure 12. The actual critical dimensions will depend on a large number of factors, such as the thickness of the capping layer formed over the TDP portion 14 (vide infra). In a next step shown in Fig. 1e, a capping layer 18 is grown over the substrate 10 and the TDP portion 14. Preferably, the capping layer 18 is a silicon oxide layer deposited using PE-CVD. It has been found that such a capping layer 18 has a tendency to spontaneously forming a channel 20 from the TDP portion 14 through the capping layer 18 such that the TDP portion 14 remains in contact with the outside world through the channels 20. As has been explained previously, the channel formation is critically linked to the value of the angle θ. In an embodiment, the PE-CVD step is executed at 200°C. It has been found that the channel formation is more easily achieved at relatively low process temperatures. Moreover, the temperature must be chosen below the TDP decomposition temperature. The silicon oxide may be deposited from a gas mixture of N_2O and SiH_4. In an embodiment, the thickness of the silicon oxide capping layer has to be thick enough to ensure that the capping layer 18 can withstand pressures that build up in the embedded TDP portion 14 during its decomposition. Further layers may be

deposited over the capping layer to strengthen the capping layer 18 to improve the structural integrity of the cavity, for instance to withstand pressures from process steps such as molding.

In a next step 1f, the capping layer-covered substrate 10 is exposed to a thermal budget with or without assistance of a UV-source or any other radiation source that accelerates the decomposition rate of the TDP to decompose the TDP portion 14. During this process, the channels 20 act as a chimney for outgassing the decomposition products of the TDP portion 14, thus yielding a MEMS structure 12 in a cavity 22 packaged in the capping layer 14. The actual temperature of the decomposition step will depend on the TDP chosen. For instance, for XP0733, a temperature of 450°C may be used. In any way, the temperature should preferably be chosen such that the decomposition process progresses at such a rate that the channels 20 are capable of outgassing the decomposition products without substantial build-up of pressure in the formed cavity 22, because an excess pressure in the cavity 22 can lead to damage to the capping layer 18, e.g. cracking.

At this point, it is noted that the device obtained after step 1f may be the completed device. In this case, the channels 20 may serve as cooling ducts for the microscopic structure 12, for instance if the microscopic structure 12 is a miniature power-consuming device.

However, if the microscopic structure 12, e.g. a MEMS structure is to be protected from environmental influences, the channels 20 may be sealed off. Fig. 1g shows an embodiment of such a sealing step. A further capping layer 24 is deposited over the capping layer 18 such that the channels 20 are effectively sealed. The further capping layer may be a metal layer, e.g. Al, and may be deposited in any suitable way. Optionally, the structure of Fig. 1f may be exposed to a predefined gas composition in order to replace the air in the cavity 22 with the predefined gas composition through the channels 20. The further capping layer 24 is preferably deposited in a subsequent step under the same gas composition. The predefined gas composition may be used to tune the properties of the microscopic structure 12, e.g. a MEMS resonator. Alternatively, the further

capping layer may be deposited under a reduced pressure in order to establish a (near-)vacuum inside the cavity 22. This is for instance useful to increase the Q-factor of a MEMS resonator.

Fig. 2 shows a SEM image of the device of the present invention after the TDP decomposition step in which a PE-CVD deposited silicon oxide capping layer 18 is formed over a TDP portion 14 having substantially vertical side walls. The channels 20 are clearly distinguishable in the SEM image, as is the formed cavity 22, thus demonstrating that the method of the present invention is capable to package a microscopic structure 12 in a cavity 22 inside a capping layer 18 without requiring an additional mask to form the outgassing channels 20.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. A method of packaging a microscopic structure (12), comprising:

forming the microscopic structure (12) on a substrate (10);

depositing a layer (14) of a thermally decomposable polymer over the substrate, thereby embedding the microscopic structure;

patterning the deposited layer (14) such that the microscopic structure is embedded in a portion of the patterned layer, the side walls of said portion (14) forming a substantially right angle with the substrate (10);

growing a capping layer (18) over the portion, wherein the substantially right angle causes the formation of at least one channel (20) from the portion (14) through the capping layer (18); and

decomposing the polymer, whereby the decomposition products escape from the portion (14) through said channel (20).

2. A method according to claim 1, further comprising sealing the channel (20) following said decomposition step.

3. A method according to claim 2, wherein said sealing step comprises depositing a further capping layer (24) over the capping layer (18).

4. A method according to claim 1 or 2, wherein the capping layer (18) is grown using plasma-enhanced chemical vapor deposition.

5. A method according to any of the preceding claims, wherein the microscopic structure (12) is a MEMS (microelectromechanical system) structure.

6. A method to any of the preceding claims, further comprising depositing an etch mask (16) over the thermally decomposable polymer layer (14) prior to said patterning step.

7. A method according to any of the preceding claims, wherein the capping layer (18) is a silicon oxide layer.

8. A device comprising:

a substrate (10) carrying a microscopic structure (12) and a capping layer (18), said capping layer comprising an embedded cavity (22) including the microscopic structure (12), the side walls of said cavity forming a substantially right angle with the substrate (10); and

a channel (20) extending from said cavity (22) through the capping layer (18).

9. A device according to claim 8, further comprising a further capping layer (24) covering the capping layer (18), the further capping layer (24) sealing the channel (20).

10. A device according to claim 8 or 9, wherein the microscopic structure (12) is a MEMS structure.

11. A device according to any of claims 9-11, wherein the capping layer (18) is a silicon oxide layer.



Fig. 1a

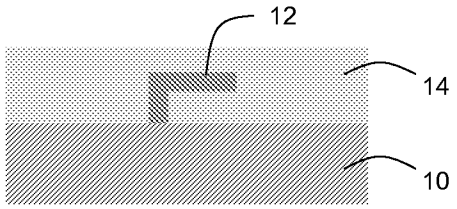


Fig. 1b

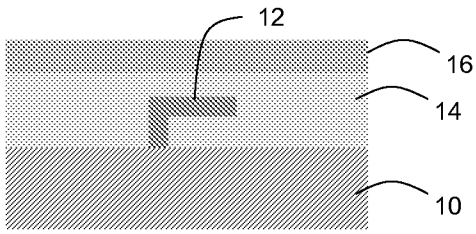


Fig. 1c

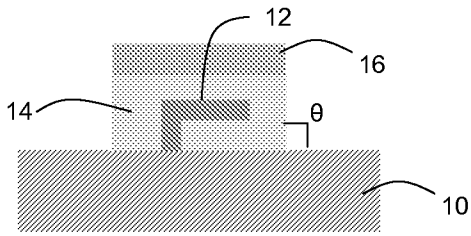


Fig. 1d

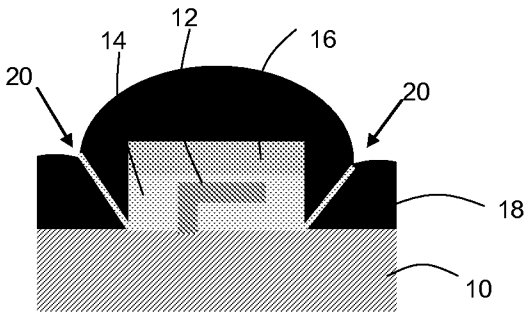


Fig. 1e

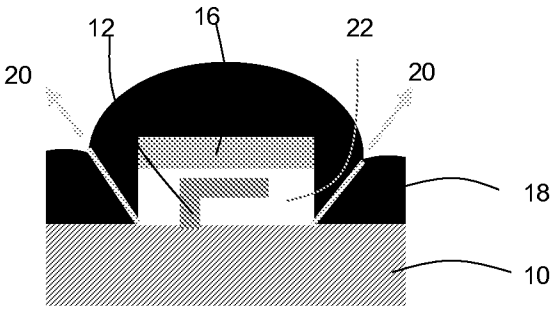


Fig. 1f

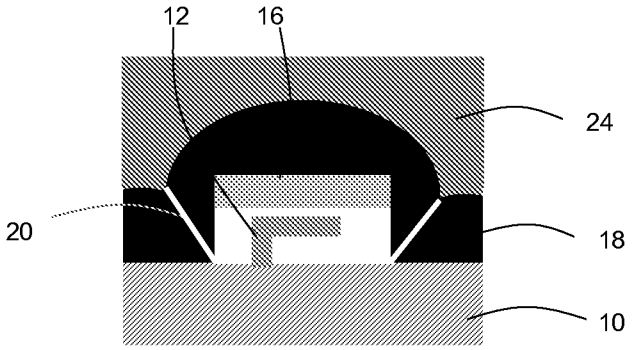


Fig. 1g

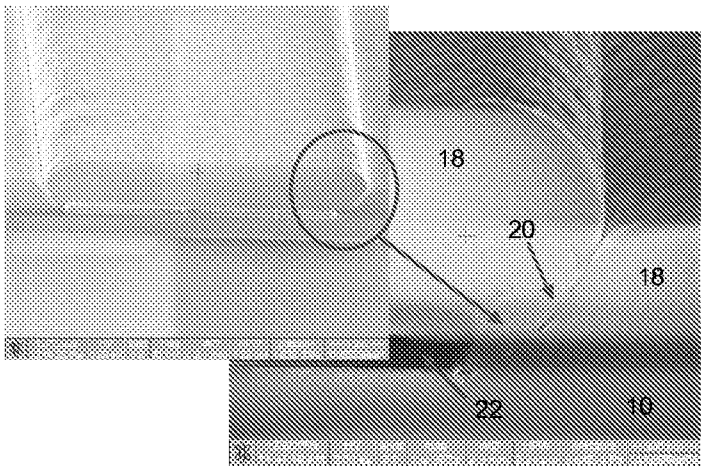


Fig. 2