(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 April 2015 (09.04.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/050810 A1

(51) **International Patent Classification**:
H02M 3/337 (2006.01)

(21) **International Application Number**:
PCT/US2014/057998

(22) **International Filing Date**:
29 September 2014 (29.09.2014)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
14/044,516 2 October 2013 (02.10.2013) US

(63) **Related by continuation (CON) or continuation-in-part (CIP) to earlier application**:
US 14/044,516 (CON)
Filed on 2 October 2013 (02.10.2013)

(71) **Applicant**: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, Texas 75265-5474 (US).

(71) **Applicant** *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, Tokyo 160-8366 (JP).

(72) **Inventor**: **COHEN, Isaac**; 8 Arista Ct., Dix Hills, NY 11746 (US).

(74) **Agent**: **DAVIS, Michael A., Jr.**; TEXAS INSTRUMENTS INCORPORATED, International Patent Manager, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) **Title**: INTERLEAVED FORWARD CONVERTER WITH WIDE INPUT AND OUTPUT DYNAMIC RANGE

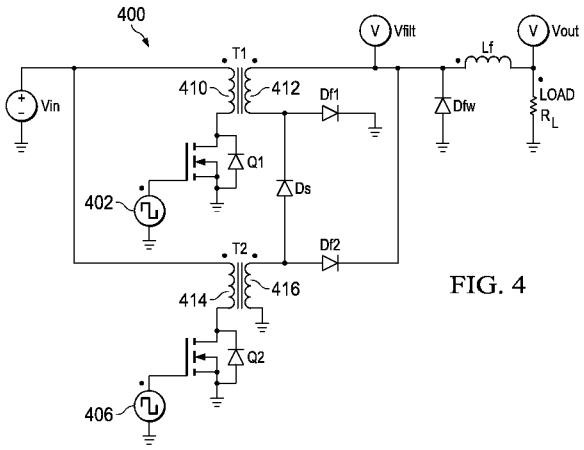


FIG. 4

(57) **Abstract**: In described examples of an interleaved forward voltage converter (400), a first inverter stage includes a first transformer (T1) having a turns ratio N1and a primary winding (410) having one terminal coupled to a source of input voltage (Vin) and another terminal coupled to a first switching transistor (Q1). A first secondary winding (412) for the first transformer (T1) has a first terminal coupled to a first terminal of a filter inductor (Lf), and a second terminal coupled to a first diode (Df1). A second converter stage includes a second transformer (T2) having a turns ratio N2 and a primary winding having one terminal coupled to the source of input voltage (Vin) and another terminal coupled to a second switching transistor (Q2). A second secondary winding (416) for the second transformer (T2) has a first terminal coupled to the first terminal of the filter inductor (Lf) through a second diode (Df2), and a second terminal coupled to a reference voltage source. A third diode (Ds) is coupled between the first terminal of the second secondary winding (416) for the second transformer (T2) and the second terminal of the first secondary winding (412) of the first transformer (T1).

WO 2015/050810 A1

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

INTERLEAVED FORWARD CONVERTER WITH WIDE INPUT AND OUTPUT DYNAMIC RANGE

[0001] This relates in general to an interleaved forward voltage converter, and in particular to a converter having a wide input and output dynamic range.

BACKGROUND

[0002] Interleaved forward voltage converters, also known as push–push converters, are known in the art. FIG. 1 shows an example of a prior art interleaved forward voltage converter 100. In the converter 100, a source of input voltage Vin is coupled to a positive terminal of a first transformer T1 of the first converter stage. The other terminal of transformer T1 is connected to ground through a first switching transistor Q1. The transistor Q1 is driven by a pulse generator 102. A secondary winding of a transformer T1 has a negative terminal connected to ground, and a positive terminal connected to one terminal of a filter inductor Lf through diode Df1. A second converter stage including transformer T2 has a positive terminal of the primary winding connected to the source of voltage, and a negative terminal connected to ground through transistor Q2. The gate of transistor Q2 is driven by pulse generator 106. The secondary winding of transformer T2 has a negative terminal connected to ground, and a positive terminal connected to the input terminal of filter inductor Lf through diode Df2. The diode Df1 and Df2 are connected at node Vfilt. A freewheeling diode Dfw is connected to the node Vfilt. A load, which is shown as a resistor R_L, is connected to the terminal on the other side of inductor Lf. An output capacitor Co is coupled across the load resistor R_L.

[0003] Transistors Q1 and Q2 are switched 180° out of phase from each other, and output voltage regulation is performed by pulse width modulation (PWM) of the gate drive signals (not shown). Operation of the circuit of FIG. 1 will now be explained in connection with FIG. 2, where the duty cycle of transistors Q1 and Q2 is 30%. In FIG. 2, the waveforms for operation of the circuit at 30% duty cycle are shown generally as 200. The currents through transistors Q1 and Q2 are shown by the waveforms I(Q1) and I(Q2). The current through the freewheeling diode Dfw is shown by the waveform I (Dfw). The voltage at the node Vfilt is shown as Vfilt, and the output voltage is shown as Vout. The voltage at Vout is shown on an expanded voltage

scale, so that the ripple can be seen. At this duty cycle, the voltages generated by the first converter and the second converter add at the terminal Dfilt, and an increased voltage is available at the terminal Vout.

[0004] Operation of the circuit of FIG. 1 will now be explained in connection with FIG. 3, where the duty cycle of transistors Q1 and Q2 is 70%. The same waveforms are shown in FIG. 3 as were shown in FIG. 2, generally as 300. Although the duty cycles of the two transistors cause them to overlap in their ON time, the current through the transistors do not overlap, and no additional voltage is generated at the node Vfilt during the period of overlap. The current through the freewheeling diode, and the voltage at both the node Vfilt and Vout, are pure DC.

[0005] The output voltage for this conventional interleaved forward voltage converter is:

$$Vout = (Vin/N) \cdot 2 \cdot D, \text{ for D less than 0.5} \quad \text{(equation 1)}$$

$$Vout = (Vin/N), \text{ for D greater than 0.5} \quad \text{(equation 2)}$$

where Vin is the input voltage, Vout is the output voltage, N is the turns ratio of the transformers, and D is the duty cycle for the transistors Q1 and Q2

[0006] Accordingly, if the duty cycle exceeds 50%, then the output voltage cannot increase.

SUMMARY

[0007] In described examples of an interleaved forward voltage converter, a first inverter stage includes a first transformer having a turns ratio N1 and a primary winding having one terminal coupled to a source of input voltage and another terminal coupled to a first switching transistor. A first secondary winding for the first transformer has a first terminal coupled to a first terminal of a filter inductor, and a second terminal coupled to a first diode. A second converter stage includes a second transformer having a turns ratio N2 and a primary winding having one terminal coupled to the source of input voltage and another terminal coupled to a second switching transistor. A second secondary winding for the second transformer has a first terminal coupled to the first terminal of the filter inductor through a second diode, and a second terminal coupled to a reference voltage source. A third diode is coupled between the first terminal of the second secondary winding for the second transformer and the second terminal of the first secondary winding of the first transformer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a schematic diagram of a prior art interleaved voltage converter.

[0009] FIG. 2 is a set of waveform graphs of the circuit of FIG. 1 at a 30% duty cycle.

[0010] FIG. 3 is a set of waveform graphs of the circuit of FIG. 1 at a 70% duty cycle.

[0011] FIG. 4 is a schematic diagram of an interleaved forward voltage converter of the example embodiments.

[0012] FIG. 5 is a set of waveform graphs of the circuit of FIG. 4 at a 30% duty cycle.

[0013] FIG. 6 is a set of waveform graphs of the circuit of FIG. 4 at a 70% duty cycle.

[0014] FIG. 7 is a schematic diagram of another interleaved forward voltage converter of the example embodiments.

[0015] FIG. 8 is a set of waveform graphs of the circuit of FIG. 7.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] FIG. 4 is a schematic diagram of an interleaved forward voltage converter 400 of the example embodiments. In FIG. 4, a first converter includes a first transformer T1 having a positive terminal of the primary winding 410 coupled to a source of input voltage Vin. The negative terminal of the primary winding 410 of transformer T1 is coupled to ground through transistor Q1. The gate of transistor Q1 is coupled to pulse generator 402. The secondary winding 412 of transformer T1 has its positive terminal connected to a first terminal of filter inductor at node Vfilt. The negative terminal of secondary winding 412 is connected to ground through diode Df1. A second converter includes transformer T2 having a positive terminal of primary winding 414 connected to the source of input voltage Vin. The negative terminal of primary winding 414 is coupled to ground through transistor Q2. The gate of transistor Q2 is coupled to pulse generator 406. The secondary winding 416 of transformer T2 has its positive terminal connected to the node Vfilt through diode Df2. A freewheeling diode Dfw is coupled from the node Vfilt to ground. A load, which is shown as resistor R_L, is coupled from the second terminal of the filter inductor Lf to ground. A third diode Ds connects the positive terminal of the secondary winding 416 of transformer T2 to the negative terminal of secondary winding 412 of transformer T1.

[0017] Operation of the circuit of FIG. 4 will now be explained in connection with FIGS. 5 and 6. FIG. 5 shows operation of the circuit of FIG. 4 at a 30% duty cycle. FIG. 6 shows operation of the circuit of FIG. 4 at a 70% duty cycle. Transistors Q1 and Q2 are switched 180° out of phase from each other, and output voltage regulation is performed by pulse width modulation (PWM) of the gate drive signals (not shown).

[0018] Comparing FIG. 5 with FIG. 2, the currents through transistors Q1 and Q2 are shown

separately in FIG. 2 and are shown combined in FIG. 5. However, in comparing FIGS. 2 and 5, the waveforms are identical. If the current through the freewheeling diode Dfw is examined in both FIGS. 2 and 5, they are identical. Similarly, the voltage Vfilt is identical in both FIGS. 2 and 5, as is the output voltage Vout. The diode Ds automatically places the two converters in series once the duty cycle exceeds 50%. Accordingly, the voltages produced by the two converters can add in series. The current through diode Ds is shown in FIG. 6 as I(Ds_p), which shows current flowing through the diode, except where only one transistor is conducting. The current through the freewheeling diode DFW is the same as shown in FIG. 3, and the voltage at the node Vfilt is a rectangular wave having a positive peak when both transistors Q1 and Q2 are conducting. The output voltage has ripple as shown in FIG. 2, but the voltage at 140 V is significantly higher than the voltage of 100 V that is produced by the prior art circuit of FIG. 1 with waveforms as shown in FIG. 3.

[0019] Another aspect of the example embodiments is shown in FIG. 7 generally as 700. The circuit of FIG. 7 can operate with either a series or parallel connected input, and either a series or parallel connected output to handle a much wider variation in input voltage. The circuit 700 can shift from one mode of operation to another on-the-fly. The circuit 700 has a first converter including a first transformer T1 having a primary winding 710, which has its positive terminal connected to a source of input voltage Vin. The negative terminal of primary winding 710 is coupled to ground through transistor Qp2 and coupled to the primary winding 714 of transformer T2 of the second converter through transistor Qs. The gate of transistor Qp2 is connected to pulse generator 704, and the gate of transistor Qs is connected to pulse generator 706. The secondary winding 712 of transformer T1 has a positive terminal connected to the first terminal of filter inductor LF at node Vfilt. The negative terminal of secondary winding 712 is coupled to ground the diode Df1. The second converter including transformer T2 has a primary winding 714 coupled to the source of input voltage Vin via transistor Qp1. The gate of transistor Qp1 is connected to pulse generator 702. The negative terminal of 714 is connected to ground. The secondary winding 716 of the second stage has a negative terminal connected to ground, and a positive terminal connected to the first terminal of filter inductor Lf through diode Df2. The positive terminal of secondary winding 716 of the second converter stage is coupled to the negative terminal of the secondary winding 712 of the first converter stage through a series connection of a diode Ds and a transistor Qsec. The gate of transistor Qsec is coupled to the gate

of transistor Qs through inverter 708. A freewheeling diode Dfw is coupled between ground and the first terminal of filter inductor Lf. A load, which is shown as a resistor Rl, is connected to the second terminal of filter inductor Lf.

[0020] The circuit of FIG. 7 can handle a greater variation in input voltage. If the input voltage is lower than a threshold, then the two primary windings 710, 714 of the transformers T1 and T2 can be connected in parallel. If the input voltage is higher than a threshold, then the two primary windings 710, 714 of the transformers T1 and T2 can be connected in series. If the primary windings 710, 714 are connected in parallel, the secondary windings 712, 716 of transformers T1 and T2 can be connected in series to obtain a voltage boost. Conversely, if the primary windings 710, 714 are connected in series, the secondary windings 712, 716 can be connected in parallel to reduce the output voltage. Operation of the circuit from one mode to another can be changed on-the-fly. Accordingly, greater flexibility in achieved for handling input voltage variations.

[0021] For connecting the primary winding 710, 714 in parallel, the two transistors Qp1 and Qp2 are used. Transistors Qp1 and Qp2 are switched 180° out of phase from each other, and output voltage regulation is performed by pulse width modulation (PWM) of the gate drive signals (not shown). The transistor Qs, which connects the primary windings 710, 714 in series, is turned off. The transistor Qsec has its gate connected to the gate of transistor Qs through inverter 708. Accordingly, with transistor Qs being OFF, transistor Qsec will be turned ON. When the duty cycle exceeds 50%, the secondary windings 712, 716 will be placed in series by the action of diode Ds and transistor Qsec. By having the primary windings 710, 714 connected in parallel and the secondary windings 712, 716, connected in series, a voltage boost will be obtained, thereby allowing the converter to operate with a lower input voltage.

[0022] For connecting the primary windings 710, 714 in series, transistor Qs is used. The output voltage is regulated by pulse width modulation (PWM) of the gate drive signal for transistor Qs (not shown). Transistors Qp1 and Qp2 are not used in this configuration. Accordingly, the two windings 710, 714 are in series between the voltage source and ground. The transistor Qsec has its gate connected to the gate of transistor Qs via inverter 708. Accordingly, with the transistor Qs being ON, transistors Qsec will be OFF, and the secondary windings 712, 716 will be in parallel through diodes Df1 and Df2. With the primary windings 710, 714 connected in series, and the secondary windings 712, 716 connected in parallel, a

voltage drop will occur at the output, thereby allowing the regulator to operate from a higher input voltage.

[0023] Both the primary windings and the secondary windings can be connected in parallel, or both the primary windings and the secondary windings can be connected in series (not shown), but this does not take advantage of changing the turns ratio of the converter to produce either a voltage boost or a voltage drop as discussed above.

[0024] FIG. 8 shows the waveforms for the circuit of FIG 7 where Qs is active. The top graph shows the respective currents I(Qp1) and I(Qp2) through transistors Qp1 and Qp2 are zero, because those transistors are not used when the primary windings are placed in series, as discussed above. The current I(Qs) through transistor Qs is shown in the second waveform at a duty cycle of 45%. As shown in the bottom waveform, a small ripple exists in the output voltage Vout.

[0025] During parallel operation, transistors Qp1 and Qp2 are active with the duty cycle between zero and Dmax. Dmax is the maximum duty cycle that will allow sufficient time for demagnetization of the transformer. Transistor Qsec is ON when both Qp1 and Qp2 are ON. The circuit reduces to an interleaved forward voltage converter with a transfer ratio of: $Vout = (Vin/N) \cdot 2 \cdot D$, where D is greater than zero and less than Dmax.

[0026] During series operation, transistor Qs has a duty cycle between zero and Dmax, and transistors Qp1 and Qp2 are OFF. The circuit reduces to a single forward converter with a DC transfer ratio of: $Vout = (Vin/N) \cdot D$ where D is between zero and Dmax.

[0027] Accordingly, in the example embodiments, the interleaved forward voltage converter has a greater flexibility in generating an output voltage.

[0028] In at least one example, a first inverter stage has a first transformer having a first secondary winding coupled to a filter inductor. A second converter stage has a second transformer having a second secondary winding coupled to the filter inductor. A diode is coupled between the first and second secondary windings to automatically connect the first and second secondary windings in series when a duty cycle of the converter exceeds 50%. An interleaved forward voltage converter can connect the two primary windings in either parallel or a series configuration. The two secondary windings can be connected in either parallel or a series configuration. Having the two primary windings in parallel and the two secondary windings in series allows the converter to operate with a lower input voltage. Having the two

primary windings in series and the two secondary windings in a parallel configuration allows the converter to operate with a higher input voltage.

[0029] In at least one version, a first converter stage includes a first transformer having a turn ratio N1 and a primary winding having one terminal coupled to a source of input voltage and another terminal coupled to a first switching transistor and a second switching transistor. A first secondary winding for the first transformer has a first terminal coupled to a first terminal of a filter inductor, and a second terminal coupled to a first diode and a third switching transistor. A second converter stage includes a second transformer having a turns ratio N2 and a primary winding having one terminal coupled to the source of input voltage and another terminal coupled to a reference voltage source. A second secondary winding for the second transformer has a first terminal coupled to the first terminal of the filter inductor to a second diode, and a second terminal coupled to the reference voltage source. The third transistor is coupled between the second terminal of the first secondary winding of the first transformer and the first terminal of the second secondary winding of the second transformer.

[0030] In at least one other version, a first inverter stage includes a first transformer that has a first secondary winding coupled to a filter inductor. A second converter stage includes a second transformer that has a second secondary winding coupled to the filter inductor. A diode is coupled between the first and second secondary windings to automatically connect the first and second secondary windings in series when a duty cycle of the converter exceeds 50%.

[0031] Also, the example embodiments include a method of operating an interleaved forward voltage converter to provide a series or parallel connection between the converters, including providing to transformers that each have a primary winding having a positive terminal coupled to a source of voltage, and that each have a secondary winding having a positive terminal coupled to one terminal of a filter inductor.

[0032] Parallel operation of the primary windings is alternatively provided by driving a first pair of transistors 180° out of phase with each other, one transistor being in series with a positive terminal of a first primary winding and other transistor being in series with the negative terminal of a second primary winding. Series operation of the primary windings is alternatively provided by driving a third transistor coupled between a negative terminal of the first primary winding and the positive terminal of the second primary winding. Parallel operation of the secondary windings is provided by coupling a negative terminal of the first secondary winding to a

reference potential through a first diode and coupling a positive terminal of the second secondary winding to the first terminal of the filter inductor through a second diode. Series operation of the secondary windings is alternatively provided by driving a fourth transistor between a negative terminal of the first secondary winding in the positive terminal of the second secondary winding.

[0033] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An interleaved forward voltage converter, comprising:

a first inverter stage including a first transformer having a turns ratio N and a primary winding having one terminal coupled to a source of input voltage and another terminal coupled to a first switching transistor;

a first secondary winding for the first transformer having a first terminal coupled to a first terminal of a filter inductor, and a second terminal coupled to a first diode;

a second converter stage including a second transformer having a turns ratio N and a primary winding having one terminal coupled to the source of input voltage and another terminal coupled to a second switching transistor;

a second secondary winding for the second transformer having a first terminal coupled to the first terminal of the filter inductor through a second diode, and a second terminal coupled to a reference voltage source;

a third diode coupled between the first terminal of the second secondary winding for the second transformer and the second terminal of the first secondary winding of the first transformer.

2. The converter of claim 1 further comprising a freewheeling diode coupled between the first terminal of the filter inductor and reference voltage source.

3. The converter of claim 2 wherein the first and second transistors are operated 180° out of phase from each other.

4. The converter of claim 1 wherein the first diode is coupled between the second terminal of the first secondary winding and the reference voltage source.

5. The converter of claim 3 wherein the first diode is coupled between the second terminal of the first secondary winding and the reference voltage source.

6. The converter of claim 1 wherein an anode of the first diode is coupled to a cathode of the second diode via the third diode.

7. The converter of claim 5 wherein an anode of the first diode is coupled to a cathode of the second diode via the third diode.

8. An interleaved forward voltage converter, comprising:

a first inverter stage having a first transformer having a first secondary winding coupled

to a filter inductor;

a second converter stage having a second transformer having a second secondary winding coupled to the filter inductor;

a diode coupled between the first and second secondary windings to automatically connect the first and second secondary windings in series when a duty cycle of the converter exceeds 50%.

9. The converter of claim 8 wherein the first and second transformers have first and second primary windings respectively, each switched to control current flow to the primary windings and each operated 180° out of phase with the other.

10. An interleaved forward voltage converter, comprising:

a first converter stage including a first transformer having a turns ratio N having a primary winding having one terminal coupled to a source of input voltage and another terminal coupled to a first switching transistor and a second switching transistor;

a first secondary winding for the first transformer having a first terminal coupled to a first terminal of a filter inductor, and a second terminal coupled to a first diode and a third switching transistor;

a second converter stage including a second transformer having a turns ratio N and having a primary winding having one terminal coupled to the source of input voltage and another terminal coupled to a reference voltage source;

a second secondary winding for the second transformer having a first terminal coupled to the first terminal of the filter inductor to a second diode, and a second terminal coupled to the reference voltage source;

wherein the third transistor being coupled between the second terminal of the first secondary winding of the first transformer and the first terminal of the second secondary winding of the second transformer.

11. The converter of claim 10 further comprising a freewheeling diode coupled between the first terminal of the filter inductor and the reference voltage source.

12. The converter of claim 10 further comprising a third diode coupled in series with the third transistor.

13. The converter of claim 10 further comprising a fourth switching transistor coupled between the source of input voltage and the one input terminal of the second primary winding.

14. The converter of claim 12 further comprising a fourth switching transistor coupled between the source of input voltage and the one input terminal of the second primary winding.

15. A method of operating an interleaved forward voltage converter so as to provide a series or parallel connection between the converters, the method comprising:

providing to transformers each having a primary winding having a positive terminal coupled to a source of voltage and each having a secondary winding having a positive terminal coupled to one terminal of a filter inductor;

providing parallel operation of the primary windings by driving a first pair of transistors 180° out of phase with each other, one transistor being in series with a positive terminal of a first primary winding and other transistor being in series with the negative terminal of a second primary winding;

alternatively providing series operation of the primary windings by driving a third transistor coupled between a negative terminal of the first primary winding and the positive terminal of the second primary winding;

providing parallel operation of the secondary windings by coupling a negative terminal of the first secondary winding to a reference potential through a first diode and coupling a positive terminal of the second secondary winding to the first terminal of the filter inductor through a second diode;

alternatively providing series operation of the secondary windings by driving a fourth transistor between a negative terminal of the first secondary winding in the positive terminal of the second secondary winding.

16. The method of claim 15 further comprising providing a diode series with the fourth transistor.

17. The method of claim 15 wherein the first pair of transistors is operated when the source of voltage is lower than a predetermined threshold.

18. The method of claim 15 wherein the third transistor operated when the source of input voltage is higher than a predetermined threshold.

19. The method of claim 17 wherein the fourth transistor is operated to increase in output voltage of the converter.

20. The method of claim 18 wherein the two secondary windings are connected in parallel.

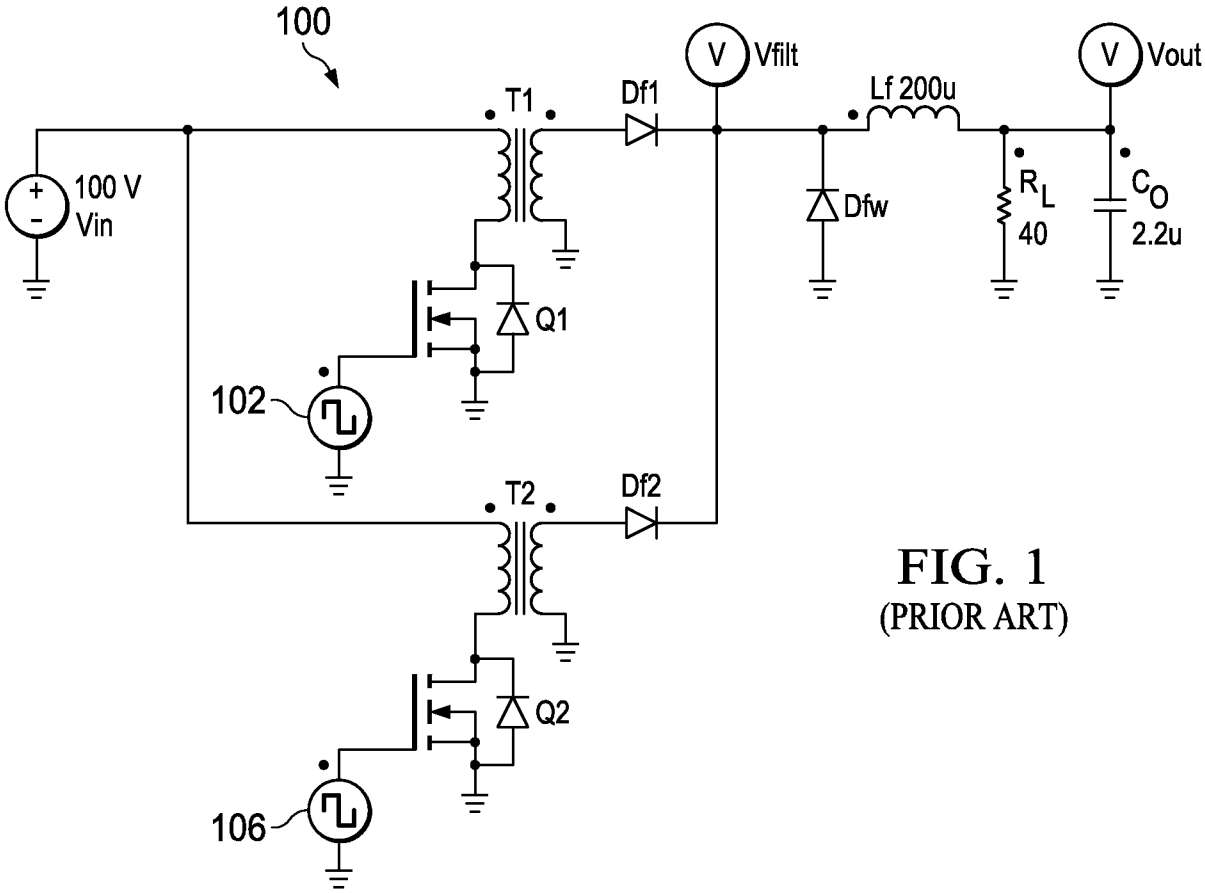


FIG. 1
(PRIOR ART)

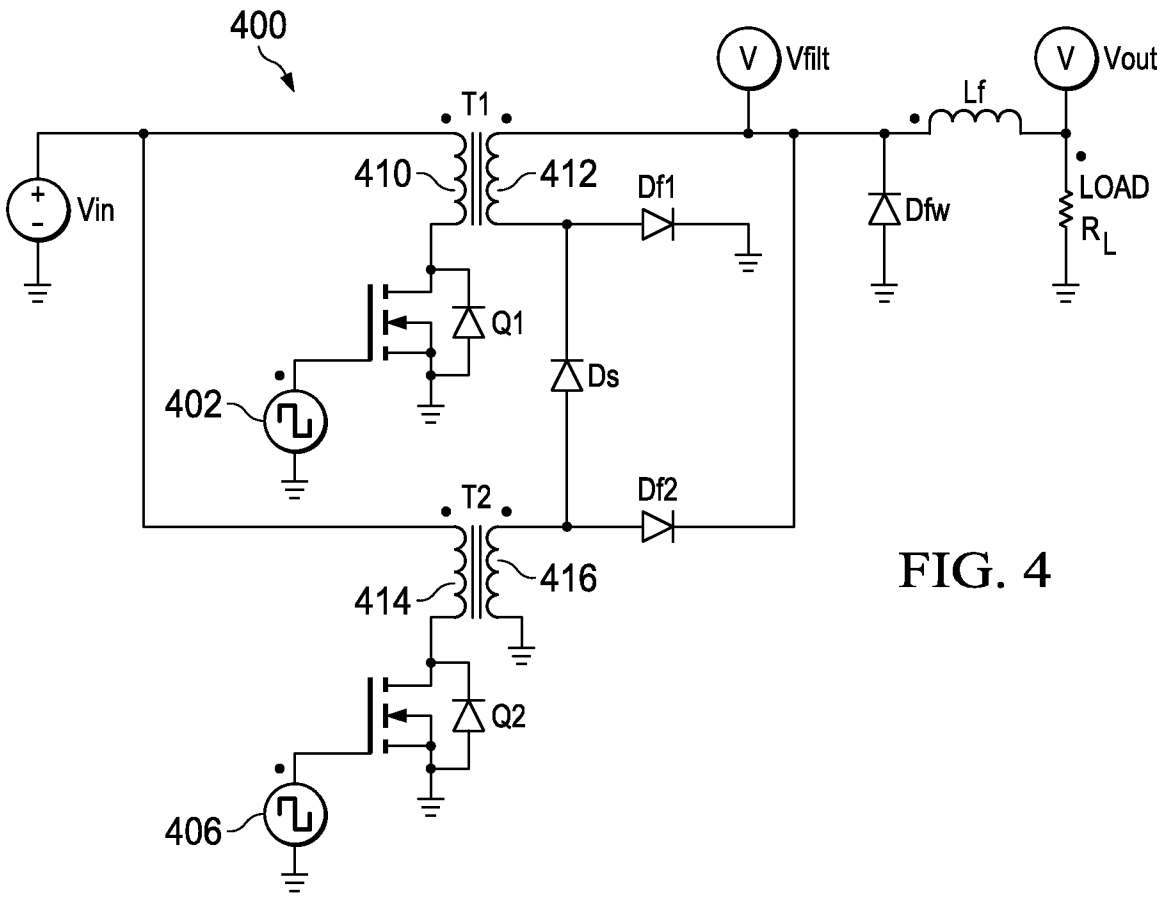


FIG. 4

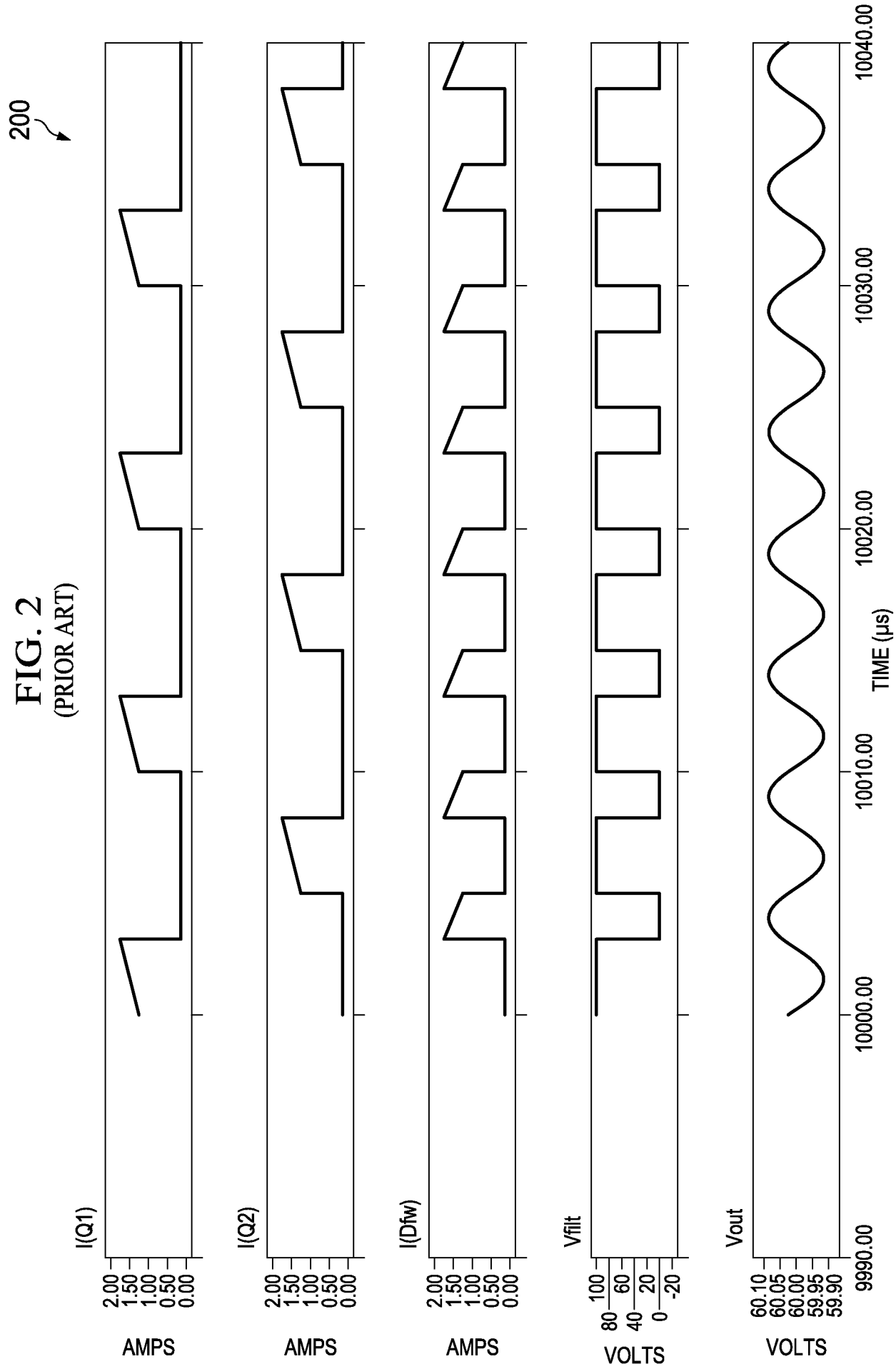
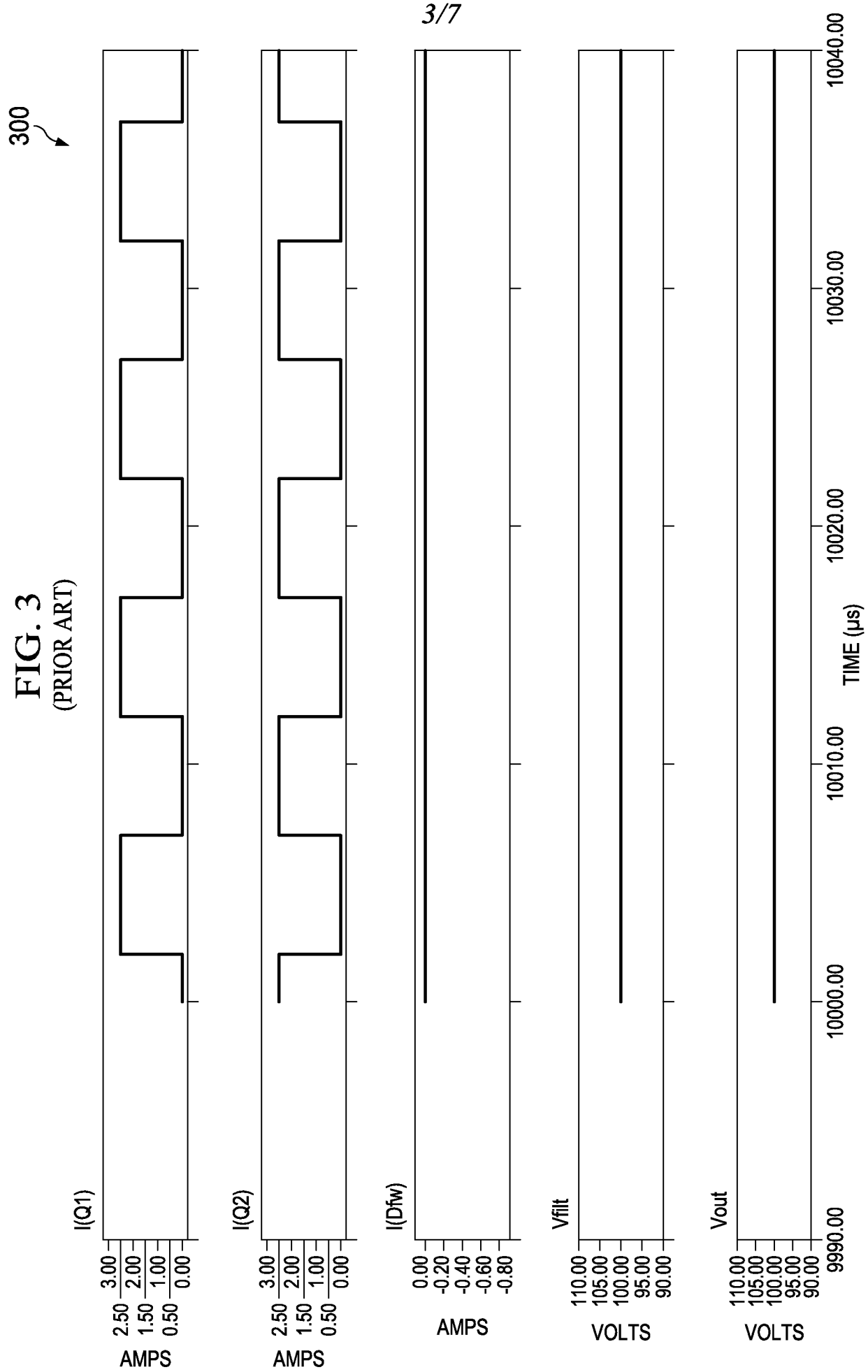
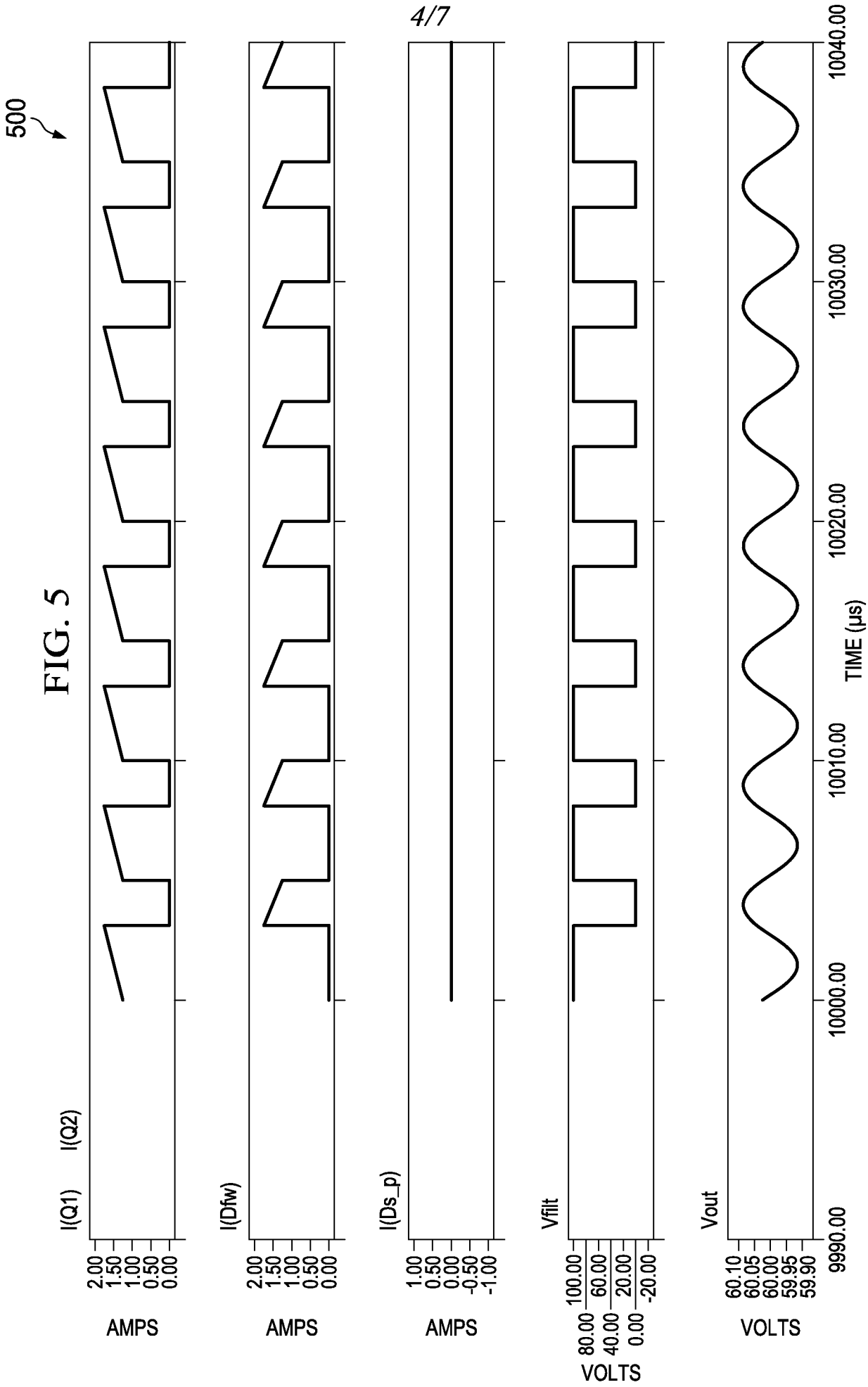


FIG. 2
(PRIOR ART)

FIG. 3
(PRIOR ART)




500
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I(Q2)
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AMPS
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0.00
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AMPS
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80.00
60.00
40.00
20.00
0.00
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VOLTS
Vout
60.10
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60.00
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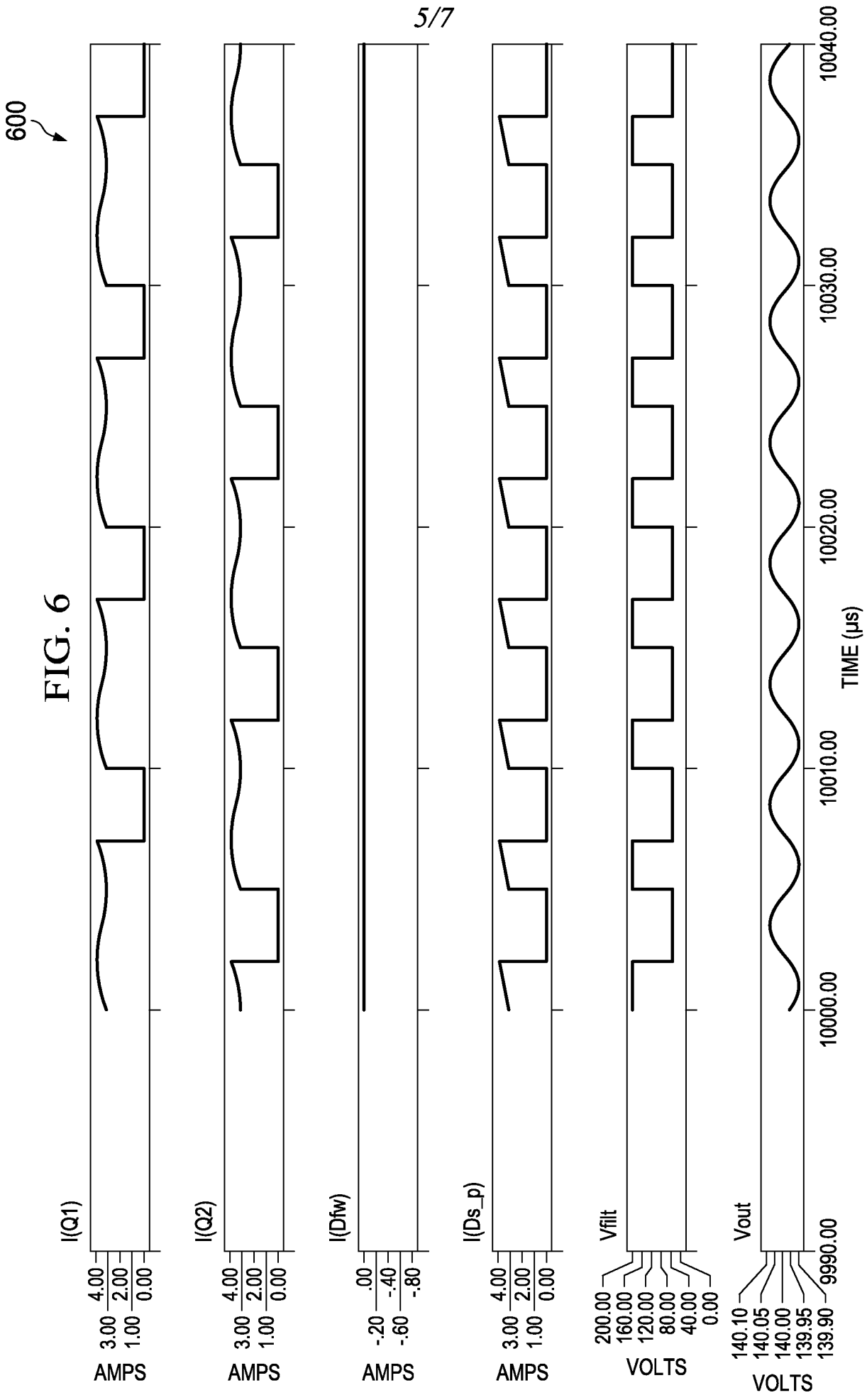
TIME (µs)

FIG. 5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AMPS
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VOLTS
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10000.00
10010.00
10020.00
10030.00
10040.00
TIME (µs)

FIG. 6

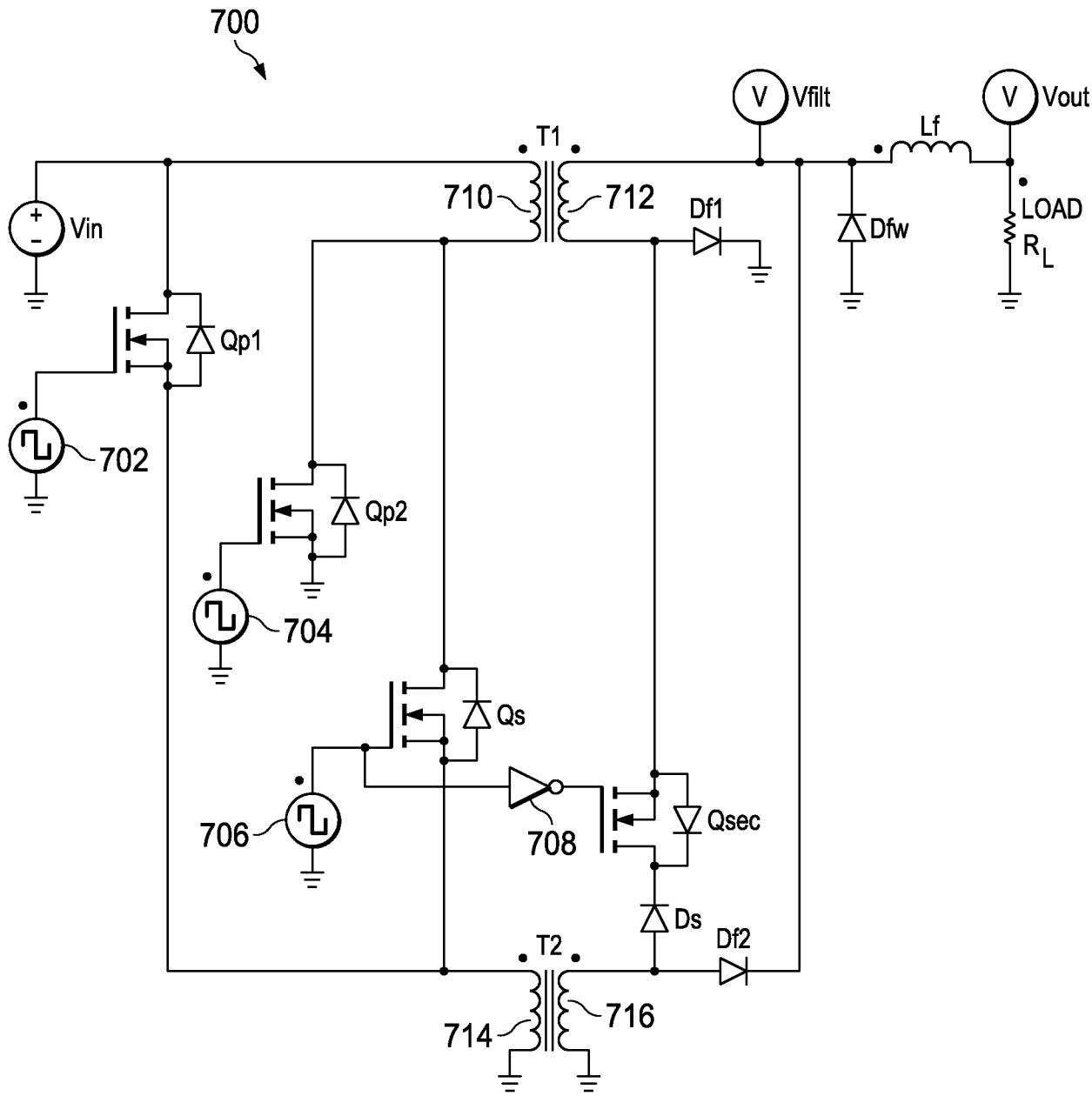
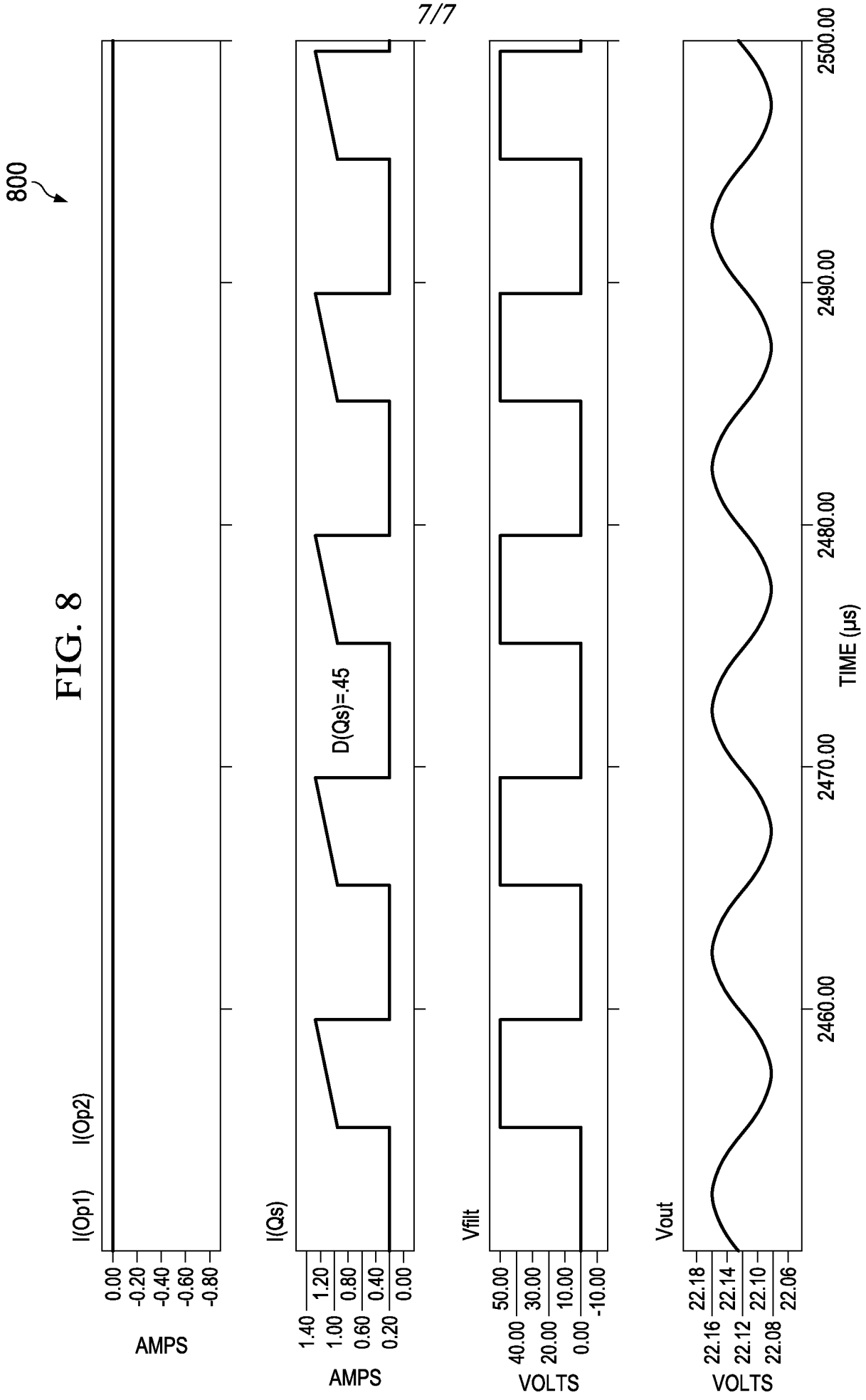

700
V
Vfilt
V
Vout
T1
Lf
710
712
Df1
Vin
Dfw
LOAD
R_L
Qp1
702
Qp2
704
Qs
706
708
Qsec
Ds
Df2
T2
714
716

FIG. 7

FIG. 8


800
I(Op1)
I(Op2)
0.00
-0.20
-0.40
-0.60
-0.80
AMPS
I(Qs)
D(Qs)=.45
1.40
1.20
1.00
0.80
0.60
0.40
0.20
0.00
AMPS
Vfilt
50.00
40.00
30.00
20.00
10.00
0.00
-10.00
VOLTS
Vout
22.18
22.16
22.14
22.12
22.10
22.08
22.06
VOLTS
2460.00
2470.00
2480.00
2490.00
2500.00
TIME (µs)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2014/057998

A. CLASSIFICATION OF SUBJECT MATTER

H02M 3/337 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 3/337, 3/335, 3/145-3/148

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TW 201338386 A (KUN SHAN UNIVERSITY) 16.09.2013	1-20
A	SU 1737667 A1 (RYAZANSKY RADIOTEKHNICHESKY INSTITUT) 30.05.1992	1-20
A	CN 101557172 A (NANJING UNIVERSITY OF AERONAUTICS AND ASTRONAUTICS) 14.10.2009	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 February 2015 (16.02.2015)	27 February 2015 (27.02.2015)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	I. Golovinova Telephone No. (499) 240-25-91