(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 August 2012 (30.08.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/116271 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2012/026479

(22) International Filing Date:
24 February 2012 (24.02.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/446,316 24 February 2011 (24.02.2011) US
13/353,431 19 January 2012 (19.01.2012) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier applications:
US 61/446,316 (CIP)
Filed on 24 February 2011 (24.02.2011)
US 13/353,431 (CIP)
Filed on 19 January 2012 (19.01.2012)

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: HIGH PIN COUNT NO-LEAD IC PACKAGES WITH HEAT-DISSIPATING PAD

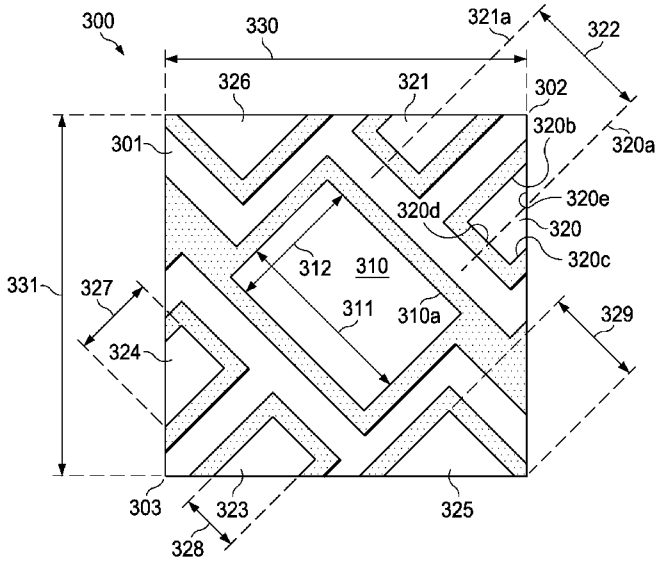

FIG. 3

(57) Abstract: A plastic no-lead integrated circuit package (300) suitable for high power applications has a pair of oblong metal pins (320, 321) exposed from a surface of the plastic (301), the pins straddling a corner (302) of the package; each pin has a long axis (320a, 321a), the long axes of the pair forming a non-orthogonal angle. Package (300) further includes a chip assembly pad (310), acting as a thermal spreader.

WO 2012/116271 A2

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

HIGH PIN COUNT NO-LEAD IC PACKAGES WITH HEAT-DISSIPATING PAD

[0001] This is related to semiconductor devices and processes and, more specifically, to structures and fabrication methods of small no-lead packages for integrated circuits (ICs) having high pin count and a pad for dissipating heat.

BACKGROUND

[0002] Plastic packages for semiconductor chips of many logic and analog integrated circuit families are often manufactured with pins arranged in the so-called Small Outline No-lead (SON) or Quad Flat No-lead (QFN) configuration. In these product categories, the no-lead packages do not have the traditional cantilevered metal leads, or pointed pins; instead, they have metallic terminals with surfaces flat with the surrounding plastic material so that these terminals can be conveniently connected (for instance by soldering) to contact pads of printed circuit boards (PCBs). The trend of the no-lead package technology is for shrinking the size of the packages.

[0003] Small no-lead package designs are constrained by the footprint of the package, the number of pins, and the process limitations as reflected by the layout rules of the leadframe. Leadframes in most SON or QFN no-lead packages, for example, have rectangle-shaped leads arranged in parallel along the four edges of the package, with one short side of the rectangle near the package edge and the long sides running between the edge and the center. Each lead has some portions of its perimeter half-etched in order to create locks for solid anchoring of the lead in the molding compound. If a chip pad can be accommodated, it usually has a rectangular shape with the four edges parallel to the four edges of the package. The polymeric compound of the plastic packages printed circuit board (PCB).

[0004] For many applications, such as handheld telephones, portable appliances, cameras, and medical equipments, the downscaling of the SON/QFN packages has so far reached an area of only 1 mm by 1 mm. One recently introduced SON/QFN package of this small size features a design with four leads shaped as triangles situated at the four corner locations and a chip pad with edges oriented at 45° with respect to the package edges. The chip pad doubles as thermal pad to spread the operational heat. Another recently introduced SON/QFN product of 1 mm by 1 mm area has six leads with the conventional rectangular shape arranged parallel along two

opposite edges of the package. In this product, each lead has a mold lock, which is formed as a half-etched extension of the lead; the extension is formed along the center line of the lead towards the package center. Near the package center, the mold locks of the leads positioned along one edge of the package come close to the mold locks of the respective leads positioned along the opposite package edge. As a consequence, the half-etched mold locks do not leave space for a chip pad; the chip is assembled on the half-etched lead mold locks by an electrically and thermally insulating layer of adhesive polymeric compound. In spite of the lack of chip pad and thus thermal pad, this product can handle power up to about 0.5 W.

SUMMARY

[0005] An analysis by the inventor of the general market trend for small plastic no-lead packages, such as SON/QFN packages with an area of 1 mm by 1 mm or less, found that the product applications call for packages with six terminals and power handling of at least 1 W. For logic and analog products, the semiconductor chips can be expected to have an area of at least 0.3 mm^2. The inventor realized that a power of 1 W or more requires a thermal pad, which can spread the operational heat, cool the junctions, and transfer the thermal energy to a heat sink.

[0006] Investigating potential structures of 1 mm by 1 mm SON/QFN packages suitable for at least 1 W power, the inventor discovered that for six-terminal packages the requirement for a large thermal pad can be satisfied for chips with an area of 0.3 mm^2 or more and widely different chip outlines (the aspect ratio of long and short edges), when the structure of the six terminals is coordinated with the chip edge outlines. In an example embodiment, where chips of about 0.3 mm^2 area have an elongated outline with an edge aspect ratio of about 3:1, as in Logic products, the preferred package terminal arrangement may be different from another example embodiment, where chips of about 0.3 mm^2 area have a more compact outline with an edge aspect ratio of about 3:2, as in analog products.

[0007] For elongated chips, the space needed for a thermal pad embedded in the 1 mm by 1mm area of the package can be created by grouping the six rectangle-shaped terminals in two sets of three terminals and aligning the sets along two opposite package edges. Each terminal has a long axis and a mold lock protruding

from the terminal, wherein the lock is shaped as an elongated beam oriented normal to the long axis. The beam of a terminal is interdigitated with a beam of an adjacent terminal. Preferably, two terminals of each set are placed in the package corners to maximize the space between terminals and their mold locks.

[0008] For compact chips, the space needed for a thermal pad embedded in the 1 mm by 1mm area of the package can be created by placing the terminals in the corners of the package and forming pairs of terminals straddling a corner; the terminals of these pairs may have oblong shape with the long axes forming a non-orthogonal angle. Preferably, the terminals of these pairs have trapezoidal shape and straddle a corner of the package. Each terminal has a long side and a parallel short side, a third end side distal from the corner, and a fourth side forming an obtuse angle with the short side and an acute angle with the long side; the long sides of the terminal pair are adjacent to each other. The package has a chip assembly pad, which acts as the thermal spreader. The third end sides of the terminal pair are adjacent and parallel to an edge of the thermal pad.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGS. 1 and 2 are side and bottom views respectively of a no-lead package with a pad for dissipating thermal energy.

[0010] FIG. 3 is a bottom view of another no-lead package with a pad for dissipating thermal energy.

[0011] FIG. 4 is a bottom view of yet another no-lead package with a pad for dissipating thermal energy.

[0012] FIG. 5 is a bottom view of yet another embodiment of no-lead package with a pad for dissipating thermal energy.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0013] FIG. 1 illustrates an example embodiment of a no-lead package generally designated 100. The example package is a miniature package encapsulated in a plastic polymeric material 110. The embodiment is classified as a plastic Small Outline No-lead (SON) package, also called a Quad Flat No-lead (QFN) package. The expression “no-lead” refers to the feature that the package terminals are not conventional cantilevered leads, but comprise flat metal pins 120.

[0014] It should be noted that herein, following widespread usage, package terminals 120 are referred to as "pins," despite the fact that they have a flat surface and do not resemble pointed objects such as nails. When a leadframe is used for an embodiment to assemble a semiconductor chip on the leadframe pad and connect the chip input/output terminals to the leadframe leads, those leads are herein also referred to as pins.

[0015] The metal pins may be coplanar with the surrounding plastic surface, or they may protrude a step 121 of about 0.05 mm from the plastic surface as shown in FIG. 1. In the examples of FIGS. 1 and 2, package 100 serves as a housing for semiconductor chips of the logic and analog device families. Inside the plastic encapsulation, yet not shown in FIG. 1, the semiconductor chip is assembled on a metallic leadframe with the chip input/output pads wire bonded to the package terminals. In the example embodiment, the width 130 of package 100 is 1.0 mm and the thickness 140 is in the range from 0.34 to 0.40 mm.

[0016] FIG. 2 indicates that sides 130 and 131 of the example package 100 have equal length so that package 100 is square-shaped; in example package 100 sides 130 and 131 are both 1.0 mm. Exposed from the surface of plastic material 110 of package 100 are six metal pins 120 and a metal pad 210 for assembling a semiconductor chip and serving as heat spreader. In the example of FIG. 2, the pins are grouped in two sets of three pins each. The pins of each set are arrayed, adjacent to each other, along an edge of the package so that the package corners are occupied by a pin. In order to equalize the distance between adjacent pins, the third pin of a set is preferably at mid-distance between the corner pins. As FIG. 2 shows, the two sets of pins are arrayed along opposite package edges.

[0017] In the example of FIG. 2, pins 120 have identical area and identical aspect ratios of their sides. In other embodiments, the pins may have different areas; they may also have different aspect ratios of their sides. While pins 120 are shown as having rectangular or square outline, in other embodiments the outline may be more general. In FIG. 2, width 122 of a pin 120 is in the range from about 0.14 to 0.20 mm, and is preferably about 0.20 mm. For a width of 0.20 mm, the space 220 between two adjacent pins is 0.20 mm, and the pin pitch 221 center-to-center is 0.40

mm. Compared to the conventional pin pitch center-to-center of 0.35 mm, pin pitch 221 is generous and thus supports efforts to increase board assembly yield. The space 220 separating adjacent leads has a center line 125.

[0018] The length of a pin is the linear dimension normal to the edge of the [package. Length 123 of a pin 120 is in the range from about 0.20 to 0.30 mm, dependent on the package area to be reserved for metal pad 210. For some embodiments belonging to the Logic product families, length 123 is preferably 0.20 mm in order to reserve maximum area for pad 210. In the direction normal to the package edge, a center line, or axis, 124 can be attributed to each pin 120.

[0019] As FIG. 2 illustrates, attached to each pin 120 is at least one metallic mold lock 223. A mold lock stabilizes the pin to which it is attached so that the pin cannot move in x-, y-, or z-direction; consequently, the pin is locked in all three dimensions. The outline of a mold lock is designed to prevent pin movements in the x- and y-dimensions; for preventing a movement in the z-direction, the metal sheet is locally thinned by partial etching so that molding compound can cover the lock area during the encapsulation process; the hardened compound inhibits a pin movement in the z-direction. Partially etched leadframe portions, such as the mold locks, are commonly referred to as half-etched leadframe portions. The half-etched mold locks 223 are hidden under the molding compound 110 and are thus depicted by dashed outlines.

[0020] As a preferred design, FIG. 2 illustrates mold locks 223 shaped as elongated beams oriented normal to the pin axis; furthermore, each beam is interdigitated with a beam of an adjacent pin. Interdigitated beams are defined herein as beams protruding from adjacent pins and reaching to the center line 125 of the space separating adjacent pins; preferably, a beam reaches across the center line 125. In preferred lock designs, a beam 223 protrudes from pin 120 at normal angle from the pin axis 124. Each beam-like mold lock may exhibit hook-like features 224 for locking against pin displacements in x- and y-directions. With interdigitated beam-like mold locks 223 providing strong locking for pins 120, there is no need for additional half-etched mold locks shaped as frames for pin widths 122, as they are

frequently employed in conventional technology towards the center of the package area.

[0021] The space thus freed up in the center portion of the package area is used to accommodate metal pad 210, operable for assembling a semiconductor chip on the inside of the package, and for spreading operational heat from the chip into the PCB outside of the package. In the example embodiment of FIG. 2, length 211 of the pad 210 portion exposed from the plastic 110 measures approximately 0.75 mm, and width 212 of the pad 210 portion exposed from the plastic 110 measures about 0.2 mm. A metal pad with an area between 0.15 and 0.25 mm^2 can handle a power of 1 W and spread the operational heat, cool the chip junctions, and transfer the thermal energy to a heat sink in the PCB.

[0022] As FIG. 2 indicates, pad 210 also includes a frame of half-etched metal surrounding the exposed metal portion in order to create mold locks for the pad. The width of the half-etched frame is between 0.06 and 0.08 mm, leaving a width between about 0.05 and 0.07 mm for the encapsulation compound. Since the metal pad inside the package available for attaching a semiconductor chip can make full use of the whole pad (exposed and half-etched portions), pad 210 is well suited to be the assembly pad for chips of the Logic and related product families. Chips of these product families have an area of approximately 0.3 mm^2 and an edge aspect ratio of about 3:1. In the example of FIG. 2, the distance 213 between the exposed metal of a pin 120 and pad 211 is about 0.2 mm, a safe distance for preventing failure by solder shorting during PCB attachment.

[0023] Illustrating another example embodiment, generally designated 300, FIG. 3 shows the bottom view of a miniature package encapsulated in a plastic polymeric material 301. The embodiment is classified as a plastic SON/QFN package, with terminals shaped as flat metal pins, preferably coplanar with the surrounding plastic surface. The package has a thickness between about 0.3 and 0.4 mm. Inside the plastic encapsulation, yet not shown in FIG. 3, a semiconductor chip is assembled on a metallic leadframe with the chip input/output pads wire bonded to the package terminals. Outside the plastic encapsulation, the chip assembly pad has a surface 310 exposed from the surface of the plastic compound 301; this exposed

surface has a length 311 between about 0.50 and 0.54 mm, preferably 0.52 mm, and a width 312 between about 0.370 and 0.380 mm, preferably 0.374 mm. A metal pad with an area between 0.15 and 0.25 mm^2 can handle a power of 1 W and spread the operational heat, cool the chip junctions, and transfer the thermal energy to a heat sink in the PCB.

[0024] In addition, pad portions of a width between about 0.06 and 0.08 mm are half-etched for creating mold locks for pad 310. Since the metal pad inside the package available for attaching a semiconductor chip can make full use of the whole pad (exposed and half-etched portions), pad 310 is well suited to be the assembly pad for chips of the analog and related product families. Chips of these product families have an area of approximately 0.3 mm^2 and an edge aspect ratio of about 3:2.

[0025] FIG. 3 indicates that sides 330 and 331 of the example package 300 have equal length so that package 300 is square-shaped; in the example package 300, sides 330 and 131 are both 1.0 mm. Exposed from the surface of plastic material 301 of package 300 are six metal pins and the metal pad 310; the exposure allows pad 310 to serve as heat spreader. The metal pins and the metal pad have half-etched metal portions serving as mold locks; since these half-etched portions are hidden under plastic compound 301, they are shaded in FIG. 3.

[0026] The package of example embodiment of FIG. 3 exhibits a pair of oblong metal pins 320 and 321, which is positioned to straddle a corner 302 of the package. In the opposite package corner 303 is an analogous pair of oblong metal pins straddling that corner. Each pin has a long axis; for pin 320, the long axis is designated 320a, for pin 321, the long axis is designated 321a. The long axes of a pin pair form a non-orthogonal angle; in the embodiment of FIG. 3, the angle is zero, which means, long axes 320a and 321a are parallel to each other. In FIG. 3, the pitch 322 of the long axes, which is the pitch of pins 320 and 321 center-to-center, is 0.35 mm; consequently, it today's design rules for pin pitch are satisfied.

[0027] In FIG. 3, the oblong pins 320 and 321 forming a pair and straddling a corner may have the shape of trapezoids. Considering the metal areas exposed from the plastic compound, each pin, for example pin 320, has a long side 320b and a parallel short side 320c; further it has a third end side 320d, which is distal from

corner 302, and a fourth side 320e that forms an obtuse angle with respect to short side 320c and an acute angle with respect to long side 320b. The long sides (such as 320b) of the pin pair may be adjacent to each other, and the third end sides (such as 320d) of the pin pair may be adjacent to and parallel with an edge 310a of chip pad 310.

[0028] The example package of FIG. 3 has a second pair of pins (323 and 324) that is placed near second corner 303 diagonal to the first corner 302. The second pair of pins is symmetrical to the first pair (320 and 321) of pins with respect to the center point of the package surface. Alternatively, in other embodiments these placement and symmetry arrangements for pins and pad may be more random in order to exactly conform with customized chip and PCB layouts.

[0029] The example package of FIG. 3 has a fifth pin 325 and a sixth pin 326. The may have isosceles triangular shape and may be placed near or into the remaining two corners of the package. In FIG. 3, the base of the triangle is placed parallel to an edge of the package. In other embodiments (see for instance FIGs. 4 and 5), the apex of each triangular pin is placed adjacent to on of the two remaining corners of the package.

[0030] Fig. 3 displays a plurality of dimensions of exposed metal objects within the guidelines of presently accepted 0.35 mm pitch design rules, which require the spacing between two metallic 0.17 mm pins to be no less than 0.18 mm. Long sides 320b of the trapezoidal pins have a length 327 of about 0.35 mm; third end sides 320d of the trapezoidal pins have a length 328 of about 0.17 mm; and the equal sides of the isosceles triangles 325 and 326 have a length 329 between about 0.25 and 0.26 mm, preferably 0.254 mm. These exposed metal objects are framed by mold locks between 0.06 and 0.08 mm wide and hidden under the encapsulation compound; the mold lock portions are shaded in FIG. 3.

[0031] Another embodiment of a square-shaped 1 mm by 1 mm plastic SON/QFN package, suitable for a power of at least 1 W and for chips with an edge aspect ratios of approximately 3:2, and designed for six pins, is shown in FIG. 4. Package side length 430 is 1.00 mm. The bottom view illustrates that the package, generally designated 400, has a large thermal pad 410 (length 411 exposed from

polymeric encapsulation compound 401 is about 0.725 mm and width 412 is about 0.50 mm) operable for assembling a semiconductor chip on the inside of the package, and for spreading operational heat from the chip into the PCB outside of the package. Metal pad 410 with an area of more than 0.36 mm^2 can handle a power of 1 W and spread the operational heat, cool the chip junctions, and transfer the thermal energy to a heat sink in the PCB.

[0032] In this example, two pairs of trapezoidal-shaped pins 420 straddle diagonally opposed package corners, similar to the package of FIG. 3. The long sides 420b of the trapezoidal pins are parallel to each other so that the design rule of 0.35 mm for the pin pitch 422 center-to-center is satisfied, with the pins being 0.18 mm wide and the spacing between the pins being no less than 0.17 mm. The fifth and sixth pins are shaped as isosceles triangles 425; the apex 425a of each triangular pin is placed adjacent to one of the two remaining corners of the package.

[0033] As a more general alternative to the trapezoidal shape of the pins in FIG. 4, a plastic SON/QFN package may have a pair of oblong metal pins exposed from a surface of the plastic, wherein the pins straddle a corner of the package. Each pin has a long axis, and the axes of the pair form a non-orthogonal angle.

[0034] In the preferred embodiment, the leadframe features (pad, pins) are half-etched to form mold locks for enhancing adhesion between the encapsulation compound and pad and pins, analogous to FIG. 3. With half-etched mold locks, the exposed side of the pins and of the chip pad shown in FIG. 4 may have different surface shapes and a smaller surface area compared to the corresponding opposite side. The smaller surface areas on the exposed side of the package may facilitate more flexible PCB trace placement.

[0035] With six pins and a chip pad, the packaged semiconductor device may have six input/output and power pins; furthermore, the backside of the semiconductor chip may be additionally biased to a separate voltage during operation. This capability offers flexibility to device applications. Generally, it is preferable that the size of the chip pad is larger than the size of the semiconductor chip that is affixed to it. One reason for this preference is that it eliminates the potential shorting of the chip to any of the pins. Another reason is that overhanging the chip over the edges of

the chip pad will cause stress on the chip during temperature excursion, which may degrade the device performance with the possibility of chip cracking at extreme operating conditions.

[0036] Yet another embodiment of a square-shaped 1 mm by 1 mm plastic SON/QFN package is illustrated in FIG. 5, wherein the package is suitable for a power of at least 1 W and for chips with an edge aspect ratios of approximately 3:2 and designed for six pins. Package side length 530 is 1.00 mm. The bottom view illustrates that the package, generally designated 500, exposes a large thermal pad 510 (length 511 exposed from polymeric encapsulation compound 501 is about 0.62 mm and width 512 is about 0.43 mm) operable for assembling a semiconductor chip on the inside of the package, and for spreading operational heat from the chip into the PCB outside of the package. Metal pad 510 with an area of more than 0.27 mm^2 can handle a power of 1 W and spread the operational heat, cool the chip junctions, and transfer the thermal energy to a heat sink in the PCB.

[0037] In example embodiment 500, two pairs of pins 520 straddle diagonally opposed package corners. Pins 520 have the shape of isosceles triangles with a side length 520b measuring about 0.20 mm. Sides 520b of the pins are parallel to each other and are separated by a space 502 of about 0.20 mm, so that the design rule of 0.35 mm for the pin pitch 522 center-to-center is satisfied. With the geometries quoted, the distance 521 is about 0.60 mm. The fifth and sixth pins are shaped as isosceles triangles 525; the apex 525a of each triangular pin is placed adjacent to one of the two remaining corners of the package. The long side 526 of isosceles triangle 525 is about 0.4 mm.

[0038] Alternatively, plastic SON/QFN packages may have a pair of metal pins exposed from a surface of the plastic so that the pins straddle a corner of the package; in addition, each pin has an axis so that the axes of the pin pair straddle the corner and form a non-orthogonal angle.

[0039] It is preferred that the leadframe features (pad, pins) of the embodiment depicted in FIG. 5 are half-etched to form mold locks for enhancing adhesion between the encapsulation compound and pad and pins, analogous to FIG. 3. With half-etched mold locks, the exposed side of the pins and of the chip pad

shown in FIG. 4 may have different surface shapes and a smaller surface area compared to the corresponding opposite side.

[0040] While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the invention applies not only to SON/QFN packages with side lengths of 1 by 1 mm, but to packages with scaled dimensions, especially to packages with smaller side lengths.

[0041] As another example, the concept of a small plastic SON/QFN package with six pins and a thermal pad for high power operation can be applied to packages, which are rectangular-shaped instead of square-shaped.

[0042] In yet another example, the material and the thickness of the metal leadframe can be selected as a function of the size of the chip so that specific product goals of the assembled package can be achieved such as final thickness, mechanical strength, minimum warpage, prevention of cracking, strong symbolization contrast, compatibility with pick-and-place machines, and minimum electrical parasitics. In addition, the starting metal of the plate may be roughened, or plated with metal layers (such as nickel, palladium, gold, and tin), to improve adhesion to polymeric compounds and solderablity to PCBs.

[0043] Those skilled in the art will appreciate that modifications may be made to the described embodiments and that many other embodiments are possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A plastic no-lead integrated circuit package, comprising:

a first pair of elongated conductive pins exposed from a surface of the plastic, the pins straddling a corner of the package; and

each pin having a long axis, the long axes of the pair forming a non-orthogonal angle.

2. The package of Claim 1, wherein the first pair of elongated pins is a pair of trapezoidal pins.

3. The package of Claim 2, wherein each trapezoidal pin has parallel long and short side, a third side distal from the corner, and a fourth side forming an obtuse angle with the short side and an acute angle with the long side.

4. The package of Claim 3, wherein the long sides of the pin pair are adjacent to each other.

5. The package of Claim 4, further including a chip assembly pad acting as thermal spreader.

6. The package of Claim 5, wherein the third end sides of the first pin pair are adjacent to and parallel with an edge of the chip pad.

7. The package of Claim 6, further including a second pair of oblong metal pins straddling another corner.

8. The package of Claim 7, further including two additional metal pins.

9. A plastic no-lead integrated circuit package, comprising:

metal pins exposed from a surface of the plastic, the pins arrayed along opposite edges of the package, the package corners occupied by pins; and

each pin having an axis and a mold lock protruding from the pin, the lock shaped as an elongated beam oriented normal to the axis, the beam interdigitated with a beam of an adjacent pin.

10. The package of Claim 9, wherein the interdigitating beams extend across the center line of the space between adjacent pins.

11. The package of Claim 10, wherein the metal pins include six pins.

12. The package of Claim 11, further including a chip assembly pad acting as thermal spreader.

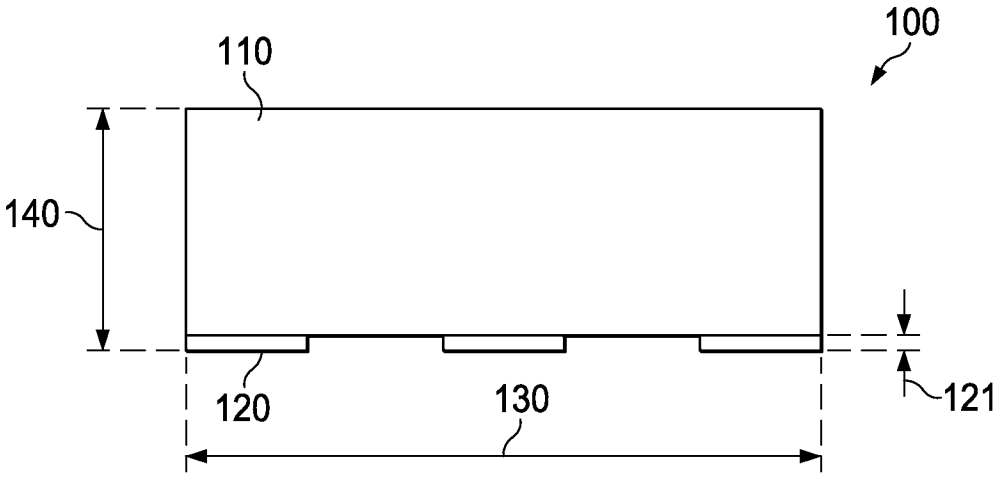
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FIG. 1

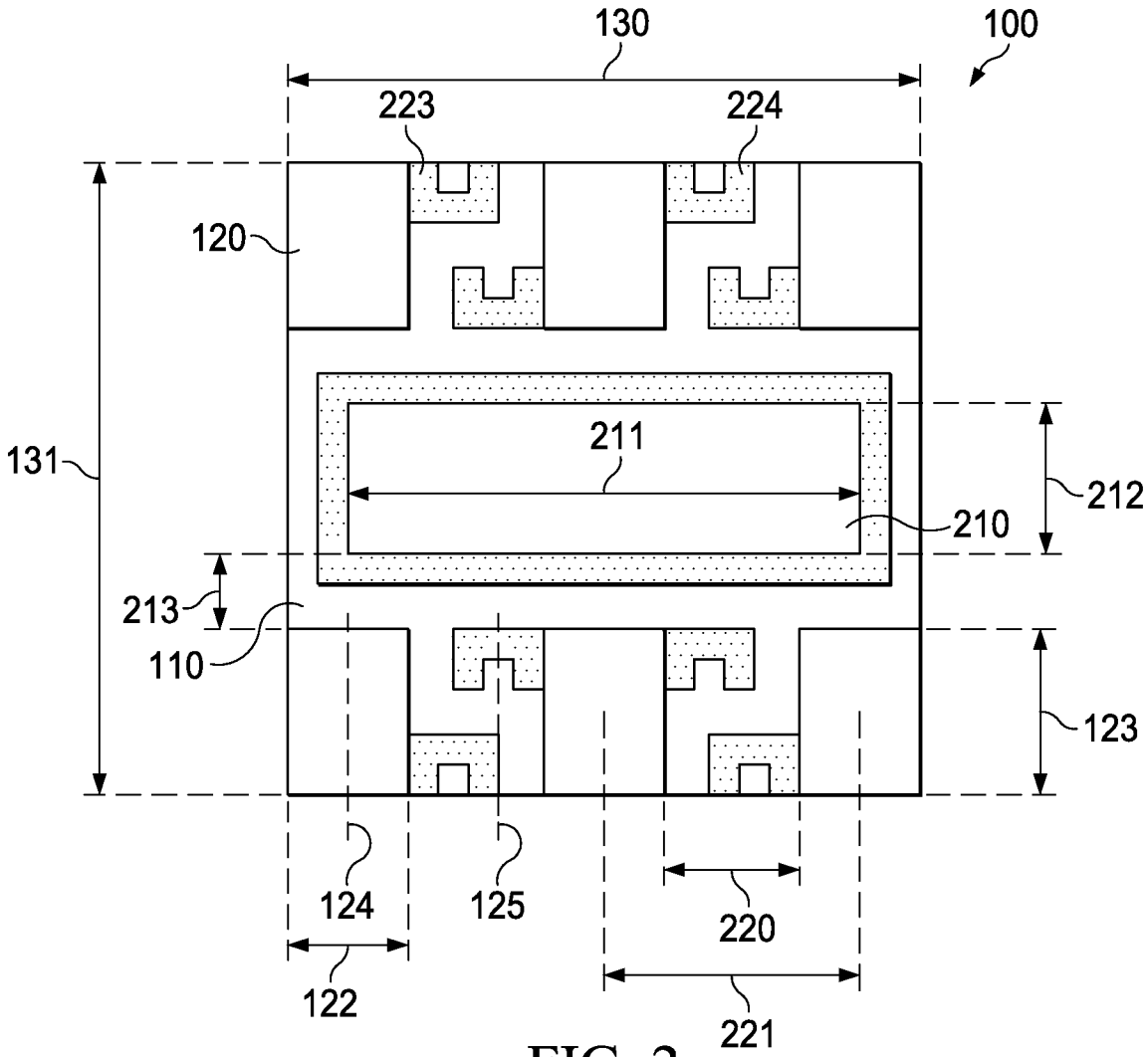
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FIG. 2

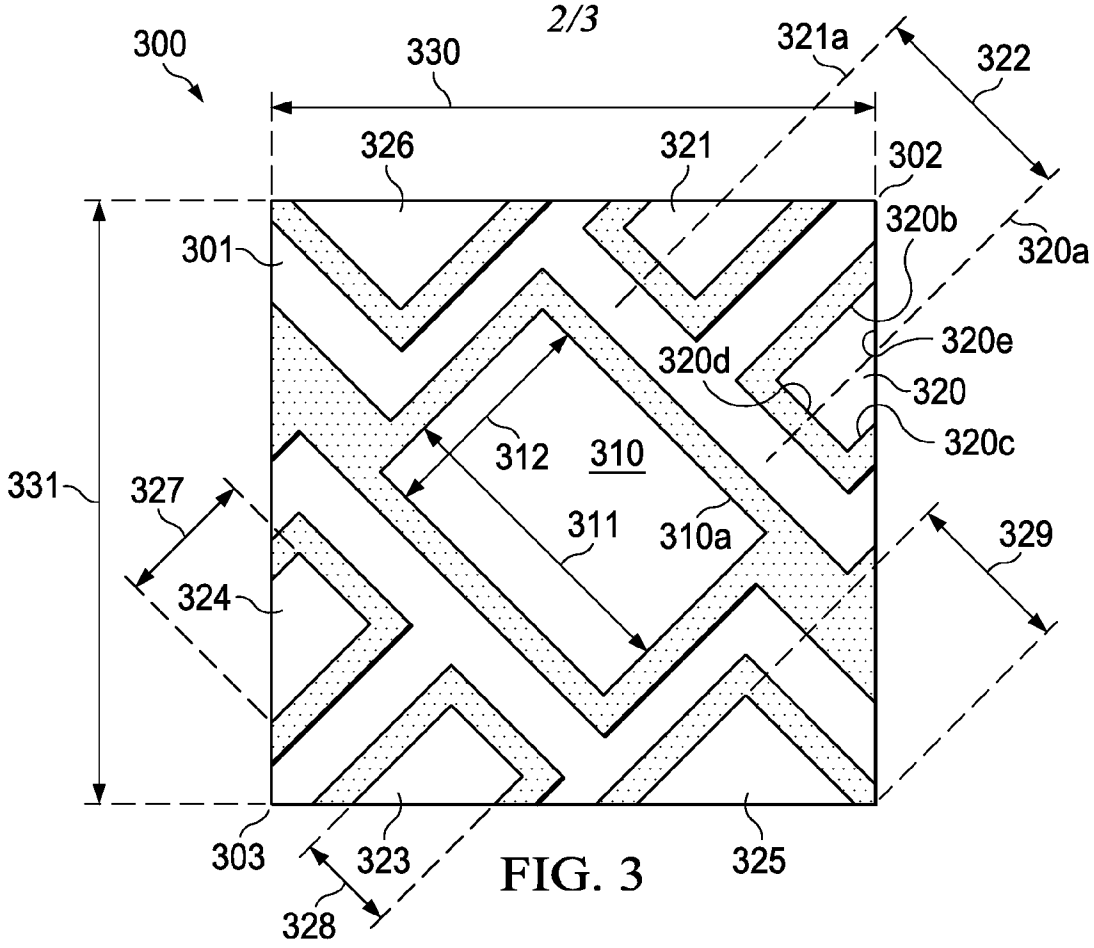
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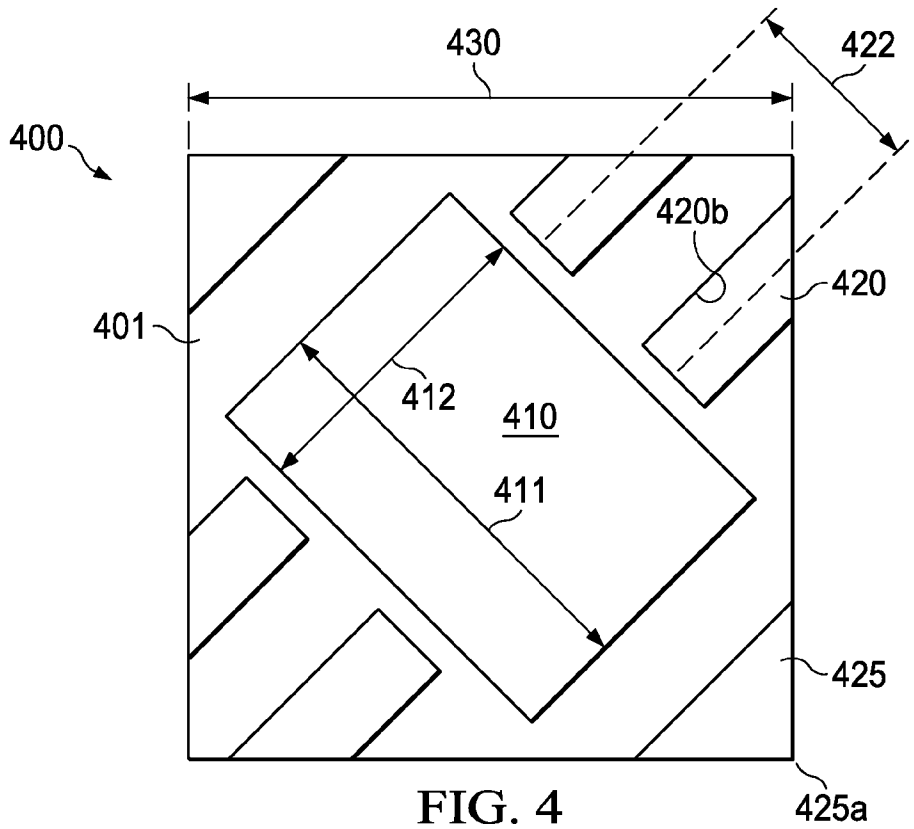
FIG. 3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410
411
425
425a

FIG. 4

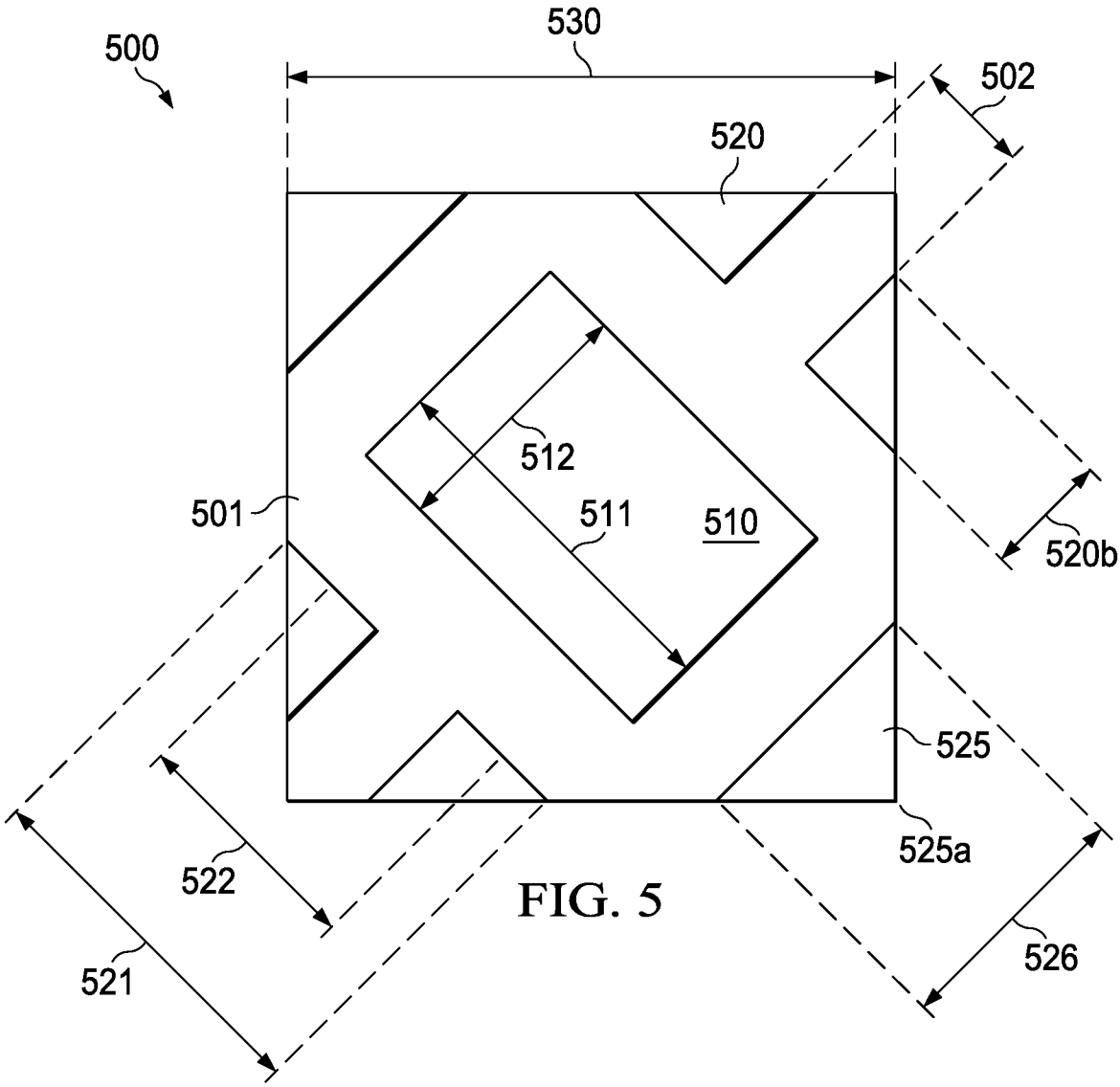

FIG. 5