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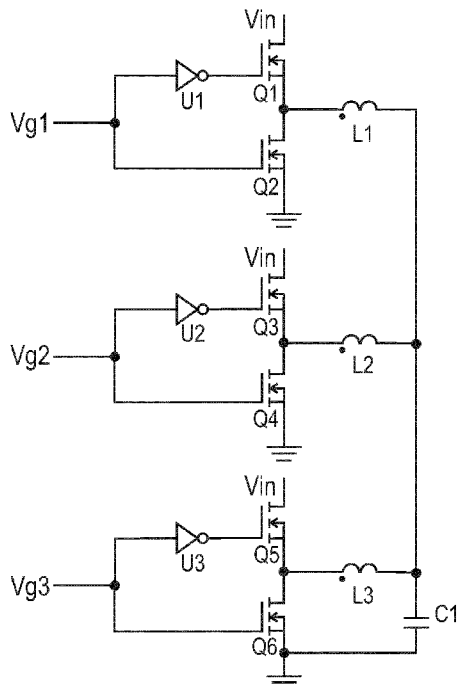
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(54) Title: MULTI-PHASE SWITCHED POWER CONVERTER

Fig. 1



prior art  
L1 = L2 = L3  
Q1 = Q3 = Q5  
Q2 = Q4 = Q6

present invention  
L1 = L2 ≠ L3  
Q1 = Q3 ≠ Q5  
Q2 = Q4 ≠ Q6

or

L1 ≠ L2 ≠ L3  
Q1 ≠ Q3 ≠ Q5  
Q2 ≠ Q4 ≠ Q6

(57) Abstract: A multi-phase power converter comprising a plurality of phases for generating an output voltage according to a switching signal and an input voltage, each phase of the plurality of phases comprising a switching element and inductance; wherein the plurality of phases is connected to a common star point, wherein an output capacitor is connected to the common star point. The phases of the multi-phase power converter are not identical in terms of their inductance. Therefore, at least one phase may be optimized for a low current such that, in low power operation, said at least one phase is optimal for lower current levels.

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## Multi-phase switched power converter

### FIELD OF THE INVENTION

The present disclosure relates to a multi-phase switched power converter.

### 5 BACKGROUND OF THE INVENTION

Contemporary designs of a power converter are chosen to meet specified performance requirements, such as high efficiency, accurate output regulation, fast transient response, low solution cost, etc. A power converter generates an output  
10 voltage and current for a load from a given input voltage. It needs to meet the current regulation or load voltage requirement during steady-state and transient conditions. Depending on the specific application, a multi-phase switched power converter may be an appropriate solution.

15 Generally, a switched power converter works by taking small chunks of energy, bit by bit, from an input voltage source, and moving them to the output. This is accomplished by means of an electrical switch and a controller which controls the rate at which energy is transferred to the output.

20 Switched power converters comprise a switchable power stage, wherein an output voltage is generated according to a switching signal and an input voltage. The switching signal is generated by a controller that adjusts the output voltage to a reference voltage. The switched power stage comprises a dual  
25 switch consisting of a high-side switch and a low-side switch an inductance and a capacitor. During a charge phase, the high-side switch is turned on and the low-side switch is turned off by the switching signal to charge the capacitor. During a discharge phase the high-side switch is turned off  
30 and the low-side switch is turned on to match the average inductor current to the load current. The switching signal is

generated as digital pulse width modulation signal with a duty cycle determined by a control law.

Switched power converters must operate over a wide range of load conditions. Buck and boost derived converters may have  
5 more than one phase for high current applications. A phase comprises a dual switching element and inductor. A plurality of identical phases is connected to a common star point to charge or discharge a common output capacitor.

In many applications, the power converter can operate at a  
10 current substantially less than the peak current and even less than the peak current for a single phase. Thus, having identical phases and current capability for each phase may not be optimal.

#### 15 BRIEF SUMMARY OF THE INVENTION

A multi-phase power converter, substantially as shown in and/or described in connection with at least one of the figures, as set forth more completely in the claims.

The phases of the multi-phase power converter are not  
20 identical in terms of their inductance. Therefore, at least one phase may be optimized for a low current such that, in low power operation, said at least one phase is optimal for lower current levels.

Moreover, the switching elements may be optimized for each  
25 phase since an optimal switching device selection depends on the operating current of that phase.

These and other advantages, aspects and novel features of the present disclosure, as well as details of an illustrated embodiment thereof, will be more fully understood from the  
30 following description and drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

Reference will be made to the accompanying drawing, wherein:

Fig. 1 shows a block-diagram of multi-phase power converter.

## 5 DETAILED DESCRIPTION OF THE INVENTION

The multi-phase power converter shown in Fig. 1 comprises three phases controlled by switching signals  $V_{g1}$ ,  $V_{g2}$ ,  $V_{g3}$  for generating an output current or voltage according to input voltage  $V_{in}$  and the switching signals.

- 10 The first phase comprises a dual switching element comprising an inverter U1 a high-side field effect transistor (FET) Q1 and a low-side FET Q2, and an inductance L1. The second phase comprises a dual switching element comprising an inverter U2 a high-side FET Q3 and a low-side FET Q4, and an inductance L2.
- 15 The third phase comprises a dual switching element comprising an inverter U3 a high-side FET Q5 and a low-side FET Q6, and an inductance L3.

The three phases are connected to a common star point to which the capacitor C1 is connected to. Each phase produces its own  
20 operating current for charging the capacitor C1.

While in the prior art the inductance L1, L2 and L3 are equal and the FETs Q1, Q2, Q3, Q4, Q5 and Q6 are identical, according to the present invention the inductance of at least one phase differs from the inductance of another phase. At  
25 least one phase may be optimized for a low current such that, in low power operation, said at least one phase is optimal for lower current levels.

For example, the third phase may be optimized for lower current levels. L1 equals L2, but L3 differs from L1 and L2.

Optimally, the inductance L3 may be selected such that the ripple current is 20% - 40% of the peak current value. For fixed input and output voltage, to first order, the ripple current is proportional to the inverse of the inductance.

5 Moreover, the dual switching elements may be optimized for each phase since an optimal switching device selection depends on the operating current of that phase. Switching elements Q5 and Q6 may be optimized with respect to their size and cost for example, for the operating current of the third phase. Q1  
10 may be identical to Q3, but Q5 may be different from Q1 and Q3. Q2 may be identical to Q4, but Q6 may be different from Q2 and Q4.

The inductance of each of the plurality of phases may be different from the inductance of another phase. Hence, each  
15 phase may be optimized for its individual operating current.

Also, the switching element of each of the plurality of phases may be different from the inductance of another phase.

The three-phase buck converter is just an example. The concept of optimized inductances and switching elements for the load  
20 conditions of an individual phase may be applied to any buck or boost converter design.

What is claimed is:

1. Multi-phase power converter comprising a plurality of phases for generating an output voltage according to a switching signal and an input voltage, each phase of the plurality of phases comprising a switching element and inductance; wherein the plurality of phases is connected to a common star point, wherein an output capacitor is connected to the common star point; and wherein the inductance of at least one phase differs from the inductance of another phase.
2. The multi-phase power converter according to claim 1, wherein the inductance is anti-proportional to a ripple inductor current.
3. The multi-phase power converter according to claim 2, wherein the inductance of the at least one phase is selected such that the ripple operating current is 20% - 40% of a peak current.
4. The multi-phase power converter according to claim 1, wherein the inductance of each of the plurality of phases differs from the inductance of another phase.
5. The multi-phase power converter according to claim 1, wherein the switching element of the at least one phase differs from the switching element of another phase.
6. The multi-phase power converter according to claim 1, wherein the switching element of the at least one phase is optimized for an operating current of said phase.

7. The multi-phase power converter according to claim 5,  
wherein the switching element is a dual switching  
element.
- 5 8. The multi-phase power converter according to claim 1,  
wherein the switching element of each of the plurality of  
phases differs from the inductance of another phase.
9. The multi-phase power converter according to claim 1  
10 being a buck-converter.
10. The multi-phase power converter according to claim 1  
being a boost-converter.

prior art  
 $L1 = L2 = L3$   
 $Q1 = Q3 = Q5$   
 $Q2 = Q4 = Q6$

present invention  
 $L1 = L2 \neq L3$   
 $Q1 = Q3 \neq Q5$   
 $Q2 = Q4 \neq Q6$

or  
 $L1 \neq L2 \neq L3$   
 $Q1 \neq Q3 \neq Q5$   
 $Q2 \neq Q4 \neq Q6$

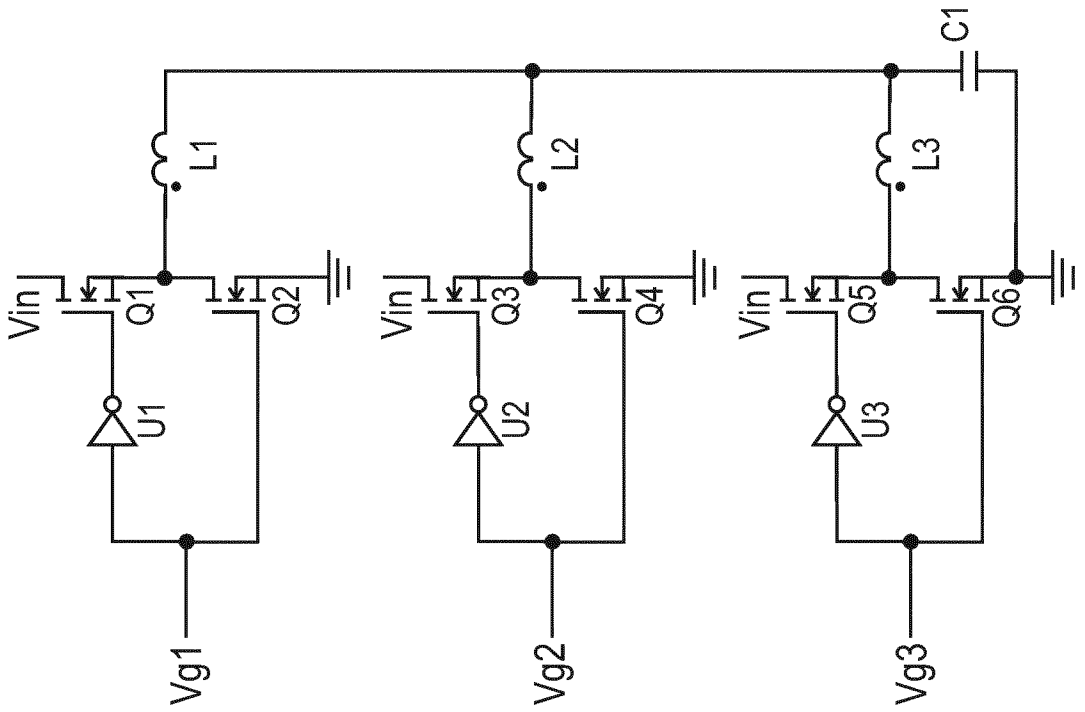


Fig. 1



INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2015/071048

A. CLASSIFICATION OF SUBJECT MATTER  
INV. H02M3/158  
ADD.  
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED  
Minimum documentation searched (classification system followed by classification symbols)  
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2012/313614 A1 (OHSHITA KAZUHIRO [JP] ET AL) 13 December 2012 (2012-12-13) paragraph [0080]; claims 1,2,5; figures 1,2	1,2,4-6, 10
X	DE 20 2014 002223 U1 (DIALOG SEMICONDUCTOR GMBH [DE]) 4 April 2014 (2014-04-04) paragraphs [0015], [0018]; figure 1	1,4,7,9
X	US 2005/093525 A1 (WALTERS MICHAEL M [US] ET AL) 5 May 2005 (2005-05-05) paragraph [0012]; figure 1	1,6
X	US 2011/169476 A1 (IKRIANNIKOV ALEXANDR [US] ET AL) 14 July 2011 (2011-07-14) abstract; figure 1	1
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Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents :

<p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p>	<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&amp;" document member of the same patent family</p>
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer <b>Marannino, M</b>
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## INTERNATIONAL SEARCH REPORT

International application No  
PCT/EP2015/071048

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>JIA WEI ET AL: "Two-stage voltage regulator for laptop computer cpus and the corresponding advanced control schemes to improve light-load performance", 2004 IEEE APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, APEC 04, IEEE, ANAHEIM, CA, USA, vol. 2, 22 February 2004 (2004-02-22), pages 1294-1300, XP010704799, DOI: 10.1109/APEC.2004.1295990 ISBN: 978-0-7803-8269-5 page 1297, paragraph IV-3 -----</p>	1-10

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Information on patent family members

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