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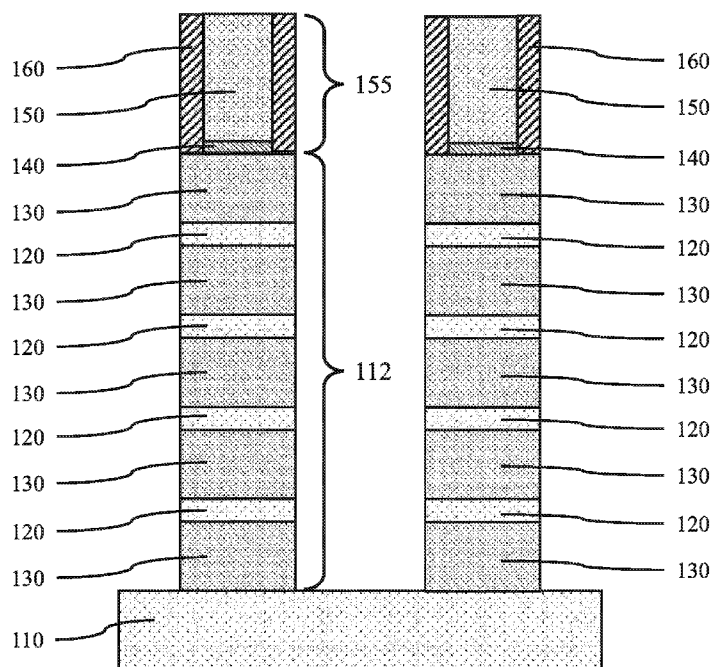


FIG. 1

(57) Abstract: A stacked device is provided. The stacked device includes a plurality of dielectric support bridges on a substrate, and a first two-dimensional (2D) channel layer on each of the plurality of dielectric support bridges. The stacked device further includes a gate dielectric sheet on the first two-dimensional (2D) channel layer, and a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer. The stacked device further includes a second gate dielectric layer on the gate dielectric sheets.



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STACKED PLANAR FIELD EFFECT TRANSISTORS WITH 2D MATERIAL CHANNELS

BACKGROUND

[0001] The present invention generally relates to 2D Channel Transistors, and more particularly to stacked, planar, 2D-channel field effect transistors.

[0002] A Field Effect Transistor (FET) typically has a source, a channel, and a drain, where current flows from the source to the drain, and a gate that controls the flow of current through the device channel. Field Effect Transistors (FETs) can have a variety of different structures, for example, FETs have been fabricated with the source, channel, and drain formed in the substrate material itself, where the current flows horizontally (i.e., in the plane of the substrate), and FinFETs have been formed with the channel extending outward from the substrate. Depending on the doping of the source and drain, an n-FET or a p-FET can be formed.

SUMMARY

[0003] In accordance with an embodiment of the present invention, a stacked device is provided. The stacked device includes a plurality of dielectric support bridges on a substrate, and a first two-dimensional (2D) channel layer on each of the plurality of dielectric support bridges. The stacked device further includes a gate dielectric sheet on the first two-dimensional (2D) channel layer, and a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer. The stacked device further includes a second gate dielectric layer on the gate dielectric sheets.

[0004] In accordance with another embodiment of the present invention, a stacked device is provided. The stacked device includes a bottom dielectric layer on a substrate, and a plurality of

dielectric support bridges on the bottom dielectric layer. The stacked device further includes a first two-dimensional (2D) channel layer on each of the plurality of dielectric support bridges and on the bottom dielectric layer, and a gate dielectric sheet on the first two-dimensional (2D) channel layer. The stacked device further includes a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer, and a second gate dielectric layer on the gate dielectric sheets.

[0005] In accordance with yet another embodiment of the present invention, a method of forming a stacked device is provided. The method includes forming one or more stacks of alternating sacrificial layers and bridging layers on a substrate, and removing the sacrificial layers to expose opposite sides of the bridging layers. The method further includes converting the bridging layers to dielectric support bridges, and forming a first two-dimensional (2D) channel layer on the exposed surfaces of the dielectric support bridges. The method further includes forming a first gate dielectric layer on the two-dimensional (2D) channel layer, and forming disposable filler sections between the dielectric support bridges. The method further includes forming a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer.

[0006] These and other features and advantages will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The following description will provide details of preferred embodiments with reference to the following figures wherein:

[0008] FIG. 1 is a cross-sectional side view showing a plurality of stacks of alternating sacrificial layers and bridging layers on a substrate, and a dummy gate structure on each of the stacks, in accordance with an embodiment of the present invention;

[0009] FIG. 2 is a cross-sectional side view showing two separate stacks of bridging layers on a substrate after removing the sacrificial layers, and a dummy gate structure on each of the stacks, in accordance with an embodiment of the present invention;

[0010] FIG. 3 is a cross-sectional side view showing the bridging layers of each of the stacks converted to dielectric support bridges, and a bottom dielectric layer formed on the substrate, in accordance with an embodiment of the present invention;

[0011] FIG. 4 is a cross-sectional side view showing a first two-dimensional (2D) channel layer formed on the dielectric support bridges and bottom dielectric layer, in accordance with an embodiment of the present invention;

[0012] FIG. 5 is a cross-sectional side view showing a first gate dielectric layer formed on the exposed surfaces of the two-dimensional (2D) channel layer, in accordance with an embodiment of the present invention;

[0013] FIG. 6 is a cross-sectional side view showing a disposable fill layer formed on the first gate dielectric layer of each stack, in accordance with an embodiment of the present invention;

[0014] FIG. 7 is a cross-sectional side view showing portions of the disposable fill layer removed from the sidewall surfaces to form disposable filler blocks between the dielectric support bridges, in accordance with an embodiment of the present invention;

[0015] FIG. 8 is a cross-sectional side view showing recessing of the disposable filler blocks, in accordance with an embodiment of the present invention;

[0016] FIG. 9 is a cross-sectional side view showing formation of inner spacers in the recesses adjoining to the disposable filler blocks, in accordance with an embodiment of the present invention;

[0017] FIG. 10 is a cross-sectional side view showing removal of exposed portions of the first gate dielectric layer, and formation of a second two-dimensional (2D) channel layer on the exposed sides of the inner spacers and the exposed sides of the first two-dimensional (2D) channel layer on the dielectric support bridges, in accordance with an embodiment of the present invention;

[0018] FIG. 11 is a cross-sectional side view showing formation of a first source/drain material layer on the second two-dimensional (2D) channel layer, and a source/drain material fill on the first source/drain material layer, in accordance with an embodiment of the present invention;

[0019] FIG. 12 is a cross-sectional side view showing removal of an upper portion of the source/drain material fill to expose a portion of the first source/drain material layer, and removal of the first source/drain material layer, second two-dimensional (2D) channel layer, and first two-dimensional (2D) channel layer, to expose the sidewall spacers, and formation of an interlayer dielectric (ILD) layer on the source/drain material fill and outside surfaces of the sidewall spacers, in accordance with an embodiment of the present invention;

[0020] FIG. 13 is a cross-sectional side view showing removal of an upper portion of the dummy gate fill that exposes the dummy dielectric layer and portions of the inside surfaces of the sidewall spacers, and removal of the dummy dielectric layer, in accordance with an embodiment of the present invention;

[0021] FIG. 14 is a cross-sectional side view showing removal of portions of the first two-dimensional (2D) channel layer and first gate dielectric layer to form a two-dimensional (2D) channel insert and a gate dielectric plug, and removal of the lower portion of the dummy gate fill

from between the dielectric support bridges to form gate cavities, in accordance with an embodiment of the present invention;

[0022] FIG. 15 is a cross-sectional side view showing a second gate dielectric layer formed on the exposed surfaces of the first gate dielectric layer and inner spacers, in accordance with an embodiment of the present invention;

[0023] FIG. 16 is a cross-sectional side view showing a conductive gate fill formed on the second gate dielectric layer and within the cavities, and a gate cap formed on the active gate structure, in accordance with an embodiment of the present invention;

[0024] FIG. 17 is a cross-sectional side view through the active gate structure perpendicular to FIG. 16 showing the conductive gate fill formed on the second gate dielectric layer and the gate cap formed on the active gate structure, in accordance with an embodiment of the present invention; and

[0025] FIG. 18 is a cross-sectional side view through a sidewall spacer and inner spacers, perpendicular to FIG. 16 and parallel with FIG. 17, showing the sidewall spacer and inner spacers on the gate dielectric sheets and the first two-dimensional (2D) channel layers, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Embodiments of the present invention provide fabrication of stacked devices with 2D-material channel(s), that can provide scaling and/or performance benefits. Using a stacked, planar, 2D-channel configuration, current density is improved for high-performance applications, compared to other nanosheet-type devices. Stacked, planar, 2D-channel FETs can provide higher current density than either gate-all-around (GAA) silicon (Si) nanosheets or GAA 2D nanosheets, for 1) various 2D layer thicknesses and 2) for various W_{sheet} (nanosheet width) from SRAM to logic.

Inherently lower short channel effects (SCE) in 2D materials allows for gate length scaling. 2D materials can carry similar effective on-state current as Si channels, with significantly thinner channels (mono/bi layer 2D channel vs. ~5nm thick Si channel), thus allowing more channels to be built in a stack, thus giving higher overall current density. A wrap-around-contact can provide for improved (reduced) contact resistance through increased interface surface area, where material selection can reduce a Schottky barrier/resistance.

[0027] Embodiments of the present invention can provide both n-type field effect transistor (nFET) devices and p-type field effect transistor (pFET) devices, where nFET and pFET devices can be formed by adjusting the materials of the 2D-material channels, the contact doping, and source/drain metal(s).

[0028] Embodiments of the present invention provide nFET/pFET multi-V_t (threshold voltage) enabled by channel replacement integration, where all multi-V_t stacks are formed using a process sequence, after forming the 2D-material channel. Multi-V_t can be formed in replacement metal gate (RMG) structures.

[0029] Embodiments of the present invention provide methods of fabricating stacked devices with 2D-material channel(s), and nFET/pFET multi-V_t (threshold voltage) devices.

[0030] Exemplary applications/uses to which the present invention can be applied include, but are not limited to: front-end-of-line (FEOL) and/or back-end-of-line (BEOL) logic structures/applications.

[0031] It is to be understood that aspects of the present invention will be described in terms of a given illustrative architecture; however, other architectures, structures, substrate materials and process features and steps can be varied within the scope of aspects of the present invention.

[0032] Referring now to the drawings in which like numerals represent the same or similar elements and initially to FIG. 1, FIG. 1 is a cross-sectional side view showing a plurality of stacks of alternating sacrificial layers and bridging layers on a substrate, and a dummy gate structure on each of the stacks, in accordance with an embodiment of the present invention.

[0033] In one or more embodiments, one or more stacks 112 of alternating sacrificial layers 130 and bridging layers 120 can be formed on a substrate 110, where the sacrificial layers 130 and bridging layers 120 can be a combination of materials that can be selectively etched relative to each other. A dummy gate structure 155 can be on each of the one or more stacks 112 of alternating sacrificial layers 130 and bridging layers 120, where the dummy gate structure 155 can be used as a mask template to trimming back layers on the substrate. The dummy gate structure 155 can include a dummy dielectric layer 140, dummy gate fill 150, and sidewall spacers 160.

[0034] In one or more embodiments, the substrate 110 can be a semiconductor material, including, but not limited to a type IV semiconductor (e.g., silicon (Si), germanium (Ge), a IV-IV compound semiconductor (e.g., silicon germanium (SiGe), silicon carbide (SiC), a III-V compound semiconductor (e.g., gallium arsenide (GaAs), gallium nitride (GaN), a II-VI compound semiconductor (e.g., Cadmium selenide (CdSe), Cadmium sulfide (CdS), Cadmium telluride (CdTe), zinc oxide (ZnO)). The substrate 110 can be a single crystal material wafer, a polycrystalline material wafer, or a semiconductor-on-insulator (SeOI) wafer.

[0035] In various embodiments, the bridging layers 120 can be silicon (Si) and the sacrificial layers 130 can be silicon-germanium (SiGe), where the sacrificial layers 130 can have a germanium concentration in a range of about 25 atomic percent (at.%) to about 75 at.%, or about 40 at.% to about 60 at.%, or about 50 at.% germanium (Ge) to allow selective removal of the sacrificial layers 130. The sacrificial layers 130 and bridging layers 120 can be formed by epitaxial growth on the

substrate 110. In various embodiments, combinations of materials other than Si and SiGe, for example, various combinations of dielectric materials having etch selectivity can be formed by conformal depositions, such as atomic layer deposition (ALD) and/or plasma enhanced atomic layer deposition (PEALD).

[0036] In various embodiments, the bridging layers 120 can have a thickness in a range of about 3 nanometers (nm) to about 7 nm, or about 4 nm to about 6 nm, or about 5 nm, although other thicknesses are also contemplated. The bridging layers 120 can have a thickness sufficient to allow formation of a dielectric support bridge that can provide structural support to a two-dimensional (2D) channel layer. Gate length reduction below 12 nm is limited by: 1) SCE for ≥ 5 nm T_{Si} or 2) quantum confinement effects degrading $R_{channel}$ for $T_{Si} < 5$ nm, where SCE can include subthreshold leakage, DIBL, etc. If a Si channel thickness is significantly (1-3nm) greater than 5nm, gate control over the channel is weakened so it is easy to have short channel effects. If the Si channel is significantly thinner (1-3nm) than 5nm, quantum confinement increases the resistance of the channel such that the device is no longer capable of carrying useful levels of electrical current.

[0037] In various embodiments, the sacrificial layers 130 can have a thickness in a range of about 7 nanometers (nm) to about 15 nm, or about 9 nm to about 12 nm, or about 11 nm, although other thicknesses are also contemplated. The sacrificial layers 130 can have a thickness sufficient to allow formation of an active gate structure on the two-dimensional (2D) channel layer.

[0038] In various embodiments, the stack can include between four (4) to six (6) bridging layers 120 and an equal number of sacrificial layers 130 where a bottom sacrificial layers 130 is closest to the surface of the substrate 110.

[0039] In various embodiments, the bridging layers 120 and sacrificial layers 130 can have a width in a range of about 15 nanometers (nm) to about 100 nm, or about 25 nm to about 75 nm, or

about 50 nm, and a length in a range of about 10 nanometers (nm) to about 100 nm, or about 12 nm to about 75 nm, or about 50 nm, although other widths and lengths are also contemplated. In various embodiments, the bridging layers 120 and sacrificial layers 130 can be from about 12 nm x 15 nm to about 100 nm x 100 nm, or about 50 nm x 50 nm, although other sizes are also contemplated.

[0040] In various embodiments, the height of a stack 112 of alternating sacrificial layers 130 and bridging layers 120 can be in the range of about 60 nm to about 75 nm, or about 62 nm to about 70, although other heights are also contemplated. The height can depend on the thicknesses of each individual layer in the stack of layers, and the aspect ratio achievable by the directional etching of the sacrificial layers 130 and bridging layers 120.

[0041] In various embodiments, the dummy dielectric layer 140 can be an insulating, dielectric material, including, but not limited to, silicon oxide (SiO), silicon nitride (SiN), a silicon oxynitride (SiON), a silicon carbonitride (SiCN), a silicon boronitride (SiBN), a silicon borocarbide (SiBC), and combinations thereof.

[0042] In various embodiments, the sidewall spacers 160 can be a hardmask material material, including, but not limited to, silicon oxide (SiO), silicon nitride (SiN), a silicon oxynitride (SiON), a silicon carbonitride (SiCN), a silicon boronitride (SiBN), a silicon borocarbide (SiBC), and combinations thereof. The dummy dielectric layer 140 can be a material that is selectively etchable relative to the sidewall spacers 160.

[0043] In various embodiments, the dummy gate fill 150 can be a selectively-etchable material relative to the sidewall spacers 160 and dummy dielectric layer 140, for example, amorphous silicon (a-Si), amorphous carbon (a-C), amorphous germanium (a-Ge), and combinations thereof.

[0044] FIG. 2 is a cross-sectional side view showing two separate stacks of bridging layers on a substrate after removing the sacrificial layers, and a dummy gate structure on each of the stacks, in accordance with an embodiment of the present invention.

[0045] In one or more embodiments, the sacrificial layers 130 are selectively removed, where the sacrificial layers 130 can be removed using a selective, isotropic etch, for example, a wet chemical etch, dry plasma etch, or combination thereof. Removal of the sacrificial layers 130 can leave the bridging layers 120 supported by material at opposite ends of the stack, which can include the dummy gate fill 150 and sidewall spacers 160 of the dummy gate structure 155 and/or oxide spacers. Removal of the bottom sacrificial layer 130 can expose a portion of the substrate surface beneath the bridging layers 120.

[0046] FIG. 3 is a cross-sectional side view showing the bridging layers of each of the stacks converted to dielectric support bridges, and a bottom dielectric layer formed on the substrate, in accordance with an embodiment of the present invention.

[0047] In various embodiments, the bridging layers 120 themselves can be a semiconductor that can be converted to an electrically insulating material, or an insulating dielectric material, for example, silicon oxide (SiO), including silicon dioxide (SiO₂), silicon nitride (SiN), silicon oxynitride (SiON), and combinations thereof. The stack(s), including the bridging layers 120 and sacrificial layers 130, could be made from dielectric materials that are selectively etchable relative to each other.

[0048] In one or more embodiments, the bridging layers 120 can be converted into dielectric support bridges 170 through a chemical reaction, for example, an oxidation process. The oxidation process can be, for example, a thermal oxidation, a wet oxidation, a dry, plasma oxidation, and combinations thereof. In a non-limiting exemplary embodiment, silicon (Si) bridging layers 120 can

be converted into silicon dioxide (SiO_2) dielectric support bridges 170 through a thermal oxidation process.

[0049] In various embodiments, the bridging layers 120/dielectric support bridges 170 would sustain 2MV/cm, which for example corresponds to about a 4 nm thickness with a low-k SiOCN spacer.

[0050] In various embodiments, the chemical reaction can also convert a top portion of the substrate 110 to a bottom dielectric layer 115, where for example, an oxidation process can form a silicon oxide (SiO) bottom dielectric layer 115. In various embodiments, the bottom dielectric layer 115 can have a thickness of about half the thickness of the bridging layers 120/dielectric support bridges 170 due to reactant diffusion into the substrate surface.

[0051] FIG. 4 is a cross-sectional side view showing a first two-dimensional (2D) channel layer formed on the dielectric support bridges and bottom dielectric layer, in accordance with an embodiment of the present invention.

[0052] In one or more embodiments, a first two-dimensional (2D) channel layer 180 can be formed on the dielectric support bridges 170 and bottom dielectric layer 115, where the first 2D-channel layer 180 can be formed by chemical vapor deposition (CVD) or a conformal deposition (e.g., ALD, PEALD). In various embodiments, the first two-dimensional (2D) channel layer 180 can be formed on the exposed surfaces of the dummy gate structure 155 and dielectric support bridges 170, where the first two-dimensional (2D) channel layer 180 can wrap around four sides of each of the plurality of dielectric support bridges 170. The first two-dimensional (2D) channel layer 180 can be formed on the surface of the bottom dielectric layer 115 by the deposition.

[0053] In one or more embodiments, the first two-dimensional (2D) channel layer 180 can be made of a two-dimensional material, including, but not limited to, indium tin oxides (ITO), indium-

aluminum-zinc-oxides (IAZO), transition metal di chalcogenides (TMDC), for example, molybdenum disulfide (MoS_2), molybdenum diselenide (MoSe_2), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), graphene, and combinations thereof. The first two-dimensional (2D) channel layer 180 can be a material that does not normally conduct, but is capable of conducting when gate voltage is applied through a dielectric separating layer. In various embodiments, the first two-dimensional (2D) channel layer 180 can be a material having a two-dimensional laminate/graphene-like structure.

[0054] In various embodiments, the first two-dimensional (2D) channel layer 180 can have a thickness in a range of about one (1) monolayer to about five (5) monolayers, or about two (2) monolayers to about four (4) monolayers, where the monolayers may be incomplete or have gaps/defects due to formation and processing. The first two-dimensional (2D) channel layer 180 can have a thickness in a range of about 0.5 nm to about 1.5 nm depending on the monolayer thickness of the material.

[0055] In a non-limiting exemplary embodiment, a molybdenum disulfide (MoS_2) two-dimensional (2D) channel layer 180, for example, can have FEOL device characteristics of: $I_{\text{on}}/I_{\text{off}} \sim 10^8$, SS (subthreshold slope) ~ 100 mV/dec, DIBL (drain-induced barrier lowering) < 30 mV/V, $L_{\text{gate}} = 40\text{-}100\text{nm}$, $t_{\text{channel}} < 1$ nm, $I_{\text{on}} = 0.4$ mA/ μm (@ $V_{\text{DS}} = 1\text{V}$).

[0056] FIG. 5 is a cross-sectional side view showing a first gate dielectric layer formed on the exposed surfaces of the two-dimensional (2D) channel layer, in accordance with an embodiment of the present invention.

[0057] In one or more embodiments, a first gate dielectric layer 190 can be formed on the exposed surfaces of the two-dimensional (2D) channel layer 180, where the first gate dielectric layer 190 can

be formed by a conformal deposition (e.g., ALD, PEALD). The first gate dielectric layer 190 can electrically insulate the first two-dimensional (2D) channel layer 180.

[0058] In various embodiments, the first gate dielectric layer 190 can be a high-k insulating, dielectric material, including, but not limited to, metal oxides, such as, hafnium oxide (HfO), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), lanthanum oxide (LaO), lanthanum aluminum oxide (LaAlO), zirconium oxide (ZrO), zirconium silicon oxide (ZrSiO), zirconium silicon oxynitride (ZrSiON), tantalum oxide (TaO), titanium oxide (TiO), barium strontium titanium oxide (BaSrTiO), barium titanium oxide (BaTiO), strontium titanium oxide (SrTiO), yttrium oxide (YO), aluminum oxide (AlO), lead scandium tantalum oxide (PbScTaO), and lead zinc niobate (PbZnNbO). The high-k material may further include dopants such as lanthanum, aluminum, magnesium, or combinations thereof.

[0059] In various embodiments, the first gate dielectric layer 190 can have a thickness in a range of about 0.5 nanometers (nm) to about 3 nm, or about 1 nm to about 2 nm, although other thicknesses are also contemplated. The first gate dielectric layer 190 can have a thickness sufficient to electrical insulation to/between adjacent current-carrying layers.

[0060] FIG. 6 is a cross-sectional side view showing a disposable fill layer formed on the first gate dielectric layer of each stack, in accordance with an embodiment of the present invention.

[0061] In one or more embodiments, a disposable fill layer 200 can be formed on the first gate dielectric layer 190 of each stack, where the disposable fill layer 200 can be formed by a conformal deposition (e.g., ALD, PEALD) to fill in the space between adjacent dielectric support bridges 170, such that the disposable fill layer 200 does not pinch off and create a void between adjacent dielectric support bridges 170.

[0062] In various embodiments, the disposable fill layer 200 can be a selectively-etchable material relative to the first gate dielectric layer 190, for example, titanium nitride (TiN), titanium carbide (TiC), amorphous silicon (a-Si), amorphous carbon (a-C), amorphous germanium (a-Ge), and combinations thereof.

[0063] FIG. 7 is a cross-sectional side view showing portions of the disposable fill layer removed from the sidewall surfaces to form disposable filler blocks between the dielectric support bridges, in accordance with an embodiment of the present invention.

[0064] In one or more embodiments, portions of the disposable fill layer 200 on the sidewalls of the sidewall spacers 160 and first gate dielectric layer 190 of each stack can be removed using a selective, directional etch, for example, a reactive ion etch (RIE), that leaves portions of the disposable fill layer 200 between adjacent dielectric support bridges 170 as disposable filler blocks 205. A thin layer of the disposable fill layer 200 may also remain on the sidewalls of the sidewall spacers 160 and first gate dielectric layer 190.

[0065] FIG. 8 is a cross-sectional side view showing recessing of the disposable filler blocks, in accordance with an embodiment of the present invention.

[0066] In one or more embodiments, portions of the disposable filler blocks 205 can be removed using a selective, isotropic etch, for example, a wet chemical etch or dry plasma etch, to form recesses adjoining disposable filler sections 207. The disposable filler sections 207 can be on the first gate dielectric layer 190 between adjacent dielectric support bridges 170. Removal of the portions of the disposable filler blocks 205 can also remove any remaining disposable fill layer 200 on the first gate dielectric layer 190 on the sidewalls of the dummy gate structure 155 and dielectric support bridges 170. Portions of the first gate dielectric layer 190 can be exposed.

[0067] In various embodiments, the disposable filler sections 207 can have a width about the same as the width of the dummy gate fill 150 and dummy dielectric layer 140.

[0068] FIG. 9 is a cross-sectional side view showing formation of inner spacers in the recesses adjoining to the disposable filler blocks, in accordance with an embodiment of the present invention.

[0069] In one or more embodiments, an inner spacer 210 can be formed in each of the recesses adjoining the disposable filler sections 207, where the inner spacer 210 can be formed by a conformal deposition and anisotropic etch-back.

[0070] In various embodiments, the inner spacers 210 can be a hardmask material, including, but not limited to, silicon oxide (SiO), silicon nitride (SiN), a silicon oxynitride (SiON), a silicon carbonitride (SiCN), a silicon boronitride (SiBN), a silicon borocarbide (SiBC), and combinations thereof. The inner spacers 210 can be the same material as the sidewall spacers 160.

[0071] FIG. 10 is a cross-sectional side view showing removal of exposed portions of the first gate dielectric layer, and formation of a second two-dimensional (2D) channel layer on the exposed sides of the inner spacers and the exposed sides of the first two-dimensional (2D) channel layer on the dielectric support bridges, in accordance with an embodiment of the present invention.

[0072] In one or more embodiments, exposed portions of the first gate dielectric layer 190 can be removed using a selective isotropic etch, for example, a wet chemical etch or dry plasma etch.

Removal of the exposed portions of the first gate dielectric layer 190 can expose the underlying portions of the first two-dimensional (2D) channel layer 180. Removal of the exposed portions of the first gate dielectric layer 190 can form gate dielectric sheets 195 between the first two-dimensional (2D) channel layer 180 on the dielectric support bridges 170 and the disposable filler sections 207. The gate dielectric sheets 195 can extend from one side of the dummy gate structure or dielectric support bridges 170 to the other side. A pair of gate dielectric sheets 195 can be on

each of the plurality of dielectric support bridges 170, where a gate dielectric sheet 195 can be on each of the opposite sides of the dielectric support bridge 170.

[0073] In one or more embodiments, a second two-dimensional (2D) channel layer 220 can be formed on the exposed sides of the inner spacers 210 and the exposed portions of the first two-dimensional (2D) channel layer 180 on the dielectric support bridges 170 and dummy gate structure 155. The second two-dimensional (2D) channel layer 220 can be formed by a conformal deposition or CVD, that also forms the second two-dimensional (2D) channel layer 220 on the first two-dimensional (2D) channel layer 180 on the bottom dielectric layer 115 and substrate 110.

[0074] In various embodiments, the second two-dimensional (2D) channel layer 220 can have a rippled profile on the dielectric support bridges 170 and dummy gate structure 155, where the removal of the portions of the first gate dielectric layer 190 created an uneven surface.

[0075] In one or more embodiments, the second two-dimensional (2D) channel layer 220 can be made of a two-dimensional material, including, but not limited to, indium tin oxides (ITO), indium-aluminum-zinc-oxides (IAZO), transition metal di chalcogenides (TMDC), for example, molybdenum disulfide (MoS_2), molybdenum diselenide (MoSe_2), tungsten disulfide (WS_2), tungsten diselenide (WSe_2), graphene, and combinations thereof. The second two-dimensional (2D) channel layer 220 can be a material that does not normally conduct, but is capable of conducting when gate voltage is applied through a dielectric separating layer. In various embodiments, the second two-dimensional (2D) channel layer 220 can be a material having a two-dimensional laminate/graphene-like structure.

[0076] In various embodiments, the second two-dimensional (2D) channel layer 220 can have a thickness in a range of about one (1) monolayer to about 50 monolayers, or about two (2) monolayers to about four (4) monolayers, where the monolayers may be incomplete or have

gaps/defects due to formation and processing. The first two-dimensional (2D) channel layer 180 can have a thickness in a range of about 0.5 nm to about 15 nm, or a range of about 0.5 nm to about 1.5 nm depending on the monolayer thickness of the material. In various embodiments, the second two-dimensional (2D) channel layer 220 can fill the space between stacks of dielectric support bridges 170.

[0077] FIG. 11 is a cross-sectional side view showing formation of a first source/drain material layer on the second two-dimensional (2D) channel layer, and a source/drain material fill on the first source/drain material layer, in accordance with an embodiment of the present invention.

[0078] In one or more embodiments, a first source/drain material layer 230 can be formed on the second two-dimensional (2D) channel layer 220, where the first source/drain material layer 230 can be formed by a conformal deposition (e.g., ALD, PEALD), and etched back using a directional etch (e.g., RIE).

[0079] In various embodiments, the first source/drain material layer 230 can be a conductive material that can minimize the contact resistance with the second two-dimensional (2D) channel layer 220, including, but not limited to, semi-metals, for example, bismuth (Bi) and antimony (Sb).

[0080] In a non-limiting exemplary embodiment, a bismuth first source/drain material layer 230 can be formed on a molybdenum diselenide (MoSe_2) second two-dimensional (2D) channel layer 220, where the contact resistance between the layers is 123 ohm-micrometer.

[0081] In various embodiments, the first source/drain material layer 230 can have a thickness in a range of about 3 nanometers (nm) to about 6 nm, or about 3 nm to about 5 nm, or about 4 nm, although other thicknesses are also contemplated.

[0082] In one or more embodiments, a source/drain material fill 240 can be formed on the first source/drain material layer 230, where the source/drain material fill 240 can fill in the spaces adjacent to or in between stacks.

[0083] In various embodiments, the source/drain material fill 240 can be a conductive material including, but not limited to, a metal, for example, aluminum (Al), tungsten (W), cobalt (Co), molybdenum (Mo), a metal compound, for example, tantalum nitride (Ta₂N₅), tantalum carbide (TaC), titanium nitride (TiN), titanium carbide (TiC), and combinations thereof.

[0084] FIG. 12 is a cross-sectional side view showing removal of an upper portion of the source/drain material fill to expose a portion of the first source/drain material layer, and removal of the first source/drain material layer, second two-dimensional (2D) channel layer, and first two-dimensional (2D) channel layer, to expose the sidewall spacers, and formation of an interlayer dielectric (ILD) layer on the source/drain material fill and outside surfaces of the sidewall spacers, in accordance with an embodiment of the present invention.

[0085] In one or more embodiments, an upper portion of the source/drain material fill 240 can be removed to expose a portion of the first source/drain material layer 230, where the upper portion of the source/drain material fill 240 can be removed using a selective isotropic etch. The removal of the upper portion of the source/drain material fill 240 can lower the top surface of the source/drain material fill 240 to between the top surface and the bottom surface of the dummy dielectric layer 140, such that the majority of the second two-dimensional (2D) channel layer 220 on the sidewall spacers 160 is exposed.

[0086] In various embodiments, the exposed portion(s) of the second two-dimensional (2D) channel layer 220 and underlying portions of the first two-dimensional (2D) channel layer 180, where the layers are the same 2D material, can be removed using a selective, isotropic etch.

Removal of the second two-dimensional (2D) channel layer 220 and underlying portions of the first two-dimensional (2D) channel layer 180 can expose the sidewall spacers 160. Removal of the portions of the first two-dimensional (2D) channel layer 180 can form a two-dimensional (2D) channel sheet 185 on the gate dielectric sheet 195 above the top disposable filler sections 207.

[0087] In one or more embodiments, an interlayer dielectric (ILD) layer 250 can be formed on the top surface of the source/drain material fill 240 and the outside surfaces of the sidewall spacers 160, where the interlayer dielectric (ILD) layer 250 can be formed by a blanket deposition, for example, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or a combination thereof. A chemical-mechanical polishing (CMP) can be used to removed excess material.

[0088] In various embodiments, the interlayer dielectric (ILD) layer 250 can be a dielectric material including, but not limited to, a flowable oxide (FOX), silicon oxide (SiO), silicon nitride (SiN), and other dielectric materials that can be later removed selective to sidewall spacers 160.

[0089] FIG. 13 is a cross-sectional side view showing removal of an upper portion of the dummy gate fill that exposes the dummy dielectric layer and portions of the inside surfaces of the sidewall spacers, and removal of the dummy dielectric layer, in accordance with an embodiment of the present invention.

[0090] In one or more embodiments, an upper portion of the dummy gate fill can be removed to form a gate cavity 260, which exposes the dummy dielectric layer 140 and portions of the inside surfaces of the sidewall spacers 160. The upper portion of the dummy gate fill 150 can be removed using a selective isotropic etch, a selective directional etch (e.g., RIE), or a combination thereof.

[0091] FIG. 14 is a cross-sectional side view showing removal of portions of the first two-dimensional (2D) channel layer and first gate dielectric layer to form a two-dimensional (2D)

channel insert and a gate dielectric plug, and removal of the lower portion of the dummy gate fill from between the dielectric support bridges to form gate cavities, in accordance with an embodiment of the present invention.

[0092] In one or more embodiments, portions of the two-dimensional (2D) channel sheet 185 on the gate dielectric sheet 195 can be removed using selective etches to form a two-dimensional (2D) channel insert 187 and a gate dielectric plug 197 between the sidewall spacers 160 and the top inner spacers 210.

[0093] In one or more embodiments, the disposable filler sections 207 can be removed using a selective, isotropic etch, where removal of the disposable filler sections 207 exposes gate dielectric sheets 195 on the dielectric support bridges 170 and inner sidewalls of the inner spacers 210. Removal of the disposable filler sections 207 can form intervening gate cavities 265 between the adjacent dielectric support bridges 170.

[0094] FIG. 15 is a cross-sectional side view showing a second gate dielectric layer formed on the exposed surfaces of the first gate dielectric layer and inner spacers, in accordance with an embodiment of the present invention.

[0095] In one or more embodiments, a second gate dielectric layer 270 can be formed on the exposed surfaces of the gate dielectric sheets 195 and inner spacers 210.

[0096] In various embodiments, the second gate dielectric layer 270 can be a high-k insulating, dielectric material, including, but not limited to, metal oxides, such as, hafnium oxide (HfO), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride (HfSiON), lanthanum oxide (LaO), lanthanum aluminum oxide (LaAlO), zirconium oxide (ZrO), zirconium silicon oxide (ZrSiO), zirconium silicon oxynitride (ZrSiON), tantalum oxide (TaO), titanium oxide (TiO), barium strontium titanium oxide (BaSrTiO), barium titanium oxide (BaTiO), strontium titanium oxide

(SrTiO), yttrium oxide (YO), aluminum oxide (AlO), lead scandium tantalum oxide (PbScTaO), and lead zinc niobate (PbZnNbO). The high-k material may further include dopants such as lanthanum, aluminum, magnesium, or combinations thereof.

[0097] FIG. 16 is a cross-sectional side view showing a conductive gate fill formed on the second gate dielectric layer and within the cavities, and a gate cap formed on the active gate structure, in accordance with an embodiment of the present invention.

[0098] In one or more embodiments, a conductive gate fill 280 can be formed on the second gate dielectric layer 270 and within the gate cavity 260 and intervening gate cavities 265.

[0099] In various embodiments, the conductive gate fill 280 can be a conductive material, including, but not limited to, a metal, for example, aluminum (Al), tungsten (W), cobalt (Co), molybdenum (Mo), a metal compound, for example, tantalum nitride (TaN), tantalum carbide (TaC), titanium nitride (TiN), titanium carbide (TiC), and combinations thereof.

[0100] In one or more embodiments, a gate cap 290 can be formed on the active gate structure, including the conductive gate fill 280 and sidewall spacers 160.

[0101] In various embodiments, the gate cap 290 can be an insulating, dielectric material, including, but not limited to, silicon oxide (SiO), silicon nitride (SiN), silicon oxynitride (SiON), silicon carbide (SiC), silicon oxycarbide (SiOC), silicon carbonitride (SiCN), silicon oxy carbonitride (SiOCN), silicon boro carbonitride (SiBCN), and combinations thereof.

[0102] FIG. 17 is a cross-sectional side view through the active gate structure perpendicular to FIG. 16 showing the conductive gate fill formed on the second gate dielectric layer and the gate cap formed on the active gate structure, in accordance with an embodiment of the present invention.

[0103] In one or more embodiments, the conductive gate fill 280 can be on four sides of each of the dielectric support bridges 170 and on three sides of the bottom dielectric layer 115. The first

two-dimensional (2D) channel layer 180 can be on opposite sides of each dielectric support bridges 170, and on a top surface of the bottom dielectric layer 115. The gate dielectric sheets 195 can be on each of the first two-dimensional (2D) channel layers 180, and the second gate dielectric layer 270 can be around the gate dielectric sheets 195, first two-dimensional (2D) channel layer 180, and dielectric support bridges 170. The gate cap 290 can be on the conductive gate fill 280.

[0104] FIG. 18 is a cross-sectional side view through a sidewall spacer and inner spacers, perpendicular to FIG. 16 and parallel with FIG. 17, showing the sidewall spacer and inner spacers on the gate dielectric sheets and the first two-dimensional (2D) channel layers, in accordance with an embodiment of the present invention.

[0105] The first two-dimensional (2D) channel layer 180 can be on opposite sides of each dielectric support bridges 170, and on a top surface of the bottom dielectric layer 115, where the first two-dimensional (2D) channel layer 180 can wrap around four sides of the gate dielectric sheets 195 and inner spacers 210. The gate dielectric sheets 195 can wrap around the inner spacers 210. The sidewall spacer 160 can be on the outer surfaces of the first two-dimensional (2D) channel layer 180. The two-dimensional (2D) channel insert 187 and a gate dielectric plug 197 are shortened portions of the first two-dimensional (2D) channel layer 180 and gate dielectric sheets 195 on the top surface of the top inner spacer 210, which do not extend into the active gate structure, as shown in FIG. 17.

[0106] The present embodiments can include a design for an integrated circuit chip, which can be created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer can transmit the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities,

directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

[0107] Methods as described herein can be used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0108] It should also be understood that material compounds will be described in terms of listed elements, e.g., SiGe. These compounds include different proportions of the elements within the compound, e.g., SiGe includes $\text{Si}_x\text{Ge}_{1-x}$ where x is less than or equal to 1, etc. In addition, other elements can be included in the compound and still function in accordance with the present principles. The compounds with additional elements will be referred to herein as alloys.

[0109] Reference in the specification to “one embodiment” or “an embodiment”, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of

the phrase “in one embodiment” or “in an embodiment”, as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

[0110] It is to be appreciated that the use of any of the following “/”, “and/or”, and “at least one of”, for example, in the cases of “A/B”, “A and/or B” and “at least one of A and B”, is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of both options (A and B). As a further example, in the cases of “A, B, and/or C” and “at least one of A, B, and C”, such phrasing is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of the third listed option (C) only, or the selection of the first and the second listed options (A and B) only, or the selection of the first and third listed options (A and C) only, or the selection of the second and third listed options (B and C) only, or the selection of all three options (A and B and C). This can be extended, as readily apparent by one of ordinary skill in this and related arts, for as many items listed.

[0111] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms “a,” “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “includes” and/or “including,” when used herein, specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

[0112] Spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, can be used herein for ease of description to describe one element's or feature's relationship to another element(s) or feature(s) as illustrated in the FIGS. It will be understood that the spatially

relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the FIGS. For example, if the device in the FIGS. is turned over, elements described as “below” or “beneath” other elements or features would then be oriented “above” the other elements or features. Thus, the term “below” can encompass both an orientation of above and below. The device can be otherwise oriented (rotated 90 degrees or at other orientations), and the spatially relative descriptors used herein can be interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being “between” two layers, it can be the only layer between the two layers, or one or more intervening layers can also be present.

[0113] It will be understood that, although the terms first, second, etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the scope of the present concept.

[0114] It will also be understood that when an element such as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements can also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements can be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

[0115] Having described preferred embodiments of a device and method of fabricating the device (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be

understood that changes may be made in the particular embodiments disclosed which are within the scope of the invention as outlined by the appended claims. Having thus described aspects of the invention, with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

WHAT IS CLAIMED IS

1. A stacked device, comprising:
a plurality of dielectric support bridges on a substrate;
a first two-dimensional (2D) channel layer on each of the plurality of dielectric support bridges;
a gate dielectric sheet on the first two-dimensional (2D) channel layer;
a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer; and
a second gate dielectric layer on the gate dielectric sheets.
2. The stacked device of claim 1, wherein the first two-dimensional (2D) channel layer wraps around four sides of each of the plurality of dielectric support bridges.
3. The stacked device of claim 1, wherein there is a pair of gate dielectric sheets on each of the plurality of dielectric support bridges.
4. The stacked device of claim 1, wherein the plurality of dielectric support bridges are made of silicon oxide (SiO₂).
5. The stacked device of claim 1, further comprising a source/drain material fill on the second two-dimensional (2D) channel layer.

6. The stacked device of claim 5, further comprising a first source/drain material layer between the source/drain material fill and the second two-dimensional (2D) channel layer.

7. The stacked device of claim 6, further comprising a bottom dielectric layer between the substrate and the plurality of dielectric support bridges.

8. The stacked device of claim 7, further comprising an active gate structure between one or more pairs of gate dielectric sheets.

9. The stacked device of claim 8, further comprising further comprising an inner spacer on opposite sides of each of the active gate structures.

10. A stacked device, comprising:
a bottom dielectric layer on a substrate;
a plurality of dielectric support bridges on the bottom dielectric layer;
a first two-dimensional (2D) channel layer on each of the plurality of dielectric support bridges and on the bottom dielectric layer;
a gate dielectric sheet on the first two-dimensional (2D) channel layer;
a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer; and
a second gate dielectric layer on the gate dielectric sheets.

11. The stacked device of claim 10, wherein the first two-dimensional (2D) channel layer is a material selected from the group consisting of indium tin oxide (ITO), indium-aluminum-zinc-oxide (IAZO), molybdenum disulfide (MoS_2), molybdenum diselenide (MoSe_2), tungsten disulfide (WS_2), and tungsten diselenide (WSe_2).

12. The stacked device of claim 11, wherein the second two-dimensional (2D) channel layer is a material selected from the group consisting of indium tin oxide (ITO), indium-aluminum-zinc-oxide (IAZO), molybdenum disulfide (MoS_2), molybdenum diselenide (MoSe_2), tungsten disulfide (WS_2), and tungsten diselenide (WSe_2).

13. The stacked device of claim 12, further comprising a first source/drain material layer on the second two-dimensional (2D) channel layer.

14. The stacked device of claim 13, further comprising a source/drain material fill on the

15. The stacked device of claim 14, further comprising an active gate structure between one or more pairs of gate dielectric sheets.

16. The stacked device of claim 15, wherein the first source/drain material layer is a material selected from the group consisting of bismuth (Bi) and antimony (Sb).

17. The stacked device of claim 16, wherein the source/drain material fill is a conductive material selected from the group consisting of aluminum (Al), tungsten (W), cobalt (Co),

molybdenum (Mo), tantalum nitride (TaN), tantalum carbide (TaC), titanium nitride (TiN), titanium carbide (TiC), and combinations thereof.

18. A method of forming a stacked device, comprising:
forming one or more stacks of alternating sacrificial layers and bridging layers on a substrate;
removing the sacrificial layers to expose opposite sides of the bridging layers;
converting the bridging layers to dielectric support bridges;
forming a first two-dimensional (2D) channel layer on the exposed surfaces of the dielectric support bridges;
forming a first gate dielectric layer on the two-dimensional (2D) channel layer;
forming disposable filler sections between the dielectric support bridges; and
forming a second two-dimensional (2D) channel layer on the first two-dimensional (2D) channel layer.

19. The method of claim 18, further comprising forming a first source/drain material layer 230 can be formed on the second two-dimensional (2D) channel layer.

20. The method of claim 18, further comprising forming a source/drain material fill on the first source/drain material layer.

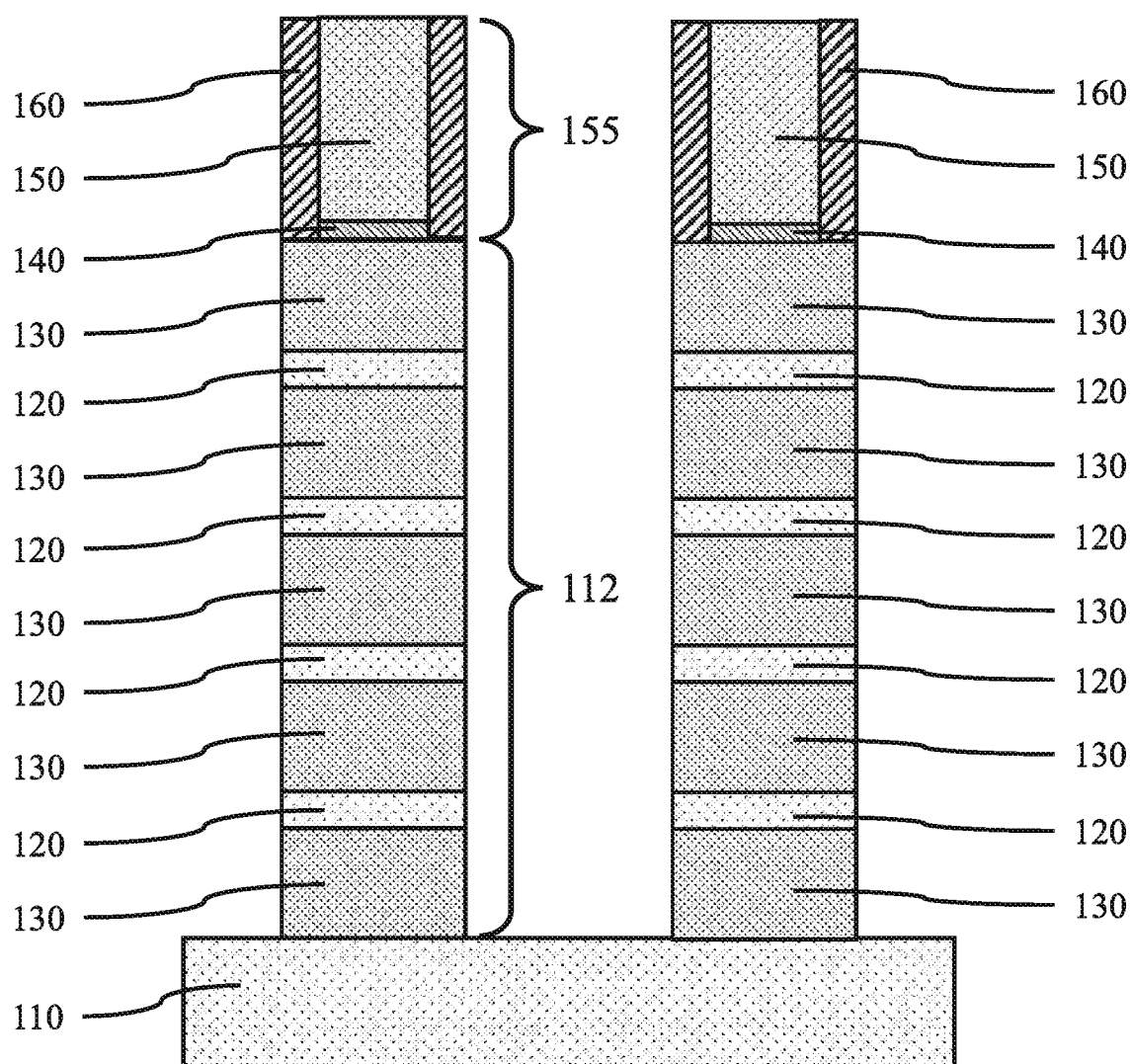


FIG. 1

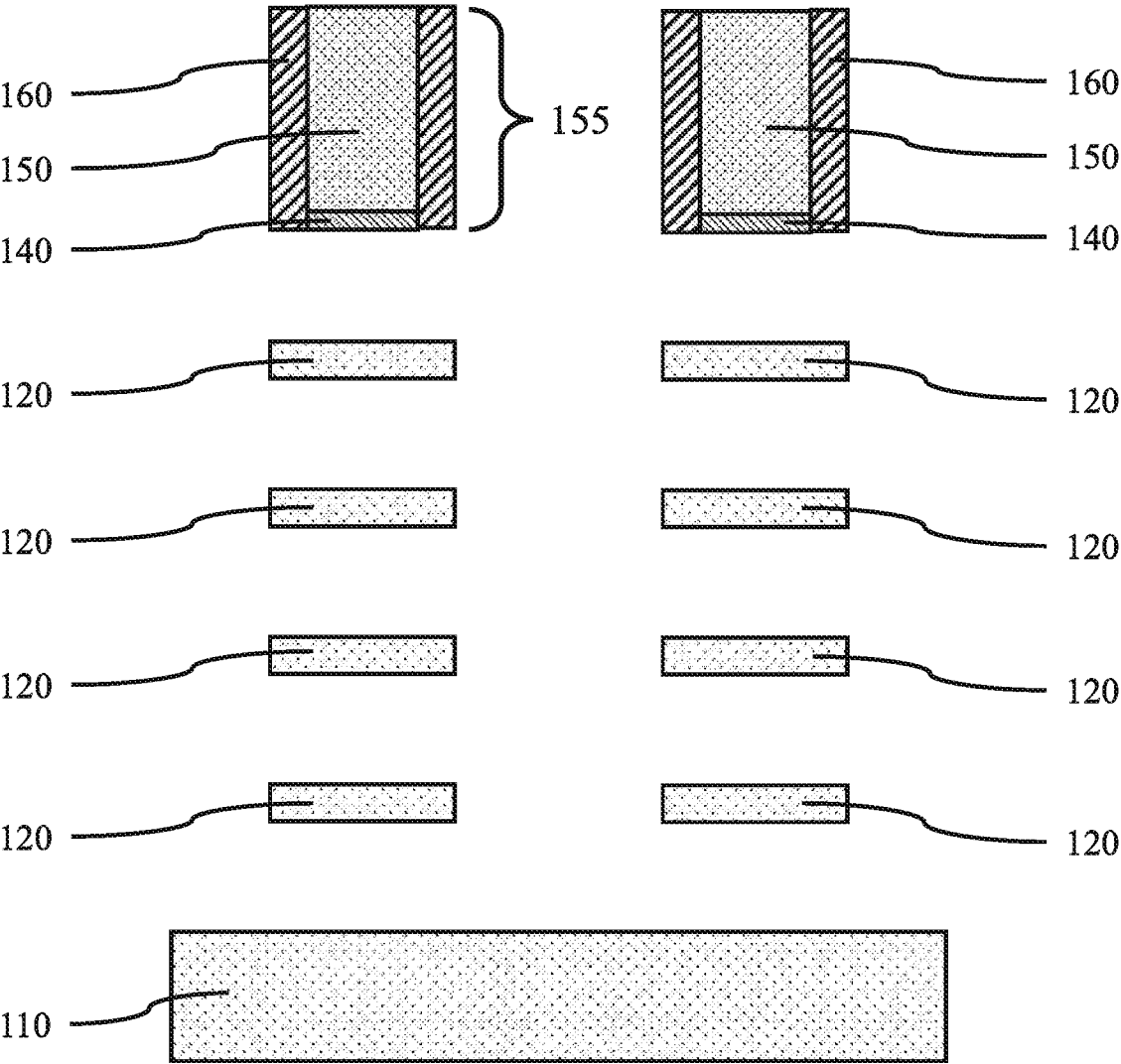


FIG. 2

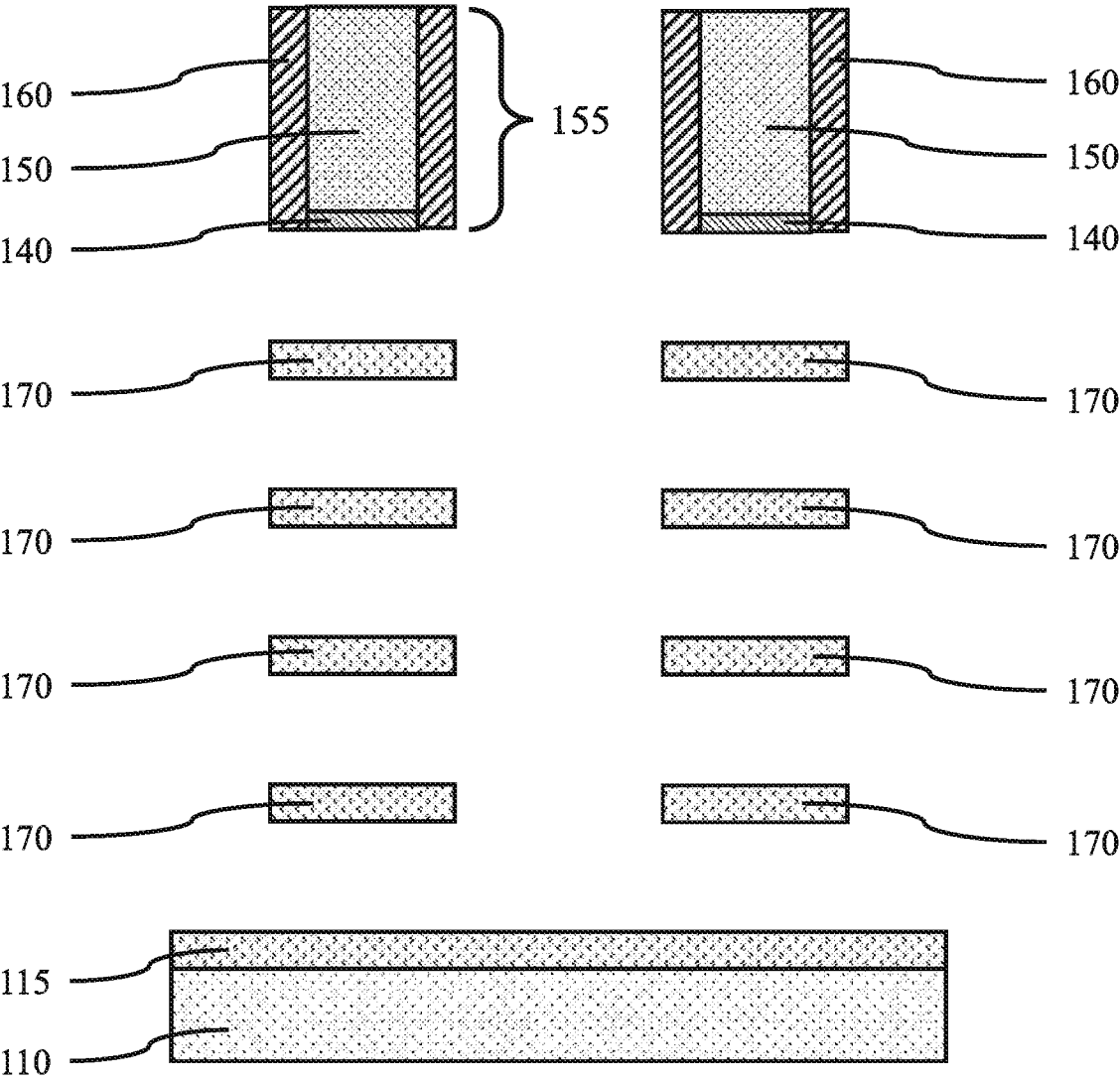


FIG. 3

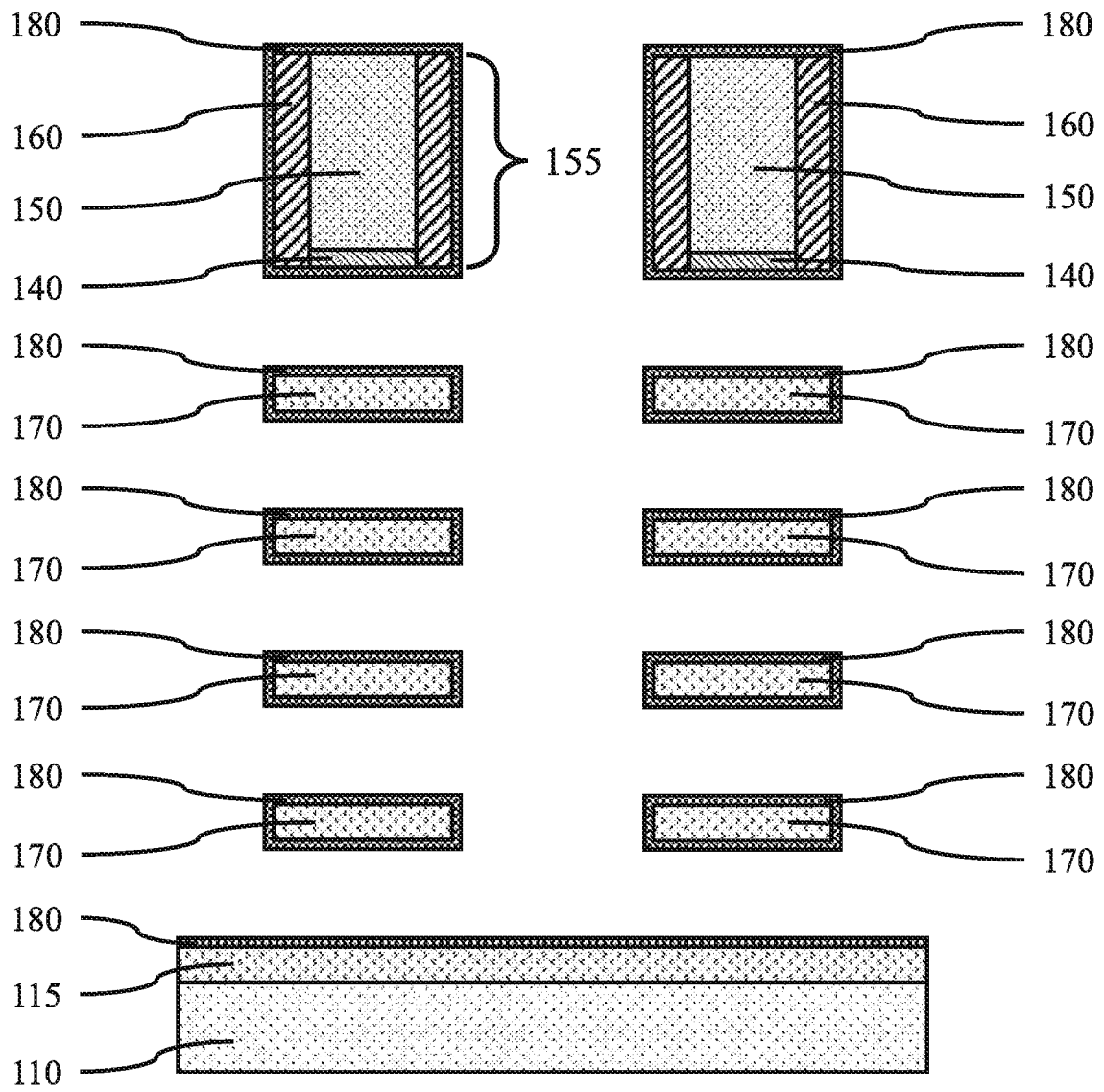


FIG. 4

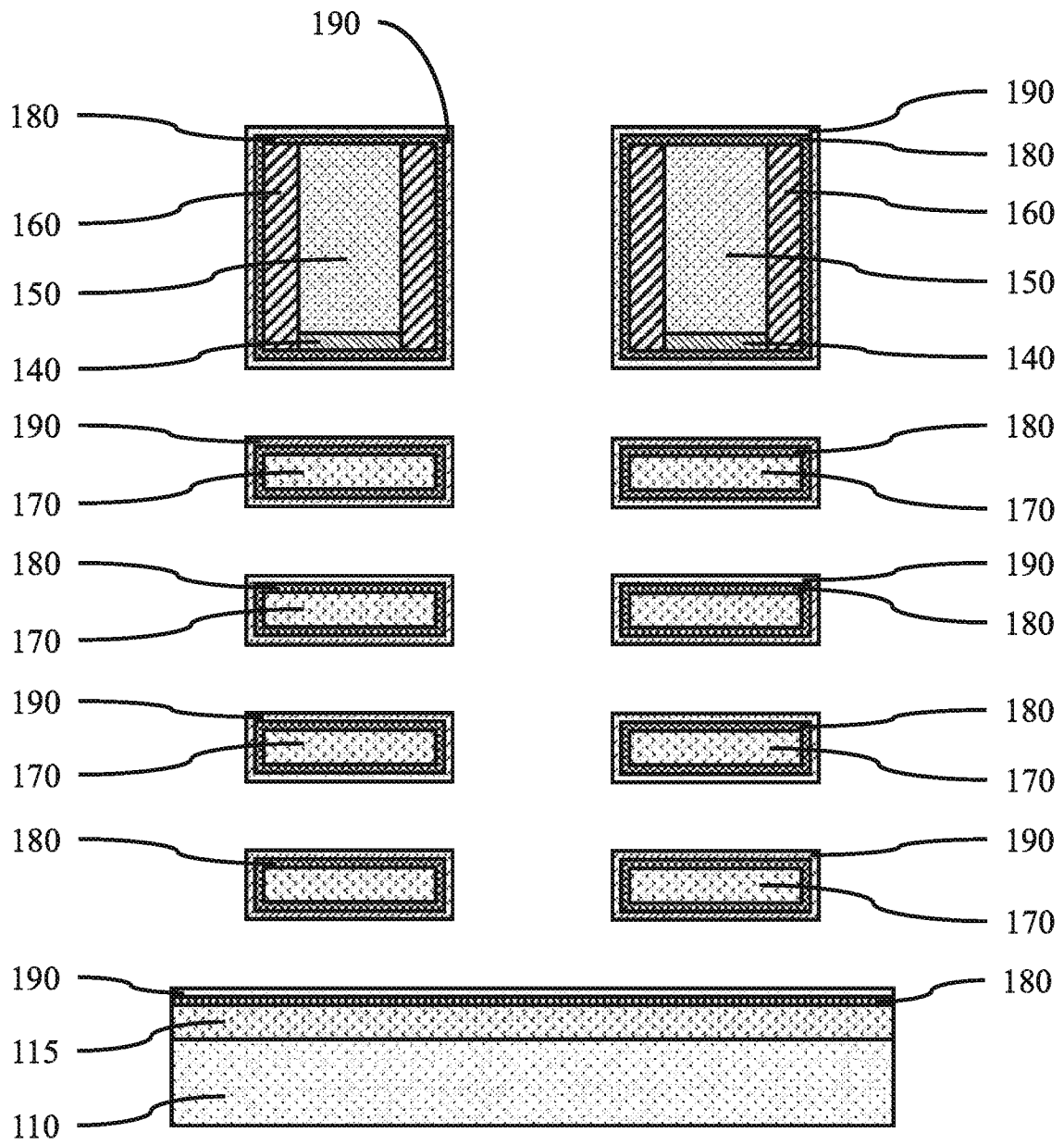


FIG. 5

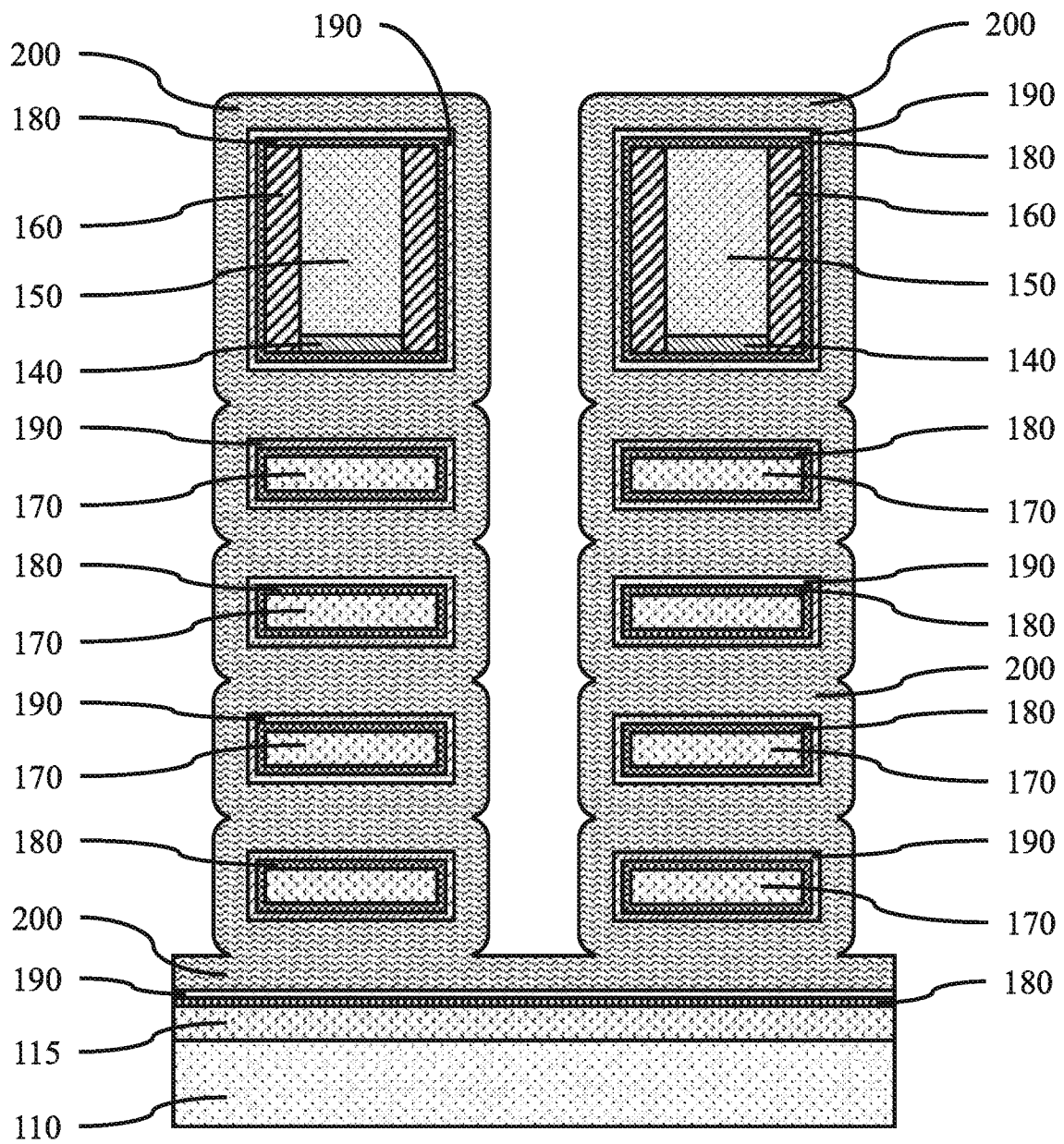


FIG. 6

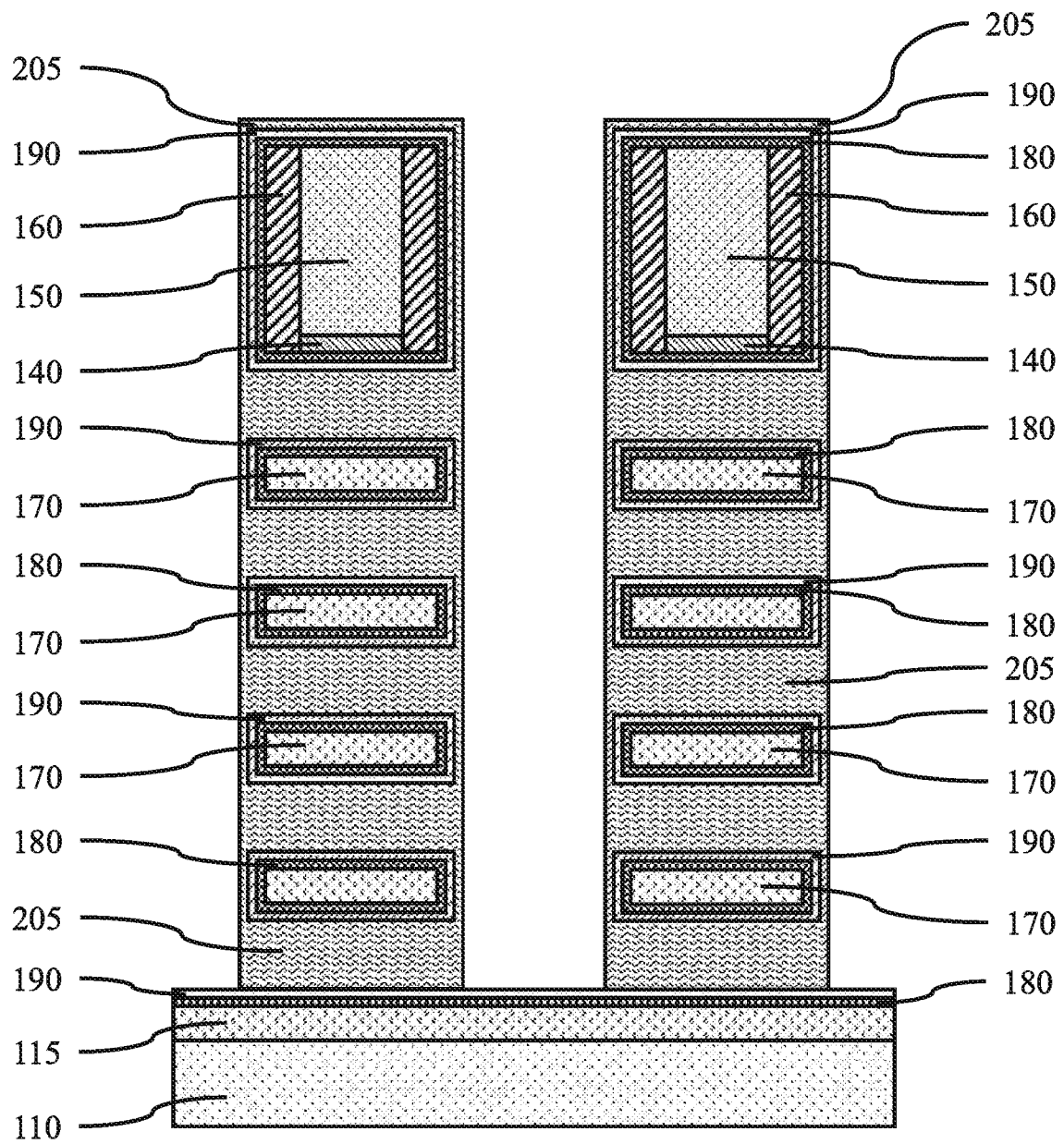


FIG. 7

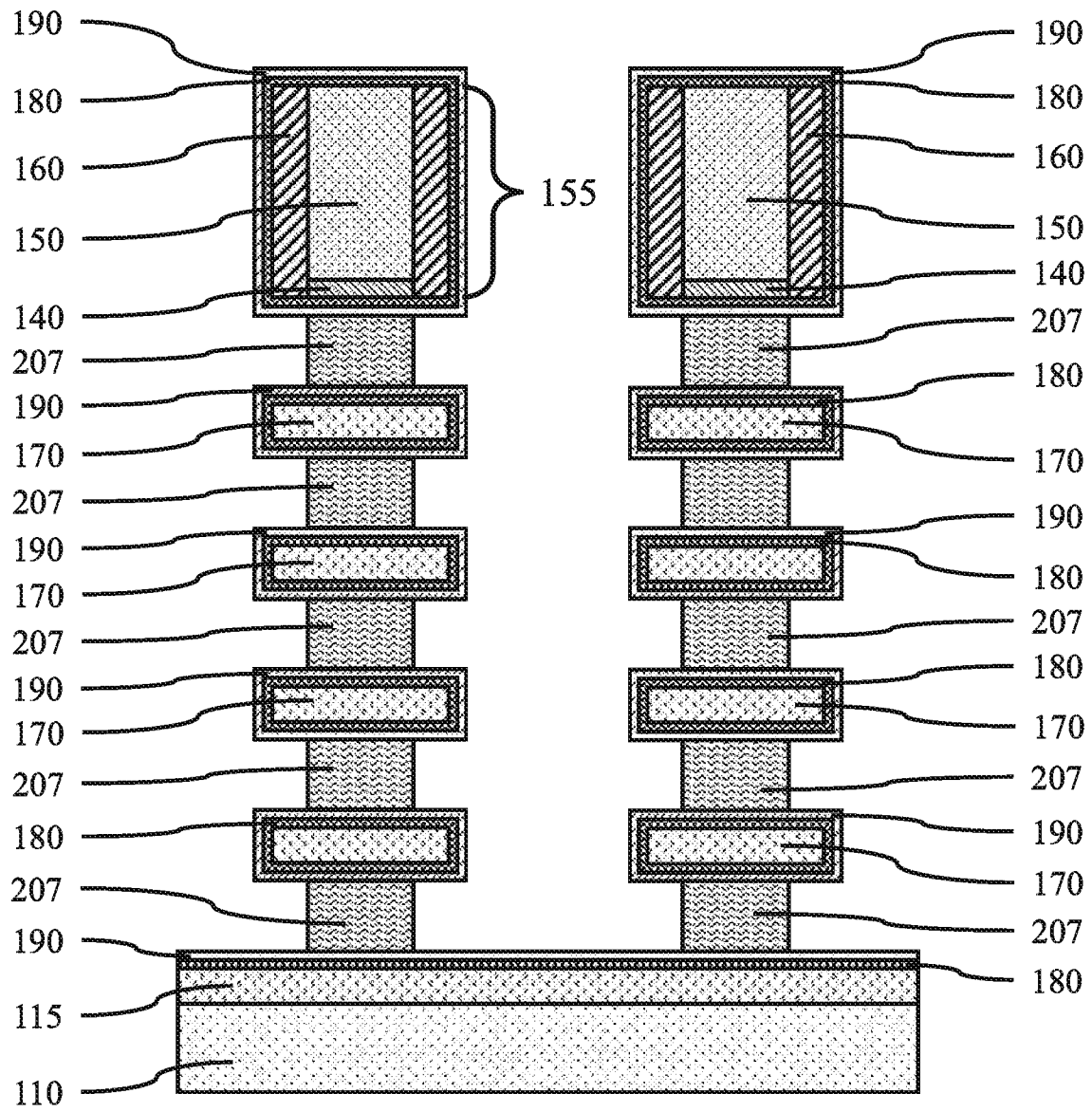


FIG. 8

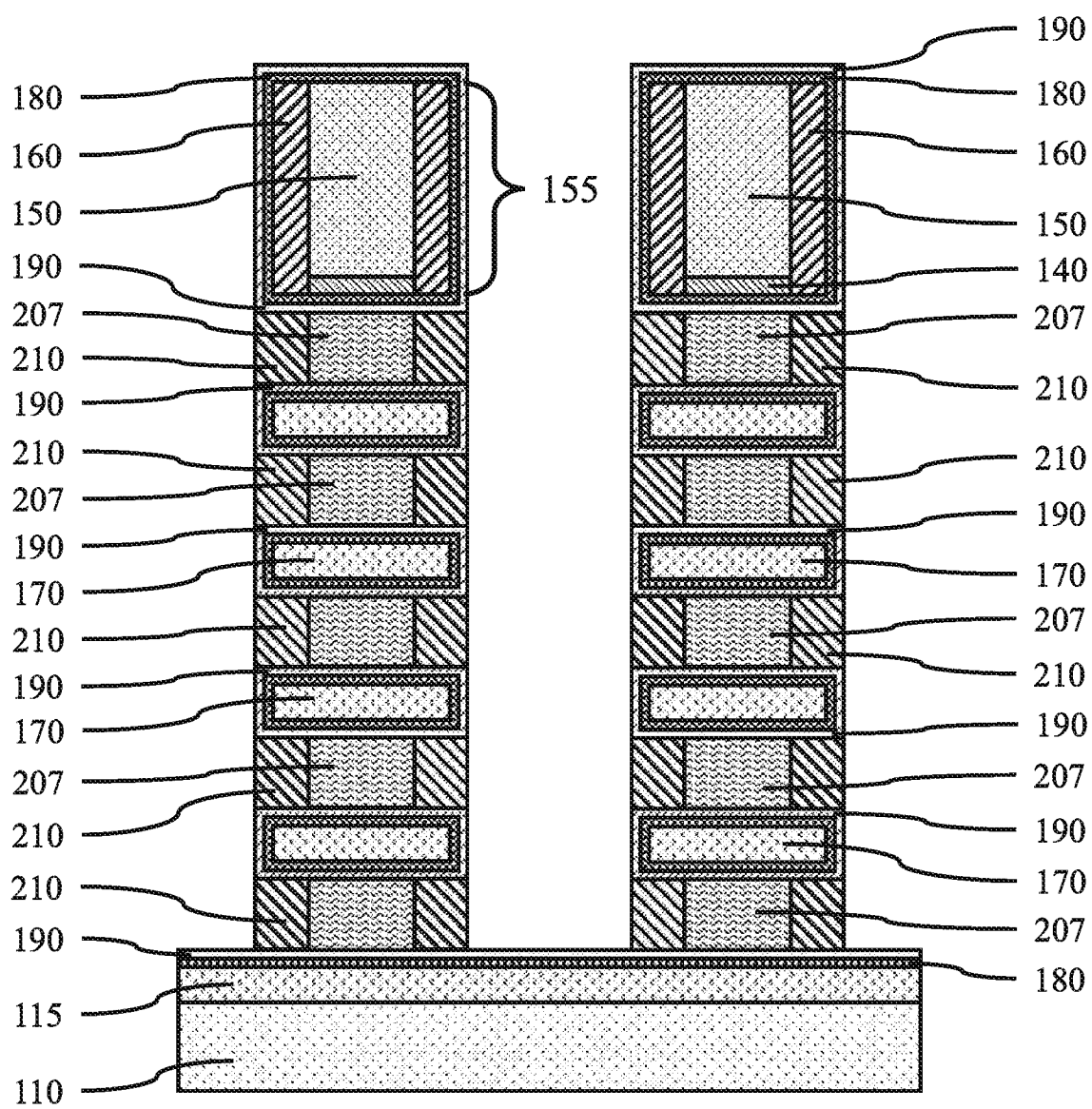


FIG. 9

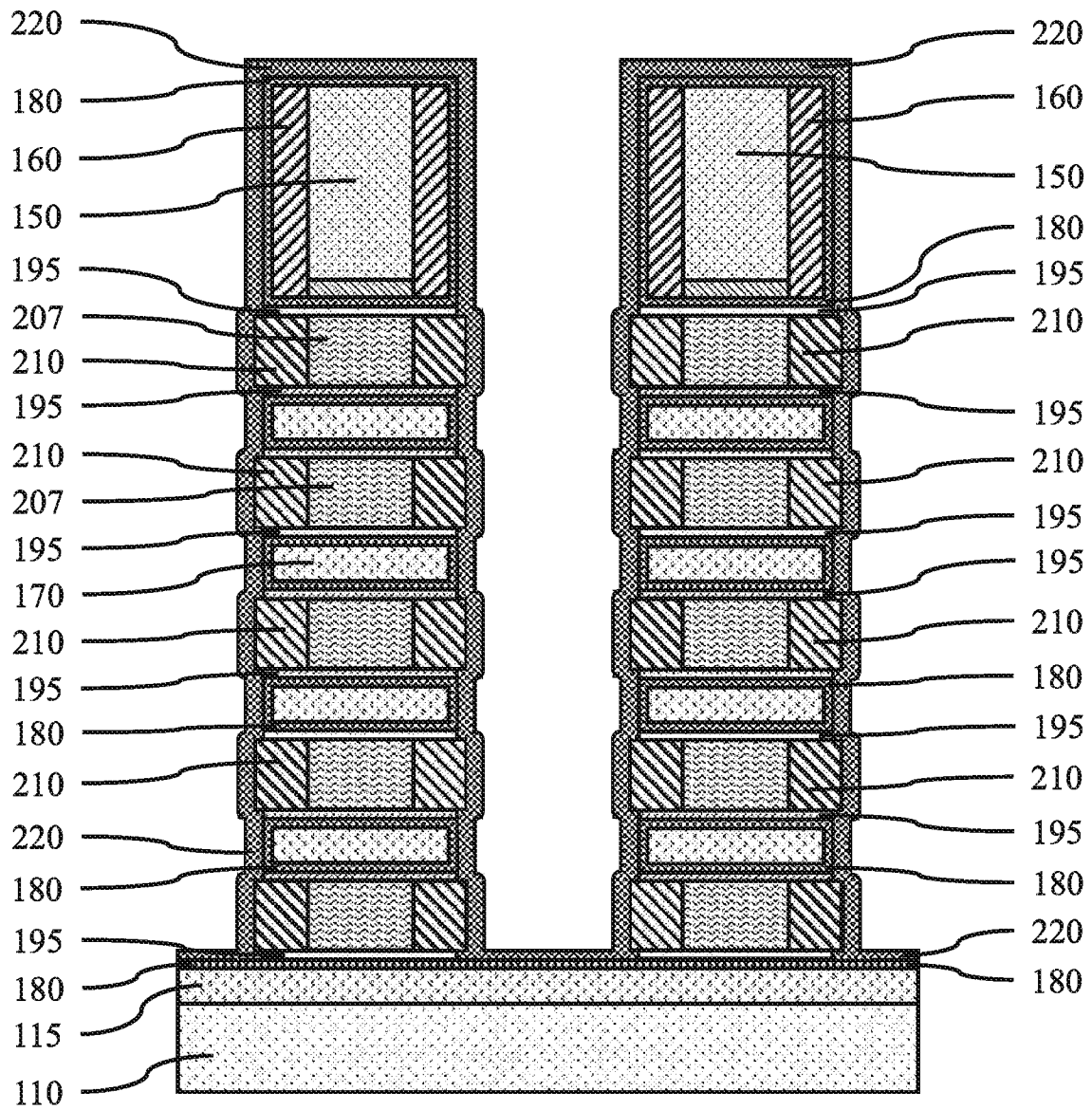


FIG. 10

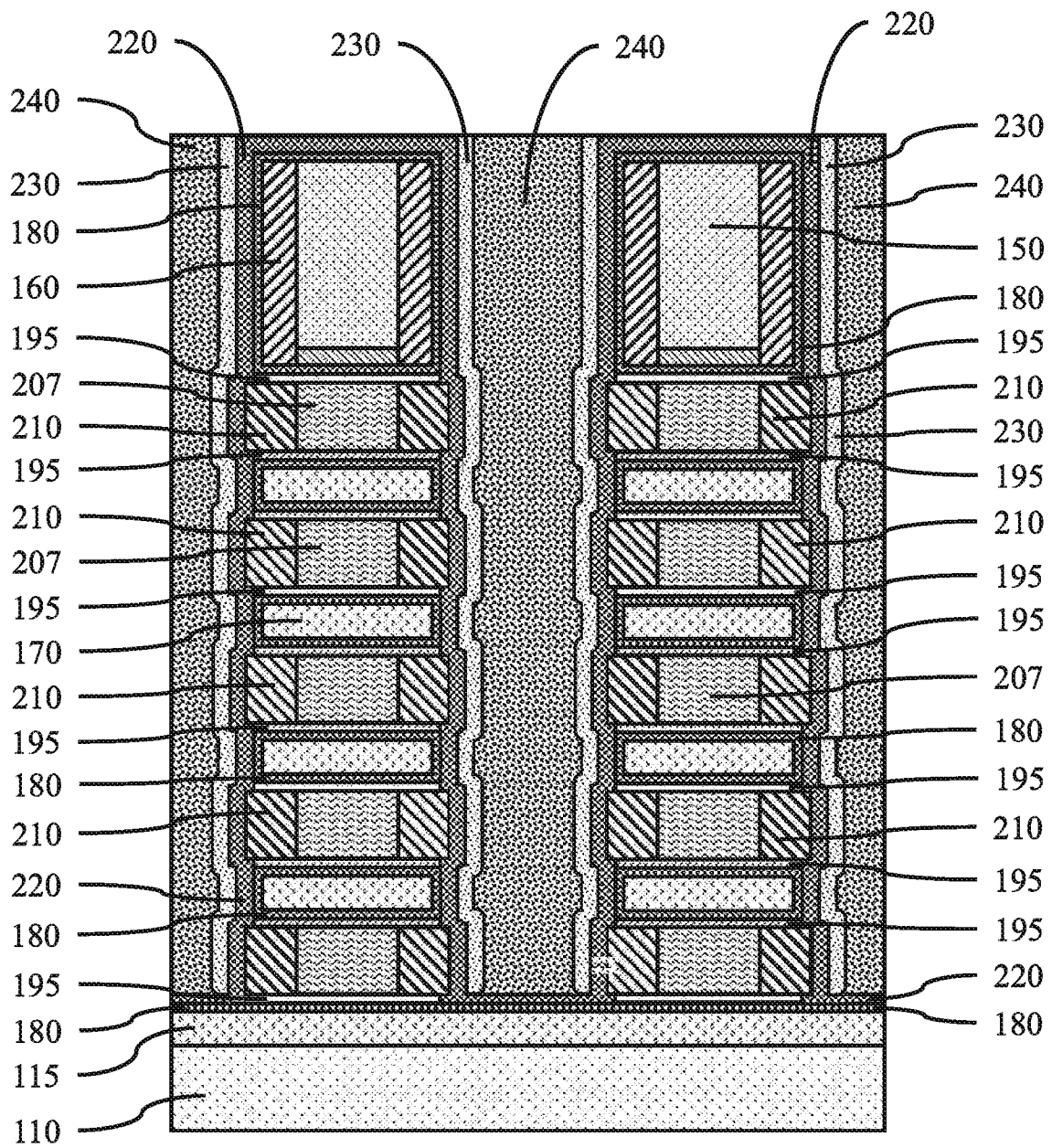


FIG. 11

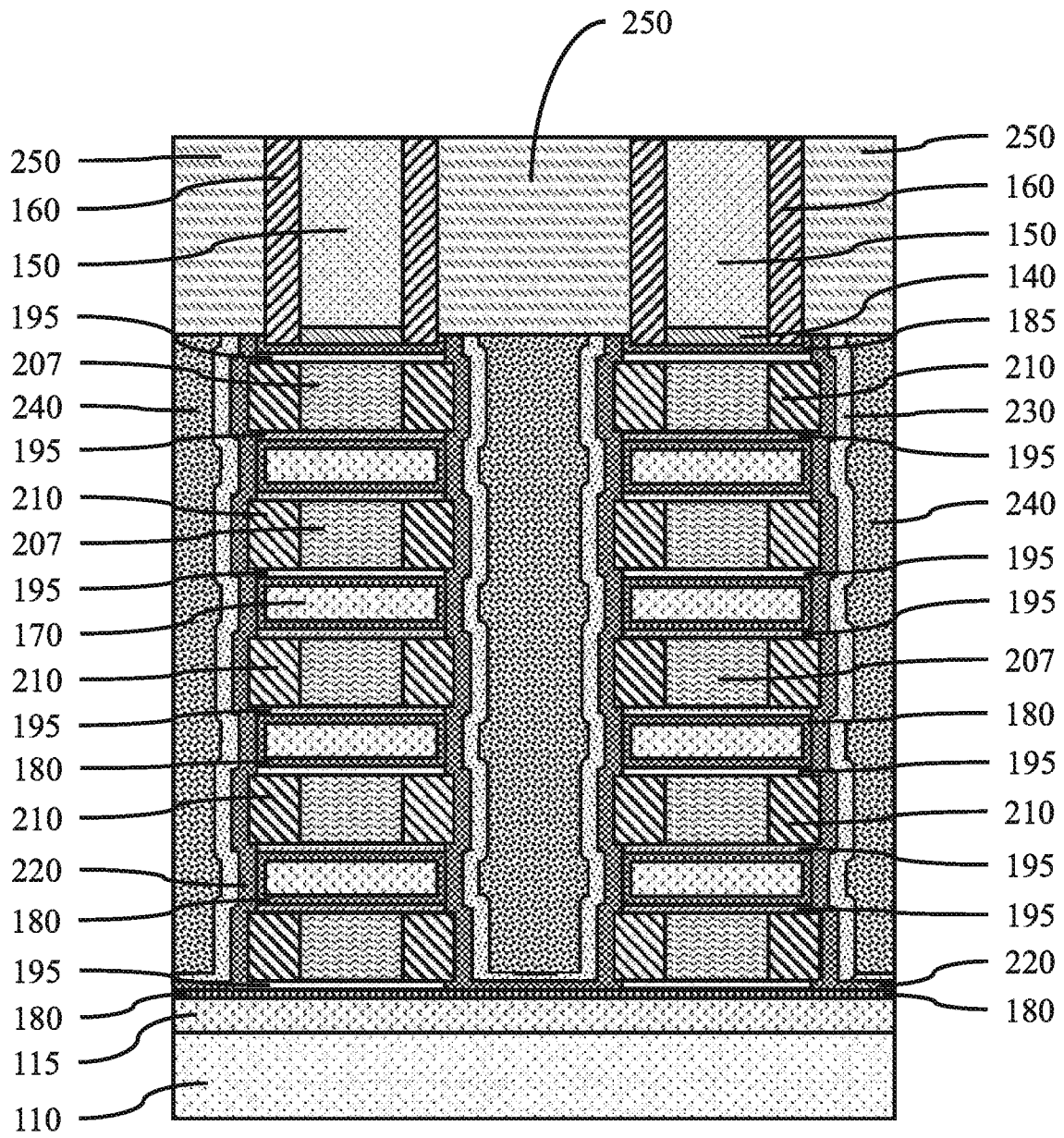


FIG. 12

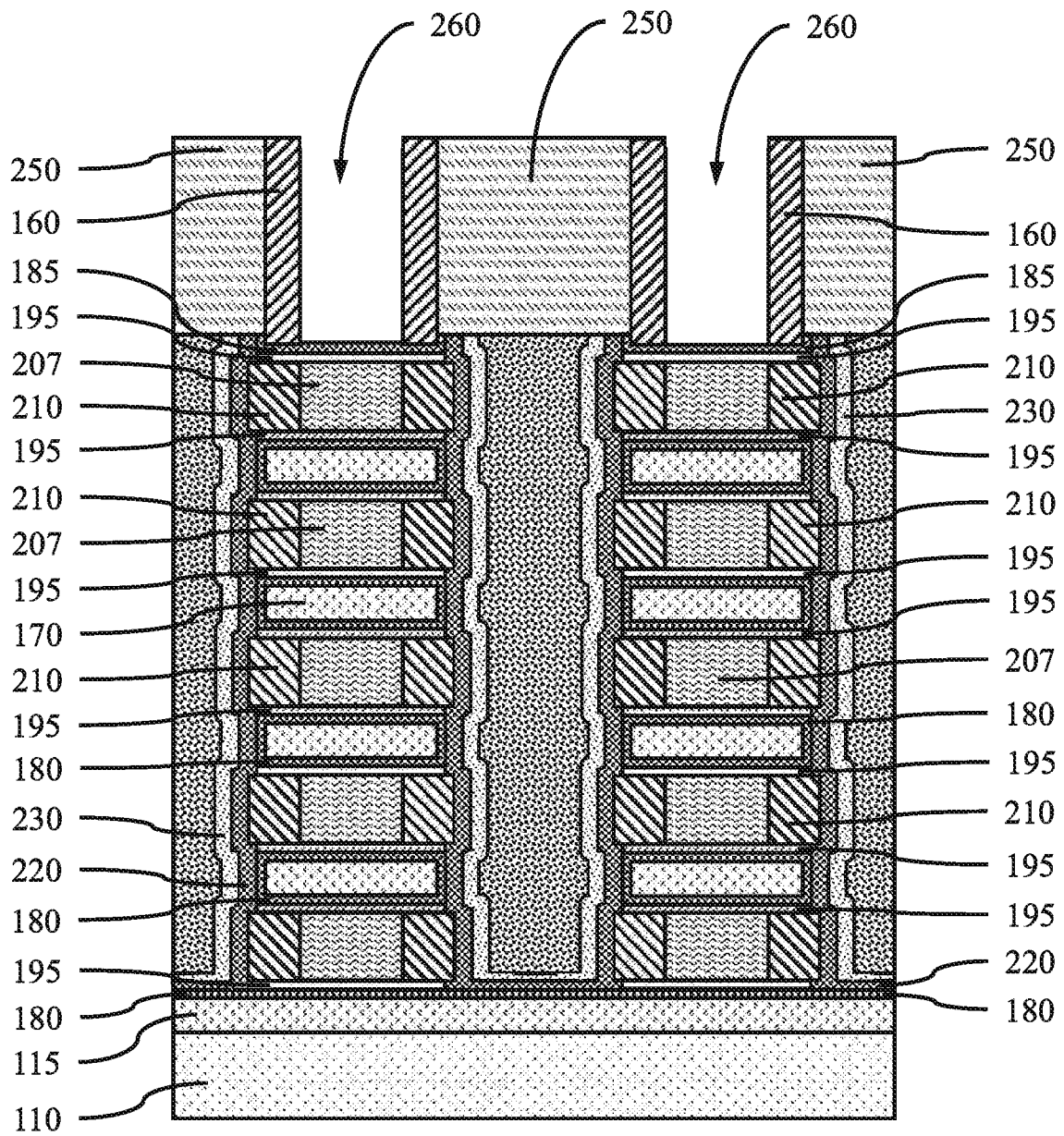


FIG. 13

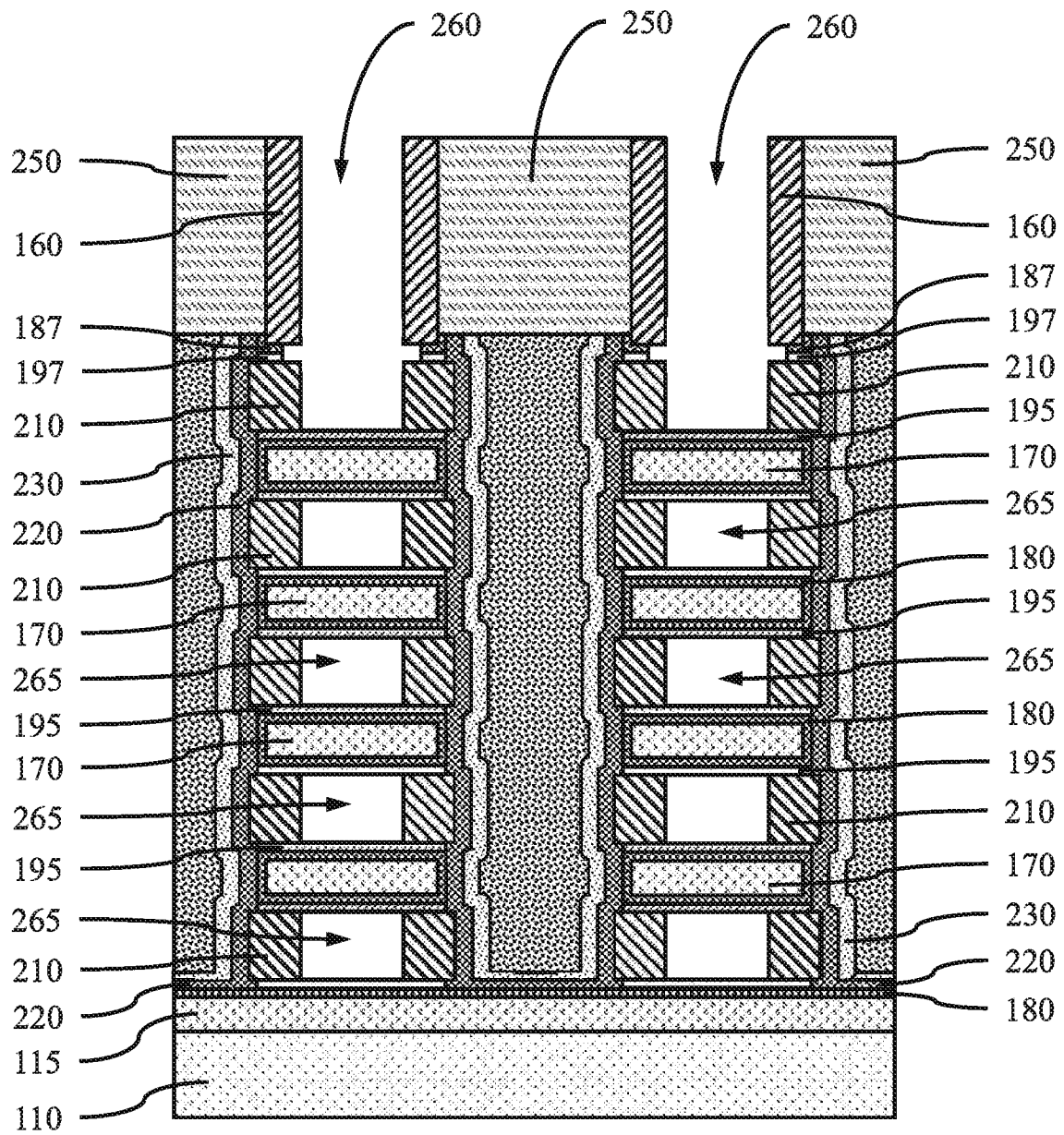


FIG. 14

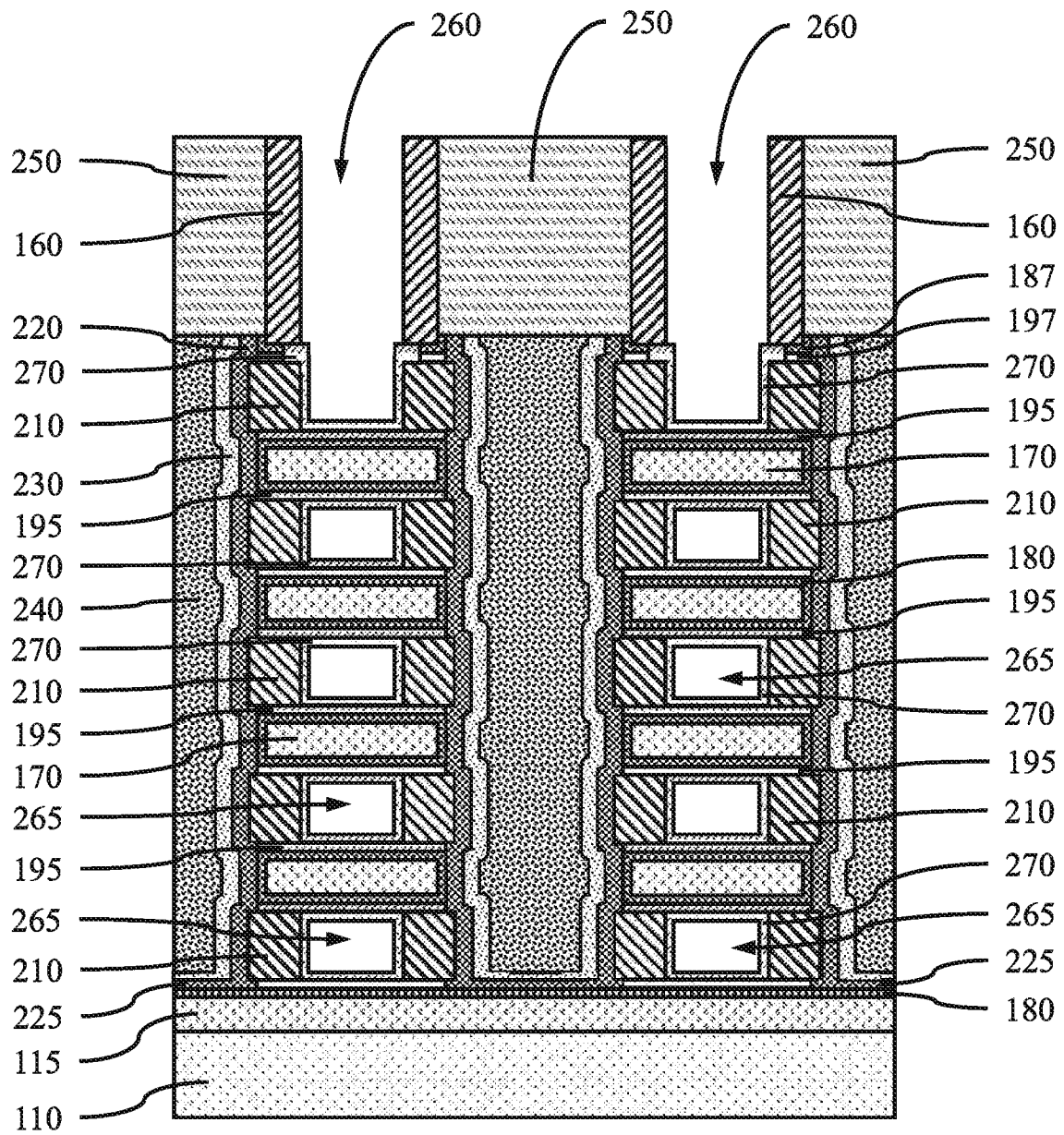


FIG. 15

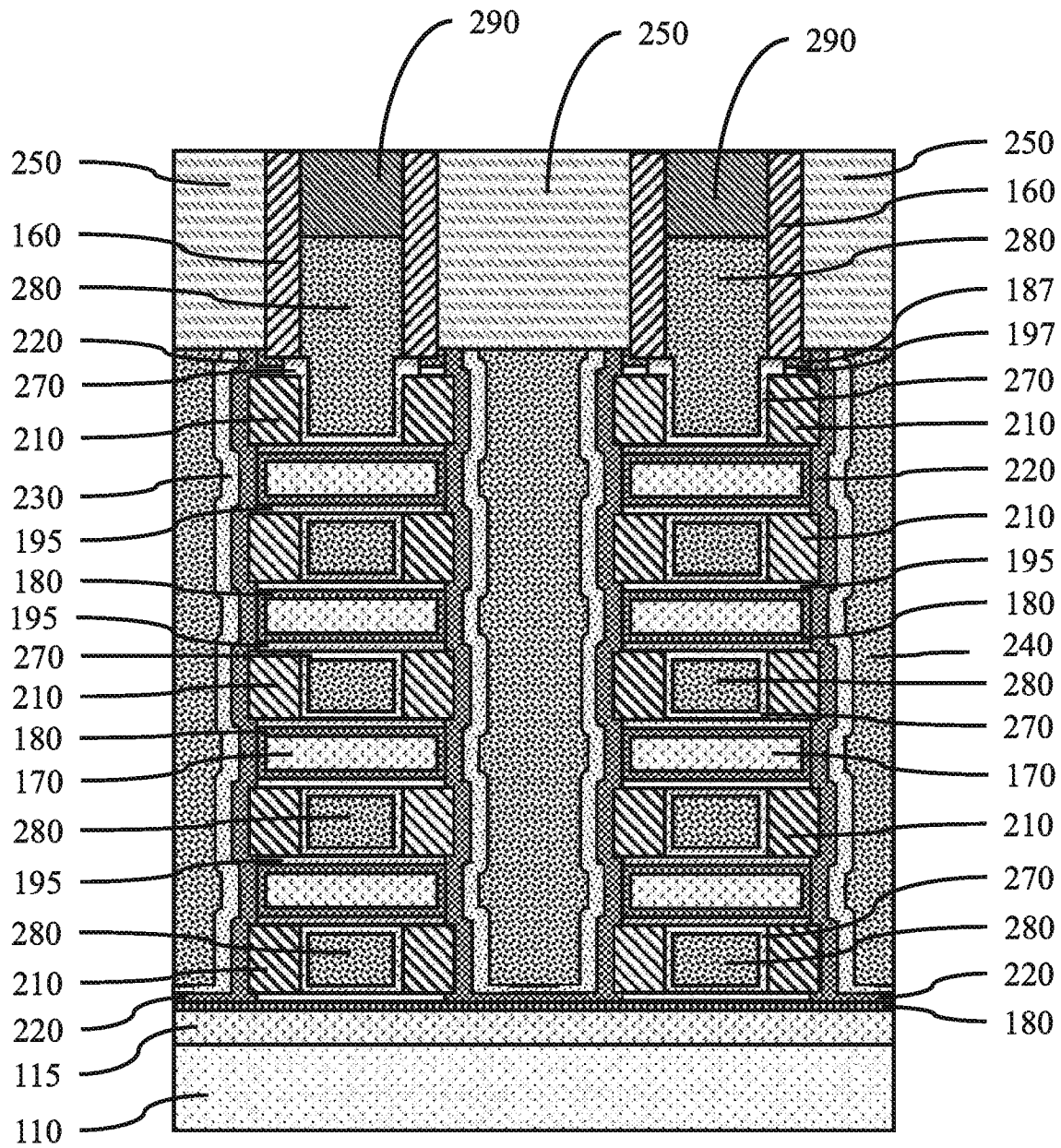


FIG. 16

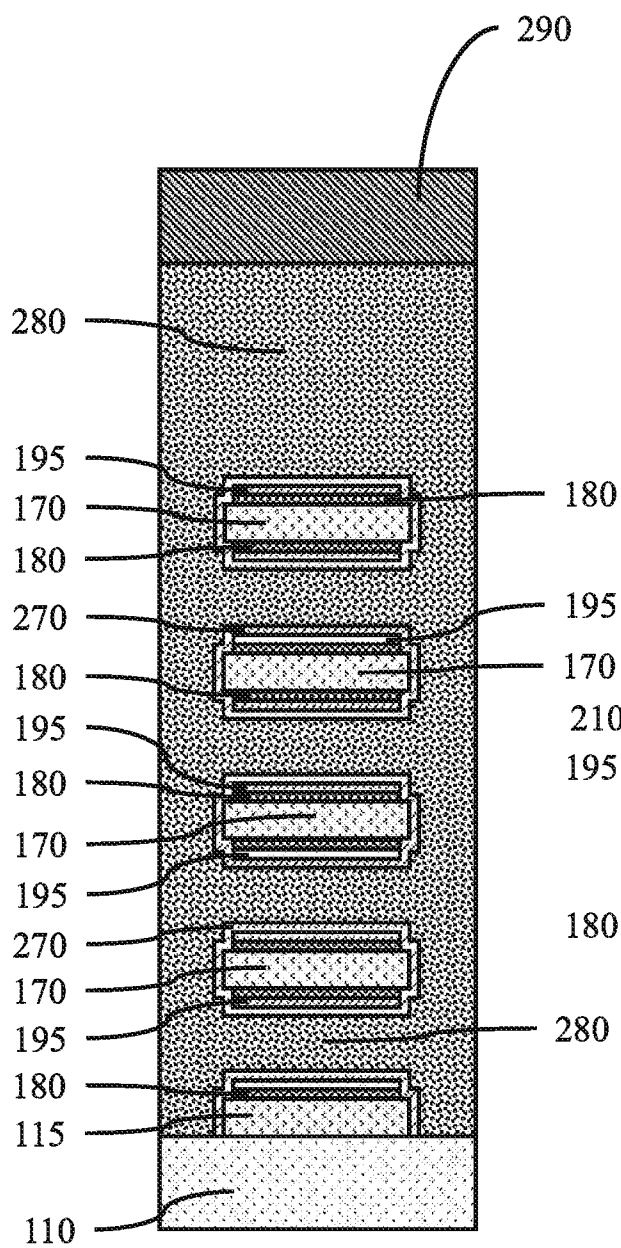


FIG. 17

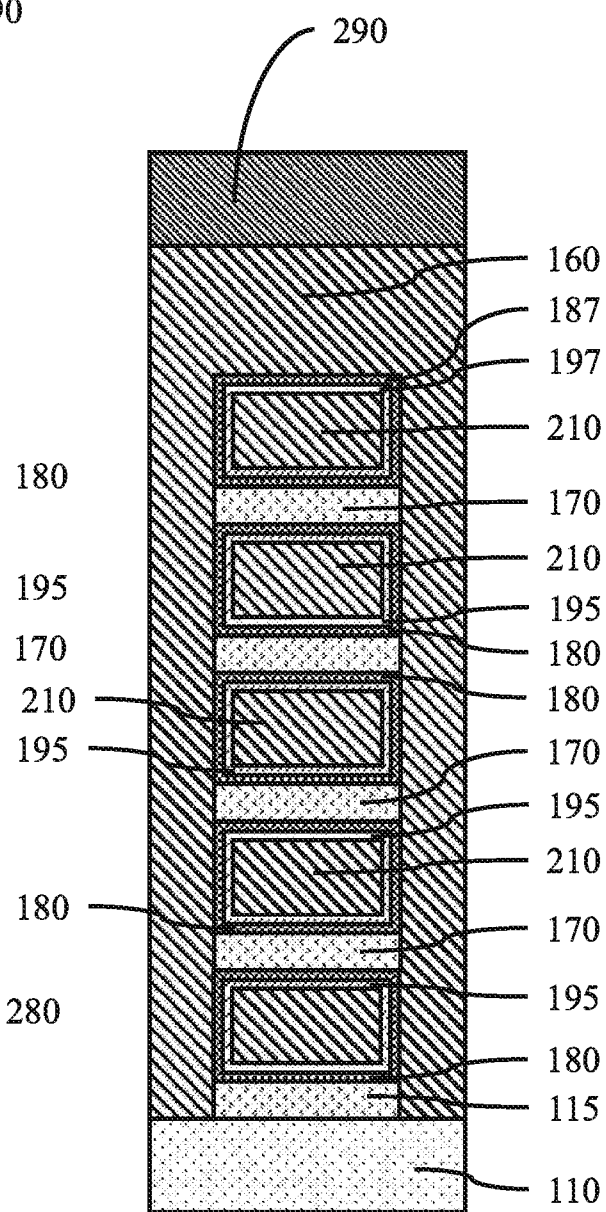


FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2022/103614

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i; H01L 21/336(2006.01)i; [] (2006.01)i; H01L 29/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI, IEEE: transistor, FET, 2D, two-dimensional, channel, stack, laminat+, vertical, planar, gate, source, drain, second, bridge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 112750908 A (GLOBALFOUNDRIES INC.) 04 May 2021 (2021-05-04) description, paragraphs [0017]-[0054], figures 1-16B	1-17
A	CN 103855091 A (INT. BUSINESS MACHINES CORP.) 11 June 2014 (2014-06-11) the whole document	1-20
A	CN 112133697 A (SAMSUNG ELECTRONICS CO., LTD.) 25 December 2020 (2020-12-25) the whole document	1-20
A	US 2016190343 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD. et al.) 30 June 2016 (2016-06-30) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

19 September 2022

Date of mailing of the international search report

23 September 2022

Name and mailing address of the ISA/CN

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6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
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Facsimile No. (86-10)62019451

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HUANG,Lina

Telephone No. 86-(10)-53961458

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2022/103614

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