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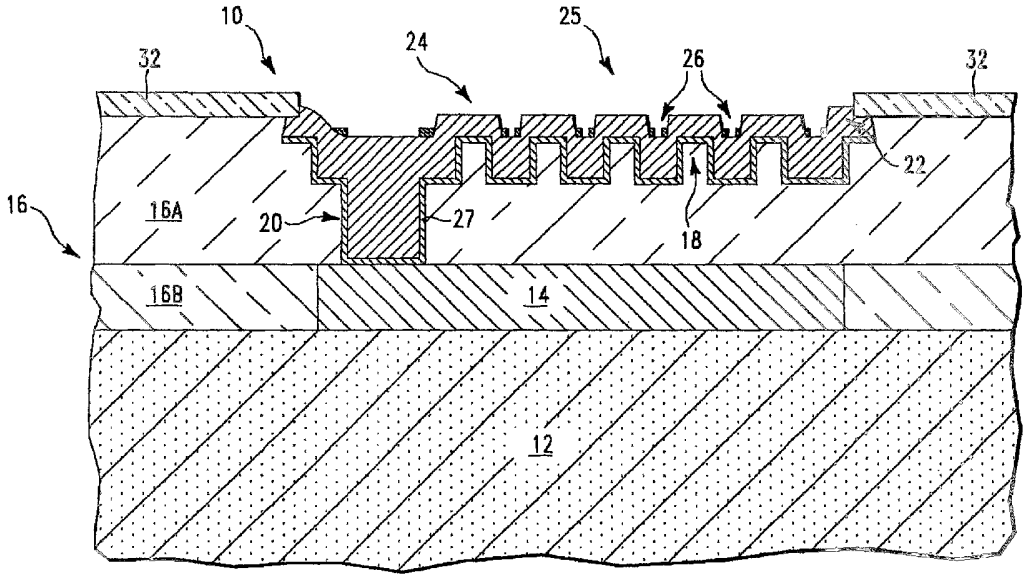
(54) Title: INTERNALLY REINFORCED BOND PADS



(57) Abstract: Disclosed is a reinforced bond pad structure having nonplanar dielectric structures and a metallic bond layer conformally formed over the nonplanar dielectric structures. The nonplanar dielectric structures are substantially reproduced in the metallic bond layer so as to form nonplanar metallic structures. Surrounding each of the nonplanar metallic structures is a ring of dielectric material which provides a hard stop during probing of the bond pad so as to limit the amount of bond pad that can be removed during probing.

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INTERNALLY REINFORCED BOND PADS

Field of the Invention

The present invention relates generally to integrated circuits and, more particularly, relates to integrated circuits having a mechanically robust bond pad.

Background of the Invention

Integrated circuits are formed on semiconductor substrates using a number of different processing operations that create the circuit elements. In order to access circuitry associated with the semiconductor substrate, bond pads are formed on the integrated circuits. Bond pads provide the means for transfer of electrical signals and power from and to the semiconductor substrate via probes, bonding wires, conductive bumps, etc.

Bond pads are typically formed of aluminum because aluminum is self-passivating and, therefore, more resistant to degradation from atmospheric pressure. Aluminum, and more recently, copper are used for the metal layers within the integrated circuit. Copper is more preferred because of its improved electromigration performance and ability to support higher current density as compared to aluminum.

In order to realize the advantages of the self-passivating character of aluminum and the superior electrical characteristics of copper, composite bond pad structures can be used in integrated circuit designs. In composite bond pad structures, copper is used for the underlying layer of the pad that interfaces with other layers in the integrated circuit. A corrosion-resistant aluminum capping layer is formed on top of the copper portion that creates an hermetic seal that protects the copper portion from atmospheric exposure. In order to physically separate the copper and aluminum portions of the composite bond pad while allowing for electrical connectivity, a relatively thin barrier metal layer may be formed at the interface.

Problems can arise in composite bond pad structures when test and probe operations are performed. To achieve good electrical continuity with the bond pad, elements such as probes must exert forces that can damage or displace portions of the bond pad surface. In addition, if the probe

exposes the underlying copper to the ambient, degradation of the copper can occur.

Another problem that can arise with bond pad structures concerns the physical force exerted on the bond pad by a probe that can propagate to lower layers based on the physical couplings within the integrated circuit. Low Young's modulus dielectrics underlying the bond pad may not be able to support such stress resulting from the force propagation.

Various solutions have been proposed for improving bond pad integrity.

Pozder et al. U.S. Patent Application Publication US 2001/0051426, discloses in Figure 2 a composite bond pad comprising copper (but alternatively could comprise aluminum), dielectric support structures and then a final layer of aluminum. The dielectric support structures can have different configurations as shown in Figure 5 of the reference. These support structures provide mechanical shielding of the interface formed between the aluminum layer and the underlying copper layer.

Ma et al. U.S. Patent Application Publication US 2002/0068385, discloses an anchored bond pad in which a bond pad is formed on a dielectric layer wherein the dielectric layer has via openings which are filled with metal. The metal-filled via openings secure the bond pad to the dielectric layer.

Ming-Tsung et al. U.S. Patent 5,703,408, discloses a bond pad structure in which stripes are formed in a sublayer which induce an irregular surface of the top metallic bond pad. An object of this particular arrangement is to increase the adhesion of the various layers that make up the bonding pad. Similarly, Mukogawa Japanese Published Patent Application JP 3-96236, the disclosure of which is incorporated by reference herein, discloses an irregular sublayer which induces an irregular surface of the top layer.

Saran et al. U.S. Patent 6,143,396, Saran U.S. Patent 6,232,662, Zhao U.S. Patent 6,198,170, and Saran et al. U.S. Patent 6,448,650, all disclose various reinforcing schemes under the bonding pad. Thus, in Saran et al. U.S. Patent 6,143,396, a metal bond pad is supported by a layer of dielectric and a reinforcing structure. In Saran U.S. Patent 6,232,662, a metal bond layer is supported by an interlevel dielectric layer and a reinforcing layer comprising metal and reinforcing dummy structures. In

Zhao U.S. Patent 6,198,170, a bonding pad is supported by a large via and several layers of alternating segments of metal and dielectric. Lastly, in Saran et al. U.S. Patent 6,448,650, a metal bonding pad is supported by a first dielectric, then an interlevel dielectric and finally by a reinforcing layer comprising alternating dielectric and metal.

A need exists for an improved bond pad that can survive forces applied by probing and packaging and which will protect the underlying metal layer, preferably which is copper.

Disclosure of the Invention

Accordingly, it is an object of the present invention to have an improved bond pad which is mechanically robust to survive the forces of probing and packaging.

It is another object of the present invention to have an improved bond pad which can survive probing and packaging and which can also protect the underlying metal layer.

These and other objects of the present invention will become more apparent after referring to the following description of the invention considered in conjunction with the accompanying drawings.

The objects of the invention have been achieved by providing, according to a first aspect of the invention, a reinforced bond pad structure comprising: a substrate; a metallic layer formed on the substrate; a dielectric layer over the metallic layer, at least one through via to the metallic layer and at least a portion of the dielectric layer comprising a plurality of nonplanar dielectric structures; a metallic bond layer conformally formed over the nonplanar structures of the dielectric layer such that the nonplanar dielectric structures are substantially reproduced in the metallic bond layer as nonplanar metallic structures, the metallic bond layer further formed in the through via so as to contact the metallic layer; and a ring of dielectric material surrounding each of the nonplanar metallic structures.

According to a second aspect of the invention, there is provided a method of forming internally reinforced bond pads, the method comprising the steps of: forming a metallic layer on a substrate; forming a first dielectric layer over the metallic layer; patterning a first portion of the first dielectric layer so as to form at least one through via to the

metallic layer and a plurality of nonplanar dielectric structures, a second portion of the first dielectric layer being unpatterned; conformally depositing a metallic bond layer over the nonplanar dielectric structures and into the through via such that the nonplanar dielectric structures are substantially reproduced in the metallic bond layer as nonplanar metallic structures; forming a second dielectric layer over the nonplanar metallic structures and the unpatterned portion of the first dielectric layer; and removing substantially all of the second dielectric layer over the nonplanar metallic structures except for a ring of dielectric material surrounding each of the nonplanar metallic structures.

Brief descriptions of the drawings

Embodiments of the invention are described below in detail, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a cross sectional view of a semiconductor device having an internally reinforced bonding pad;

Figures 2 to 5 illustrate a preferred process for forming the semiconductor device of Figure 1;

Figure 6 is a top view of the internally reinforced bonding pad; and Figure 7 is an enlarged partial cross sectional view of an internally reinforced bonding pad being probed.

Detailed description of the drawings

Referring to the Figures in more detail, and particularly referring to Figure 1, there is shown a cross sectional view of a semiconductor device 10 having a reinforced bond pad structure 25. The semiconductor device 10 includes a substrate 12 which may be semiconductor material such as silicon, silicon germanium, and the like, or more typically, is a previous wiring level already fabricated on the semiconductor material. For the sake of clarity, details of any previous wiring levels are not shown. Also included in semiconductor device 10 is metallic layer 14 formed on substrate 12 and dielectric layer 16 formed on metallic layer 14 as well as substrate 12. Dielectric layer 16 may be comprised of two separately formed dielectric layers 16A, 16B, if desired. The metallic material may be aluminum or copper but preferably is copper. The nominal thickness of the metallic layer is usually 0.4 to 1.2 microns. The dielectric layer 16 is then patterned to form at least one through via 20

and a plurality of nonplanar dielectric structures 18. The thickness of the dielectric layer 16 is nominally 0.5 to 10 microns.

A metallic bond layer 22, preferably aluminum, is then conformally formed over the nonplanar dielectric structures 18. The thickness of the metallic bond layer 22 above the nonplanar dielectric structures 18 should be about 0.4 to 1.5 microns, preferably 1.2 microns. Since the metallic bond layer 22 is conformally formed, the nonplanar dielectric structures 18 will be substantially reproduced in the metallic bond layer 22 to form nonplanar metallic structures 24. By "substantially reproduced" is meant that the general shape is reproduced but not exactly. That is, where the sides of the nonplanar dielectric structures 18 may be vertical, the sides of the nonplanar metallic structures 24 may be sloped. Also, where the corners of the nonplanar dielectric structures 18 may be sharp, the corners of the nonplanar metallic structures 24 may be rounded. The metallic bond layer 22 also fills through via 20 to make electrical contact with metallic layer 14.

Lastly, the completed reinforced bond pad structure 25 includes a ring of dielectric material 26 around the nonplanar metallic structures 24. It has been found that this ring of dielectric material 26, in addition to the nonplanar dielectric structures 18, is beneficial during probing of the bond pad. The ring of dielectric material 26 may be any dielectric material such as silicon nitride (SiN_x) or silicon oxide (SiO_2) and in a thickness of about 0.1 to 0.2 microns. A top view of the bond pad structure 25 with the nonplanar metallic structures 24 and rings of dielectric material 26 is illustrated in Figure 6.

The underlying nonplanar dielectric structures 18 provide mechanical support to the bond pad structure 25 during probing. In addition, as frequently happens, the overlying metallic bond layer 22 may be scraped off during probing but the nonplanar dielectric structures 18 and ring of dielectric material 26 prevent the probe from removing all of the metallic bond layer 22. The nonplanar dielectric structures 18 and ring of dielectric material 26 cooperate to provide a hard stop to the probe. Referring to Figure 7, probe 40 moving in the direction indicated by arrow 42 has removed a portion of nonplanar metallic structure 24. The cumulative total of the removed portions of nonplanar metallic structures 24 is indicated by ball 44. As can be seen from Figure 7, the ring of dielectric material 26 provides a hard stop beyond which the probe 40 can not remove any further metallic material of nonplanar metallic structure 24.

The nonplanar dielectric structures 18, and hence also nonplanar metallic structures 24, can take any form such as columns or stripes. Viewed from the top, the nonplanar metallic structures 24 can be circles (as shown in Figure 6), rectangles or polygons. No matter their shape, they should be spaced closer together than the diameter (or other cross sectional dimension) of the probe so that the probe cannot penetrate in between the nonplanar dielectric structures 18 to adversely affect the remaining metallic bond layer 22. For example, for an 18 micron probe tip, the nominal spacing of the nonplanar dielectric structures 18 should be a maximum of about 17 microns. Further, it is preferable that the nonplanar dielectric structures 18 should be made as small as possible, on the order of 0.5 to 1 microns in width. The size of the nonplanar dielectric structures 18 is limited only by lithography and etch capabilities. Moreover, it is best to have the nonplanar dielectric structures 18 spaced as far apart as possible so long as they are less than the probe dimension.

If metallic layer 14 is copper and metallic bond layer 22 is aluminum, it would be desirable to have a barrier layer 27 at the bottom of through via 20. Such a barrier layer 27 could comprise, for example, Ta/TaN, TaN, Ti/TiN, W or a combination thereof. As a practical matter, the barrier layer 27 would be present throughout the bond pad structure 25 as shown in the Figures.

Referring now to Figures 2 through 5, the method for forming the reinforced bond pad structure 25 of Figure 1 will be discussed. Referring first to Figure 2, metallic layer 14 (the last internal wiring level) is conventionally formed on substrate 12. Thereafter, dielectric layer 16 (or separate dielectric layers 16A, 16B) is conventionally formed on substrate 12 and metallic layer 14. Dielectric layer 16 is patterned by conventional means to form through via 20 and nonplanar dielectric structures 18. As noted previously, if metallic layer 14 is copper and the metal to be subsequently deposited in through via 20 is aluminum, then it may be desirable to deposit barrier layer 27 at the bottom of through via 20.

Thereafter, as shown in Figure 3, a blanket layer of metallic material is deposited over dielectric layer 16 and then patterned to result in the structure shown in Figure 3. The metallic bond layer 22 fills the through via 20 with metallic material 30 and fills the spaces between nonplanar dielectric structures 18 with metallic material 28. Also formed at this time are nonplanar metallic structures 24 which substantially correspond in shape to nonplanar dielectric structures 18.

The method of depositing metallic bond layer 22 is unimportant to the present invention. Generally speaking, the thickness of the metallic bond layer 22 should be greater than the height of the nonplanar dielectric structures 18. As an example, if the height of the nonplanar dielectric structures 18 are 0.85 microns, the thickness of the metallic bond layer 22 could be 1.2 microns.

Referring now to Figure 4, dielectric layer 32 is conventionally blanket deposited over dielectric layer 16 and metallic bond layer 22. Portions of dielectric layer 32 are masked 34 and then the unmasked portions of the dielectric layer 32 are subjected to a dry etchant such as reactive ion etching (RIE), indicated by arrows 36, to substantially remove all of dielectric layer 32 over metallic layer 22. After RIE (or other suitable etching step), there is only a small portion of the dielectric layer 32 left surrounding the nonplanar metallic structures 24. These remaining small portions of the dielectric layer 32 are the ring of dielectric material 26 that surrounds each of the nonplanar metallic structures 26 as shown in Figure 5.

CLAIMS

1. A reinforced bond pad structure comprising:

a substrate;

a metallic layer formed on the substrate;

a dielectric layer over the metallic layer, at least one through via to the metallic layer and at least a portion of the dielectric layer comprising a plurality of nonplanar dielectric structures;

a metallic bond layer conformally formed over the nonplanar structures of the dielectric layer such that the nonplanar dielectric structures are substantially reproduced in the metallic bond layer as nonplanar metallic structures, the metallic bond layer further formed in the through via so as to contact the metallic layer; and

a ring of dielectric material surrounding each of the nonplanar metallic structures.

2. The reinforced bond pad structure of claim 1 wherein the metallic layer is copper.

3. The reinforced bond pad structure of claim 1 wherein the metallic bond layer comprises aluminum.

4. The reinforced bond pad structure of claim 1 wherein the nonplanar metallic structures comprise columns or stripes.

5. The reinforced bond pad structure of claim 1 wherein the nonplanar dielectric structures have vertical sides.

6. The reinforced bond pad structure of claim 1 wherein there is a barrier layer between the metallic layer and the metallic bond layer.

7. The reinforced bond pad structure of claim 1 wherein the ring of dielectric material comprises silicon nitride or silicon oxide

8. A method of forming internally reinforced bond pads, the method comprising the steps of:

forming a metallic layer on a substrate;

forming a first dielectric layer over the metallic layer;

patterning a first portion of the first dielectric layer so as to form at least one through via to the metallic layer and a plurality of nonplanar dielectric structures, a second portion of the first dielectric layer being unpatterned;

conformally depositing a metallic bond layer over the nonplanar dielectric structures and into the through via such that the nonplanar dielectric structures are substantially reproduced in the metallic bond layer as nonplanar metallic structures;

forming a second dielectric layer over the nonplanar metallic structures and the unpatterned portion of the first dielectric layer; and

removing substantially all of the second dielectric layer over the nonplanar metallic structures except for a ring of dielectric material surrounding each of the nonplanar metallic structures.

9. The method of claim 8 wherein the nonplanar metallic structures comprise columns or stripes.

10. The method of claim 8 wherein the nonplanar dielectric structures have vertical sides.

11. The method of claim 8 wherein there is a barrier layer between the metallic layer and the metallic bond layer.

12. The method of claim 8 wherein the ring of dielectric material comprises silicon nitride or silicon oxide.

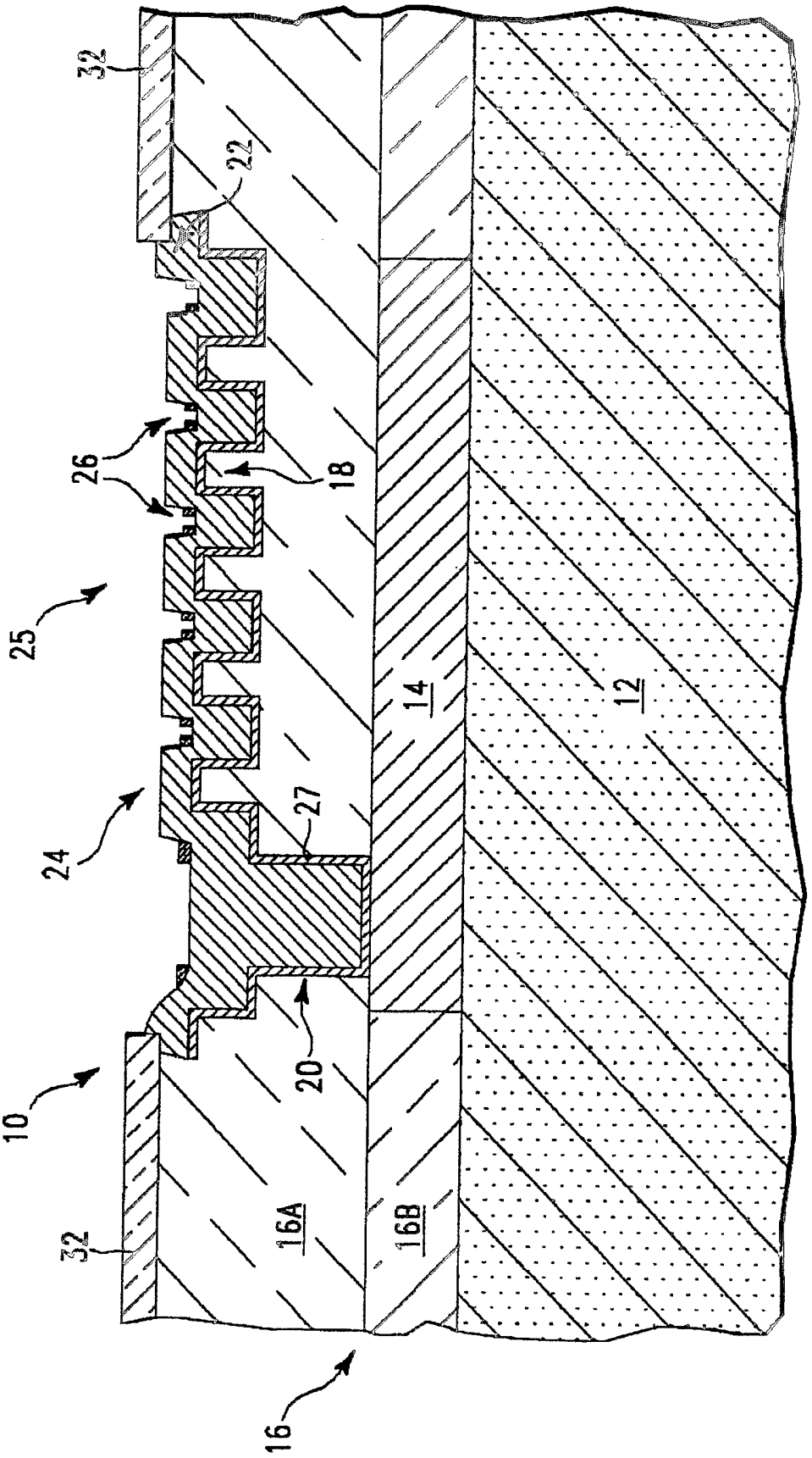

FIG. 1

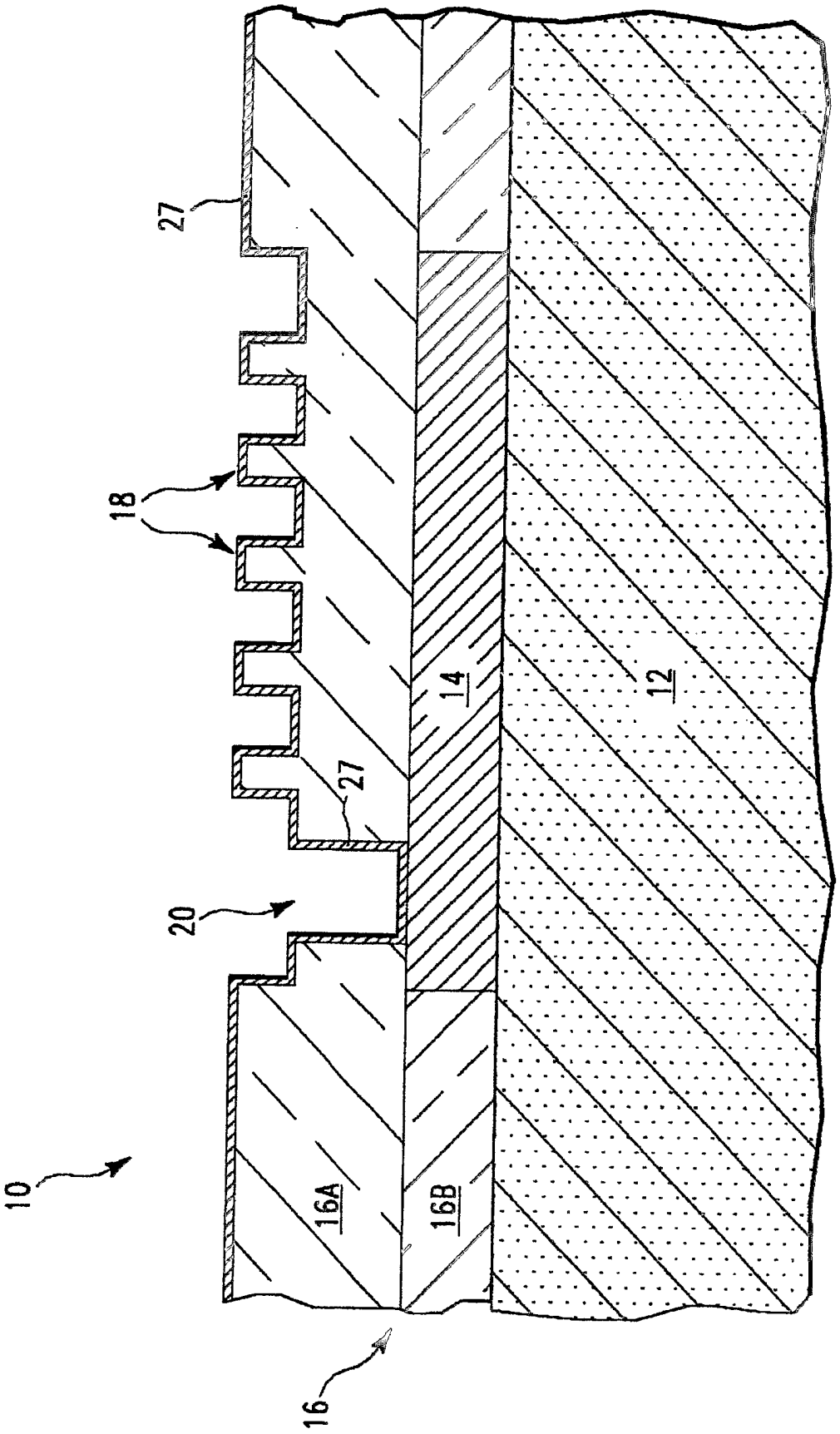

FIG. 2

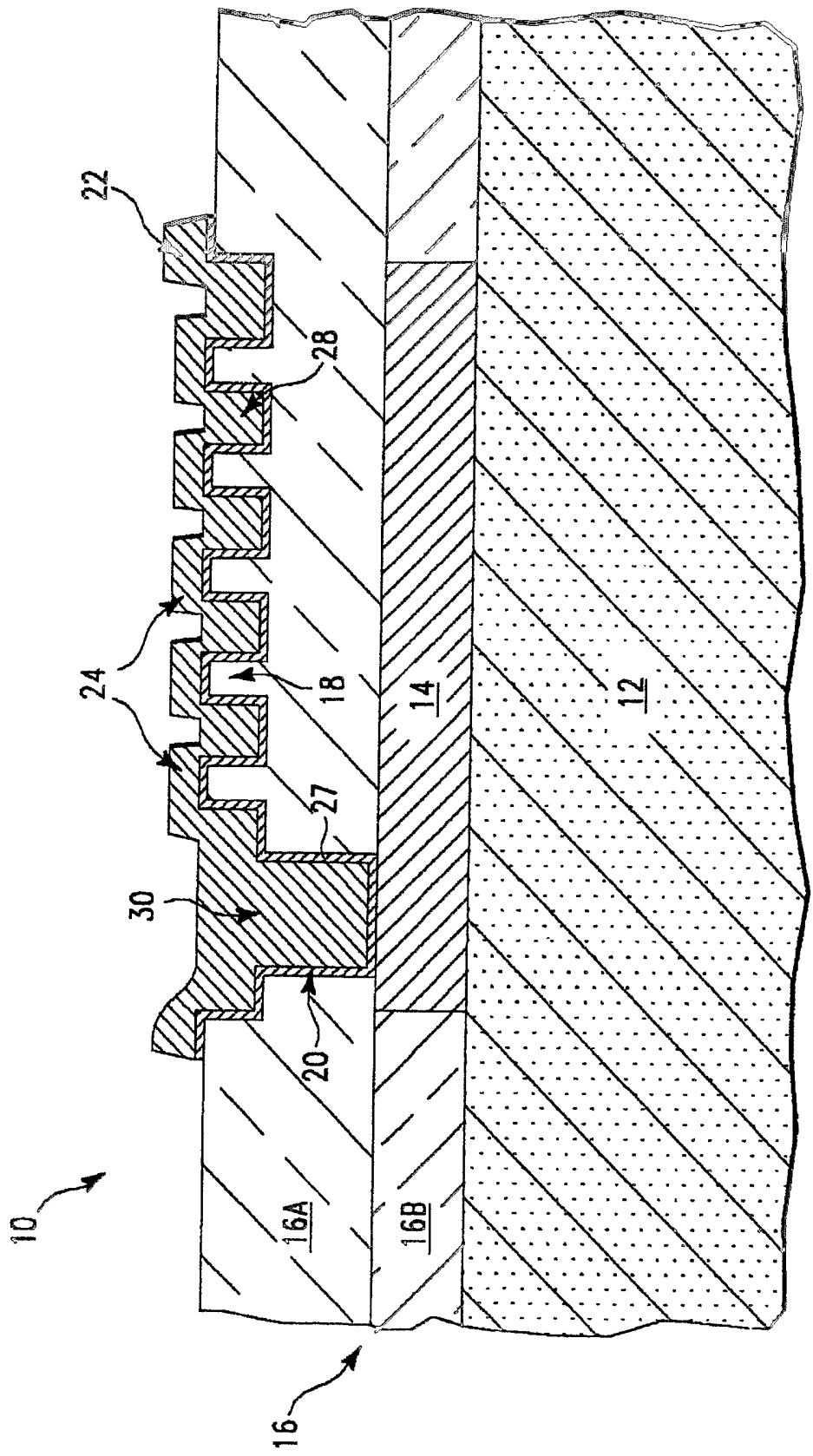

FIG. 3

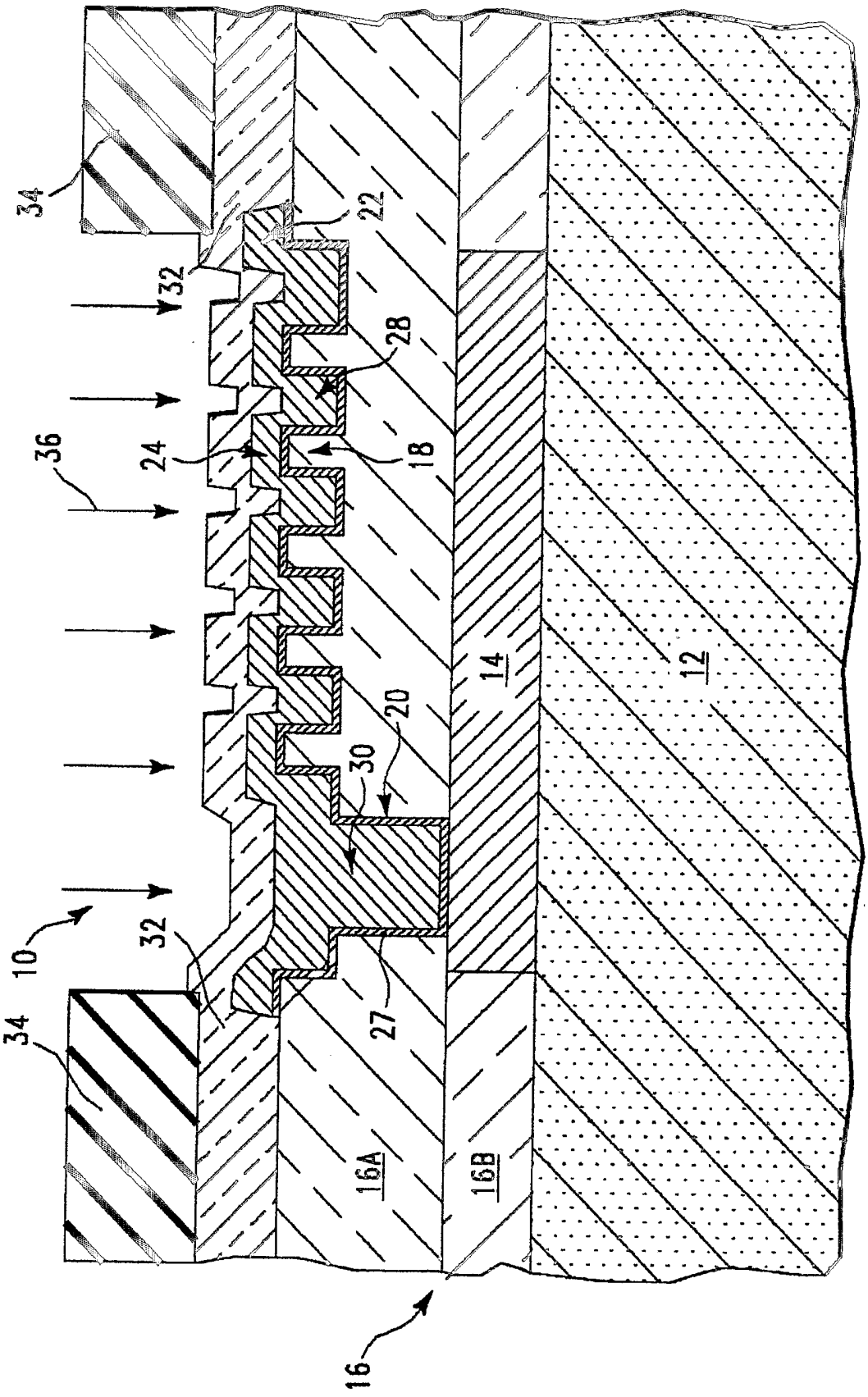

FIG. 4

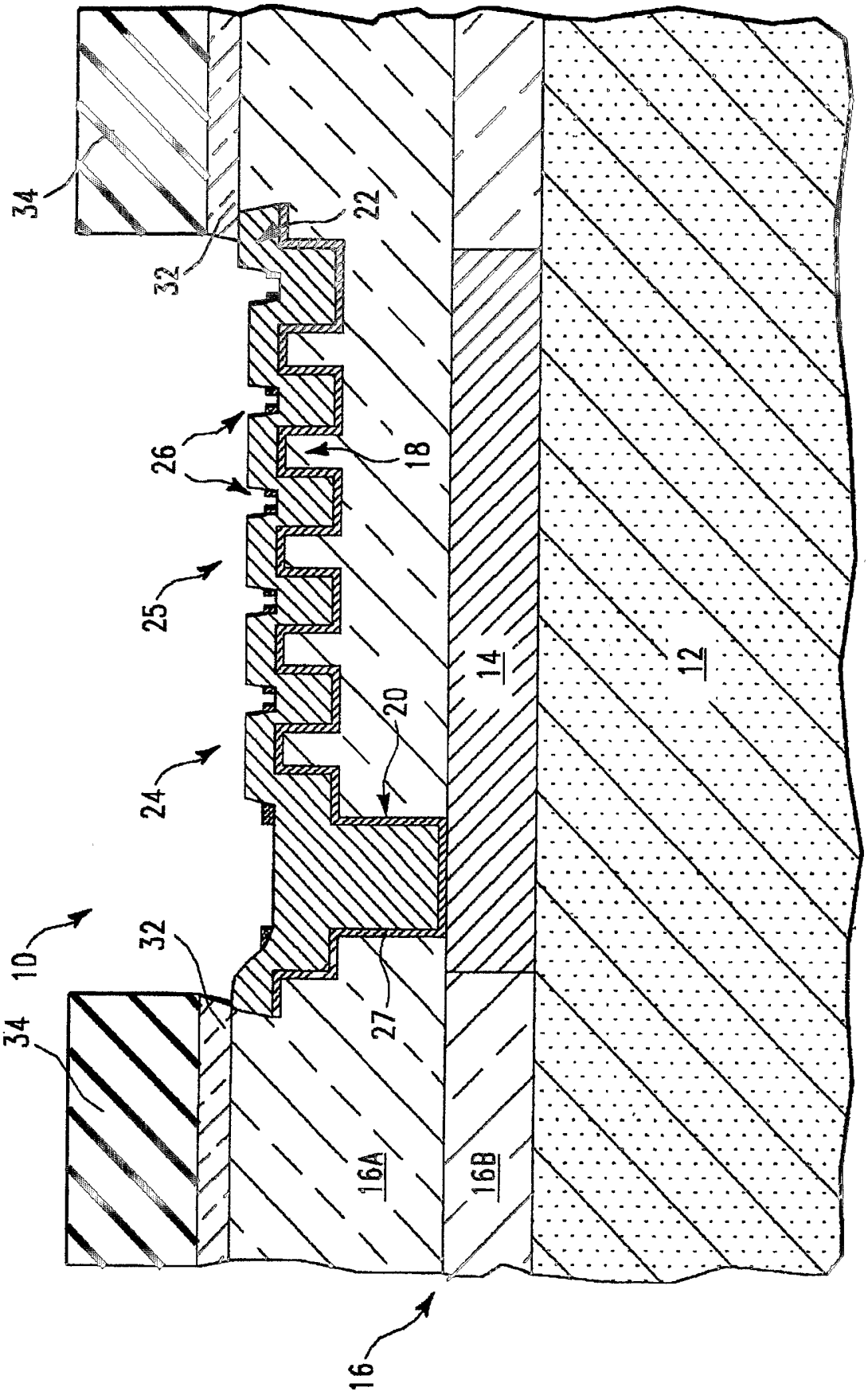

FIG. 5

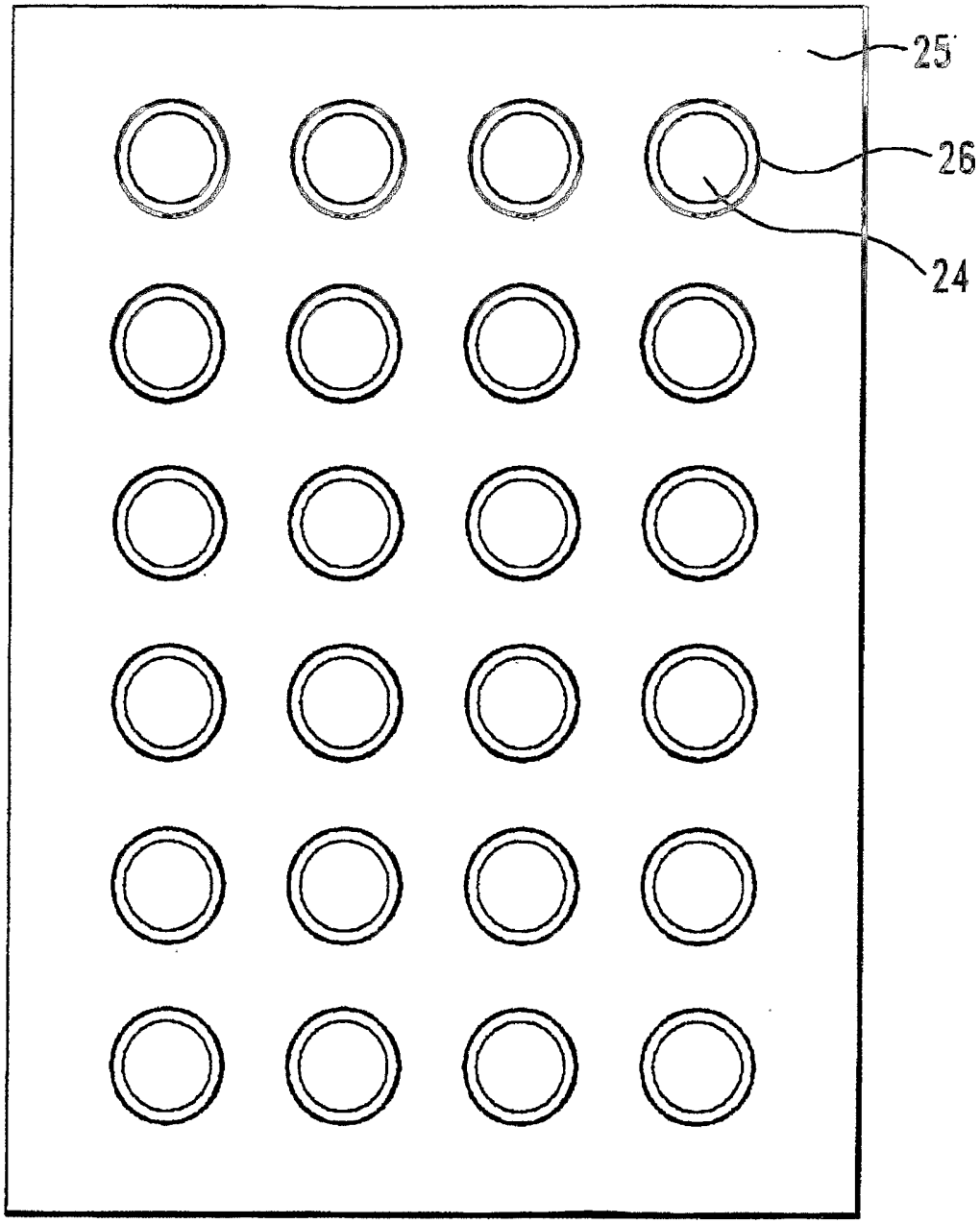

FIG. 6

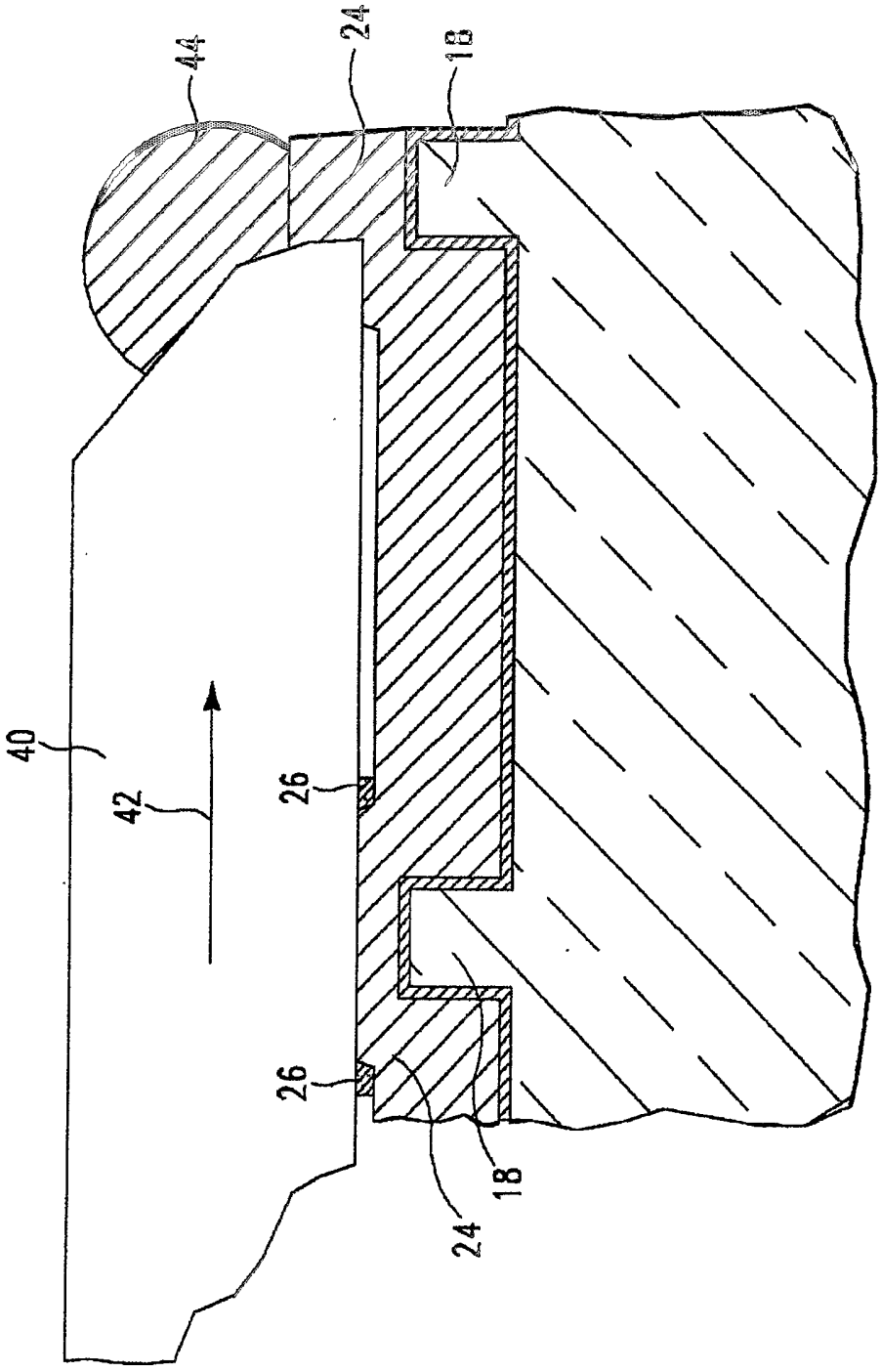

FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/60 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 400 021 B1 (CHO SOON JIN) 4 June 2002 (2002-06-04) column 3, line 59 - column 5, line 4 figures 4-10	1-12
X	US 6 306 750 B1 (HWANG RUEY-LIAN ET AL) 23 October 2001 (2001-10-23) column 1, line 56 - column 2, line 32 column 2, line 57 - column 3, line 60 figures 1a,1b,2,3a,3b,4	1-12
X	US 2001/051426 A1 (POZDER SCOTT K ET AL) 13 December 2001 (2001-12-13) cited in the application figures 2,5 paragraphs '0017!, '0018!, '0025! - '0029!, '0032!, '0034!	1-12

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 July 2004	02/08/2004

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 09, 30 July 1999 (1999-07-30) -& JP 11 121457 A (MATSUSHITA ELECTRON CORP), 30 April 1999 (1999-04-30) abstract paragraphs '0008!, '0009! figures 1-5	1,4,5, 8-10
A	PATENT ABSTRACTS OF JAPAN vol. 2002, no. 08, 5 August 2002 (2002-08-05) -& JP 2002 110730 A (RICOH CO LTD), 12 April 2002 (2002-04-12) abstract	1,6,8,11

INTERNATIONAL SEARCH REPORT

nformation on patent family members

International Application No
PCT/GB2004/001313

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6400021 B1	04-06-2002	KR 2001004529 A JP 2001035969 A	15-01-2001 09-02-2001
US 6306750 B1	23-10-2001	NONE	
US 2001051426 A1	13-12-2001	CN 1305224 A JP 2001156070 A	25-07-2001 08-06-2001
JP 11121457 A	30-04-1999	NONE	
JP 2002110730 A	12-04-2002	NONE	