US 20070187773A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2007/0187773 A1

YANG et al. (43) Pub. Date: Aug. 16, 2007

(54) STRUCTURE AND METHOD TO INDUCE STRAIN IN A SEMICONDUCTOR DEVICE CHANNEL WITH STRESSED FILM UNDER THE GATE

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(21) Appl. No.: **11/738,883**

(22) Filed: **Apr. 23, 2007**

Related U.S. Application Data

(62) Division of application No. 10/906,054, filed on Feb. 1, 2005.

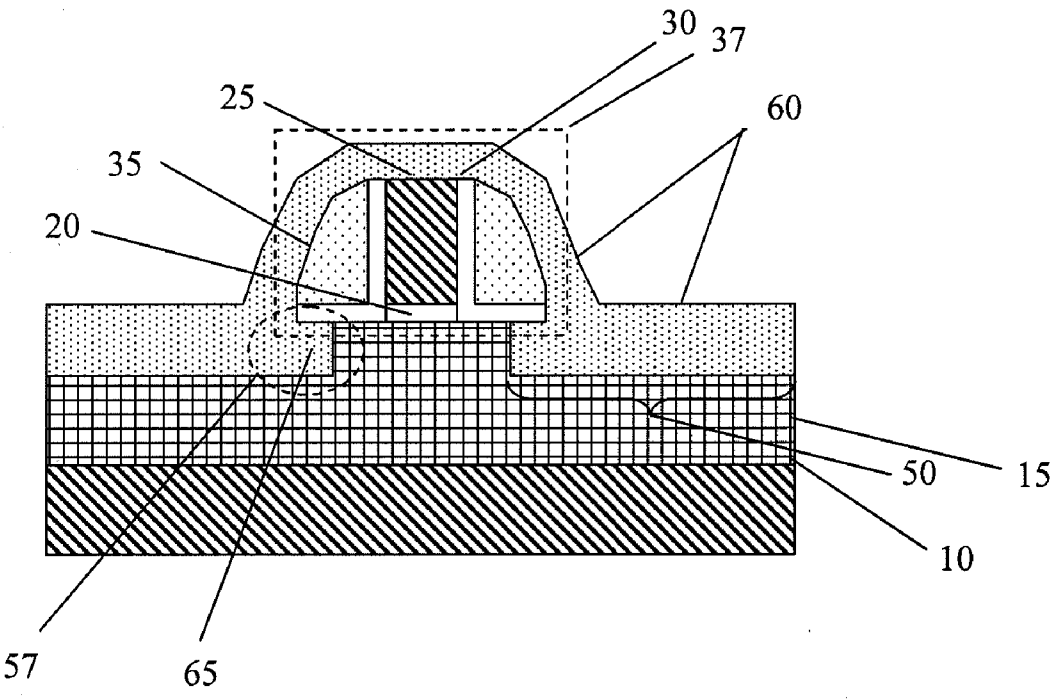
Publication Classification

(51) **Int. Cl.**
H01L 29/94 (2006.01)

(52) **U.S. Cl.** **257/369**; 257/E27

(57) **ABSTRACT**

A semiconductor device is provided with a stressed channel region, where the stress film causing the stress in the stress channel region can extend partly or wholly under the gate structure of the semiconductor device. In some embodiments, a ring of stress film surrounds the channel region, and may apply stress from all sides of the channel. Consequently, the stress film better surrounds the channel region of the semiconductor device and can apply more stress in the channel region.



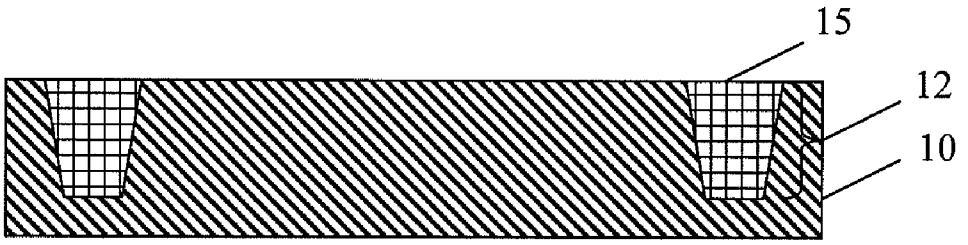


FIGURE 1

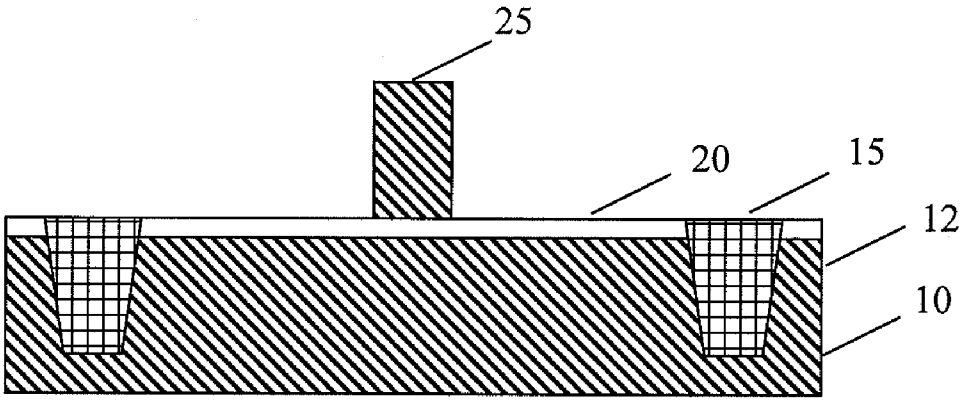


FIGURE 2

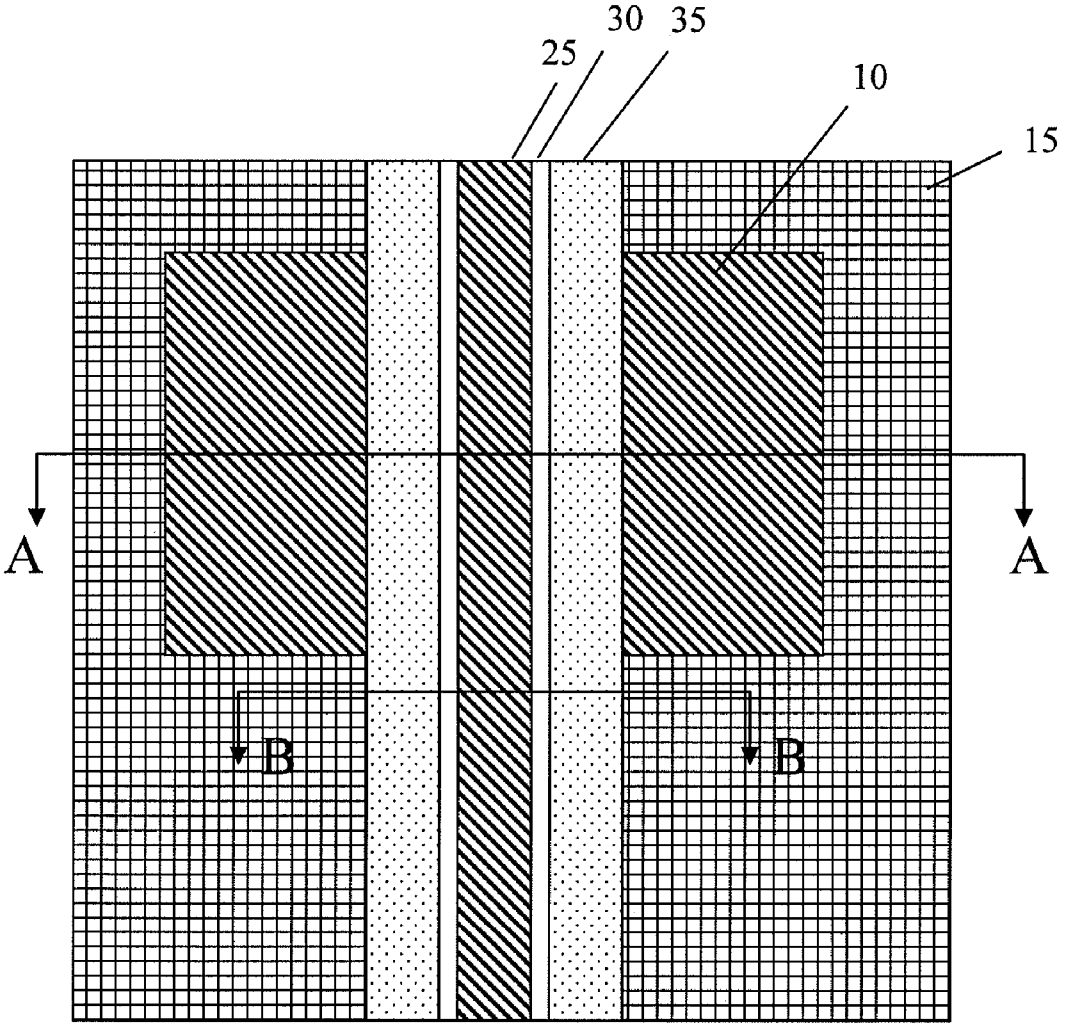


FIGURE 3

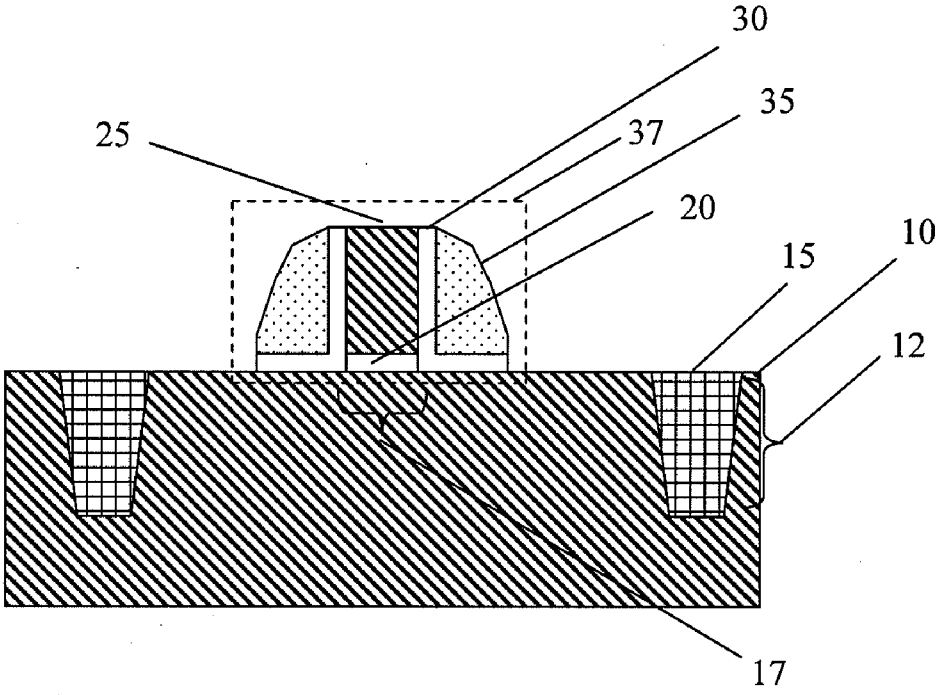


FIGURE 4

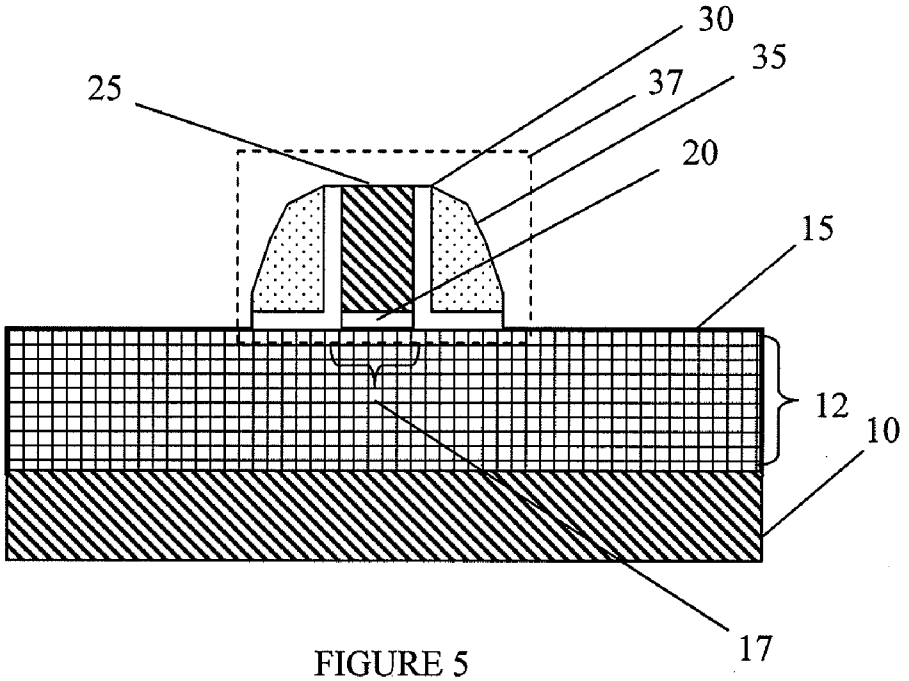


FIGURE 5

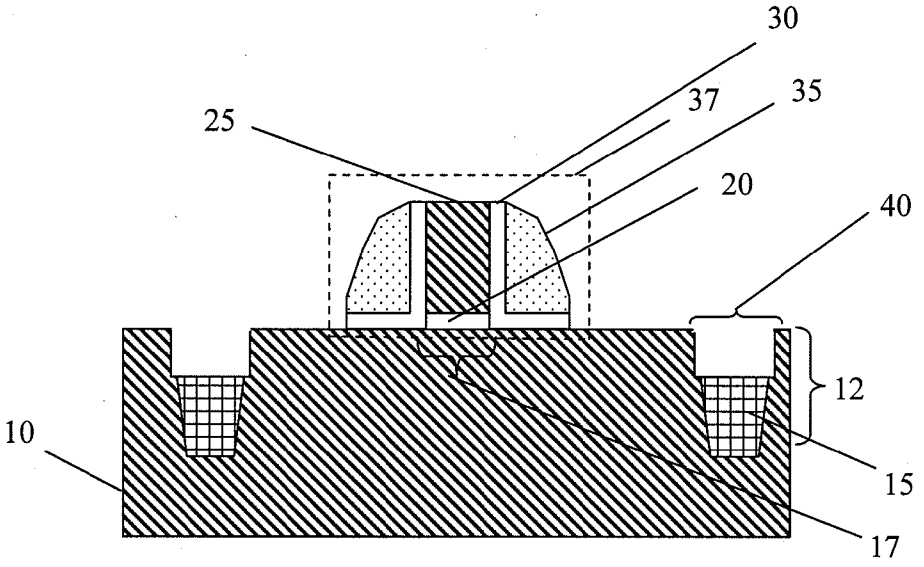


FIGURE 6

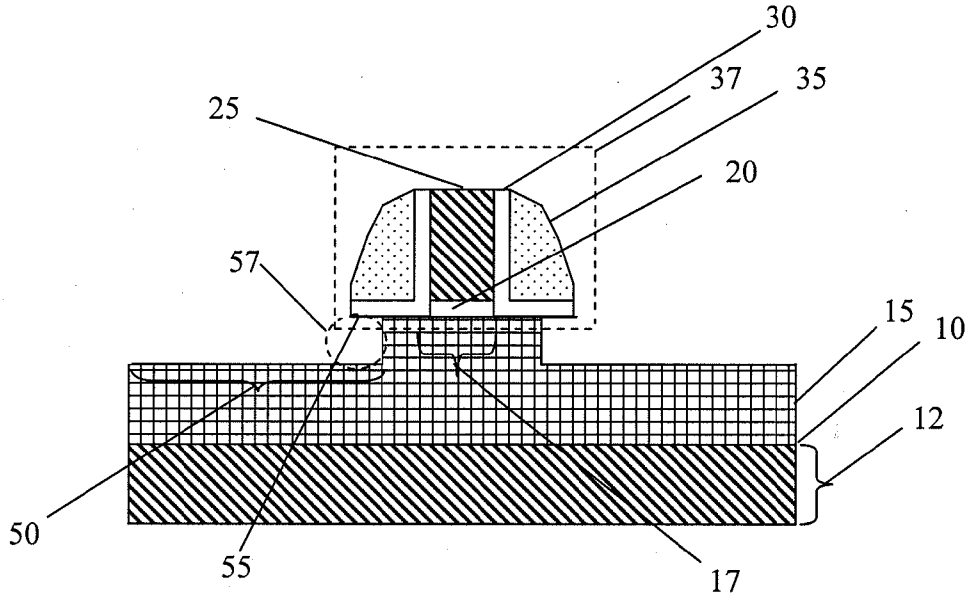


FIGURE 7

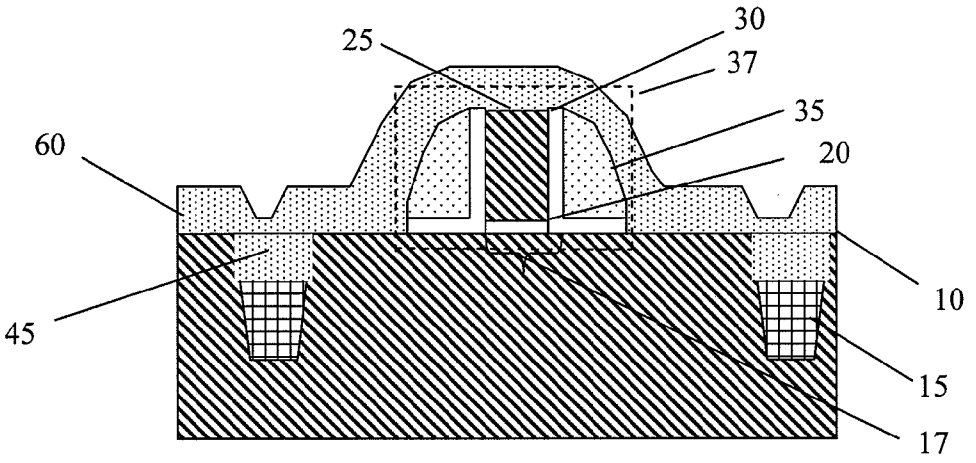


FIGURE 8

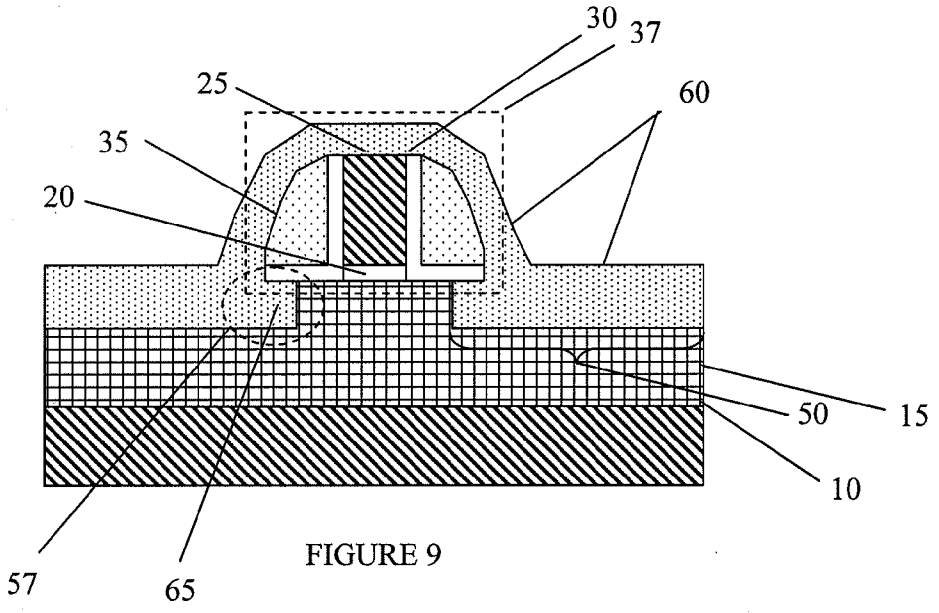


FIGURE 9

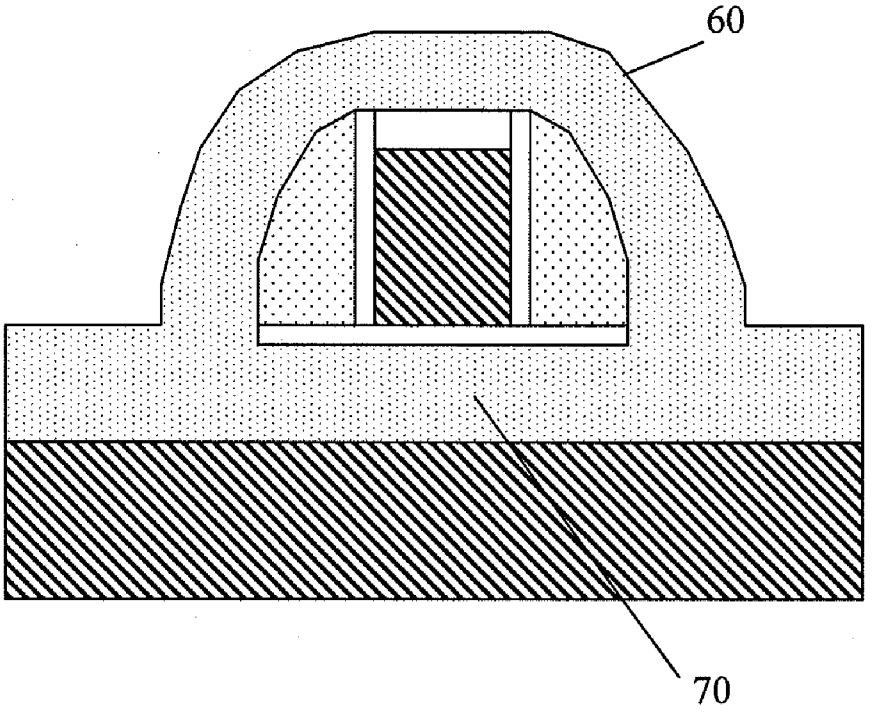


FIGURE 10

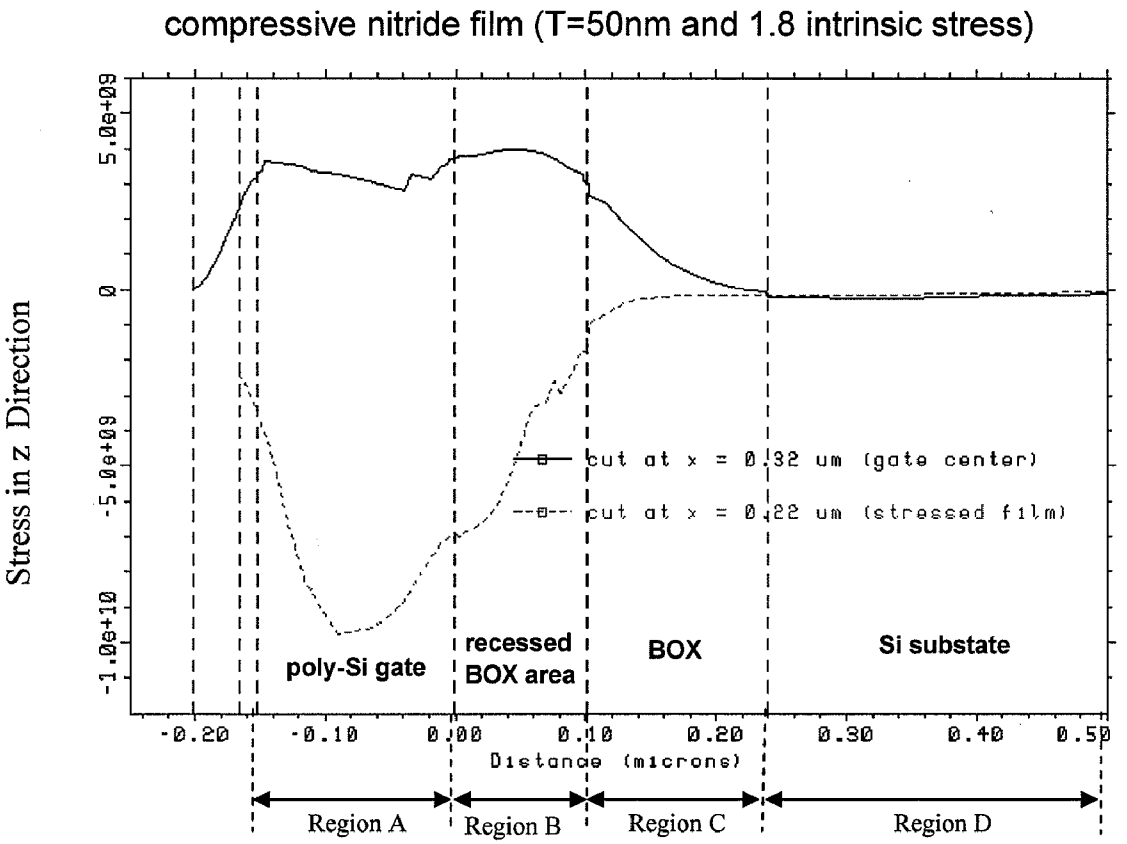

compressive nitride film (T=50nm and 1.8 intrinsic stress)
Stress in z Direction
5.0e+09
0
-5.0e+09
-1.0e+10
cut at x = 0.32 um (gate center)
cut at x = 0.22 um (stressed film)
poly-Si gate
recessed BOX area
BOX
Si substate
-0.20
-0.10
0.00
0.10
0.20
0.30
0.40
0.50
Distance (microns)
Region A
Region B
Region C
Region D

FIGURE 11

STRUCTURE AND METHOD TO INDUCE STRAIN IN A SEMICONDUCTOR DEVICE CHANNEL WITH STRESSED FILM UNDER THE GATE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of copending U.S. patent application Ser. No. 10/906,054 filed on Feb. 1, 2005, the contents of which are incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The invention relates to CMOS devices and method of manufacture and more particularly to CMOS devices with stressed channels and method of manufacture.

[0003] Metal-oxide semiconductor transistors generally include a substrate made of a semiconductor material, such as silicon. The transistors also typically include a source region, a channel region and a drain region within the substrate. The channel region is located between the source and the drain regions. A gate stack, which usually includes a conductive material gate or gate conductor on top of a gate oxide layer and sidewall spacers, is generally provided above the channel region. More particularly, the gate oxide layer is typically provided on the substrate over the channel region, while the gate conductor is provided above the gate oxide layer. The sidewall spacers help define locations of source and drain ion implantation and form self-aligned silicide.

[0004] It is known that the amount of current flowing through a channel of a semiconductor device which has a given electric field across it is proportional to the mobility of the carriers in the channel. Thus, by increasing the mobility of the carriers in the channel, the operation speed of the transistor can be increased.

[0005] It is further known that mechanical stresses within a semiconductor device substrate can modulate device performance by, for example, increasing the mobility of the carriers in the semiconductor device. The mechanical stress can be induced by STI, gate spacer, an etch stopping layer or by silicide. So, certain types of stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses may be created in the channel of the n-type devices (e.g., nFETs) and/or p-type devices (e.g., pFETs). It should be noted that the same stress component, for example tensile stress or compressive stress, improves the device characteristics of one type of device (i.e., n-type device or p-type device) while negatively affecting the characteristics of the other type device.

[0006] For example, tensile stress along the channel direction increases electron mobility in an nFET device while decreasing hole mobility in a pFET. On the other hand, tensile stress perpendicular to the gate oxide surface degrades nFET performance, but improves pFET performance.

[0007] One method of creating stress in the channel of a CMOS device includes forming a film of stressed material over the CMOS device. Thus, some of the stress in the stressed film is coupled to the substrate of the CMOS device thereby generating stress in the channel of the CMOS device. Because the enhanced carrier mobility due to mechanical stress is proportional to the amount of stress, it is desirable to create as much stress in the channel as possible. Additionally, stresses in the stressed film are generated due to appropriately adjusting characteristics in the stressed film deposition process, or introducing stress-producing dopants into the stressed film. It should be noted that such methods of producing a stressed film are limited to producing a stress film with an internal stress on the order of a couple of GigaPascal (GPa).

[0008] Consequently, with the maximum stress of a stressed film being limited to a couple of GPa, it is desirable to develop improved methods and structures for coupling the stress in a stressed film into the channel region of a CMOS device to increase the amount of stress in the channel.

SUMMARY OF THE INVENTION

[0009] In first aspect of the invention, a method of making a CMOS device with a stressed channel includes forming a silicon island comprising a top surface and a sidewall, and arranging an oxide gate on the top surface and above a sidewall of the silicon island. The method also includes arranging a stress film below the gate oxide and adjacent a sidewall of the silicon island.

[0010] In another aspect of the invention, a method of making a CMOS device with a stressed channel includes forming a silicon island comprising a top surface and multiple sidewalls, and arranging a gate oxide and gate stack on the top surface and above a sidewall of the silicon island. The method also includes surrounding a portion of the silicon island around the multiple sidewalls with a stress film.

[0011] In another aspect of the invention, a CMOS device with a stressed channel includes a silicon island comprising a top surface and a sidewall, and a gate oxide and gate stack arranged on the top surface and above a sidewall of the silicon island. The CMOS device also includes a stress film arranged below the gate oxide and adjacent a sidewall of the silicon island.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGS. **1-2** illustrate steps in fabricating a semiconductor device in accordance with the invention;

[0013] FIG. **3** illustrates a top view of a semiconductor device in accordance with the invention;

[0014] FIGS. **4-10** illustrate steps in fabricating a semiconductor device in accordance with the invention; and

[0015] FIG. **11** is a graph of stress versus distance in a semiconductor device in accordance with the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0016] The invention reduces the electrical resistance of a channel in a semiconductor device which causes an increase in device operation speed. The invention also enhances stress in a channel of a semiconductor device by applying stress to the channel. Consequently, the invention applies

stress to a channel with a stress film deposited either partially or completely under the gate. Accordingly, some embodiments of the invention completely surround the semiconductor device channel continuously on all sides thereby enhancing the amount of stress applied to the channel. The invention additionally allows for reducing the resistance of a channel in a semiconductor device by increasing the mobility of carriers or holes. Accordingly, the invention allows for producing semiconductor channels having higher stress levels and a correspondingly higher frequency or current response.

[0017] In one embodiment, the invention creates a unique structure so that high stressed silicon nitride film is introduced to the bottom part of the gate in the STI oxide region. Oxide is recessed so that, for example, Si_3N_4, can be deposited partially or completely under the gate. Additionally, the invention can induce strain in the adjacent channel region, which is especially effective for narrow width transistors.

[0018] Referring to FIG. **1**, a silicon substrate **10** has a trench **12** formed therein. The trench **12** may be formed by any of the processes well known in the art for forming a trench in a silicon substrate such as, for example, a dry etch process.

[0019] After the trench **12** is formed, the trench is filled with a STI oxide **15** to form a shallow trench isolation structure or STI. Other dielectrics beside oxide may be used to fill the trench **12**. The trench **12** may be filled with the STI oxide **15** by any of the processes well known in the art for depositing an oxide in a trench, such as, for example, HDP (high density plasma) oxide. After the trench **12** is filled with the STI oxide **15**, the STI oxide **15** deposited on the surface of the silicon substrate **12** is removed and the surface is planarized so that the surface of the silicon substrate **12** and the surface of the STI oxide **15** in the trench **12** are co-planar.

[0020] Referring to FIG. **2**, a gate oxide **20** is formed on the surface of the silicon substrate **10**. The gate oxide **20** can be formed by any of the methods well known in the art such as, for example, an oxidation followed with nitridation anneal. After the gate oxide **20** is formed, a layer of polysilicon is deposited. Once the polysilicon has been deposited on the gate oxide **20**, the polysilicon is patterned and etched to form a polysilicon gate **25**. The polysilicon can be deposited and etched by any of the methods well known in the art for polysilicon deposition and etching such as, for example, CVD polysilicon deposition with dry etch patterning.

[0021] Optionally, as shown in FIG. **3**, a layer of the oxide **30** may be conformably deposited on the silicon substrate **10**, the STI oxide **15** and on the sides of the polysilicon gate **25**. Dielectric sidewalls **35** are formed by depositing a dielectric over the thin oxide **30**, and etching those portions of the dielectric to leave the sidewalls **35** in place polysilicon gate **25**. The sidewall **35** may directly contact the side of the polysilicon gate **25**, where the thin oxide **30** is not included.

[0022] Referring still to FIG. **3**, a top down view of the resulting structure is shown where a silicon substrate **10** is surrounded by a STI oxide **15**. On top of portions of the silicon substrate **10** and the STI oxide **15** is a polysilicon gate **25**. On either side of the polysilicon gate **25** are thin oxides **30**. Sidewall spacers **35** are adjacent to each thin oxide **30**. Also shown are two lines A-A' and B-B' indicating cross-sections shown in subsequent figures. The cross-section indicated by A-A' is taken through a central region of the device and thus includes the channel region under the polysilicon gate **25**. Cross-section B-B' is taken to one side of the semiconductor device through the STI oxide region **15** and thus is outside the channel region of the device.

[0023] FIGS. **4**, **6** and **8** show cross-sections taken along the line A-A' of FIG. **3** at various stages of fabrication of the first embodiment of the invention. FIGS. **5**, **7** and **9** correspond to a cross-section taken along B-B' of FIG. **3** at various stages of fabrication of the first embodiment of the invention. Referring to FIG. **4**, the A-A' horizontal cross-section shows a silicon substrate **10** having trenches **12** formed therein. The trenches **12** are filled with a STI oxide **15**. The silicon substrate **10** has a channel region **17**. Above the channel region **17** is a gate structure **37** which includes a gate oxide **20**. Also included in the gate structure **37**, on top of the gate oxide **20**, is a polysilicon gate **25**. On either side of the polysilicon gate **25** and on a portion of the top surface of the silicon substrate **10** next to the gate oxide **20** are thin oxide spacers **30**. Formed against the sides and tops of thin oxide spacers **30** are a nitride sidewall **35**.

[0024] Referring to FIG. **5**, the B-B' cross-section shows a substrate **10** with a STI oxide **15** thereon. On top of the STI oxide **15** is the gate oxide **25** with a polysilicon gate **25** arranged thereupon. On either side of the polysilicon gate **25** and on top surfaces of the STI oxide **15** proximate the gate **25** is a thin oxide spacer **30**. On the side and tops of the thin oxide spacer **30** are nitride sidewalls **35**.

[0025] Accordingly, FIGS. **4** and **5** show, respectively, two cross-sections taken through the device shown in FIG. **3**. FIG. **4** shows a cross-section through the device including the channel region **17**, and FIG. **5** shows a cross-section through the device outside the channel region **17** which includes the STI oxide **15**.

[0026] FIG. **6** shows cross-section along A-A' of FIG. **3** showing portions of the STI oxide **15** removed from the upper portions of the trenches **12** in the substrate **10**. Removing a portion of the STI oxide **15** from the upper portion of the trench **12** forms a trough **40**. The trough **40** of FIG. **6** corresponds substantially to the top portion of the trench **12**.

[0027] Referring to FIG. **7**, a cross-section along the line B-B' of FIG. **3** is shown for the same step in the fabrication process as FIG. **6**. The etching process, which formed the trough **40** of FIG. **6**, also formed a broad trench **50** in the STI oxide **15** running parallel to the gate structure **37**. Additionally, the etching process etched a portion of the STI oxide **15** from underneath the sidewall **35** and a portion of the thin oxide spacer **30**. Accordingly, an overhang **55** of the sidewall spacer **35** is formed. Additionally, a cavity or tunnel **57** is formed in the STI oxide **15** under a portion of the sidewall **35**. It should be noted that in some embodiments, the tunnel **57** may extend partially under the polysilicon gate **35** or further to pass through the STI oxide **15** completely under the gate structure **37** to the other side of the gate structure **37** to meet a similar tunnel from the other side of the gate structure **37** thereby completely penetrating through a region under the gate structure **37**. Because portions of the STI oxide **15** are etched away, the trough **40** and broad trench **50** may be formed without an additional masking step.

[0028] Referring to FIG. **8**, the cross-section along A-A' shows a stressed nitride film **60** being formed over the gate structure **37**, top surface of the silicon substrate **10** and filling the troughs **40** above the STI trenches **12**. Accordingly, those regions of the STI trenches **12**, which had the upper portions of the STI oxide **15** removed have now been filled with a stress film **45**. Thus, the portions of the stress film **45** in the tops of the STI trenches **12** (i.e., the trough **40**) run approximately parallel to the gate structure **37**. Additionally, the portions of the stress film **45** in the tops of the STI trenches **12** are formed at about the same level in the silicon substrate **10** as the channel region **17** of the device.

[0029] Referring to FIG. **9**, the cross-section along B-B' shows the stressed film **60** covering the gate structure **37**. The stressed nitride film **60** is deposited into the broad trenches **50** and additionally is deposited into the tunnel region **65** underneath the overhang **55** of the sidewall. Accordingly, a portion of the stress film **60** is deposited under a portion of the gate structure **37**, and may be referred to as a sub-gate stress film **65**. The sub-gate stress film **65**, in the tunnel **57**, is deposited at a level similar to the channel region **17** of the semiconductor device.

[0030] As can be seen in FIGS. **8** and **9**, a channel region **17** of the semiconductor device is surrounded on substantially all sides by a stress film **60**. The stress film **60** lies at a level in the silicon substrate **10** approximately level to the channel region **17** and extends along the silicon substrate approximately parallel to the gate structure **37**. Additionally, a portion of the stress film **60** extends under the gate structure **37** in tunnel regions **57** to form the sub-gate stress film **65**. Thus, the stress film **60** lies at a region approximately level to the stress channel **17**, extending under the gate structure **37**. Due to being almost completely surrounded by stress film, the channel region **17** is subjected to higher levels of stress caused by the stress film **60**.

[0031] Referring to FIG. **10**, in some embodiments, the stress film **60** extends completely under the gate structure **37** to form a sub-gate stress film **70**. Such a structure is formed by etching a tunnel under the gate structure **37** and depositing the stress film therein. In this embodiment, the channel region **17** of the semiconductor device is entirely surrounded by the stress film **60** approximately level to the channel region **17**.

[0032] Accordingly, the stress film is able to apply stress all around the channel region **17** and squeeze the channel region **17** in a compressive manner. It should be noted that in embodiments of the invention, the stress film **60** is configured so that the stress is applied in a direction that is perpendicular to a surface of the substrate, also referred to as the "Z-direction." It should also be noted that as the size of semiconductors are reduced, such a technique allows for ever increasing stresses to be applied to the channel region of the semiconductor device. Additionally, the orientation of stress in a stress film **60** can be adjusted by adjusting the chemistry and deposition parameters of the stress film **60** during deposition of the stress film **60** and thus, alter the magnitude and direction of stress caused in the channel region **17** of the semiconductor device.

[0033] Referring to FIG. **11**, a graph of stress in various regions of a device having a sub-gate stress film is shown. The Y-axis of the graph represents stress in the Z-direction which is perpendicular to an upper surface of the silicon substrate. The X axis represents distance in microns across the semiconductor device. In the graph, region A represents the region of the device which includes the polysilicon gate. Region B includes the region of the device extending least partially under the gate. Region C includes that portion of the semiconductor device adjacent to the channel region. And Region D includes the silicon substrate away from the channel region such as, for example, the cross-section represented by A-A' of FIG. **3**. Additionally, the solid line of the graph represents measurements made on a cross-section through the center of the channel region. The dashed line represents measurements made on a cross-section through the stress film region of the semiconductor device, such as, for example, along the cross-section represented by B-B' of FIG. **4**.

[0034] As can be seen by the dashed line representing stress through the stress film, the stress is about 1×10^{10} Pa in Region A and drops to about 5×10^{9} Pa in Region B. The stress then relatively flattens out to about 0 Pa in Region C and remain at 0 Pa in Region D. The solid line shows the stress in Region B being about 3×10^{9} Pa in Region A as well as Region C. In Region C the stress drops from about 3×10^{9} Pa to about 0 Pa and remains at about 0 Pa in Region D. The data are for a compressive nitride film where T=50 nm and the intrinsic stress is 1.8 GPa.

[0035] As discussed above, embodiments of the invention include forming a stress film partially or completely underneath the gate region of a semiconductor device where a STI oxide would normally be formed. By forming such a sub-gate stress film under a gate, in addition to stress film being formed in the substrate parallel to the gate structure, the amount of stress that can be applied to the channel of the semiconductor device by the stress film may be increased. It should also be noted the stress film replaces portions of the STI oxide and can abut directly against the silicon substrate.

[0036] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.

What is claimed is:

1. A CMOS device with a stressed channel, comprising:

a silicon island comprising a top surface and at least one sidewall;

a gate structure comprising at least a gate oxide and a gate stack arranged on the top surface and above a sidewall of the at least one sidewall of the silicon island; and

a stress film arranged beneath the gate oxide and adjacent the sidewall of the at least one sidewall of the silicon island.

2. The device of claim 1, further comprising the stress film being in contact with the sidewall of the at least one sidewall of the silicon island.

3. The device of claim 1, wherein the silicon island comprises four sidewalls and the stress film is arranged adjacent the four sidewalls.

4. The device of claim 1, wherein the stress film extends from a first side of the gate oxide to a second side of the gate oxide below the gate oxide along another sidewall of the at least one sidewall of the silicon island.

5. The device of claim 1, wherein the stress film covers the gate structure of the CMOS device.

6. The device of claim 1, wherein the stress film comprises Si_3N_4.

7. The device of claim 1, wherein the stress film is configured to create a stress in the stressed channel with a direction approximately perpendicular to the top surface of the silicon island.

8. The device of claim 7, wherein the stress film is configured to create a stress in a direction parallel to the top surface of the silicon island.

9. The device of claim 1, wherein the gate structure extends beyond at least the sidewall of the at least one sidewall of the silicon island.

10. The device of claim 1, further comprising an etched tunnel extending under the gate stack adjacent the sidewall of the at least one sidewall of the silicon island.

11. The device of claim 10, wherein the etched tunnel creates a passage underneath the gate structure from a first side of the gate structure to a second side of the gate structure.

12. The device of claim 10, wherein the stress film extends completely under the gate structure, to form a sub-gate stress film.

13. The device of claim 11, wherein the stress film is deposited in the passage, filling the passage and forming a sub-gate stress film.

14. A CMOS device with a stressed channel, comprising

a silicon island comprising a top surface and multiple sidewalls;

a gate structure comprising at least a gate oxide and a gate stack on the top surface, the gate structure extending beyond a sidewall of the silicon island; and

a stress film surrounding a portion of the silicon island around the multiple sidewalls.

15. The device of claim 14, wherein the stress film surrounds substantially all of the silicon island around the multiple sidewalls.

16. The device of claim 14, wherein the stress film extends from a first side of the gate oxide to a second side of the gate oxide below the gate stack along another sidewall of the silicon island.

17. The device of claim 14, wherein the stress film covers the gate structure of the CMOS device.

18. The device of claim 14, wherein the stress film creates a stress in the stressed channel with a direction approximately orthogonal to the top surface of the silicon island, along with a stress in the direction parallel to the top surface of the silicon island.

19. The device of claim 14, wherein the stress film comprises Si_3N_4.

20. The device of claim 14, further comprising a tunnel under the gate stack adjacent the sidewall of the silicon island.

* * * * *