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(71) Applicant (for all designated States except US): **ADVANCED MICROFAB, LLC** [US/US]; 101 W. Big Beaver Road, Suite 1400, Troy, MI 48084 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KUMAR, Krishna, G.** [US/US]; 731 Kirts Blvd., Troy, MI 48084 (US). **CHOKSI, Nishit, A.** [IN/US]; 5585 Woodfield, Troy, MI 48098 (US). **CHALIL, Joseph, M.** [US/US]; 7285 Mill-rock Ave., Shelby Twp, MI 48317 (US).

(74) Agents: **MACKENZIE, Kevin, S.** et al.; Gifford, Krass, Sprinkle, Anderson & Citkowski, PC, 2701 Troy Center Drive, Suite 330, Post Office Box 7021, Troy, MI 48007-7021 (US).

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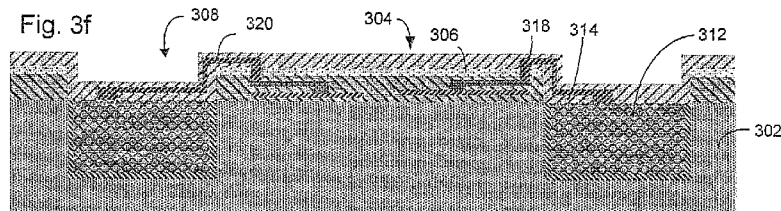
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(54) Title: METHOD OF FORMING MONOLITHIC CMOS-MEMS HYBRID INTEGRATED, PACKAGED STRUCTURES



(57) Abstract: A method of forming Monolithic CMOS-MEMS hybrid integrated, packaged structures includes the steps of providing: providing at least one semiconductor substrate having a CMOS device area including dielectric layers and metallization layers; applying at least one protective layer overlying the CMOS device area; forming at least one opening on the protective layer and patterning the dielectric and metallization layers to access the semiconductor substrate; forming at least one opening on the semiconductor substrate by etching the dielectric and metallization layers; applying at least one filler layer in the at least one opening on the semiconductor substrate; positioning at least one chip on the filler layer, the chip including a prefabricated front face and a bare backside; applying a first insulating layer covering the front face of the chip providing continuity from the semiconductor substrate to the chip; forming at least one via opening on the insulating layer covering the chip to access at least one contact area; applying at least one metallization layer overlying the insulating layer on the substrate and the chip connecting the metallization layer on the substrate to the at least one another contact area on the chip; applying a second insulating layer overlying the metallization layer on the at least one chip; applying at least one interfacial layer; applying at least one rigid substrate overlying the interfacial layer; and applying at least one secondary protective layer overlying the rigid substrate.



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A. CLASSIFICATION OF SUBJECT MATTER***H01L 21/8238(2006.01)i, H01L 27/092(2006.01)i, B82B 3/00(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/8238; B81B 1/00; H01L 21/469; G01L 9/00; H01L 23/02; G01L 9/16; H01L 21/31; B81C 1/00; H01L 23/053

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: hybrid, package, CMOS-MEMS, monolithic

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1808405 A2 (HONEYWELL INTERNATIONAL INC.) 18 July 2007 See paragraphs [0014]-[0046]; and figures 1-4.	1-40
A	US 2007-0224832 A1 (PETER ZURCHER) 27 September 2007 See abstract; paragraphs [0017]-[0031]; and figures 1-8.	1-40
A	JP 2001-185635 A (LUCENT TECHNOL INC.) 06 July 2001 See abstract; paragraphs [0010]-[0013]; and figure 1.	1-40
A	US 6012336 A1 (EATON; WILLIAM P. et al.) 11 January 2000 See abstract; column 11, line 24 - column 16, line 51; and figures 4a-4v.	1-40
A	KR 10-2009-0031360 A (SCHOTT AG) 25 March 2009 See abstract; paragraphs [0083]-[0102]; and figures 5a-5g.	1-40

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

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Authorized officer

KIM, Sang Keol

Telephone No. 82-42-481-5742



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