(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 December 2013 (12.12.2013)

(10) International Publication Number
WO 2013/185089 A1

(51) International Patent Classification:
H01L 29/778 (2006.01) *H01L 29/205* (2006.01)

(21) International Application Number:
PCT/US2013/044808

(22) International Filing Date:
7 June 2013 (07.06.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/656,875 7 June 2012 (07.06.2012) US

(71) Applicant: IQE KC, LLC [US/US]; 200 John Hancock Road, Taunton, MA 02780 (US).

(72) Inventors: CAO, Yu; 158 Plymouth Drive, No. 2B, Norwood, MA 02062 (US). **LABOUTIN, Oleg**; 3 Adam Street, No. 8, South Easton, MA 02375 (US). **JOHNSON, Wayne**; 173 Depot Street, Easton, MA 02334 (US).

(74) Agents: PIERCE, N., Scott et al.; Hamilton, Brook, Smith & Reynolds, P.C., 530 Virginia Rd, P.O. Box 9133, Concord, MA 01742-9133 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: DOUBLE ALUMINUM NITRIDE SPACERS FOR NITRIDE HIGH ELECTRON-MOBILITY TRANSISTORS

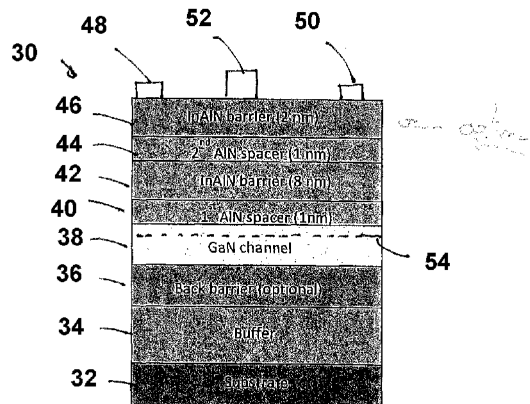

FIG . 2

(57) Abstract: An epitaxial structure and a high electron mobility transistor (HEMT) employing the epitaxial structure includes a first spacer layer over a channel layer, a first barrier layer over the first spacer layer, and a second spacer layer over the first barrier layer.

WO 2013/185089 A1

DOUBLE ALUMINUM NITRIDE SPACERS FOR NITRIDE HIGH ELECTRON-MOBILITY TRANSISTORS

RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 61/656,875, filed on June 7, 2012. The entire teachings of the above application are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] Optimization of gallium nitride (GaN) high electron mobility transistors (HEMTs) for high frequency applications involves complex tradeoffs between the epitaxial layer design and the device fabrication and layout. The thickness of the barrier layer component of the HEMT structure can be a limiting factor because, as thickness of the barrier layer decreases, HEMT gate leakage can become a significant factor affecting performance, especially in radio frequency (RF) applications. A thin barrier can lead to electrons tunneling through the barrier layer, thereby reducing reliability or rendering the transistor inoperable altogether. Reducing gate leakage also helps improve device performance, as measured by parametrics such as on/off ratio, maximum operating frequencies, and power consumption.

[0003] One option to decrease electron tunneling in GaN-based HEMTs is to increase the effective barrier height by introducing a spacer layer of aluminum nitride between a gallium nitride channel layer of the HEMT and an indium aluminum gallium (InAlGaN) nitride barrier layer. Such a spacer layer causes a positive conduction band offset between the aluminum nitride of the spacer layer material and barrier layer materials, typically comprised of aluminum gallium nitride (AlGaN), indium aluminum nitride (InAlN), or indium aluminum gallium nitride (InAlGaN). However, the effectiveness of an aluminum nitride spacer layer between a channel layer and the barrier layer of a HEMT structure is limited and there is a need for a HEMT structure that can help minimize or eliminate the problems of gate leakage in devices employing thin barrier layers.

SUMMARY OF THE INVENTION

[0004] The invention generally is directed to an epitaxial structure that includes a first spacer layer between a channel layer and a first barrier layer, and a second spacer layer between the first barrier layer and a second barrier layer, and to a method of forming such an epitaxial structure.

[0005] In one embodiment, the invention is an epitaxial structure that includes a substrate and a buffer layer on the substrate. A channel layer is over the buffer layer and includes a 2-dimensional electron gas region distal to the buffer layer. The first spacer layer is over the channel layer and a first barrier layer is over the first spacer layer. A second spacer layer is over the first barrier layer. In one embodiment, a second barrier layer is over the second spacer layer.

[0006] In another embodiment, the invention is a method of forming a epitaxial structure that includes the steps of forming a substrate, forming a buffer layer on the substrate and forming a channel layer over the buffer layer. The first spacer layer is formed over the channel layer, a second barrier layer is formed on the first spacer layer, while a second spacer layer is formed on the first barrier layer, whereby a 2-dimensional electron gas region is formed in the channel layer distal to the buffer layer as a result of forming the first and second barrier layers. In one embodiment, a second barrier layer is formed over the second spacer layer.

[0007] This invention has many advantages. For example, the inventors have discovered that, unexpectedly, the inclusion of a second spacer layer, interposed between two barrier layers, significantly decreases the likelihood and effect of electrons tunneling through the barrier layer in a HEMT structure relative to an epitaxial structure having the same overall thickness of combined spacer and barrier layers, but employing only a single spacer layer between the channel layer and the barrier layer. Although not wishing to be limited to any particular theory, it is believed that the effective barrier height for electrons is increased by employing a second spacer layer interposed within a barrier layer, but without significant deleterious effect on the performance of the HEMT structures relative to HEMT structures having the same combined thickness of spacer and barrier layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a schematic representation of an epitaxial structure of the prior art, showing an aluminum nitride spacer layer between a gallium nitride channel layer and an aluminum nitride barrier layer.

[0009] FIG. 2 is a schematic representation of an epitaxial structure of the invention, showing a second aluminum nitride spacer layer partitioning upper and lower barrier layers.

[0010] FIG. 3 is a simulated plot showing the effective barrier heights of an indium aluminum nitride barrier layer in the epitaxial structure of a prior art HEMT structure, such as is represented in FIG. 1.

[0011] FIG. 4 shows a simulated plot of the effective barrier heights of an indium aluminum nitride barrier layer where two aluminum nitride spacers are employed, as in the embodiment of the invention schematically represented in FIG. 2.

[0012] FIG. 5 is a simulated plot of 2-dimensional gas density (2DEG) versus separation between aluminum nitride spacers for an HEMT structure of the prior art and two embodiments of HEMT structures of the invention.

[0013] FIG. 6 is a plot of sheet resistance measured by a contactless sheet resistance probe system versus separation between the aluminum nitride spacers and for two HEMT structures of the prior art and two HEMT structures of the invention.

[0014] FIG. 7 is the channel current plotted as a function of gate bias from the FETs on the control sample and the other two samples with double AlN spacers. The drain bias was fixed at 6V. The source is grounded. The gate bias swept from -6V to +2V. The leakage current in the OFF state is more than 2 orders of magnitude lower than that in the control sample.

[0015] FIG. 8 is the gate leakage current plotted as a function of gate bias from the FETs on the control sample and the other two samples with double AlN spacers. The drain bias was fixed at 6V. The source is grounded. The gate bias swept from -6V to +2V. The gate leakage current in the OFF state is 1-2 orders of magnitude lower than that in the control sample.

[0016] DETAILED DESCRIPTION OF THE INVENTION

[0017] A description of example embodiments of the invention follows.

[0018] The teachings of all patents, published applications and references cited herein are incorporated by reference in their entirety.

[0019] The invention generally is directed to an epitaxial structure and to a method of forming an epitaxial structure having first and second spacer layers, wherein the second spacer layer is interposed between the first and second barrier layers of the epitaxial structure.

[0020] In one embodiment of an epitaxial structure 10 of the prior art, shown in FIG. 1, the epitaxial structure includes substrate 12, buffer layer 14 over substrate 12, and optionally, back barrier layer 16 over buffer layer 14. Channel layer 18, formed of a suitable material, such as gallium nitride (GaN), is disposed over back barrier layer 16. Spacer layer 20, having a typical thickness of about 1 nm, overlays channel layer 18. Indium aluminum nitride (InAlN) barrier layer 22, typically having a thickness of about 11 nm, overlays spacer layer 20. When a layer is referred to as being "on" or "over" another layer or substrate, it can be directly on the layer or substrate, or an intervening layer also may be present.

[0021] As understood by those of skill in the art, an epitaxial structure can contain many distinct layers that are, either collectively or individually, designed to achieve desired device characteristics. An epitaxial structure is typically formed over a substrate. Examples of substrate materials for GaN-based epitaxial structures include sapphire (Al2O3), silicon carbide (SiC), silicon (Si), gallium nitride (GaN), or aluminum nitride (AlN). For a GaN-based FET, such as a HEMT, a buffer layer with high electrical resistivity is typically formed over the substrate. For HEMT epitaxial structures, a channel layer is typically formed over the buffer layer and a barrier layer is typically formed over the channel layer. The barrier layer should be formed from a material with larger bandgap than the material used to form the channel layer. When the barrier layer and channel layer are formed using appropriate materials and methods, a large electron concentration can be developed in the channel layer adjacent to the barrier layer. The electrons in this region exhibit high mobility and this collective group of electrons is referred to as a 2-dimensional electron gas (2DEG). It should be noted that certain optional layers may be present or absent in a HEMT epitaxial structure depending on its design. Of particular note, a channel layer may not be employed and, if a large bandgap barrier layer is formed

over a buffer layer with smaller bandgap, a 2DEG can be formed in the region of the buffer layer adjacent to the barrier layer. There may also be intervening layers between the channel layer and the barrier layer. A common example is a spacer layer formed directly on the channel layer and between the channel layer and barrier layer. Such a spacer layer can be used to enhance properties of the 2DEG such as electron mobility and electron concentration. For GaN-based HEMTs, a common structure employs a GaN buffer layer, GaN channel layer, AlN spacer layer, and AlGaN barrier layer, although many permutations are possible. Suitable material properties (e.g., bandgap) for the respective layers of GaN-based epitaxial structures are known in the art.

[0022] A layer that is "directly on" another layer or substrate means that no intervening layer is present. It should also be understood that when a layer is referred to as being "on" or "over" another layer or substrate, it may cover the entire layer or substrate, or a portion of the layer or substrate.

[0023] One embodiment of an epitaxial structure of the invention, suitable for use as a high electron mobility transistor (HEMT) device is shown in FIG. 2. As represented substantially therein, epitaxial structure 30 includes substrate 32 and buffer layer 34 overlaying substrate. Examples of suitable materials of substrate include silicon carbide (SiC), sapphire (Al_2O_3) and silicon (Si). Typically, buffer layer 34 includes at least one material selected from the group consisting of gallium nitride (GaN), indium gallium nitride (InGaN), aluminium gallium nitride (AlGaN). The average thickness of buffer layer 34 typically is in a range of between about 0.1 μm and about 10 μm. Optional back barrier layer 36 overlays buffer layer. Typically, the average thickness of back barrier layer is in a range of between about 10 nm and about 1000 nm. Channel layer 38, formed of a suitable material, such as gallium nitride (GaN), overlays optional back barrier layer. In one embodiment, channel layer 38 consists essentially of $In_xGa_{1-x}N$, where $0 \leq x \leq 1$. Typically, the average thickness of channel layer 38 is in a range of between about 10nm and about 500nm. In one embodiment, the average thickness of channel layer 38 is about 100 nm.

[0024] First spacer layer 40 overlays channel layer 38. Examples of suitable materials of first spacer layer 40 includes aluminum nitride (AlN), aluminum

gallium nitride (AlGaN). Preferably, first spacer layer 40 includes aluminum nitride (AlN). In one embodiment, first spacer layer 40 has an average thickness in the range of between about 0.5 and about 1nm. In a preferred embodiment, first spacer layer has an average thickness in the range between about 0.5 and about 1nm. In a particularly preferred embodiment, aluminum nitride spacer layer has a thickness of about 1nm.

[0025] First barrier layer 42 overlays first spacer layer 40. Examples of suitable materials of first barrier layer 42 include aluminum nitride (AlN), aluminum gallium nitride (AlGaN), Indium aluminum nitride (InAlN). The average thickness of the first barrier layer 42 typically is in a range of between about 1 and about 30. Preferably, the average thickness of first barrier layer 42 is in a range of between about 2 and about 10. In one particular embodiment, the average thickness of the first barrier layer 42 is about 2 and 6 nm.

[0026] Second aluminum nitride spacer layer 44 overlays first barrier layer 42. Examples of suitable materials of second spacer layer 44 are the same as those of first spacer layer 40. First 40 and second 44 spacer layers can be formed of the same or different materials. The average thickness of second spacer layer 44 typically is a range of between about 0.5 and about 1 nanometers (nm). In a preferred embodiment, the range of average thickness is between about 0.5 and about 1. In the particular preferred embodiment, the average thickness of the second spacer layer 44 is about 1 nm.

[0027] Second barrier layer 46 overlays second spacer layer 44. Examples of suitable materials of second barrier layer 46, and suitable average thickness ranges of second barrier layer 46 are the same as those of first barrier layer 42. Second barrier layer 46 is optional.

[0028] Typically the combined thickness of first barrier layer 42, second spacer layer 44 and second barrier layer 46 is in a range between about 5 and about 30. Preferably, the average thickness of first barrier layer 42 is about 8 nm, the average thickness of second spacer layer 44 is about 1 nm, and the average thickness of second barrier layer 46 is about 2 nm. In another embodiment, the combined thickness of first barrier layer 42, second spacer layer 44 and second barrier layer 46 is in a range between about 0.5 nm and about 20 nm. In a particularly preferred

embodiment, the combined thickness of the first barrier layer 42, second spacer layer 44 and second barrier layer 46 is about 11 nm.

[0029] Doping and doping levels suitable for the various layers of the epitaxial structure of the invention are those typically known to those of skill in the art.

[0030] In one embodiment, the invention is a high electron mobility transistor (HEMT) structure of the invention. In one embodiment of an HEMT of the invention, shown in FIG. 2, source terminal 48 is in electrical communication with second barrier layer 46 and a drain terminal 50 is in electrical communication with at least one of first barrier layer 42 and second barrier layer 46. Further, gate 52 is in direct electrical communication with at least one of first barrier layer 42 and second barrier layer 46, and is located between source terminal 48 and drain terminal 50, as shown in FIG. 2.

[0031] In another embodiment, the invention is a method of forming an epitaxial structure that includes the steps of forming substrate 32, forming buffer layer 34 on substrate 32, optionally forming back barrier layer 36 over buffer layer 34, forming channel layer 38 over buffer layer 34 or optional back barrier layer 36, forming first spacer layer 40 on channel layer 38, forming first barrier layer 42 on first spacer layer 40, forming second barrier layer 44 on first spacer layer 40, and forming second barrier layer 46 on second spacer layer 44, whereby 2-dimensional electron gas 54 is formed in channel layer 38 distal to buffer layer 43 as a result of forming first 42 and second 46 barrier layers. Suitable methods of forming the various layers of epitaxial structure 30 of the invention are known to those of skill in the art.

[0032] In another embodiment the invention is a method of forming a high electron mobility transistor (HEMT) structure employing the epitaxial structure of the invention. The method includes, in addition to epitaxial structure 30, forming source 48 and drain 50 terminals in electrical communication with second barrier layer 46, and gate terminal 52 that is in direct electrical communication with at least one of first barrier layer 42 and second barrier layer 46, and between source terminal 48 and drain terminal 50.

[0033] The following are non-limiting examples of embodiments of the invention.

EXEMPLIFICATION

[0034] Example 1 (Prophetic)

[0035] A band diagram is simulated using software to simultaneously solve Poisson and Schrodinger equations in 1 dimension.. The bandgap is 6.2 eV for AlN., 3.4 eV for GaN, and 4.6 eV for lattice matched InAlN. The surface barrier height for InAlN is 2.5 eV. As shown in FIGs. 3 and 4, the AlN spacer thickness is 1nm. The total barrier (AlN+InAlN thickness was fixed at 12 nm. The distribution of 2DEG density is plotted as a function of the depth from the surface.

[0036] As can be seen in FIGs. 3 and 4, the effective barrier height ϕ_{eff} is the barrier height of InAlN, of about 2.5 eV. In the structure with a second AlN spacer, the conduction band offset (Ec) between indium aluminum nitride (InAlN) and aluminum nitride (AlN) causes an effective barrier height of about, 3.05 eV, which is roughly a 22% increase over an equivalent epitaxial structure having only a single AlN spacer. This helps to block electrons flowing from the gate to the channel and hence reduce gate leakage.

[0037] Example 2 (Prophetic)

[0038] As can be seen in FIG. 5, 2-dimensional electron gas (2DEG) density is simulated with and without a second AlN spacer. The plot shown in FIG. 5 was constructed with total barrier thickness fixed at 11 nm (InAlN and second AlN spacer layer). Changing the AlN spacer position does not significantly change 2DEG density.

[0039] As can be seen in FIG. 6, two control samples, having an indium aluminum nitride (InAlN) barrier layer without a second aluminum barrier, were grown in an MOCVD reactor operating at low pressure. The structure consists of a thin gallium nitride (GaN) nucleation layer, 1.9 μm thick carbon-GaN buffer layer, 15 nm thick GaN channel, 1 nm aluminum nitride spacer, and doped 11 nm thick in the indium aluminum nitride (InAlN) barrier. Growth temperature was about 750°C for the barrier layer 42 and 46 and about 1030°C for the GaN channel layer 38. Two more samples were grown with the second AlN spacer inserted in the middle of the InAlN barrier. Separation of the two AlN spacers was 2 nm and 6 nm for the two

samples. The growth conditions for the second AlN spacer were the same in the control samples.

[0040] The two control samples show sheet resistance range between 193 and 200 ohms/sq. The structures with the second aluminum nitrite (AlN) spacer exhibit sheet resistance of 206 and 183 ohms/sq, respectively, which are very close to the control range, indicating there is no degradation in 2 DEG transport properties.

[0041] Example 3

[0042] HEMT devices were fabricated using a control sample and two other samples with second AlN spacers. The fabricated gate length was ~1 μm. The separation between gate and drain was ~3 μm. The separation between gate and source was ~1 μm. The source-drain bias was fixed at 6V. The gate bias was swept between -6 and 2V. FIG. 7 shows the plot of the channel current as a function of the gate bias. At off state, the drain-source current in the control sample is ~3e-5 A/mm, compared to 1.5e-6 A/mm and 9e-8 A/mm in the samples with the second AlN spacer layer. Thus the devices can be turned off more completely at OFF status. The ON/OFF ratio is improved more than two orders of magnitude in the sample with the 6 μm separation between two AlN spacers. FIG. 8 shows the gate leakage current as a function of gate bias. The gate leakage at OFF state is reduced by more than two orders of magnitude.

EQUIVALENTS

[0043] While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

[0044] The relevant teachings of all patents, published patent applications, and publications cited are incorporated herein by reference in their entirety.

CLAIMS

What is claimed is:

1. An epitaxial structure, comprising:
   a) a substrate;
   b) a buffer layer on the substrate;
   c) a channel layer over the buffer layer, wherein the channel layer includes a 2-dimensional electron gas;
   d) a first spacer layer on the channel layer;
   e) a first barrier layer on the first spacer layer;
   f) a second spacer layer on the first barrier layer; and
   g) a second barrier layer on the second spacer layer;

2. The epitaxial structure of claim 1, wherein the first and second barrier layers are each independently formed of at least one member of the group consisting of aluminum nitride, aluminum gallium nitride, indium aluminum nitride, and indium aluminum gallium nitride.

3. The epitaxial structure of claim 2, wherein the first and second barrier layers each independently consist essentially of $In_yGa_zAl_{1-y-z}N$, where $0.03 \leq y \leq 0.3$ and $0.01 \leq z \leq 0.1$.

4. The epitaxial structure of claim 3, wherein the channel layer consists essentially of $In_xGa_{1-x}N$, where $0 \leq x \leq 1$.

5. The epitaxial structure of claim 4, wherein the first spacer layer is formed of a material selected from the group consisting of aluminum nitride, aluminum gallium nitride.

6. The epitaxial structure of claim 5, wherein the second spacer layer is formed of a material selected from the group consisting of aluminum gallium nitride, indium aluminum gallium nitride.

7. The epitaxial structure of claim 6, wherein the average collective thickness of the first and second barrier layers, and the second spacer layer is about 11 nm.

8. The epitaxial structure of claim 7, wherein the first barrier layer has an average thickness of about 8 nm, the second barrier layer has an average thickness of about 2 nm and the second spacer layer has an average thickness of about 1 nm.

9. The epitaxial structure of claim 8, wherein the first spacer layer has an average thickness of about 1 nm.

10. The epitaxial structure of claim 9, wherein the substrate is formed of at least one material selected from the group consisting of silicon carbide (SiC), sapphire (Al_2O_3), silicon (Si), gallium nitride (GaN), and aluminum nitride (AlN).

11. The epitaxial structure of claim 10, further including a back barrier layer between the buffer layer and the channel layer.

12. The epitaxial structure of claim 11, wherein the buffer layer includes at least one material selected from the group consisting of gallium nitride, indium gallium nitride and aluminum gallium nitride.

13. The epitaxial structure of claim 1, wherein the epitaxial structure is a high electron mobility transistor.

14. The epitaxial structure of claim 13, further including:
    a) a source terminal in electrical communication with the second barrier layer;
    b) a drain terminal in electrical communication with the second barrier layer; and

c) a gate in electrical communication with at least one of the first and second barrier layers and between the source and drain terminals.

15. A method of forming an epitaxial structure, comprising the steps of:
 a) forming a buffer layer on a substrate;
 b) forming a channel layer on the buffer layer;
 c) forming a first spacer layer on the channel layer;
 d) forming a first barrier layer on the first spacer layer;
 e) forming a second spacer layer on the first barrier layer; and
 f) forming a second barrier layer on the second spacer layer whereby a 2-dimensional electron gas region is formed in the channel layer as a result of forming the first and second barrier layers.

16. The method of claim 15, wherein the first and second barrier layer are each independently formed of at least one member of the group consisting of aluminum nitride, aluminum gallium nitride, indium aluminum nitride and indium aluminum gallium nitride.

17. The epitaxial structure of claim 16, wherein the first and second barrier layers each independently consist essentially of $In_yGa_zAl_{1-y-z}N$, where $0.03 \leq y \leq 0.3$ and $0.01 \leq z \leq 0.1$.

18. The method of claim 17, wherein the channel layer includes at least one member selected from the group consisting of gallium nitride and indium gallium nitride.

19. The method of claim 18, wherein the first spacer layer is formed of a material selected from the group consisting of aluminum nitride, aluminum gallium nitride.

20. The method of claim 19, wherein the second spacer layer is formed of a material selected from the group consisting of aluminum gallium nitride, indium aluminum gallium nitride.

21. The method of claim 20, wherein the average collective thickness of the first and second barrier layers, and the second spacer layer, is about 11 nm.

22. The method of claim 21, wherein the first barrier layer has an average thickness of about 8 nm, the second barrier layer has an average thickness of about 2 nm and the second spacer layer has an average thickness of about 1 nm.

23. The method of claim 22, wherein the first spacer layer has an average thickness of about 1 nm.

24. The method of claim 23, wherein the substrate is formed of at least one material selected from the group consisting of silicon carbide, sapphire silicon, gallium nitride, and aluminum nitride.

25. The epitaxial structure of claim 24, further including a back barrier layer between the buffer layer and the channel layer.

26. The method of claim 25, wherein the buffer layer includes at least one material selected from the group consisting of gallium nitride.

27. The epitaxial structure of claim 26, wherein the epitaxial structure is a high electron mobility transistor.

28. The method of claim 27, further including the steps of:
    a) forming a source terminal in electrical communication with the second barrier layer;

b) forming a drain terminal in electrical communication with the second barrier layer; and

c) forming a gate terminal in electrical communication with at least one of the first and second barrier layers between the source and drain terminals.

29. An epitaxial structure, comprising:

a) a substrate;

b) a buffer layer on the substrate;

c) a channel layer over the buffer layer, wherein the channel layer includes a 2-dimensional electron gas region;

d) a first spacer layer on the channel layer;

e) a first barrier layer on the first spacer layer; and

f) a second spacer layer on the first barrier layer.

30. A method of forming an epitaxial structure, comprising the steps of:

a) forming a substrate;

b) forming a buffer layer on the substrate;

c) forming a channel layer over the buffer layer;

d) forming a first spacer layer on the channel layer;

e) forming a first barrier layer on the first spacer layer; and

f) forming a second spacer layer on the first barrier layer,
whereby a 2-dimensional electron gas region is formed in the channel layer as a result of forming the first and second barrier layers.

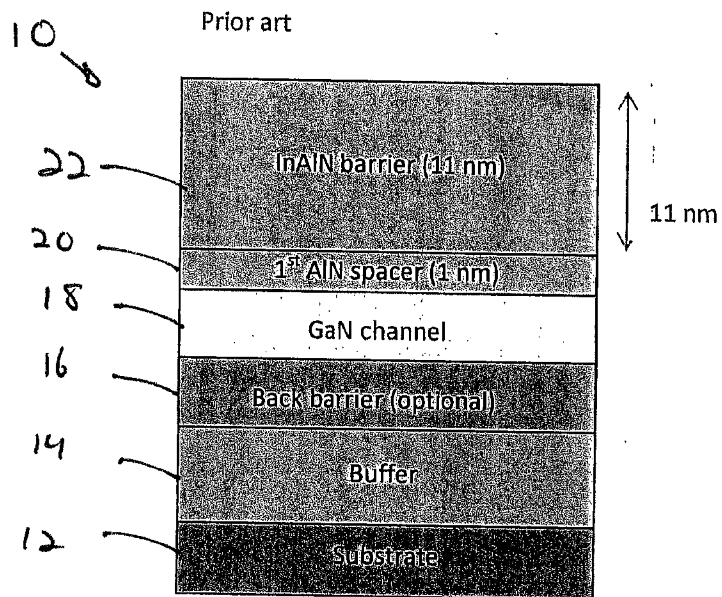

Fig. 1
(PRIOR ART)

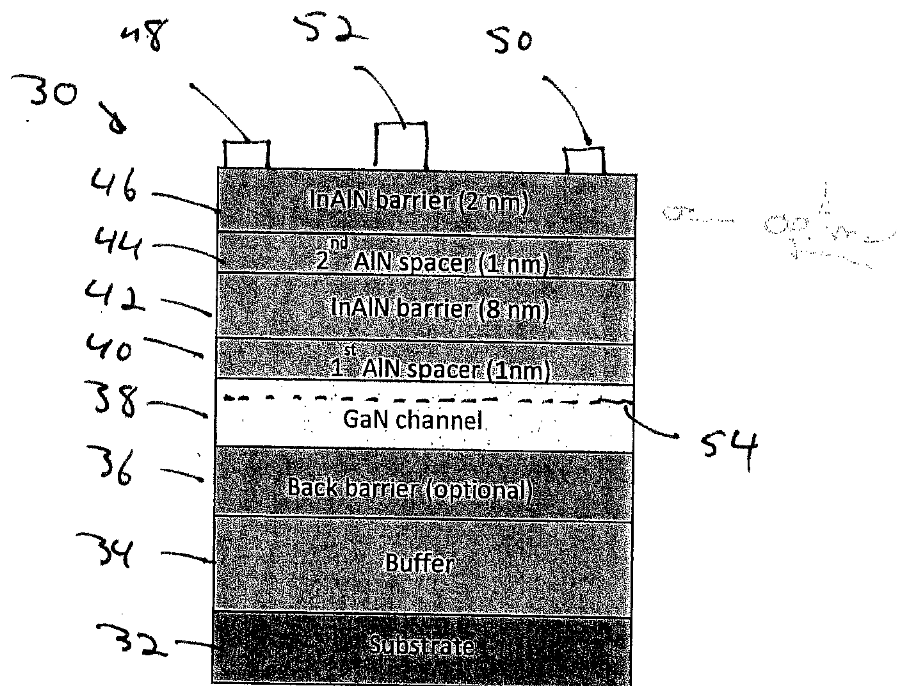

FIG. 2

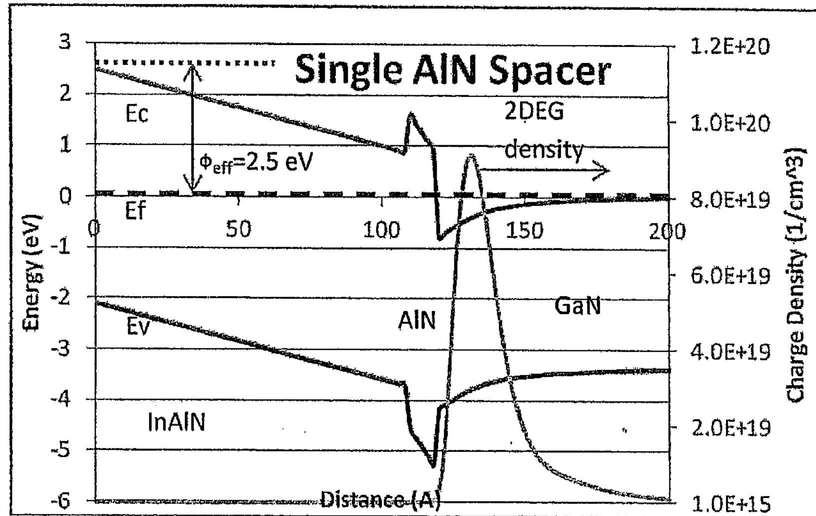

FIG. 3

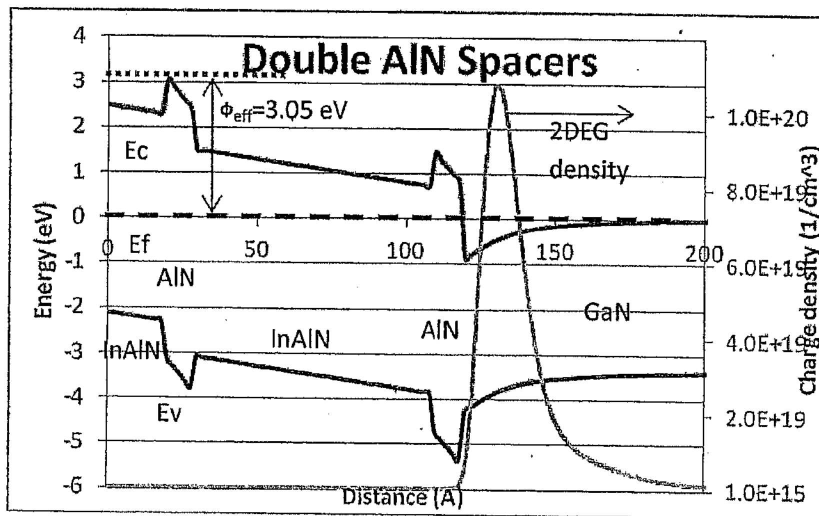

FIG. 4

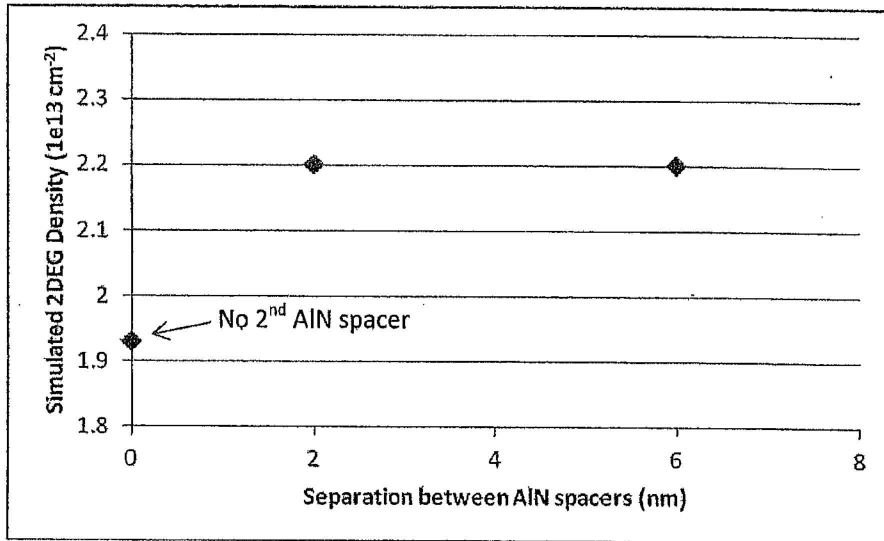

FIG. 5

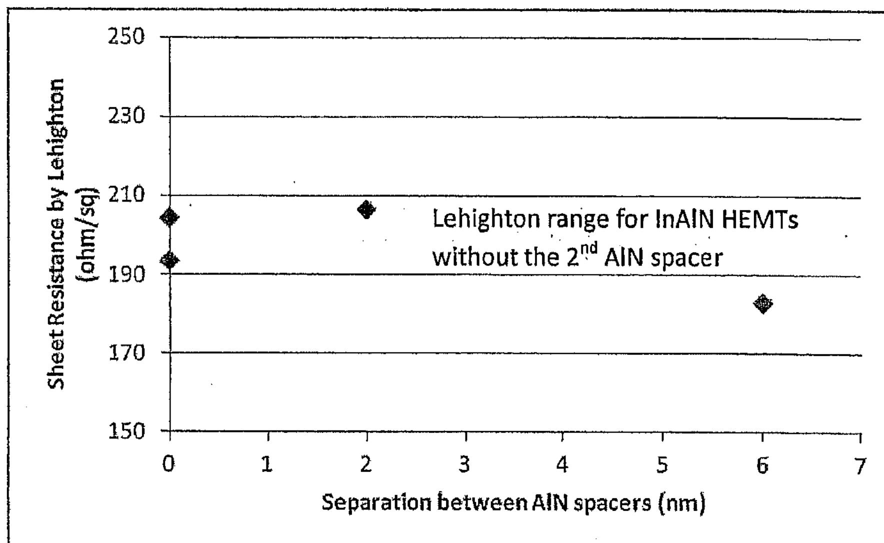

FIG. 6

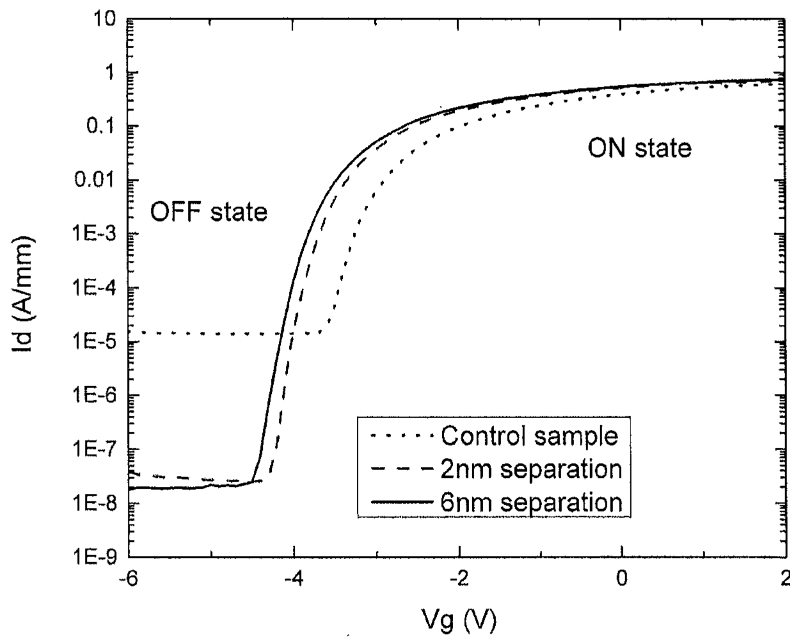

FIG. 7

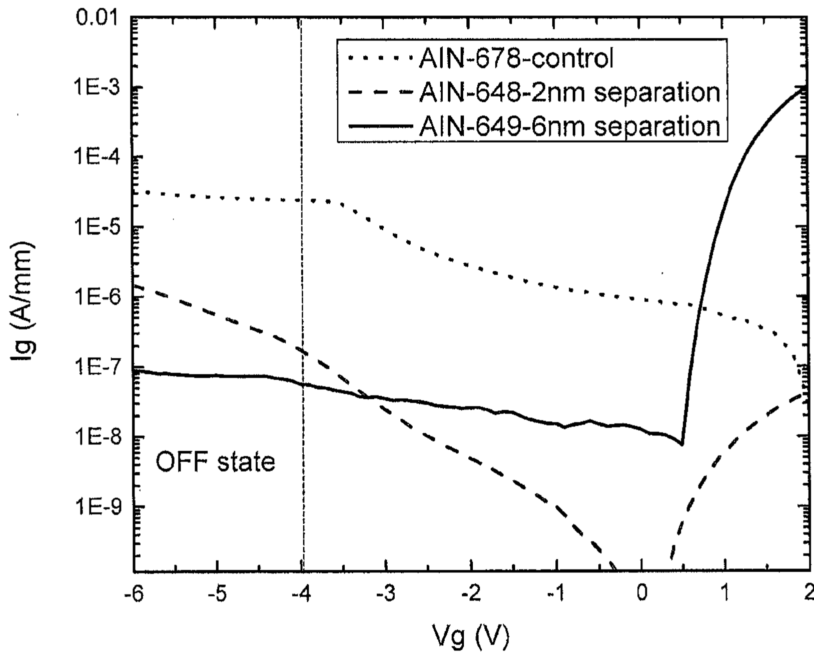

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/044808

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/778 H01L29/205
ADD. H01L29/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2012/014883 A1 (NGK INSULATORS LTD [JP]; MIYOSHI MAKOTO [JP]; SUGIYAMA TOMOHIKO [JP];) 2 February 2012 (2012-02-02) figure 1 and associated text -& EP 2 600 394 A1 (NGK INSULATORS LTD [JP]) 5 June 2013 (2013-06-05)	1-30
X	US 2010/102359 A1 (KHAN M ASIF [US] ET AL) 29 April 2010 (2010-04-29)	1-7, 13-21, 29,30
A	figures 7, 8 and associated text	11,25
X	WO 2004/107406 A2 (UNIV TEXAS [US]; DUPUIS RUSSELL D; CHOWDHURY UTTIYA) 9 December 2004 (2004-12-09) figures 14, 15 and associated text	1,2, 13-16, 29,30

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 August 2013	13/08/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Moehl, Sebastian

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/044808

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CHOWDHURY U ET AL: "Modulation-doped superlattice AlGaN barrier GaN/AlGaN HFETs", JOURNAL OF CRYSTAL GROWTH, ELSEVIER, AMSTERDAM, NL, vol. 272, no. 1-4, 10 December 2004 (2004-12-10), pages 318-321, XP004658490, ISSN: 0022-0248, DOI: 10.1016/J.JCRYSGRO.2004.08.058 figure 1 and associated text -----	1,2, 13-16, 29,30

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/044808

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2012014883 A1	02-02-2012	CN 103003931 A EP 2600394 A1 US 2013134439 A1 WO 2012014883 A1	27-03-2013 05-06-2013 30-05-2013 02-02-2012
EP 2600394 A1	05-06-2013	CN 103003931 A EP 2600394 A1 US 2013134439 A1 WO 2012014883 A1	27-03-2013 05-06-2013 30-05-2013 02-02-2012
US 2010102359 A1	29-04-2010	US 2010102359 A1 WO 2008127469 A2	29-04-2010 23-10-2008
WO 2004107406 A2	09-12-2004	US 2005006639 A1 WO 2004107406 A2	13-01-2005 09-12-2004