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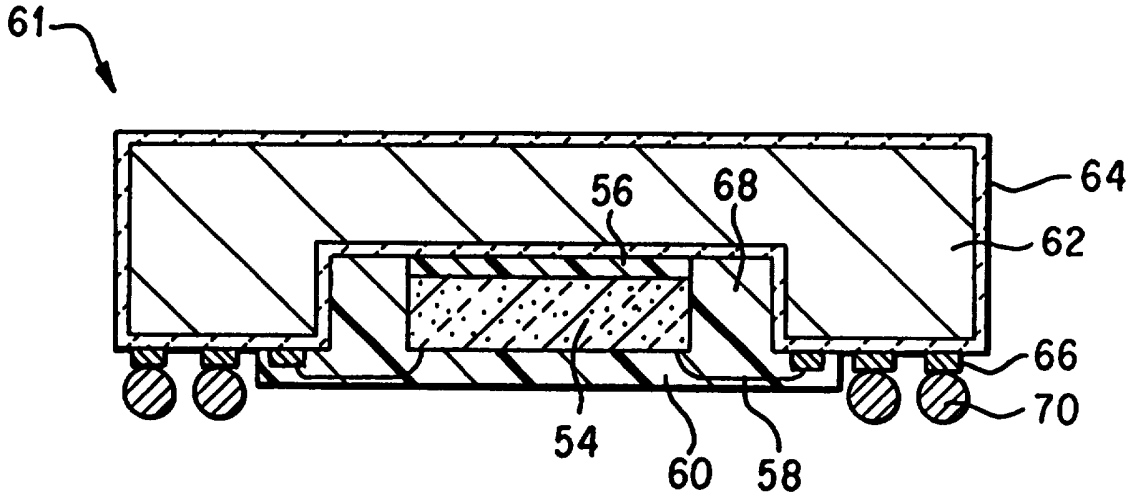
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(54) Title: INTEGRALLY BUMPED ELECTRONIC PACKAGE COMPONENTS



(57) Abstract

There is disclosed a component (61) for electronic packaging applications. A metallic substrate (62) having a centrally disposed cavity (68) is coated with an electrical isolating layer (64). Circuit traces (66) electrically interconnect a semiconductor device (54) with solder balls (70). A potting compound (60) encapsulates the integrated circuit device (54) and a portion of the circuit traces (66).

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INTEGRALLY BUMPED ELECTRONIC PACKAGE COMPONENTS

This invention relates to components for electronic packages having integral bumps. More particularly, leadframes and package bases contain unitary protrusions for electrical interconnection to external circuitry.

Microelectronic devices are typically manufactured from a semiconductor material such as silicon, germanium or gallium/arsenide. The semiconductor material is fashioned into a die, a generally rectangular structure having circuitry formed on one surface. Along the periphery of that electrically active surface are input/output pads to facilitate electrical interconnection to external circuitry.

The semiconductor device is brittle and requires protection from moisture and mechanical damage. This protection is provided by an electronic package. The electronic package further contains an electrically conductive means to transport electrical signals between the semiconductor device and the external circuitry.

One electronic package is disclosed in U.S. Patent No. 4,939,316 to Mahulikar et al. The patent discloses separate anodized aluminum or aluminum alloy base and cover components defining a cavity. A leadframe is disposed between the base and the cover and adhesively bonded to both. A semiconductor device is encased within the cavity and electrically interconnected to the inner lead ends of the leadframe. The outer lead ends of the

leadframe extend beyond the package perimeter and are interconnected to external circuitry.

A similar electronic package having an anodized aluminum or aluminum alloy base component and a cover formed from a material other than aluminum is disclosed in U.S. Patent No. 5,155,299 to Mahulikar et al.

The available space on a printed circuit board is limited and it is desirable to minimize the peripheral area of a package. The peripheral area of a leaded package extends beyond the perimeter of the package base and cover to a point defined by the outer lead portions of the leadframe.

To minimize the peripheral area of an electronic package, electrical interconnection may be through the base of a package. One such electronic package is disclosed in U.S. Patent No. 4,965,227 to Chang et al. A plurality of terminal pins support and are electrically interconnected to a flexible metal tape formed into a desired circuit pattern. One end of the terminal pins, the flexible metal circuit and a semiconductor device are then encapsulated in a molding resin. The molding resin defines the package perimeter with the unencapsulated end of the terminal pins extending outward from the package base.

The terminal pins are thin, 0.51 mm (0.020 inch) diameter copper, as an example, and may be up to 12.7 mm (0.5 inch) long. The pins are prone to bending and care is required to maintain pin alignment. The pins are plugged into mating holes on a printed circuit board. Care is also required when drilling the holes to insure an accurate fit.

A cross between a leaded package and a pin grid array package is disclosed in U.S. Patent No. 4,677,526 to Muehling. The outer leads of a leadframe are bent to a 90° angle relative to the plane defined by the inner leads. The inner leads and a semiconductor device are encapsulated in a molding resin with the outer lead portions extending through the package base.

A disadvantage with this package is that the radius of curvature is dependent on the leadframe material and the temper of that material. If the radius is formed too tightly, the leadframe material may crack or "orange peel". Generally, the ratio of the minimum bend radius to the leadframe thickness, mbr/t, is between about 1 and 2 for copper alloy leadframes. A 0.25 mm (0.010 inch) thick leadframe requires a radius of curvature of at least 0.25 mm (0.010 inch) to prevent lead fracture.

Metallic solder pads and solder balls are used in a ball grid array and land grid array packages as disclosed in U.S. Patent No. 5,241,133 to Mullen, III et al. The patent discloses an electronic package having an insulating substrate with circuit traces on a first side and a uniform array of solder pads on an opposing second side. A semiconductor device is mounted to the first side of the substrate and electrically interconnected to the circuit traces. Conductive vias electrically interconnect the circuit traces and the solder pads. A molded plastic cover encapsulates the device and inner lead ends.

A ball grid array package having a metallic base is disclosed in PCT International Publication

WO94/22168 entitled "Ball Grid Array Electronic Package", Published September 29, 1994 . A metallic base component has an array of holes. The walls of the holes are electrically nonconductive. If, for example, the base is aluminum or an aluminum alloy, the hole walls are made nonconductive by anodization. Terminal pins, a solder or a conductive adhesive extend through the holes terminating approximately in the plane defined by the outside surface of the base.

A problem with ball grid array packages is the coefficient of thermal expansion (C.T.E.) mismatch between the semiconductor package and a printed circuit board causes the solder balls to be extended or compressed with temperature variations. This flexing fatigues the solder balls and eventually causes failure of the solder joint.

A solution to solder fatigue is disclosed in U.S. Patent No. 4,581,680 to Garner. Metallization pads are formed in recesses on the package base. The depth of the recesses increases with the distance between the recess and the center of the package base. Longer length solder joints around the periphery of the package provide improved flexibility to compensate for the C.T.E. mismatch.

There exists, however, a need for an improved leadframe having outer leads perpendicular to the inner leads. There exists also a need for a ball grid array electronic package or land grid array electronic package that reduces solder fatigue.

Accordingly, it is a first object of the invention to provide a leadframe having outer lead ends substantially perpendicular to the inner lead

portion that is not constrained by a minimum bend radius dependent on the thickness. It is a second object of the invention to provide a ball grid electronic package that has reduced solder fatigue.

It is a feature of the invention that both the first object and the second object are met by integrally bumped package components. It is a feature of the invention that a leadframe is formed by etching outer lead protrusions from a relatively thick strip of an electrically conductive material. The protrusions are formed by etching rather than stamping and the minimum bend radius is not dependent on the leadframe thickness. It is an advantage of the invention that the radius may approach zero.

Another feature of the invention is that integral bumps are formed in the package substrate. These bumps support the package and form standoffs to prevent the weight of the package from distorting the solder balls. It is an advantage of the invention that the integral bumps reduce the volume of the solder required to interconnect the package and a printed circuit board increasing the number of thermal cycles before fatigue failure.

The above stated objects, features and advantages, as well as others, will be apparent from the specification and drawings that follow.

Figure 1 shows in top perspective view a metallic strip prepared for etching to form a leadframe in accordance with the invention.

Figure 2 shows in cross sectional representation the metallic strip of Figure 1.

Figure 3 shows in cross sectional representation the metallic strip following a first etching operation.

Figure 4 shows in cross sectional representation the etched metallic strip of Figure 3 having a polymer backing layer.

Figure 5 shows in cross sectional representation the metallic strip following a second etching operation.

Figure 6 shows in perspective view the leadframe of the invention.

Figure 7 shows in cross sectional representation a cavity down molded plastic electronic package formed according to the invention.

Figure 8 shows in bottom planar view the cavity down package of Figure 7.

Figure 9 shows in cross sectional representation a ball grid array electronic package according to an embodiment of the invention.

Figure 10 shows in cross sectional representation a leaded electronic package in accordance with the invention.

Figure 11 shows in cross sectional representation a ball grid array electronic package including a polymer sealant standoff.

Figure 12 shows in cross sectional representation a ball grid array electronic package having a wire bond shelf.

Figure 13 shows in cross sectional representation a flip chip bonded electronic package having a polymer sealant standoff.

Figure 14 shows in cross sectional representation a cavity down ball grid array electronic package having integral bumps.

Figure 15 shows in cross sectional representation a cavity up ball grid array electronic package having a multilayer circuit.

Figure 16 shows in cross sectional representation a cavity up ball grid array electronic package having a flip chip bonded semiconductor device.

Figure 17 shows in cross sectional representation a cavity down ball grid array electronic package having a flip chip bonded semiconductor device.

Figure 18 shows in cross sectional representation two integrally bumped electronic packages nested together.

Figure 19 shows in cross sectional representation a stamped leadframe having bumps in accordance with an embodiment of the invention.

Figure 20 shows in cross sectional representation the leadframe of Figure 19 after etching to electrically isolate the leads.

Figure 1 shows in a perspective view a first method for the manufacture of a leadframe from a metallic strip 10 in accordance with the invention while Figure 2 illustrates the same metallic strip when viewed along cross-sectional line 2-2.

The metallic strip 10 is formed from any electrically conductive material that is readily etched such as copper, copper alloys and iron-nickel alloys. Copper alloys are preferred because of the high electrical conductivity of copper and the ease

with which copper is etched. Suitable copper alloys included those designated by the Copper Development Association (CDA) as C194 (nominal composition by weight 2.35% iron, 0.03% phosphorous, 0.12% zinc, balance copper) and C7025 (nominal composition by weight 3.0% nickel, 0.65% silicon, 0.15% magnesium and the balance copper).

The thickness of the metallic strip 10 is determined by the desired thickness of the integral bumps as described below. Typically, the thickness of the metallic strip 10 is from about 0.15 millimeter to about 0.51mm (0.006 to 0.020 inch) and preferably from about 0.20mm to about 0.30mm (0.008 to 0.012 inch).

A first side 12 of the metallic strip 10 is coated with a first resist 14. The first resist 14 is any polymer that resists attack in the chemical solution used to etch the metallic strip 10 and is also preferably photoimageable to facilitate circuit manufacture. One suitable first resist is "RISTON" (trademark of DuPont, Wilmington, DE). The resist is applied by any suitable method such as spraying, screening or dipping. The entire first side 12 of the metallic strip 10 is preferably coated with the first resist 14.

The opposing second side 16 is selectively coated with a second resist 18. The second resist 18 is any polymer that is chemically resistant to the etching solution and may have the same composition as the first resist 14. The second resist 18 is deposited as a plurality of discrete pads 20 corresponding to a desired array of bumps in the integrally bumped leadframe. A centrally

positioned discrete pad 22 may be included if an integral heat sink is also desired.

The resist coated metallic strip 10 is immersed in a suitable chemical etch solution. For a copper alloy, immersion in an aqueous solution containing a mixture of cupric chloride and hydrochloric acid at a temperature of 55°C will etch the metallic strip at a rate of about 0.04mm (0.0016 inch) per minute. As illustrated in Figure 3, the metallic strip 10 is immersed in the etch solution for a time sufficient to etch those portions of the metallic strip not covered with the second resist 18 to a remaining thickness, "R", of from about 0.013mm to about 0.1mm (0.0005-0.004 inch).

The second resist 18 is then removed by dissolution in a suitable solvent. For RISTON, sodium carbonate is a suitable solvent for portions not exposed to ultraviolet radiation while sodium hydroxide is suitable for those portions exposed to ultraviolet radiation. Removal of the second resist 18 exposes the integral bumps 24 as illustrated in Figure 4. The integral bumps 24 are unitary with the metallic strip 10 and form the outer lead portions of the leadframe.

The remainder, "R", of the metallic strip 10 after etching is thin and it is preferable to support the etched metallic strip 10. A polymer resin 26 fills the etched portion between the integral bumps 24. The polymer resin is chemically resistant to the etch solutions and also effective for increasing the rigidity of the etched metallic strip. One suitable polymer 26 is an epoxy.

The polymer resin 26 fills the etched portions to a height less than the height of the integral bumps 24. Preferably, the integral bumps 24 extend from about 0.1mm to about 0.4mm (0.004-0.015 inch) above the height of the polymer resin 26.

The first resist 14 is now imaged into desired circuit patterns. This imaging may be by photolithography as known in the art. A mask partially obscures the first resist 14 from a radiating polymerization source such as an ultraviolet (UV) light. Those portions 28 of the first resist 14 exposed to the UV light polymerize and are not removed in a selected solvent (for a "positive" photoresist). The portions 30 of the first resist shielded from the UV source are readily removed by the selected solvent.

After removal of the unexposed portions 30 of the first resist 14, the metallic strip 10 is immersed in a suitable etch solution. To avoid chemical dissolution of the integral bumps 24, either the bumps are coated again with resist or the strip 10 is only partially immersed in the chemical solution with the integral bumps remaining outside the solution.

The chemical solution etches electrical isolation channels 32 through the remainder, "R", of the metallic strip 10 as shown in Figure 5 completing the leadframe.

The integral bumps 24 may be coated with a solderable material 34 such as gold or tin to facilitate bonding to a printed circuit board. Alternatively, the integral bumps are coated with a tin/lead alloy solder or other low melting

temperature solder. The solderable material 34 is preferably applied by electrolytic plating and has a thickness of from about 1 to about 5 microns with gold coatings being toward the low end of the range and solder coatings toward the high end of the range.

The opposing side 36 of the leadframe may be entirely or selectively coated with a wire bondable layer 38 such as silver or aluminum. The wire bondable layer has a thickness of from about 0.5 to about 2 microns and is preferably applied either electrolytically, for silver, or by vapor deposition, for aluminum.

The leadframe 40 is illustrated in a perspective and partially cross sectional view in Figure 6. The metallic strip has been etched to form a plurality of electrically isolated leads 42 each having an outer portion 44 terminating at an integral bump 24 extending beyond the depth of a supporting polymer resin 26. The leads 42 have an inner lead portion 46 extending toward a central region of the leadframe 40.

Optionally, as illustrated in Figures 1 and 6, a centrally positioned heat spreader 48 is formed from the same metallic strip. One or more semiconductor devices are then bonded to either the heat spreader 48 or to the polymer resin 26 and electrically interconnected to the inner lead portions 46.

The advantages of the leadframe 40 as compared to prior art leadframes is that the outer lead portions 44 extend downward, rather than outward reducing the peripheral dimensions of an electronic

package. The outer lead portions 44 are formed substantially perpendicular to the inner lead portions 46 by etching, rather than bending. As a result, the angle, α, between the outer lead portions 44 and inner lead portions 46 approaches 90° and is not limited by mbr/t.

Figure 7 illustrates a cavity down electronic package 50 utilizing the leadframe 40 of the invention. The outer lead portion 44 extends beyond a polymer resin 26 for electrical interconnection to external circuitry. The inner lead portion 46 is patterned into circuit traces and a heat spreader 48. To electrically isolate circuit traces and prevent contamination from causing a short circuit, a backing layer 52 may be applied over the inner lead portion. One suitable backing layer is a polymer such as epoxy or polyimide. A second suitable backing layer 52 is a metallic substrate coated with an electrically insulating layer similar to the package bases described below.

At least one semiconductor device 54 is bonded to the heat spreader 48 by a suitable die attach material 56. Any conventional die attach material may be utilized such as a low melting temperature lead/tin alloy solder or a silver filled epoxy adhesive. The semiconductor device is electrically interconnected to the inner lead portion 46 of the leadframe 40 by small diameter bond wires 58 or by thin strips of copper foil as known from tape automated bonding ("TAB").

After electrical interconnection, a potting compound 60 such as an epoxy or a silicone encapsulates the semiconductor device 54, bond wires

58 and a portion of the inner leads 46 adjacent the bond wires.

Figure 8 illustrates the package 50 in bottom planar view with the potting compound removed for clarity. The outer lead portions 44 extend upward supported by the polymer resin 26. The semiconductor device 54 is bonded to the heat spreader 48 and electrically interconnected to the inner lead portions 46.

An alternative method of manufacturing the leadframe is illustrated in cross sectional representation in Figures 19 and 20. In Figure 19, a metallic strip 10 is mechanically deformed, such as by deep drawing or cupping, to form a plurality of integral bumps 24 and, optionally, a heat spreader 48. A polymer resin 26 is applied to support the leads and a second resist 18 is applied to the second side 16 of the metallic strip 10.

The second resist 18 is patterned, such as by photolithography, to form desired circuit patterns. The leadframe structure is immersed in a suitable etching solution, taking care not to etch the integral bumps 24, electrically isolating the inner lead portions as shown in Figure 20. The leadframe 40' is then used in the same manner as the leadframe 40 described above.

An advantage with the leadframe 40' is that the integral bumps 24 are formed by stretching the metallic strip 10. The bumps are thinner than the undeformed portions 59 of the metallic strip and are very compliant. C.T.E. mismatch between the printed circuit board and the electronic package is compensated by flexing of the integral bumps 24

reducing the cyclical stress applied to the solder bumps, thereby reducing fatigue.

Figure 9 illustrates a ball grid array package 61 in accordance with an embodiment of the invention. The ball grid array package 61 has a base 62. The base 62 may be any suitable material such as a metal, polymer or ceramic. Metals are preferred to exploit the high thermal conductivity, etchability and machinability. If the base 62 is electrically conductive, the base is coated with an electrically insulating layer 64.

A preferred material for the metallic base is aluminum or an aluminum alloy. The electrically insulating layer 64 is then an anodization layer. Aluminum is light weight and applies less weight to the solder balls than a similarly sized base formed from a more dense material. The reduced weight leads to less creep in the solder balls as a function of time. Creep is a problem in that the closely spaced solder balls could contact forming a short circuit.

Anodized aluminum is not wet by molten solder balls. The solder balls therefore do not migrate away from the desired trace location. The infrared emissivity of black integrally anodized aluminum allows effective heat transfer. The packages of the invention work well with current surface mount technology (SMT) infrared solder reflow equipment.

Aluminum has a low elastic modulus and a minimal compressive and expansive effect on the solder balls reducing solder ball fatigue.

The base 62 can be formed from other anodizable metals such as titanium or a titanium alloy or from

a non-anodizable metal such as copper. If a non-anodizable metal is used, the metal may be coated with an electrically insulating layer 64 such as Al_2O_3 or polymer. Also suitable are metals capable of forming a refractory oxide layer in situ, such as a copper alloy containing from about 2% to about 12% by weight aluminum.

Circuit traces 66 are formed on the insulating layer by any suitable means. A conductive ink may be deposited by screen printing and copper electrolytically deposited on the conductive ink to a desired thickness and electrical conductivity. Alternatively, the circuit traces 66 may be deposited by vapor deposition or by direct writing. If the insulating layer 64 is an insulating sheet such as an organic polymer, a metallic foil may be bonded to the sheet and photoimaged into desired circuit patterns using conventional flexible circuit techniques.

A semiconductor device 54 is bonded to a central portion of the base 62 by a die attach 56. Optionally, to reduce the height of the wire bonds 58, a cavity 68 is formed in the base 62. The device 54 is electrically interconnected to the circuit traces 66 by the wire bonds 58. The device, wire bonds 58 and that portion of the circuit traces 66 adjacent the wire bonds 58 are then encapsulated in a potting compound 60.

Peripheral portions of the circuit traces 66 are bonded to solder balls 70 for electrical interconnection to external circuitry. Alternatively, the package base may contain recessed dimples for alignment of the solder balls. Circuit

traces or electrically conductive vias provide contact with the solder balls.

When the electrically insulating layer 64 is an anodic film, the film has a uniform dispersion of pores as disclosed in U.S. Patent No. 5,066,368 to Pasqualoni et al. Superior adhesion to a polymeric die attach material 56 and potting compound 60 is obtained when the pore size is from about 50 to about 500 angstroms. However, the pores interfere with the deposition of the circuit traces 66. Accordingly, in a preferred embodiment of the invention, in that portion of the insulating layer underlying the polymers the pores are not sealed. The remainder of the insulating layer is preferably sealed.

The anodization layer is sealed by any conventional process such as immersion in boiling water for 15-30 minutes or immersion in a hot aqueous solution containing nickel acetate.

The portion of the insulating layer 64 that will underlie the die attach material 56, as well as optionally, the side walls of the cavity 68 are masked during the sealing step to retain open pores.

A leaded package 80 in accordance with the invention is illustrated in cross sectional representation in Figure 10. The package has a metallic base 62 coated with an electrically insulating layer 64. The leads 82 of a leadframe are either bonded to the insulating layer 64 by a polymer adhesive 84 or bonded to a circuit trace 66 by a low temperature solder 86 or other conductive medium.

If the insulating layer is an anodic film, the pores are preferably sealed on all surfaces except those that contact a polymer adhesive or polymer die attach. A potting compound then seals the semiconductor device 54, the wire bonds 58 and either the inner lead portion or circuit trace portion adjacent the wire bonds.

Figure 11 illustrates in cross sectional representation an electronic package 90 that resists fatigue of the solder balls 70. Solder ball fatigue is caused by cyclical expansion and contraction of the solder balls when the electronic package 90 and a printed circuit board 92 have different coefficients of thermal expansion. When the printed circuit board is FR-4, a fire resistant, glass filled epoxy, the C.T.E. is about equal to that of copper $180x10^{-7}/°C$. If the package base 62 is aluminum, the C.T.E. is about $230x10^{-7}/°C$ and if the package base as alumina, the C.T.E. is about $60x10^{-7}/°C$.

By the inclusion of a standoff 94, expansion and contraction of the solder balls 70 is minimized, reducing solder creep, solder fatigue and squashing of the solder balls. Also, C.T.E. mismatch induced stress in the plane of the base (X&Y directions) is reduced. The standoff 94 is material having a yield stress greater than that of the solder forming the solder balls 70. A typical solder composition is 60% Sn/40% Pb has a mean tensile strength of about 52.5MPa (7.61 ksi) and a limiting creep rupture strength of 1000 hours at a stress of 4.5MPa (650 psi) at 26°C. The limiting creep rupture strength is 1000 hours at a stress of 1.4MPa (200 psi) at

80°C. The creep rupture strength is the stress that will cause fracture in a creep test at a given time in a specified environment.

A polymer suitable as a standoff with a yield stress above this value is an epoxy. The standoff 94 prevents the spacing between the package 90 and the printed circuit board 92 from changing in response to temperature fluctuations. Preferably, the C.T.E. of the polymer sealant is as low as possible so as not to contribute to cycling of the solder balls.

While the standoff may be any suitable material, adhesives are preferred. The standoff is then applied as a ring about the perimeter of the package 90 providing greater environmental protection for the semiconductor device 54.

Figure 12 illustrates in cross sectional representation an electronic package 100 having a wire bond shelf 102. The wire bond shelf 102 is substantially coplanar with the surface 104 of the package base 62 having circuit traces 66. The coplanarity facilitates uniform deposition of the circuit traces by a line of site deposition process such as vapor deposition and also screen printing of photoresists and conductive inks. The side walls 106 between the wire bond shelf 102 and the surface 104 form an angle of less than 90°C and preferably between about 40°C and 60°C to facilitate uniform deposition of the circuit traces 66 and other materials. As with prior embodiments, a potting compound 60 may be utilized to seal the semiconductor device 54 and wire bonds 58.

Figure 13 illustrates in cross sectional representation, an electronic package 110 with a semiconductor device 54 directly bonded to a printed circuit board 92. This technique is called flip chip bonding or controlled collapse chip connection (C4) and is more fully described in PCT International Publication W095/08188 entitled "Flip Chip in Metal Electronic Package", Published March 23, 1995.

The large number of small solder balls 70 that electrically interconnect the device 54 to circuit traces 112 on the printed circuit board 92 are particularly prone to fatigue failure and creep. The failure of even a single solder ball may render the entire device ineffective. By using a standoff 94 as described above, cyclic compression and expansion of the solder balls 70 is minimize reducing fatigue. X&Y direction C.T.E. induced stress is also reduced.

Figure 14 illustrates in cross sectional representation an electronic package 120 having a base component 122 that further reduces solder fatigue. The base 122 has a plurality of integral bumps 124 unitary with the base and formed by stamping, milling or chemical etching. Alternatively, the base 122 is formed by molding or sintering. The base 122 and the integral bumps are coated with an insulating layer 126 if formed from an electrically conductive material. No insulating layer is required if the base is formed from an electrically nonconductive material such as alumina or aluminum nitride.

Preferably, the base 122 is formed from an anodizable metal such as aluminum or an aluminum alloy and the insulating layer 126 is an anodic film having a thickness of from about 5 microns to about 50 microns and preferably from about 10 microns to about 25 microns.

The integral bumps have a peak 128 to valley 130 height of from about 0.4mm to about 0.8mm (0.015-0.030 inch) and preferably from about 0.5mm to about 0.65mm (0.020-0.025 inch).

The integral bumps 124 separate the electronic package 120 from the printed circuit board 92 and as a result, only a small diameter solder ball 70 is required to bond the package to the printed circuit board. The reduced volume of the solder balls reduces the amount of compression and expansion, minimizing fatigue failure and creep.

The circuit traces 66 electrically interconnect the semiconductor device 54 to the solder balls 70. To facilitate deposition of the circuit traces 66, the angle, β, between the plane of the wire bond shelf 102 and the integral bump 124 is either between 30° and 60° or between 120° and 150° depending on the direction of measurement. Preferably, the angle, β, is either between 40° and 50° or between 130° and 140°.

The peak 128 of the integral bumps 124 may be coated with a solderable material 132 to facilitate solder ball 70 attachment. Suitable solderable materials include gold, tin, and tin/lead alloy solders.

Figure 15 illustrates a cavity up electronic package 140 having a circuit 142 bonded to the

insulating layer 126 of a metallic base 122. The circuit 142 may be a single conductive layer formed on the insulating layer by any known metallization technique or may comprise one or more conductive layers 144 separated and bonded by one or more electrically insulating layers 146. Typically, the conductive layers are a copper or copper alloy foil and the intervening insulating layers 146 a polyimide. Circuit traces are photolithographically formed in the conductive layers. The semiconductor device 54 is electrically interconnected to the circuit traces by wire bonds 58.

A conductive via 148 is formed through the base 122. The walls of a through hole of a metallic base is made electrically nonconductive by coating with an insulating layer 150 such as an anodic film. The hole is then filled with a conductive material such as a solder, silver filled polymer or a copper terminal pin. Alternatively, the vias 148 are filled by vapor deposition when forming the conductive circuit traces 144. The conductive material interconnects the conductive layers 144 with circuit traces 66 extending to the peaks 128 of the integral bumps 124.

Figure 16 illustrates in cross sectional representation a cavity up ball grid electronic package 160 having a flip chip bonded semiconductor device 54. The package 160 has a base 122 that is preferably metallic. If the base 122 is electrically conductive, then an insulating layer 126 is provided. Circuit traces 162 are formed on a surface 164 of the base 122. Included with the circuit traces is a conductive array 166 that aligns

with an array of input/output pads on an electrically active face of the semiconductor device 54. Solder balls 70 electrically interconnect the conductive array 166 to the semiconductor device 54.

One or more conductive vias 148 electrically interconnect the circuit traces 162 with circuit traces 66 formed on the integral bumps 124 on the opposing side of the base.

Figure 17 shows in cross sectional representation a cavity down ball grid array electronic package 170. This package is free of conductive vias increasing the ease of manufacture and reliability.

A semiconductor device 54 is bonded to the package base 122 by a die attach material 56 that may be a low melting temperature solder or a polymer adhesive. Thermal greases and other highly thermally conductive materials such as silver or graphite filled adhesives are also desirable to maximize the conduction of heat from the device 54 to the base 122.

A circuit board 172 having either a C.T.E. close to that of the semiconductor device 54, that of the base 122 or intermediate thereof, is bonded to and electrically interconnected to the device 54 through solder balls 70. The circuit board 172 has a support layer 174, an interior array of circuit traces 176 aligning with input/output pads on the semiconductor device 54 and an exterior array of circuit traces 178 electrically interconnected to circuit traces on the surface of the package base 122.

When the semiconductor device is silicon, the support layer 174 can be alumina, FR-4 glass filled epoxy or other suitable material. The circuit traces are any suitable material such as copper on a moly-manganese metallization.

A cover 180, either a discrete cover adhesively bonded to the base 122, as illustrated, or a potting compound, encapsulates the device 54.

Figure 18 illustrates in cross sectional representation a unique application of the integrally bumped packages of the invention. The conductive bumps of a first package 190 may be bonded to and electrically interconnected to circuit traces 192 formed on a second package 194. Through the use of integral bumps 124 and circuit traces formed on an insulative layer 126, any number of electronic packages may be nested, greatly increasing the package density on a printed circuit board.

While the electronic packages of the invention have been described in terms of primarily metallic bases, the bases can also be formed from other suitable materials such as plastics, ceramics, metal/ceramic composites (cermets) and glass/ceramic composites (cerglasses).

It is apparent that there has been provided in accordance with this invention, a method for the manufacture of a leadframe and an electronic package having integral bumps that fully satisfies the objects, features and advantages set forth hereinbefore. While the invention has been described in combination with specific embodiments thereof, it is evident that many alternatives,

modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

IN THE CLAIMS:

1. A method for the manufacture of a leadframe (40), characterized by the steps of:

a) providing a metallic strip (10) having a thickness, "t" and opposing first (12) and second sides (16) that define a plane;

b) selectively removing portions of said metallic strip from said second side (16) to form a reduced thickness portion "R" with a thickness less than "t" and integral bumps (24) with a thickness of about "t" extending substantially perpendicularly outward from said plane;

c) selectively removing the remainder of portions of said reduced thickness portion "R" to form a plurality of leads (42), each said lead (42) having a reduced thickness portion "R" and an integral bump portion (24).

2. The method of claim 1 characterized in that a polymer resin (16) is deposited on the reduced thickness portion "R" from said second side (16).

3. The method of claim 1 characterized in that said first side (12) is bonded to a support substrate (52).

4. A method for the manufacture of a leadframe (40'), characterized by the steps of:

a) providing a metallic strip (10) having opposing first (12) and second sides (16);

b) mechanically deforming selected portions of said metallic strip (10) to from integral bumps (24) extending outward from said second side (16);

c) depositing a polymer support layer (26) on undeformed portions (59) of said second side (16) such that the combined thickness of said undeformed portion (59) and of said polymer support layer (26) is less than the height of said integral bump (24);

d) selectively removing portions of said undeformed portion (59) to form leads (42), each said lead (42) having an undeformed portion (59) and an integral bump (24).

5. The method of anyone of claims 1-4 characterized in that at least an outwardmost portion of said integral bump (24) is coated with a solderable material (34).

6. The method of anyone of claims 1-4 characterized in that at least a portion of the first side (12) is coated with a wire bondable material (38).

7. A component (62) for an electronic package (61, 100), characterized by:

a metallic substrate (62) having first (104) and second substantially planar opposing sides; and

an insulative layer (64) coating said metallic substrate (62), said insulative layer (64) containing a first portion with a plurality of pores and a second portion that is substantially pore free.

8. The metallic substrate (62) of claim 7 characterized in that said first portion is adapted to receive a polymer (60).

9. The metallic substrate (62) of claim 8 characterized in that said second portion is adapted to receive a metallization (66).

10. The metallic substrate (62) of claim 8 characterized in that said first portion includes a chip receiving cavity (68) having a depth "d" in said first side (104).

11. The metallic substrate (62) of claim 10 characterized in that a wire bonding shelf (102) is disposed on a wall (106) of said cavity (68) at a depth less than "d".

12. The metallic substrate (62) of claim 11 characterized in that said wall (106) between said wire bonding shelf (102) and said first side (104) forms an angle of from about 30° to about 60° or from about 120° to about 150°.

13. The metallic substrate (62) of claim 12 characterized in that circuit traces (66) interconnect said wire bonding shelf (102) and said first side (104).

14. The metallic substrate (62) of claim 13 characterized in that said circuit traces terminate at metallic pads adapted to receive a solder.

15. The metallic substrate (62) of claim 13 characterized in that said circuit traces (66) terminate at solder balls (70).

16. The metallic substrate (62) of claim 7 characterized in that a plurality of integral bumps (124) extend from a side of said substrate (62).

17. The metallic substrate (62) of claim 16 characterized in that a circuit trace (66) extends to an outward most portion (128) of at least a portion of said integral bumps (124).

18. The metallic substrate (62) of claim 17 characterized in that the outward most portion (128) of at least some of said integral bumps (124) is coated with a solderable material (132).

19. The metallic substrate (62) of claim 17 characterized in that conductive vias (148) extend from said first side of said substrate (62) to said second side of said substrate (62).

20. A ball grid array electronic package component (90), characterized by:

a substrate (62) having opposing first and second sides;

a metallized array (66) formed on said first surface;

solder balls (70) bonded to said metallized array; and

a standoff (94) integral with the perimeter of said first side, said standoff (94) having a height effective to minimize fatigue of said solder balls (70).

21. The component (90) of claim 20 characterized in that said standoff (94) has a yield strength greater than the yield strength of said solder balls (70).

22. The component (90' of claim 21 characterized in that said standoff (94) is a polymer adhesive bonded to both said substrate (62) and to an external printed circuit board (92).

23. An electronic package (80), chacterized by:

an aluminum or aluminum alloy base (62) having first and second opposing sides;

an anodization layer (64) coating at least a portion of said base (62);

a cavity formed in said first surface;

a semiconductor (54) device bonded to the base of said cavity;

a leadframe (82) bonded (84) to said base (62) and electrically interconnected to said semiconductor device (54); and

a potting compound (60) filling said cavity and encapsulating said semiconductor device (54) and the inner lead portion of said leadframe (82).

24. An electronic package (61), characterized by:

an aluminum or aluminum alloy base (62) having first and second opposing sides;

an anodization layer (64) coating at least a portion of said base (62);

a cavity (68) formed in said first surface;

a semiconductor device (54) bonded to the base of said cavity;

a metallized circuit trace (66) extending from said cavity to a peripheral portion of said base and electrically interconnected to said semiconductor device (54); and

a potting compound (60) filling said cavity and encapsulating said semiconductor device (54) and an inner portion of said circuit trace (66).

25. The electronic package (61) of claim 24 characterized in that portion of said anodization layer (64) underlying said potting compound (60) contains pores and that portion of said anodization layer (64) underlying said metallized circuit trace (66) is sealed.

AMENDED CLAIMS

[received by the International Bureau on 27 December 1995 (27.12.95); original claim 24 amended; new claims 26-31 added; remaining claims unchanged (2 pages)]

24. A component for a ball grid array electronic package (61) having improved thermal conductivity and reduced solder member creep, characterized by:

a base (62) selected from the group consisting of aluminum and aluminum alloys having first and second opposing sides;

an anodization layer (64) coating at least a portion of said base (62);

a cavity (68) formed in said first surface; and

a metallized circuit trace (66) on said anodization layer (64) extending from said cavity (68) to a peripheral portion of said first surface of said base (62), said metallized circuit trace (66) bonded to a solder member (70).

25. The electronic package (61) of claim 24 characterized in that portion of said anodization layer (64) underlying said potting compound (60) contains pores and that portion of said anodization layer (64) underlying said metallized circuit trace (66) is sealed.

26. The component of claim 24 characterized in that said anodization layer (64) contains a uniform dispersion of pores.

27. The component of claim (26) characterized in that said pores have an average diameter of from 50 angstroms to 500 angstroms.

28. The component of claim (26) characterized in that said solder member (70) is solder balls bonded to a peripheral portion of said metallized circuit trace (66).

29. The component of claim (26) characterized in that said solder member (70) is solder pads bonded to a peripheral portion of said metallized circuit trace (66).

30. The component of claim 26 characterized in that said metallized circuit trace (66) is directly on said anodization layer (64).

31. The component of any one of claims 24-30 characterized in that said component further includes a semiconductor device (54) bonded to the base of said cavity (68) and is electrically interconnected to said metallized circuit trace (66); and

a cover (60) encapsulating said semiconductor device (54) and an inner portion of said metallized circuit trace (66).

STATEMENT UNDER ARTICLE 19

In reference to the above-identified International patent application, this is a response to the PCT International Search Report mailed 31 October, 1995 having a statutory period for response set to expire on 31 December, 1995. Replacement pages 31/1 and 31/2 are enclosed to replace page 31 originally filed with this international application. As a result of this amendment, claim 24 has been amended and claims 26-31 have been added. Claims 1-23 and 25 are unchanged. No claims have been canceled.

JP-A-63-291,439 was cited as a category "Y" reference against claims 24 and 25. The reference appears to show a pin grid array package having an electrically non-conductive base. Applicant believes the base is electrically non-conductive because the terminal pins 6 extend through the base without an intervening insulating layer. An electrically conductive layer 4 is formed on a top surface of the non-conductive package substrate. An insulating layer 5 is formed over the conductive layer 4 and further extends around the package substrate and along the surfaces of the terminal pins 6. Applicants believe that this layer is necessary to provide electrical isolation between the terminal pins 6 and a second electrically conductive layer 17. Applicant's interpretation of the package is supported by the abstract to JP-63-291,439 that identifies reference numeral 4 as a "conductor circuit"; reference numeral 5 as an "insulating layer" and reference numeral 17 as a "metal layer".

There is nothing in JP-63-291,439 to teach or suggest a package base that is formed from aluminum or an aluminum alloy coated with an anodization layer and having metallized circuit traces formed on that anodization layer. Applicant's claim 24 and the claims dependent therefrom should be given an affirmative statement as to novelty, inventive step and industrial applicability.

Inclusion of this amendment and consideration of the claims as amended by the International Preliminary Examination Authority is respectfully requested. If the International Bureau requires additional information, it is invited to contact Applicant's attorney at the telephone number listed below.

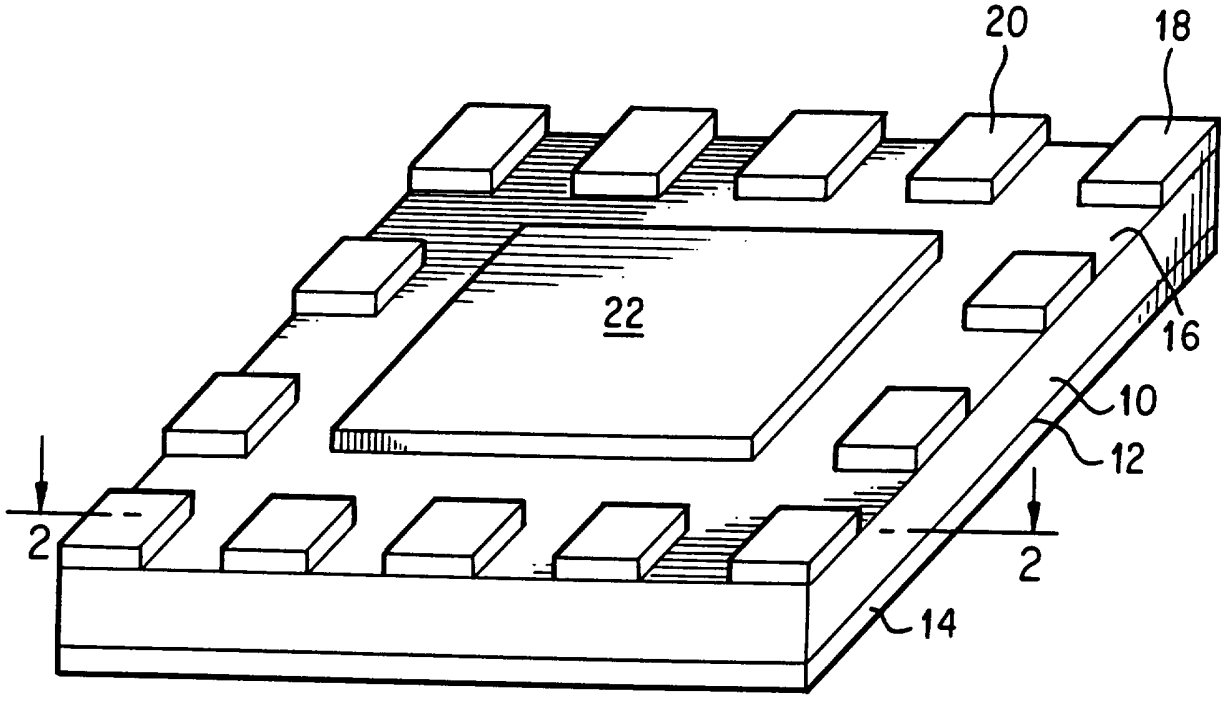


FIG. 1

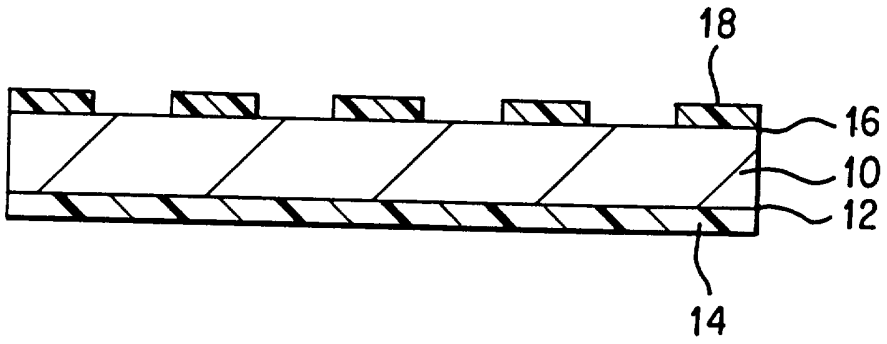


FIG. 2

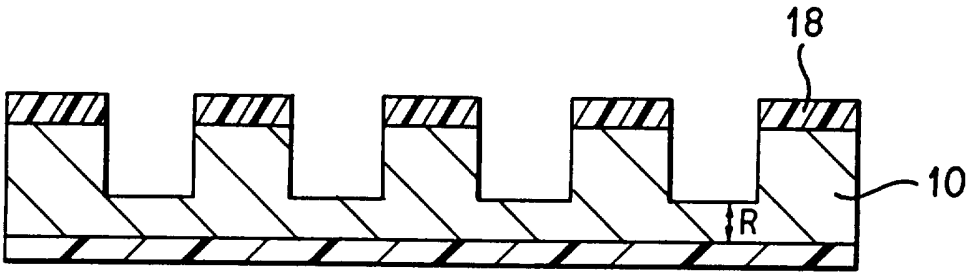


FIG. 3

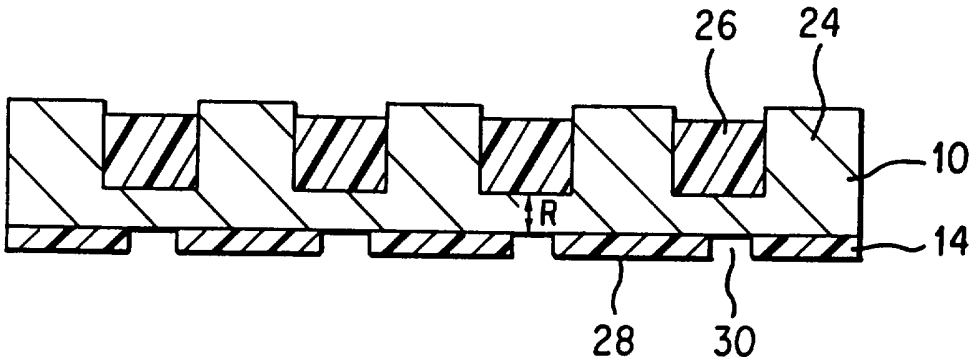


FIG. 4

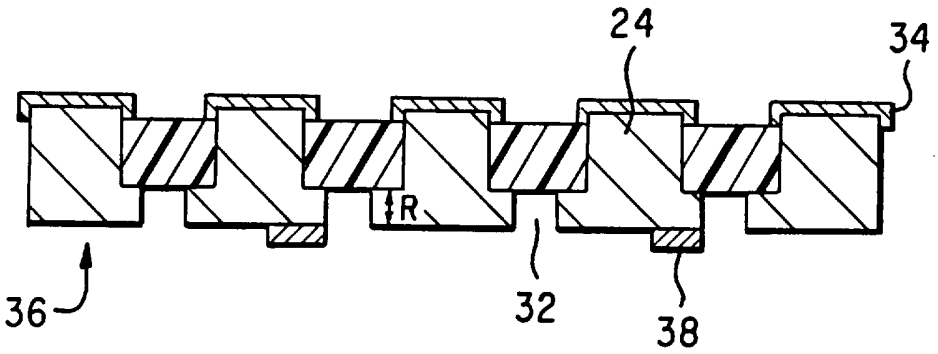


FIG. 5

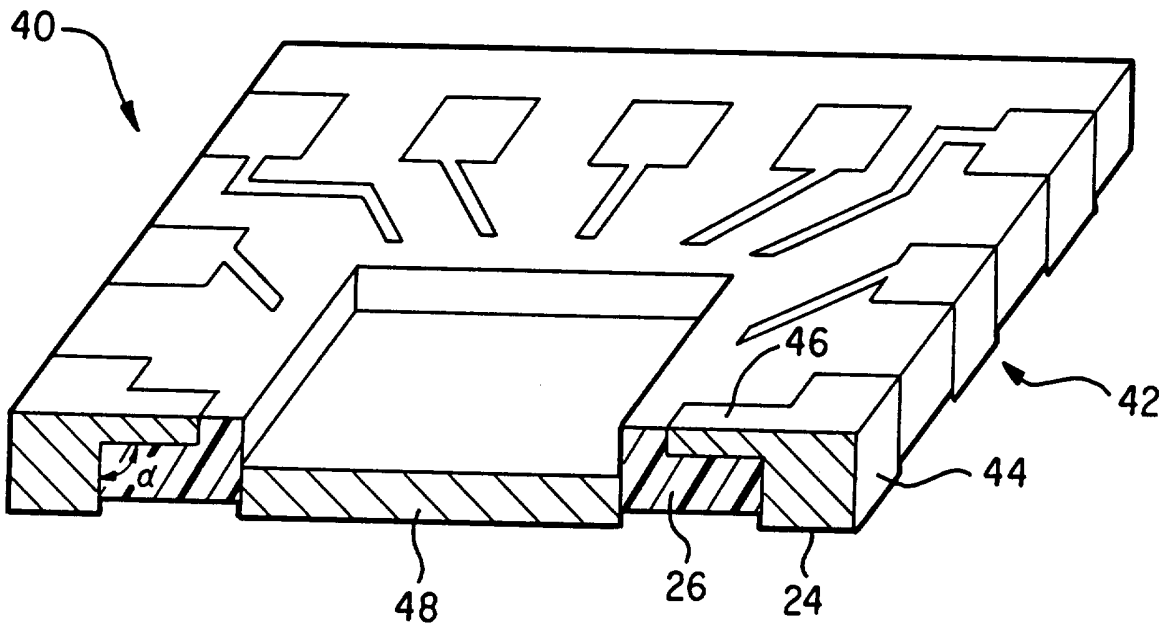


FIG. 6

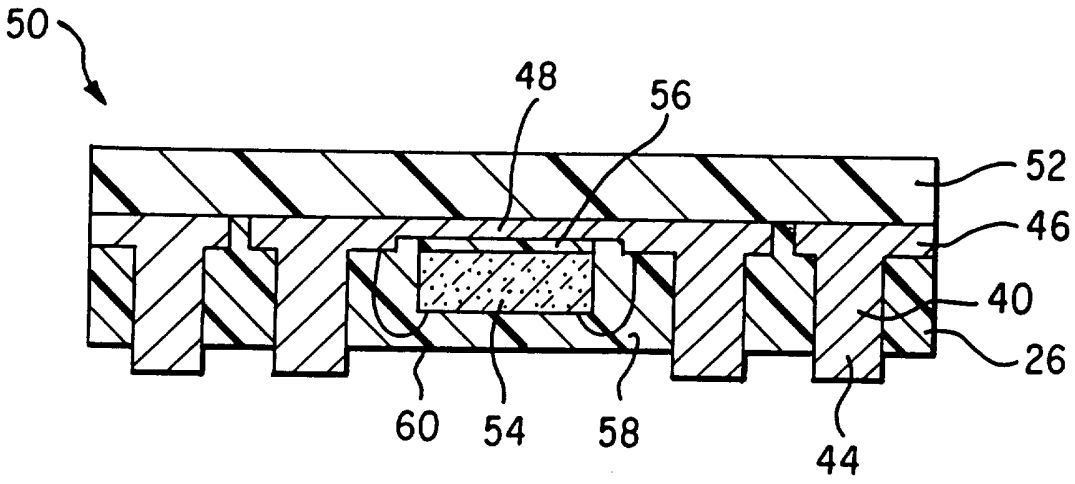


FIG. 7

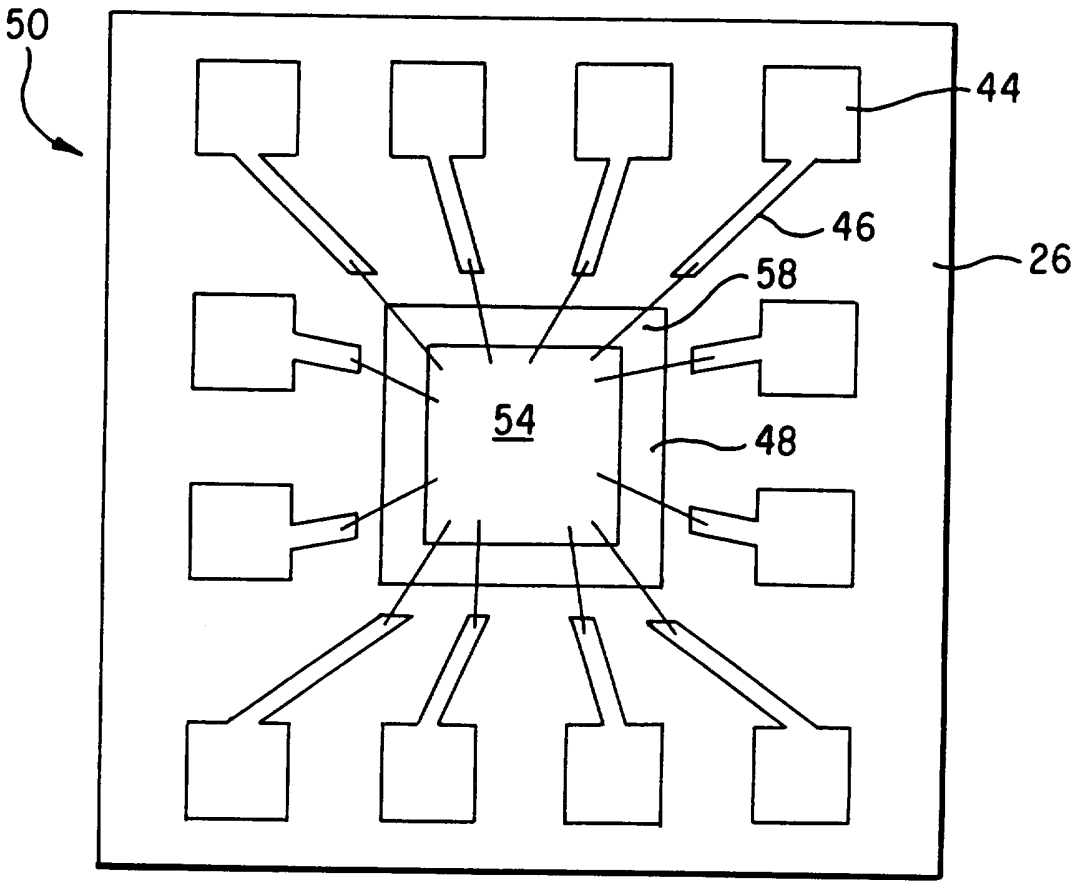


FIG. 8

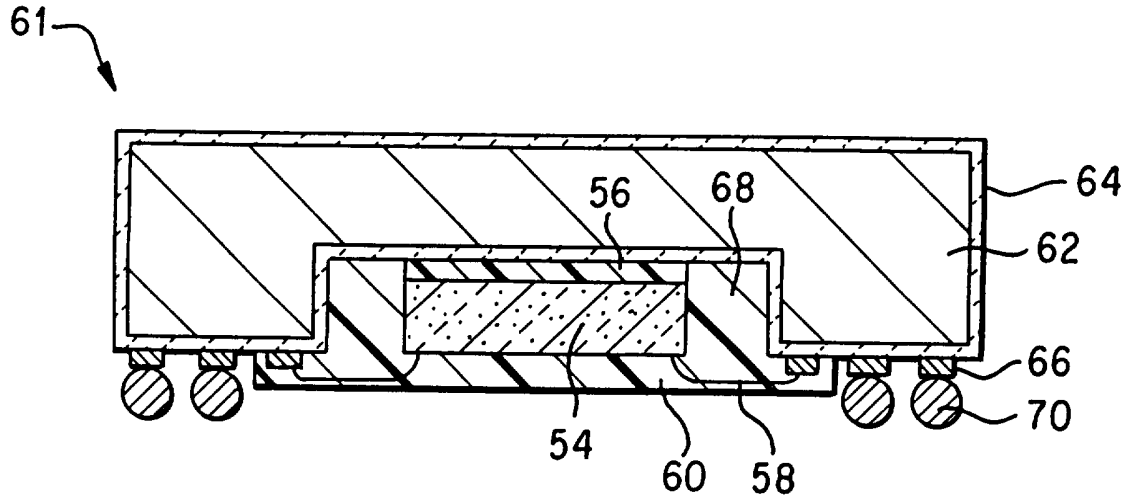


FIG. 9

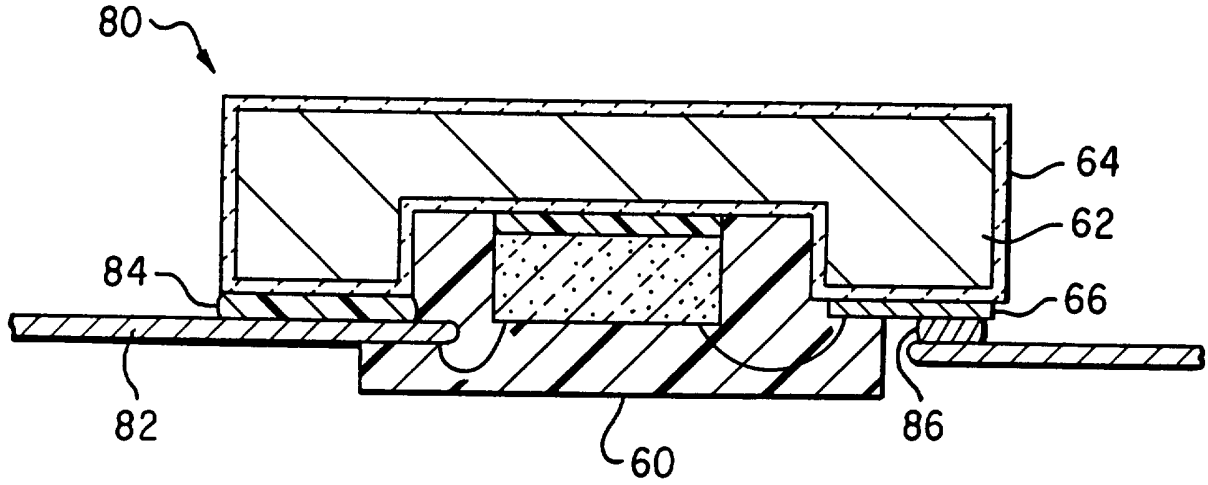


FIG. 10

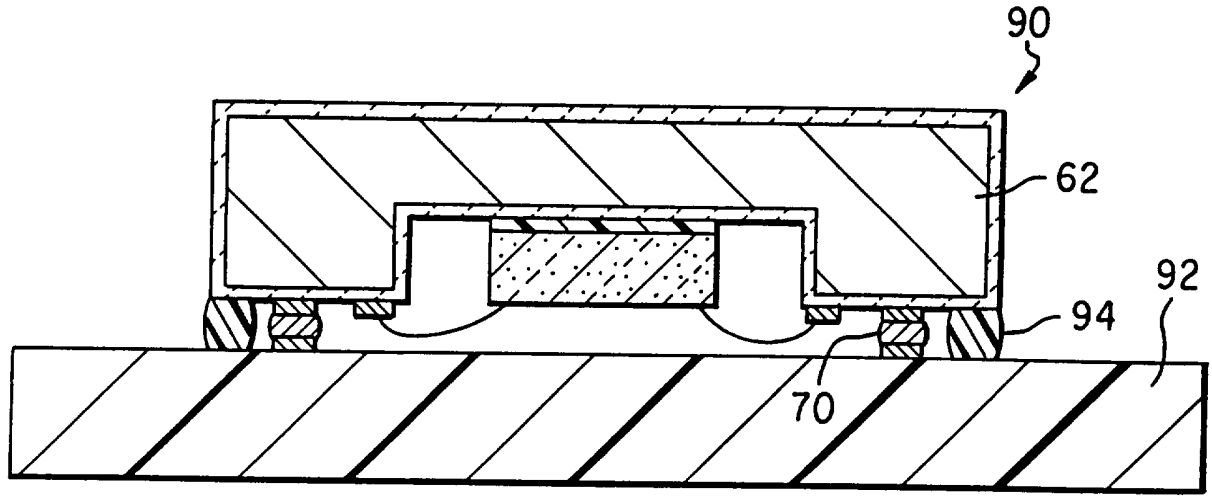


FIG. 11

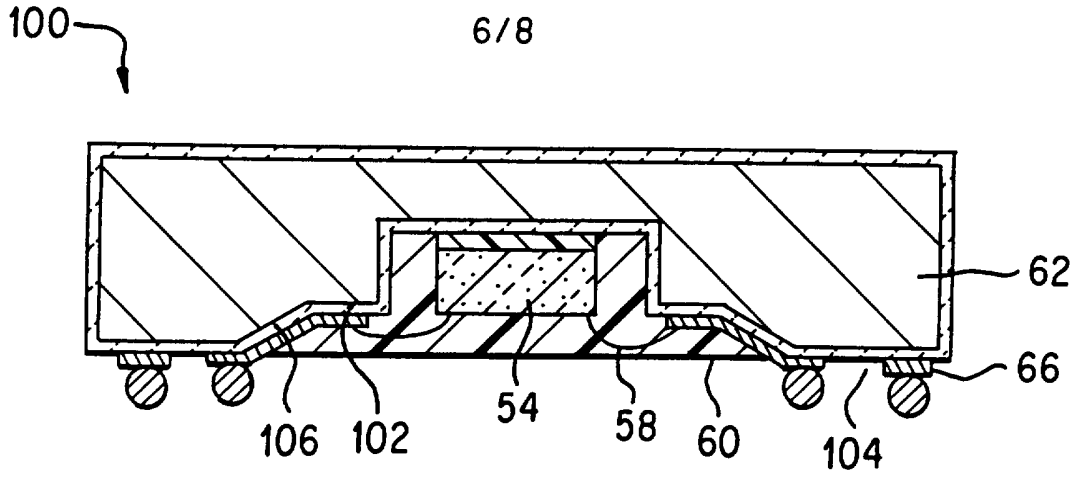


FIG. 12

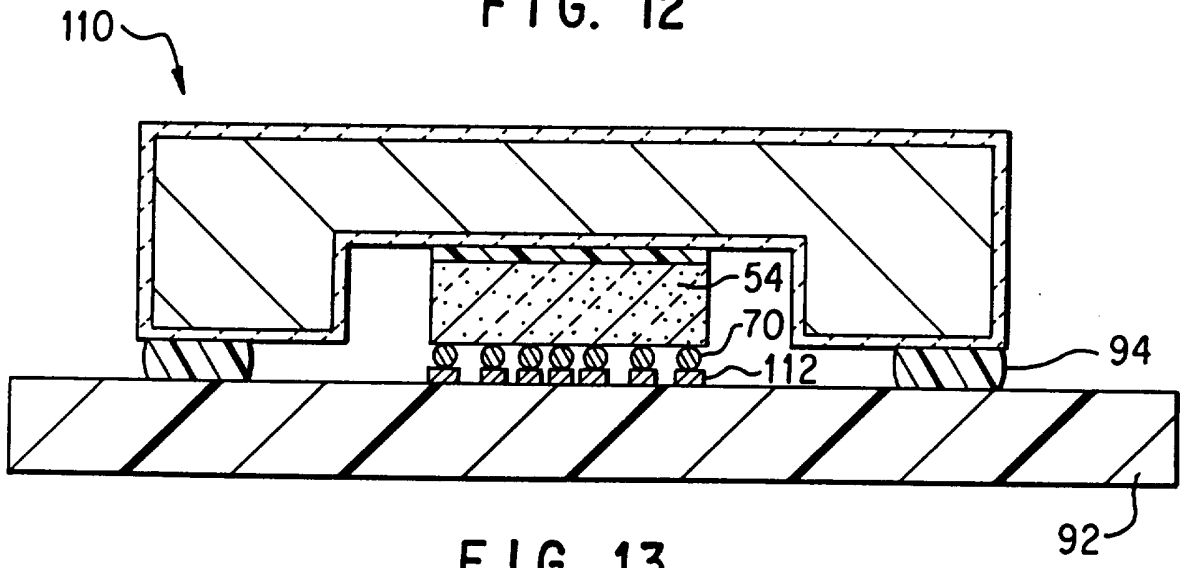


FIG. 13

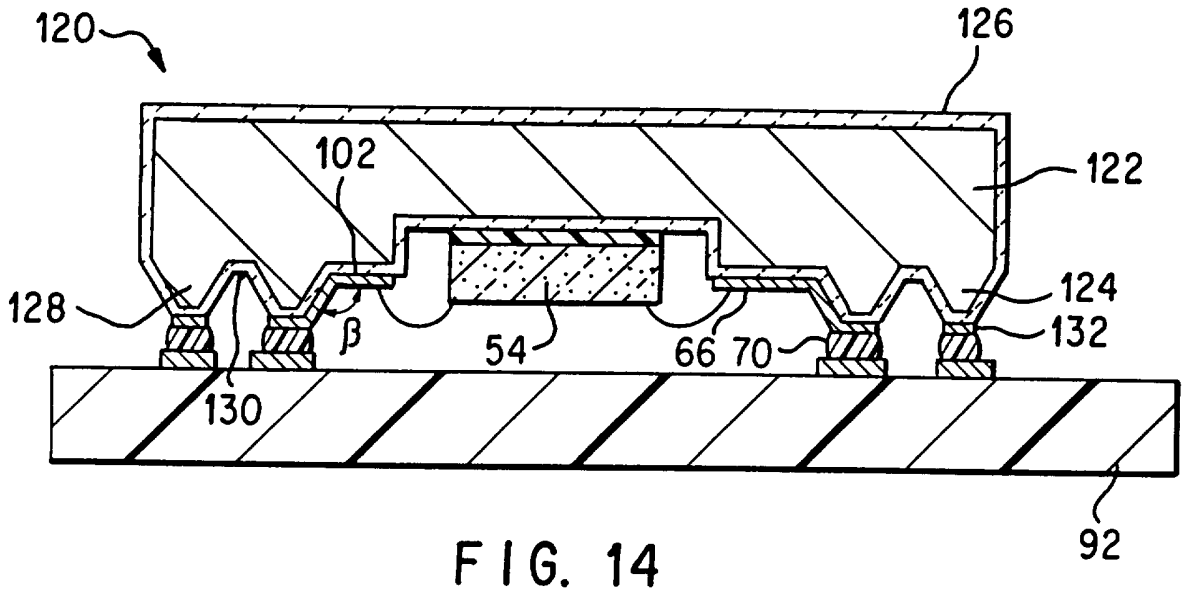


FIG. 14

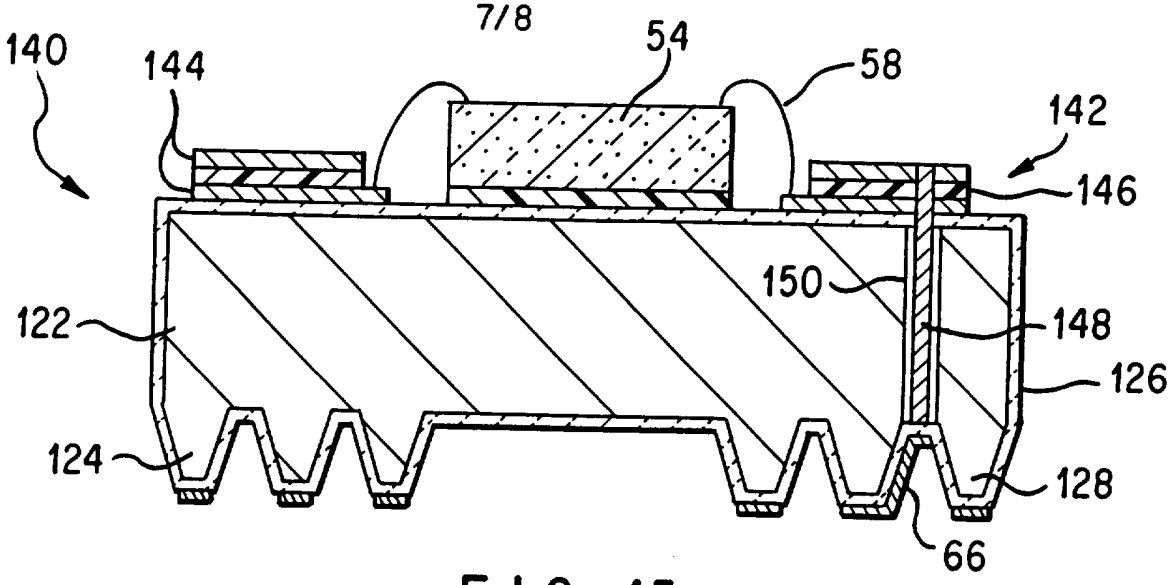


FIG. 15

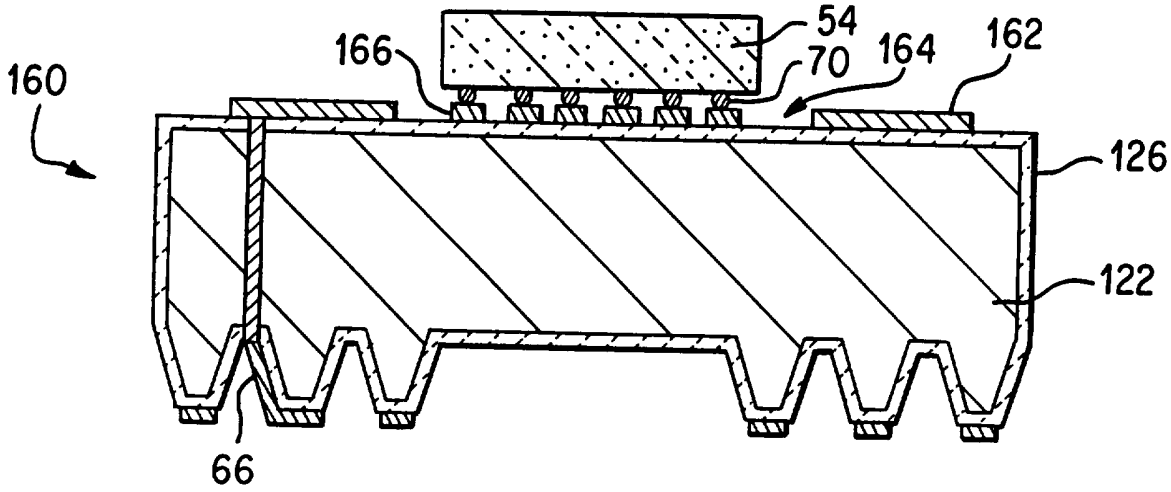


FIG. 16

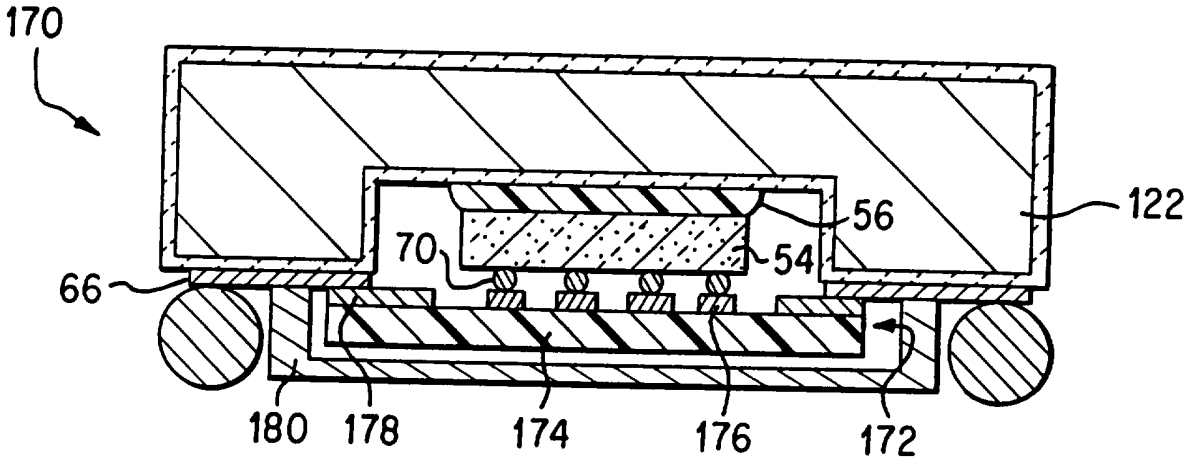


FIG. 17

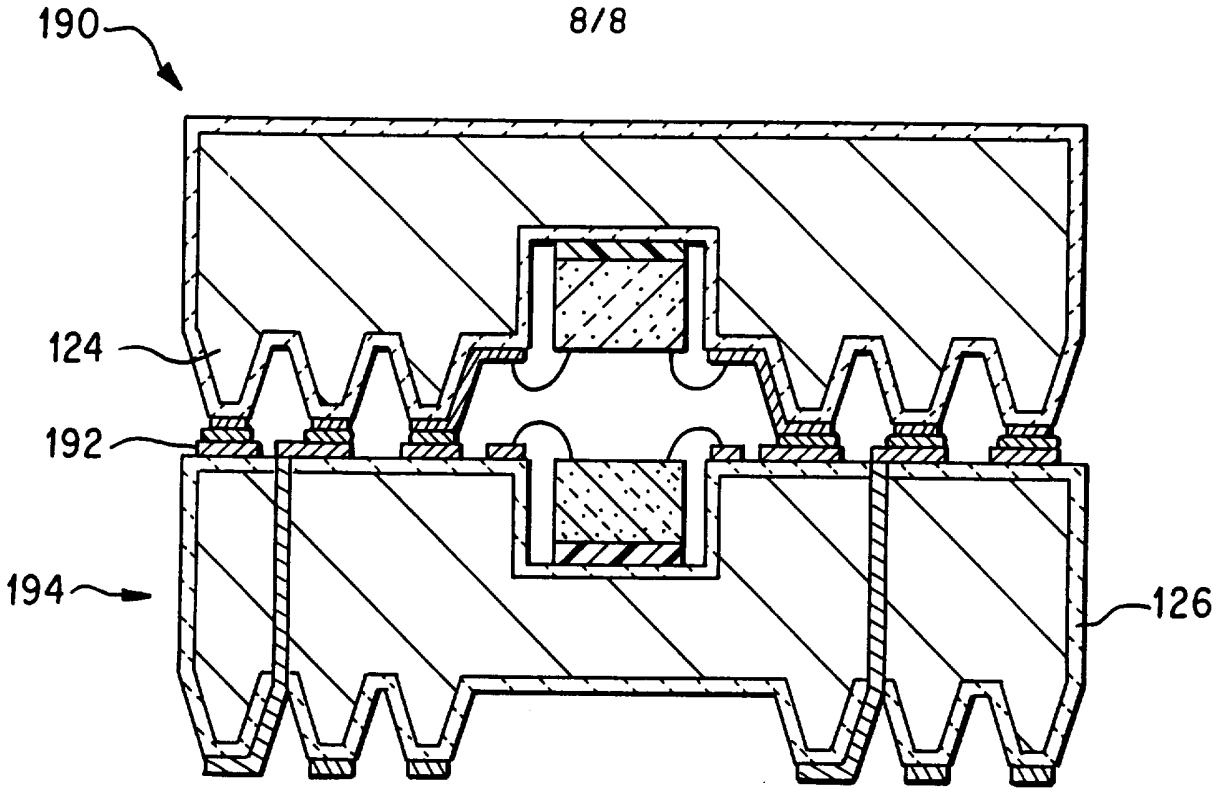


FIG. 18

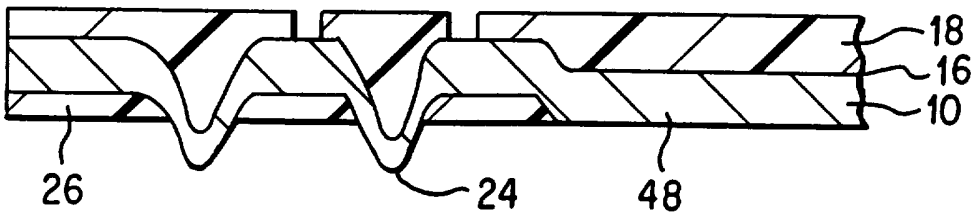


FIG. 19

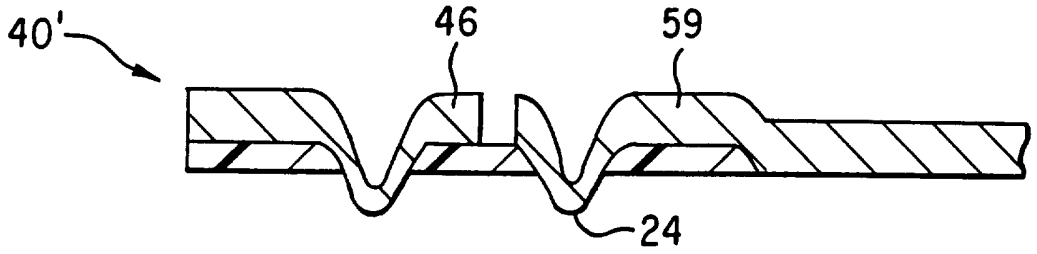


FIG. 20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/08305

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H05K 1/03, 1/05, 3/00, 3/44, 7/02; B05D 1/36,3/14

US CL :Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 29/830; 174/250, 256, 257, 260; 361/748, 761, 762, 764; 427/264, 287, 409, 410; 428/901

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS search terms: metal substrate, aluminum, anodized or anodised, anodized coating, porous insulating layer or porous insulating coating.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,677,526 (MUEHLING) 30 JUNE 1987, col. 6, lines 1-26	1-6
X	US,A, 4,633,035 (McMONAGLE) 30 DECEMBER 1986, col. 1, lines 47-59 and col. 2, lines 36-45.	7-9
Y	JP,A, 63-291439 (MATSUSHITA ELECTRIC WORKS LTD) 29 NOVEMBER 1988, See the Abstract.	7-11 and 16-25
Y	JP,A, 2-12933 (NEC CORPORATION) 17 JANUARY 1990, See entire Abstract.	12-15
Y	JP,A, 3-177055 (SUMITOMO ELECTRIC IND LTD) 01 AUGUST 1991, See entire Abstract.	12-15

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

23 SEPTEMBER 1995

Date of mailing of the international search report

31 OCT 1995

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Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/08305

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP,A, 1-238148 (FUJI ELECTRIC COMPANY LTD) 22 SEPTEMBER 1989, See Abstract.	20-22
X	US, 4,153,988 (Doo) 15 MAY 1979, See figures 2-12	1-4 and 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/08305

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

29/830; 174/250, 256, 257, 260; 361/748, 761, 762, 764; 427/264, 287, 409, 410; 428/901