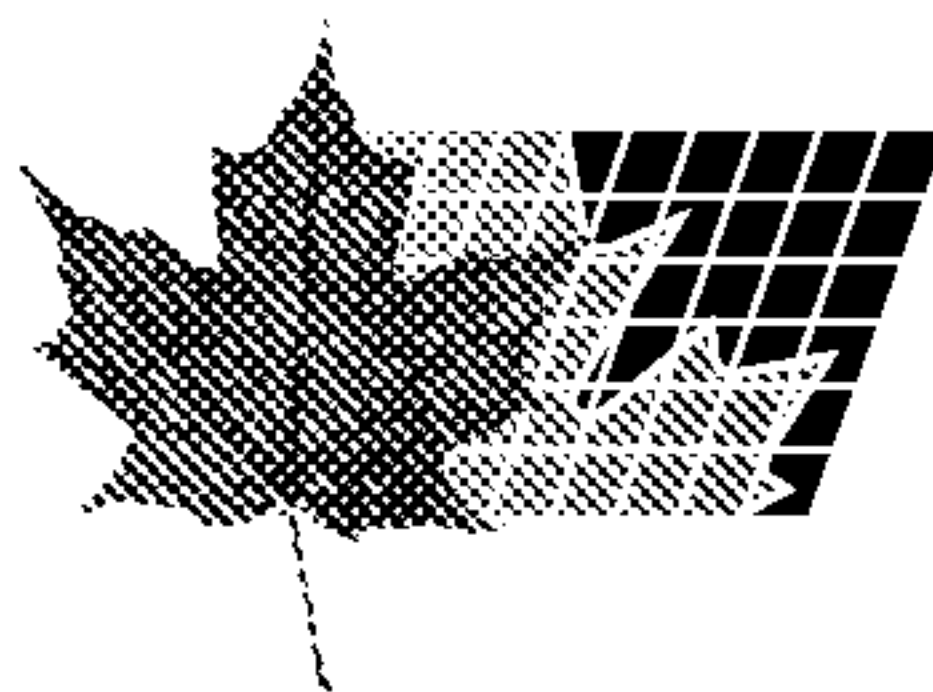




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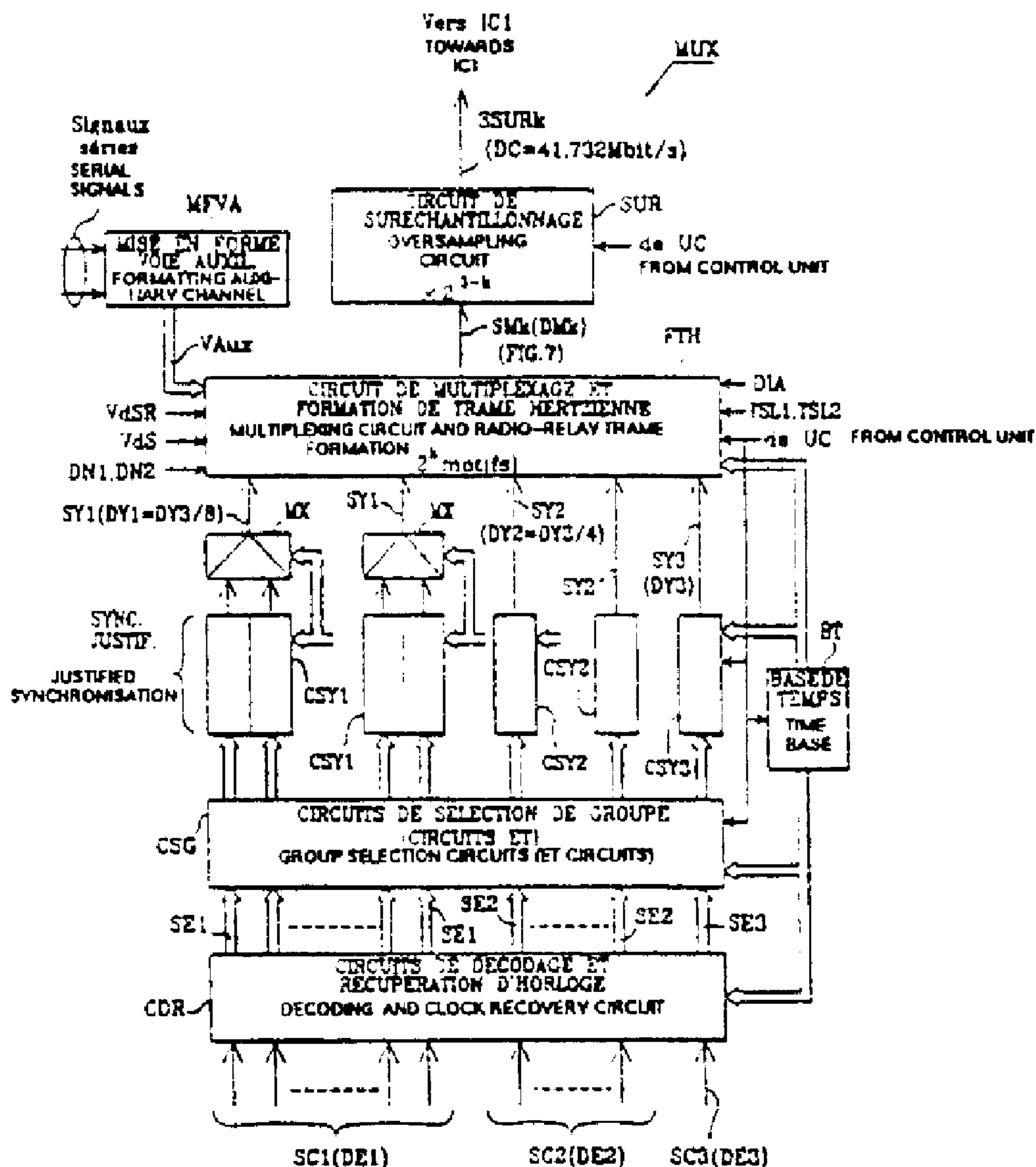
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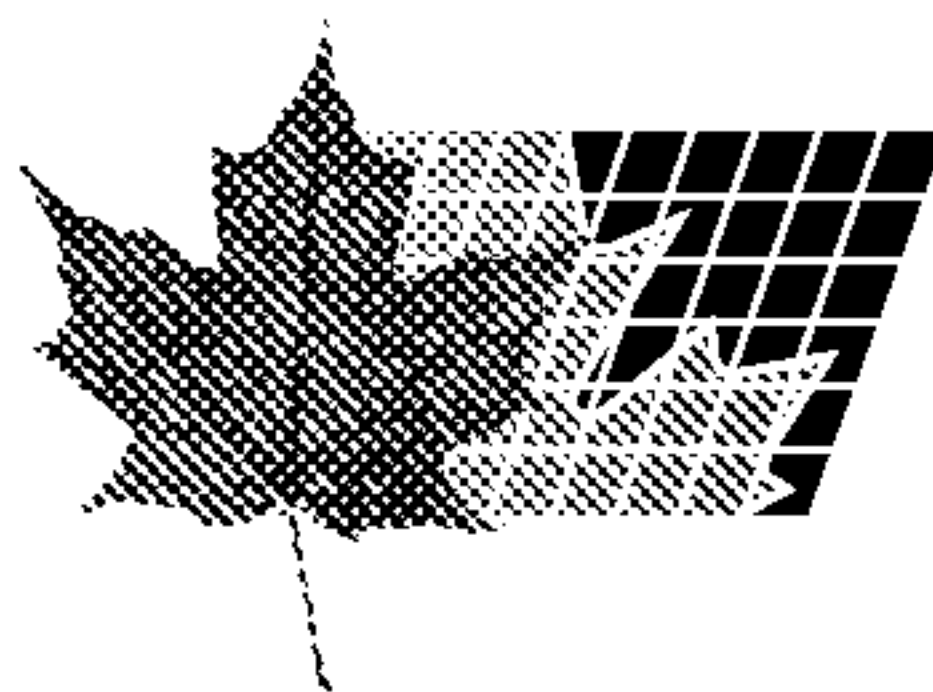
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(54) **TRAME NUMERIQUE POUR STATION HERTZIENNE**

(54) **DIGITAL FRAME FOR RADIO-RELAY STATION**





(57) Une station hertzienne est rendue compatible avec la transmission d'un groupe sélectionné quelconque parmi des groupes de signaux plésiochrones à multiplexer (SE1, SE2, SE3) ayant des débits sensiblement multiples entre eux, afin d'inclure dans la station des circuits programmables communs aux groupes, indépendamment du débit du signal multiplex résultant du multiplexage. Une trame de durée prédéterminée est formée en synchronisant les signaux plésiochrones dans le groupe sélectionné en des signaux synchrones (SY1, SY2, SY3) ayant des débits multiples entre eux, en attribuant à chaque signal synchrone un nombre de motifs de structure prédéterminée dans la trame égal à la partie entière du quotient de la division du débit du signal synchrone par le plus petit débit des signaux plésiochrones, et en insérant dans chaque motif des bits du signal synchronisé respectif en nombre prédéterminé et des bits supplémentaires (BS) en nombre prédéterminé.

(57) The invention concerns a radio-relay station made compatible with the transmission of any selected group among a group of plesiochronous signals with multiplexer (SE1, SE2, SE3) with substantially mutually multiple speeds, so as to include in the station programmable circuits common to the groups, independently of the multiplex signal speed resulting from the multiplexing. A frame of predetermined duration is formed by synchronising the plesiochronous signals in the selected group into synchronous signals (SY1, SY2, SY3) with mutually multiple speeds, by assigning to each synchronous signal a number of patterns of predetermined structure in the frame equal to the whole part of the quotient of the division of the synchronous signal by the smallest speed of the plesiochronous signal, and by inserting into each pattern bits of the respective synchronised signal in predetermined number and supplementary bits (BS) in predetermined number.

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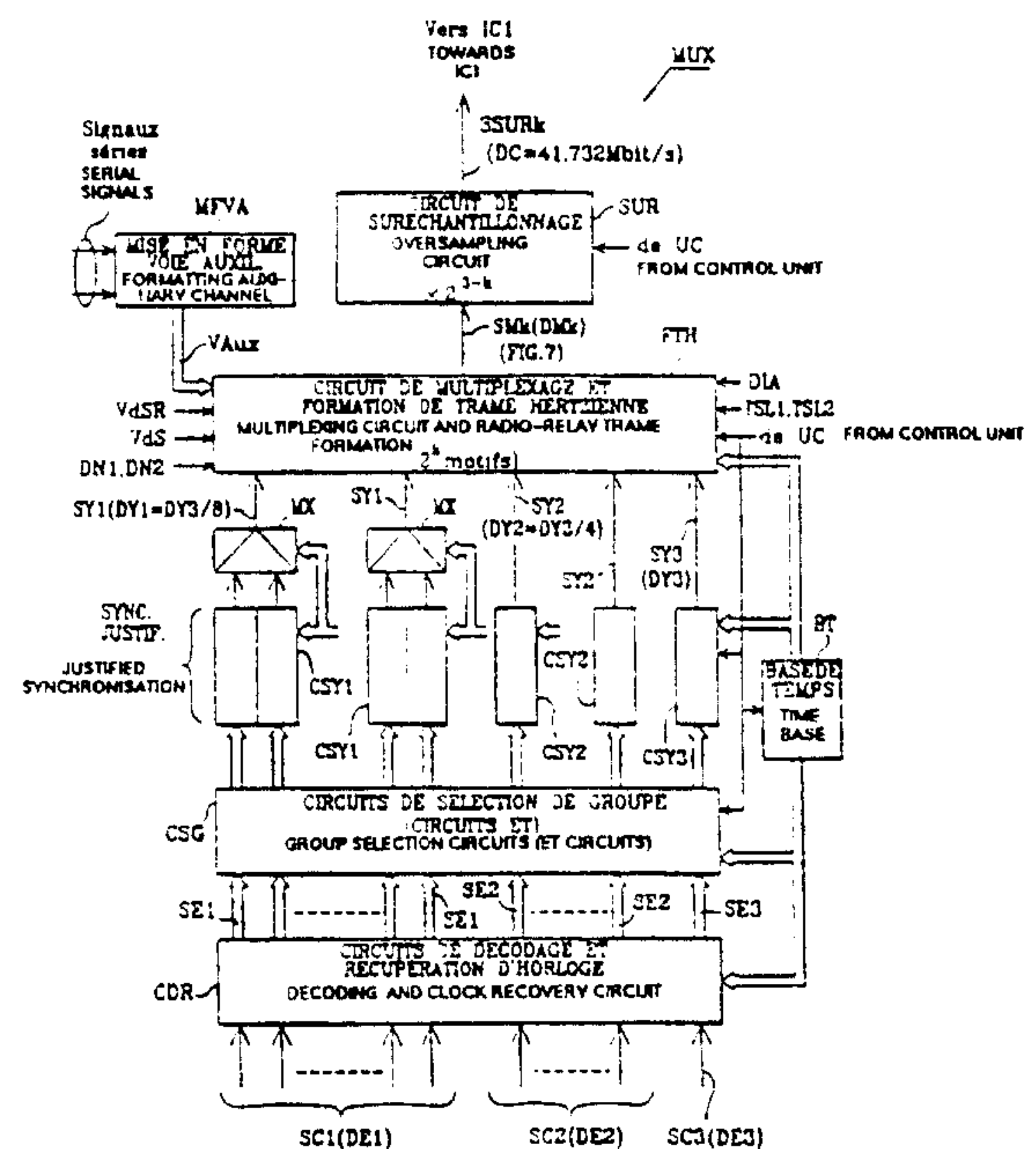
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(57) Abstract

The invention concerns a radio-relay station made compatible with the transmission of any selected group among a group of plesiochronous signals with multiplexer (SE1, SE2, SE3) with substantially mutually multiple speeds, so as to include in the station programmable circuits common to the groups, independently of the multiplex signal speed resulting from the multiplexing. A frame of predetermined duration is formed by synchronising the plesiochronous signals in the selected group into synchronous signals (SY1, SY2, SY3) with mutually multiple speeds, by assigning to each synchronous signal a number of patterns of predetermined structure in the frame equal to the whole part of the quotient of the division of the synchronous signal by the smallest speed of the plesiochronous signal, and by inserting into each pattern bits of the respective synchronised signal in predetermined number and supplementary bits (BS) in predetermined number.

(57) Abrégé

Une station hertzienne est rendue compatible avec la transmission d'un groupe sélectionné quelconque parmi des groupes de signaux plésiochrones à multiplexer (SE1, SE2, SE3) ayant des débits sensiblement multiples entre eux, afin d'inclure dans la station des circuits programmables communs aux groupes, indépendamment du débit du signal multiplex résultant du multiplexage. Une trame de durée prédéterminée est formée en synchronisant les signaux plésiochrones dans le groupe sélectionné en des signaux synchrones (SY1, SY2, SY3) ayant des débits multiples entre eux, en attribuant à chaque signal synchrone un nombre de motifs de structure prédéterminée dans la trame égal à la partie entière du quotient de la division du débit du signal synchrone par le plus petit débit des signaux plésiochrones, et en insérant dans chaque motif des bits du signal synchronisé respectif en nombre prédéterminé et des bits supplémentaires (BS) en nombre prédéterminé.



BACKGROUND OF THE INVENTION

The present invention concerns a digital frame having a predetermined duration resulting from the multiplexing of plesiochronous digital signals, and a method of forming such a frame.

The invention is used in particular in a radio station which comprises an essentially digital transceiver at the base of the station and a radio transceiver at the top of a building or a mast, for example, and connected by transmission cable to the first transceiver.

A group of plesiochronous digital signals having bit rates standardized at 2.048 Mbit/s or 8.448 Mbit/s, for example, is applied to the transceiver which multiplexes the signals into a particular frame. Each group of plesiochronous signals corresponds to a particular radio station.

However, radio beam users are increasingly confronted with the problem of optimizing their radio stations to adapt them to changing customer requirements. For a given radio beam, if the stations exchanging a multiplex signal at 2×2 Mbit/s must exchange a multiplex signal at 4×2 Mbit/s or 8 Mbit/s, for example, many circuits must be modified and changed in all the stations to adapt them to the characteristics of the new multiplex signal to be transmitted, in particular its bit rate and frame characteristics.

30

OBJECTS OF THE INVENTION

An object of the present invention is to reduce the

cost of a radio station by introducing into it circuits which can be selected and programmed according to the bit rates of plesiochronous signals to be multiplexed in any group selected from a plurality of groups of plesiochronous signals so that the radio station can be used regardless of the bit rates of the signals of the selected group. More particularly, another object of the invention is to provide a digital frame of predetermined duration which contributes to achieving the above object.

SUMMARY OF THE INVENTION

A digital frame having a predetermined duration resulting from the multiplexing of plesiochronous digital signals, is characterized in that it includes patterns having a common structure and a predetermined length which are independent of the bit rates of the plesiochronous digital signals to be multiplexed of a group selected from a plurality of groups of plesiochronous digital signals having bit rates which are substantially multiples of each other. The patterns includes a predetermined number of additional bits and a predetermined number of bits of respective synchronous signals having bit rates which are multiples of each other and result from synchronization of plesiochronous digital signals of the selected group. Each plesiochronous digital signal of the selected group is allocated a number of patterns in the frame equal to the integer part of the quotient on dividing the bit rate of said each plesiochronous digital signal of the selected group by the lowest bit rate of the plesiochronous digital signals.

As a general rule, the number of patterns of the frame is equal to the integer part of the quotient on dividing the sum of the bit rates of the plesiochronous

digital signals of the selected group by the lowest bit rate of the plesiochronous digital signals and is therefore relatively well suited to the requirements of the users.

5 The structure of the frame is modular and the structure of the patterns is constant regardless of the bit rates of the plesiochronous signals of the groups, enabling use of the same circuits in radio emitting and receiving means of a radio station, independently of the
10 bit rate of the multiplex signal including the frame and corresponding to the selected group. As will emerge in the subsequent description of preferred embodiments of the invention, these circuits are programmable only as a function of the bit rate of the multiplex signal. The
15 patterns of the frame have a constant individual transmission capacity.

 Several plesiochronous signals at the lowest bit rate are often addressed to the same terminal equipment. They can therefore be multiplexed into a synchronous
20 signal. In this case, said quotient is replaced by the quotient obtained on dividing the bit rate of said each plesiochronous digital signal of the selected group by the product of the lowest bit rate of the plesiochronous digital signals and a predetermined integer which is
25 equal to a submultiple of the integer part of the quotient on dividing the bit rate of plesiochronous signals just higher than said smallest bit rate by said smallest bit rate ; a synchronous signal corresponding to the selected group has the lowest bit rate resulting from
30 synchronization and multiplexing of a number of plesiochronous digital signals at the lowest bit rate equal to the predetermined integer ; a single pattern is allocated in the frame to said synchronous signal having the lowest bit rate.

35 In practice, the additional bits are divided

between an alignment word, a constant allocation field, a variable allocation field varying as a function of the bit rate of a multiplex signal including the frame corresponding to the selected group, and an error
5 correcting code field, said fields having respective predetermined lengths.

The constant allocation field includes frame synchronization bits and preferably bits for collecting error information and/or quality bits.

10 The variable allocation field can include bits of an auxiliary channel whose offered bit rate increases as the bit rate of the multiplex signal increases. The variable allocation field can include bits which are reserved for a predetermined number of telephone and/or
15 data transmission channels and whose number decreases as the bit rate of the selected multiplex signal increases. The variable allocation field can include bits allocated to a telephone service channel whose number decreases as the bit rate of the selected multiplex signal increases ;
20 the constant allocation field includes a bit indicating a call request on the telephone service channel.

The invention concerns too a method of forming a digital frame conforming above. It is characterized by the following steps : constituting groups of
25 plesiochronous digital signals from a plurality of given plesiochronous digital signals having bit rates which are substantially multiples of each other, the sums of the bit rates of the plesiochronous digital signals in the group being substantially multiples of each other,
30 selecting one of the plesiochronous digital signal groups, synchronizing the plesiochronous digital signals in the selected group to yield synchronous signals having bit rates which are multiples of each other, allocating each synchronous signal a number of patterns of
35 predetermined structure in the frame equal to the integer

part of the quotient on dividing the bit rate said each synchronous signal by the lowest bit of the plesiochronous digital signals, and forming a multiplex signal including said frame by inserting in each pattern a predetermined number of bits of the respective synchronized signal and a predetermined number of additional bits.

The synchronous signals are obtained by constituting a frame made up of a synchronization word, stuffing indication bits and bits of the corresponding plesiochronous digital signal to raise the bit rate to a submultiple of the highest synchronous signal bit rate.

In one variant, the signals at the lowest bit rate are synchronized and multiplexed in groups of two. In this case, said quotient is replaced by the quotient on dividing the bit rate of said each synchronous signal by the product of the lowest bit rate of the plesiochronous digital signals and a predetermined integer which is equal to a submultiple of the integer part of the quotient on dividing the bit rate of the plesiochronous signals just higher than said lowest bit rate by said lowest bit rate. The step of synchronizing plesiochronous digital signals to the lowest bit rate is replaced by a step of multiplexing and synchronizing the plesiochronous digital signals at the lowest bit rate into synchronous signals in numbers of equal to said quotient on dividing the bit rate of said each synchronous signals by said product when said selected group includes plesiochronous digital signals at the lowest bit rate in a number at least equal to said quotient.

According to one advantageous aspect of the invention, a radio station transceiver is modular and programmable in order to reduce its manufacturing cost. More particularly, the method includes the steps of:

- providing a plurality of modular synchronizing

means for synchronizing the plesiochronous digital signals, and

5 - operating a number of synchronization means equal to the number of plesiochronous digital signals of the selected group and programmed in accordance with the bit rates thereof.

10 If the resulting signal must be transmitted through a transmission medium with a predetermined bit rate, such as transmission cables between transceivers of a radio station, the bit rate of the multiplex signal is at most equal to the constant bit rate on a transmission medium, and the multiplex signal is oversampled with an oversampling ratio between the bit rate of the transmission medium and the bit rate of the multiplex
15 signal to transmit an oversampled resultant signal at said constant bit rate on the transmission medium regardless of the bit rate of the multiplex signal and therefore regardless of the bit rates of the plesiochronous digital signals of the selected group.

20 In a radio station where the transmission medium such as a cable connects a transceiver at the base of a radio station and a radio transceiver of the radio station, the method comprises in the radio transceiver a step of undersampling the oversampled resultant signal
25 with the reciprocal of the oversampling ratio and a step of selecting filters as a function of the oversampling ratio. The bandwidths of the selected filters increase as the bit rate of the multiplex signal increases.

30 According to another aspect of the method of the invention, inserting additional bits into the frame includes inserting a frame alignment word, a constant allocation field, a variable allocation field which varies as a function of the bit rate of the multiplex signal and an error correcting code field, said fields
35 having respective predetermined lengths.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become more clearly apparent in the light of the following description of several preferred embodiments of the invention, which is given with reference to the corresponding accompanying drawings, in which:

- FIG. 1 is a block diagram of a radio station emitting a frame according to the invention ;

- FIG. 2 is a block diagram of a multiplexing device which is included in a transceiver of the radio station specifically for implementing the frame forming method of the invention ;

- FIG. 3 is a signal diagram showing the formation of synchronization frames for two plesiochronous digital signals at the same nominal bit rate and the formation of a modular frame according to the invention in the multiplexing device ;

- FIGS. 4 to 6 show respectively three synchronization frames for synchronous signals at different bit rates produced in the multiplexing device ;

- FIG. 7 shows a modular frame according to the invention produced by the multiplexing device ;

- FIGS. 8 to 10 show the composition of respective variable allocation fields for different modes of operation of the multiplexing device ; and

- FIG. 11 shows a frame structure of an auxiliary channel in a maximum bit rate multiplex signal.

Referring to FIG. 1, a radio link station essentially includes a station transceiver ETR which is generally installed inside a building and a radio transceiver ERA located either on the roof of the

building or on a mast near the building. The transceivers are connected by a bidirectional transmission coaxial cable CA which can be up to several hundred meters long.

5 The first transceiver ETR time-division multiplexes component plesiochronous digital signals SC1, SC2, SC3, which for example have been routed through the switched network, into a resulting signal having a "modular" frame according to the invention to be transmitted on the cable CA with a constant bit rate DC. The second transceiver
10 ERA generates a microwave signal at a frequency of a few gigahertz modulated by the resulting signal from the transceiver ETR in order to emit it via an antenna AN. The transceivers ETR and ERA also receive a radio frequency signal containing a modular frame according to
15 the invention and demultiplex it into plesiochronous digital signals.

 In the embodiment of the invention shown in FIG. 1 the first transceiver ETR essentially comprises a digital multiplexing device MUX and a digital demultiplexing
20 device DMUX, an interface IC1 with the cable CA and a microprocessor-based control unit UC with a keypad. The second transceiver ERA essentially comprises an interface IC2, a modulation and radio emission circuit CEM, an undersampling circuit SOE between the output of the
25 interface IC2 and a programmable digital emit filter FIE preceding the circuit CEM, a radio reception circuit CRE, a duplexer DU between the circuits CEM and CRE and an antenna AN, an oversampling circuit SUE between a demodulation and digital filtering circuit FIR following
30 on from the circuit CRE and the interface IC2, and a microcontroller MC. As will become clear in the course of the remainder of the description, the modifications introduced by the invention are essentially concentrated in the digital multiplexing and demultiplexing devices
35 MUX and DMUX and, to a lesser degree, in the circuits

SOE-CEM and CRE-SUE of the transceiver ERA.

The remainder of the description covers in detail the constitution of a digital frame in the multiplexer MUX according to the invention as a function of numerical values for the bit rate, duration, frequency and length expressed as numbers of bits, and given herein by way of example.

The multiplexing device MUX in the transceiver ETR at the base of the radio link station can receive component plesiochronous digital signals SC1, SC2, SC3 having standardized bit rates $DE1 = 2.048$ Mbit/s, $DE2 = 8.448$ Mbit/s and $DE3 = 34.368$ Mbit/s, i.e. having bit rates which are substantially integer multiples of each other, since $DE3 \approx 4.DE2$ and $DE2 \approx 4.DE1$. The bit rate DC on the cable CA is constant and equal to 41.732 Mbit/s, which imposes as see below a sum of the bit rates of the plesiochronous signals to be multiplexed together incoming the transceiver ETR not greater than the incoming maximum bit rate $DE3 = 34.368$ Mbit/s.

The frame structure according to the invention transmitted on the cable CA is common to four modes of operation M0 to M3 which respectively correspond to numbers of plesiochronous signals at the lowest bit rate of 2.048 Mbit/s equal to the first four powers of 2. Table 1 below shows the groups of plesiochronous signals corresponding respectively to these operating modes:

30

TABLE 1

MODE		GROUPS
M3	2x2 Mbit/s	2 x 2.048 Mbit/s
M2	4x2 Mbit/s	4 x 2.048 Mbit/s 8.448 Mbit/s

M1	8x2 Mbit/s	$8 \times 2.048 \text{ Mbit/s}$ $4 \times 2.048 + 8.448 \text{ Mbit/s}$ $2 \times 8.448 \text{ Mbit/s}$
M0	16 x 2 Mbit/s	$16 \times 2.048 \text{ Mbit/s}$ $12 \times 2.048 \text{ Mbit/s} + 8.448 \text{ Mbit/s}$ $8 \times 2.048 \text{ Mbit/s} + 2 \times 8.448 \text{ Mbit/s}$ $4 \times 2.048 \text{ Mbit/s} + 3 \times 8.448 \text{ Mbit/s}$ $4 \times 8 \text{ Mbit/s}$ 34.368 Mbit/s

Thus at least two multiplexed signals SC1 at 2.048 Mbit/s or one signal SC2 at 8.448 Mbit/s or one signal SC3 at 34.368 Mbit/s are transmitted and at most sixteen signals SC1 at 2.048 Mbit/s or four signals SC2 at 8.448 Mbit/s are multiplexed and transmitted. The multiplexing device therefore has at most sixteen inputs for signals SC1, four inputs for signals SC2 and one input for a signal SC3.

In a variant of table 1, instead of the lowest bit rate of the plesiochronous signals being equal to 2.048 Mbit/s, it can be equal to 4.096 Mbit/s.

More generally, the sums of the bit rates of the plesiochronous signals of the groups, i.e. the products of respective integers and the lowest bit rate of the plesiochronous signals defining the modes of operation, are multiples of each other.

As shown in FIG. 2, the digital multiplexing device MUX essentially includes decoding and clock recovering circuits CDR, a group selecting circuit CSG, synchronization circuits CSY, a multiplexing and radio frame forming circuit FTH and an oversampling circuit SUR.

The decoding and clock recovering circuits CDR

convert the plesiochronous signals SC1, SC2, SC3 in the line code respectively into incoming plesiochronous binary signals SE1, SE2, SE3 and recover clock signals corresponding to the bit rates of those signals. The line
 5 code is a bipolar code such as the HDB3 code, for example. The recovered clock signals correspond to the actual bit rates of the plesiochronous signals and vary within specific limits on either side of the nominal bit rates DE1 = 2.048 Mbit/s, DE2 = 8.448 Mbit/s and DE3 =
 10 34.368 Mbit/s because the original clocks of the plesiochronous signals are independent.

The multiplexing device MUX therefore includes $16 + 4 + 1 = 21$ decoding and clock recovering circuits to which there respectively correspond 21 synchronization
 15 circuits.

The group selecting circuit CSG comprises as many AND circuits as there are circuits CDR or CSY for selecting a group of incoming plesiochronous digital signals SE1, SE2, SE3 from the groups defined in table 1.
 20 Group selection is controlled by the control unit UC as a function of characteristics of the selected group and the selected mode Mk entered at the keyboard, where k is an integer in the range from 0 to 3. The incoming plesiochronous signals of the selected group are applied
 25 with the corresponding clock signals only to the corresponding synchronization circuits via the circuit CSG.

In the synchronization circuits SSY, the incoming plesiochronous signals SE1, SE2, SE3 are synchronized to
 30 form synchronized signals SY1, SY2, SY3 with respective bit rates DY1, DY2, DY3 significantly higher than the nominal bit rates DE1, DE2, DE3.

All the synchronization circuits CSY1, CSY2 and CSY3 have an identical structure and their operation
 35 differs only in how the frequency dividers are programmed

by the control unit UC in order to adapt clock signals in each circuit to the nominal bit rate DE1, DE2, DE3 of the respective incoming plesiochronous signal SC1, SC2, SC3. Consequently, the synchronization circuits are
 5 interchangeable and the number in operation depends on what is required at the time, i.e. on the number of incoming plesiochronous signals. In practice, a synchronization circuit CSY1, CSY2, CSY3 constitutes a module with a decoding and clock recovering circuit CDR
 10 and an AND circuit of the group selector circuit CSG. This modular nature of the multiplexer MUX makes a significant contribution to reducing the cost of manufacture of the first transceiver ETR.

The incoming plesiochronous signals are
 15 synchronized by positive stuffing and phase comparison with appropriate clock signals produced by a common time base BT.

As shown in FIG. 3, the bit rate DY1, DY2, DY3 of the synchronous signal SY1, SY2, SY3 produced in the
 20 corresponding synchronization circuit CSY1, CSY2, CSY3 depends on the one hand on systematic insertion of predetermined numbers of bits of a synchronization word MS and stuffing indication bits IJ in each frame of the synchronous signal and on the other on insertion of
 25 positive stuffing bits BJ in order to make up the difference between the higher constant bit rate of the synchronous signal and the bit rate of each incoming signal. In FIG. 3, it is assumed that two plesiochronous signals SEa and SEb at the same nominal bit rate DE are
 30 to be synchronized as two synchronous signals SYa and SYb of bit rate DY, whose frames can be phase-shifted relative to each other, and then multiplexed by patterns MTa, MTb into a modular frame according to the invention, as described below. Each synchronous signal frame is
 35 divided into a plurality of sectors, generally 3 to 6

sectors having a predetermined length. Hereinafter, frame and sector or word lengths are expressed in bit.

Each sector has a header including the synchronization word MS and a stuffing indication bit IJ
 5 for the single plesiochronous signal, or two or more stuffing indication bits corresponding to plesiochronous signals at the same bit rate multiplexed bit by bit, such as two signals SE1 in the FIG. 2 embodiment. The first sector of the frame includes, after the header, a
 10 stuffing bit BJ associated with the respective incoming plesiochronous signal. The other bits in each sector are payload bits of the incoming plesiochronous signal.

In the embodiment shown in FIG. 2, a synchronized
 15 signal SY1 at bit rate $DY1 = 4.347 \text{ Mbit/s}$ results from synchronizing two incoming plesiochronous signals at the nominal bit rate $DE1 = 2.048 \text{ Mbit/s}$ via two synchronization circuits CSY1 and a multiplexer MX, a synchronous signal SY2 at the bit rate of $DY2 =$
 20 8.694 Mbit/s results from the synchronization of a single incoming plesiochronous signal at the nominal bit rate $DE2 = 8.448 \text{ Mbit/s}$ via a synchronization circuit CSY2, and a synchronous signal SY3 at the bit rate of $DY3 =$
 25 34.777 Mbit/s results from the synchronization of a single incoming plesiochronous signal at the nominal bit rate $DE3 = 34.368 \text{ Mbit/s}$ via a synchronization circuit CSY3. The synchronous signals SY1, SY2 and SY3 which respectively correspond to the operating modes M0, M1 and M3 have bit rates which are submultiples of the highest
 30 synchronous signal bit rate $DY3$, since $DY1 = DY3/8$ and $DY2 = DY3/4$, the bit rate of a synchronous signal corresponding to mode M1, i.e. a bit rate of $2.DY2 = 4DY1 = DY3/2$, being deduced by multiplexing two synchronous signals SY2 or four synchronous signals SY1, for example.
 35 The bit rates of the synchronous signals, which are

different from each other but integer submultiples of each other, enable to form frame patterns having a structure established in the circuit FTH, as described below, and common to all the multiplexed signals SM0 to SM3 resulting from multiplexing of type $M \times 2.048$ Mbit/s, or $P \times 8.448$ Mbit/s, or $M \times 2.048 + P \times 8.448$ Mbit/s, where M and P are integers not greater than 16 and 4. In particular, the multiplex signals SM1, SM2 and SM3 are the result of multiplexing signals belonging to groups of type $4(2^{k-1}-P)DE1 + P.DE2$, where P is an integer in the range from 0 to $2^{k-1} \leq 4$ for $k = 1, 2$ or 3.

FIGS. 4 to 6 show respective synchronization frames TSY1, TSY2 and TSY3 for the synchronous signals SY1, SY2 and SY3 respectively.

Referring to FIG. 4, two incoming plesiochronous signals SE1 at $DE1 = 2.048$ Mbit/s are synchronized by positive stuffing using two stuffing bits BJ in the first sector of the corresponding frame TSY1 in two synchronization circuits CSY1 and multiplexed bit by bit in a multiplexer MX. The characteristics of the frame TSY1 with three sectors are indicated in table 2 below.

TABLE 2

Characteristics	Synchronization in MX and CSY1
Bit rate : $2 \times SE1$ (Mbit/s)	$DE1 = 2.048$
Frame bit rate (Mbit/s)	$DY1 = 4.347$
Frame length (bits)	324
Frame frequency (kHz)	13.417
Number of sectors	3
Composition of sectors:	
- bits $2 \times SE1$	102
- additional bits	6
Allocation of frame bits	

- two signals SE1	2 x 153
- synchronization word SW	9
- stuffing indication IJ	2 x 3
- free bits FB	3
Stuffing for SE1:	
- stuffing bit BJ	1
- minimum rate	0.3484
- nominal rate	0.3591
- maximum rate	0.3697

5 A synchronization circuit CSY2 processes an incoming plesiochronous signal SE2 at 8.448 Mbit/s by positive stuffing and produces a synchronized signal SY2 having a frame TSY2 shown in FIG. 5. The characteristics of the frame TSY2 with five sectors are indicated in table 3 below.

TABLE 3

Characteristics	Synchronization in CSY2
Bit rate of SE2 (Mbit/s)	DE2 = 8.448
Frame bit rate (Mbit/s)	DY2 = 8.694
Frame length (bits)	540
Frame frequency (kHz)	16.101
Number of sectors	5
Composition of sectors:	
- bits of SE2	105
- additional bits	3
Allocation of frame bits	
- bits of SE2	525
- synchronization word SW	10
- stuffing indication IJ	5
Stuffing for SE2:	
- stuffing bit BJ	1
- minimum rate	0.2705
- nominal rate	0.2967

- maximum rate	0.3230
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5 A circuit CSY3 processes an incoming plesiochronous signal at 34.368 Mbit/s by positive stuffing and produces a synchronized signal SY3 having a frame TSY3 shown in FIG. 6. The frame TSY3 includes only one bit of a multiframe synchronization word of 10 bits included in the first of the six sectors of the frame. Thus a multiframe includes 10 frames. The characteristics of the frame TSY3 are indicated in table 4 below.

10

TABLE 4

	Characteristics	Synchronization in CSY3
Frame	Bit rate of SE3 (Mbit/s)	DE3 = 34.368
	Frame rate (Mbit/s)	DY3 = 34.777
	Frame length (bits)	534
	Frame frequency (kHz)	65.126
	Number of sectors	6
	Composition of sectors - bits of SE3 - additional bits	88 1
	Allocation of frame bits - bits of SE3 - synchronization word SW - stuffing indication IJ	528 1 5
	Stuffing for SE3 - stuffing bit BJ - minimum rate	1 0.2612

	- nominal rate	0.2823
	- maximal rate	0.3034
Multi-frame	Multiframe length (bits)	5340
	Number of frames	10
	Allocation of bits of the multiframe	
	- SE3 and IJ	5330
	- multiframe synchronisation word	10

Referring again to FIGS. 2 and 3, each of the synchronous signals SY1, SY2, SY3 corresponding to the plesiochronous signals of the group selected in the circuit CSG is applied to the multiplexing and modular frame forming circuit in order to include it in one or more elementary patterns. Each elementary pattern conforms to the MPEG2 frame recommendation and has a length of 1 632 bits, regardless of the group selected and the bit rate of the multiplex signal SMk. An elementary pattern is assigned a synchronous signal SY1 at the lowest bit rate $DY1 = 4.347 \text{ Mbit/s}$ when the signal SY1 belongs to the selected group ; or the equivalent of a signal SY1 in a synchronous signal SY2 at $DY2 = 8.694 \text{ Mbit/s}$, i.e. half the signal SY2 ; or the equivalent of a signal SY1 in a synchronous signal SY3 at $DY3 = 34.777 \text{ Mbit/s}$, i.e. one eighth of the synchronous signal SY3 at $DY3 = 34.777 \text{ Mbit/s}$.

As shown in FIG. 7, an elementary pattern is divided into two sectors each of 816 bits including 680 payload bits from a synchronous signal SY1, SY2, SY3 and 136 additional bits. In the first sector, the additional bits are divided between a frame alignment word MVT on 8

bits at the start of the sector and a variable allocation field AV of 120 bits and a constant allocation field of 8 bits at the end of the first sector. In the second sector of the pattern the additional bits are divided between 8 bits of the constant allocation field at the start of the sector and an error correcting code, field CCE of 128 bits at the end of the sector, for example a Reed Solomon code.

In each sector, 680 locations are occupied by bits of a single synchronous signal equivalent to those of two plesiochronous incoming signals at the low bit rate of 2.048 Mbit/s. Because an elementary pattern can be allocated to a synchronized signal SY1 at the bit rate DY1, two patterns are allocated to a synchronous signal SY2 at the bit rate $DY2 = 2 \times DY1$ and eight patterns are allocated to the synchronous signal SY3 at the bit rate $DY3 = 8 \times DY1$. A single periodic pattern is contained in the multiplex signal SM0 when operating mode M0 is selected, i.e. when two plesiochronous signals at $DE1 = 2.048$ Mbit/s are selected, and eight periodic patterns are contained in the multiplex signal SM3 when operating mode M3 is selected, i.e. when the incoming signal at $DE3 = 34.368$ Mbit/s is selected.

Thus a modular radio frame according to the invention comprises 2^k elementary patterns when operating mode Mk is selected to produce a multiplex signal SMk at the bit rate DRk where $0 \leq k \leq 3$. The frame frequency is constant and equal to $DY1/1360 = DY3/(1360 \times 8) = 3.196$ kHz and the elementary pattern duration decreases by half from one multiplex signal SMk to the next SM(k+1).

The modularity of the frame according to the invention is tied to the modularity of the synchronization circuits CSY1, CSY2 and CSY3: the structure of a pattern is constant, like that of the synchronization circuit, and the number of patterns in

the frame of constant duration and the number of synchronization circuits in service are determined as a function of the number and the bit rates of plesiochronous incoming signals to be multiplexed.

5 Thus a modular frame according to the invention is made up of:

- in mode M0, $2^0 = 1$ single pattern MT1 for a signal SY2 resulting from multiplexing two signals SE1 at DE1 = 2.048 Mbit/s;

10 - in mode M1, $2^1 = 2$ = integer part of $DE2/(2 \cdot DE1)$ patterns MT1 and MT2 respectively allocated to two pairs of signals SE1 at DE1 = 2.048 Mbit/s, i.e. two synchronous signals SY1, or one signal SE2 at DE2 = 8.448 Mbit/s;

15 - in mode M2, $2^2 = 4$ = integer part of $2 \cdot DE2/(2 \cdot DE1)$ patterns respectively allocated to four pairs of signals SE1 at DE1 = 2.048 Mbit/s, i.e. four synchronous signals SY1; or two pairs of signals SE1 and one signal SE2 at DE2 = 8.448 Mbit/s; or two signals SE2;

20 - in mode M3, $2^3 = 8$ = integer part of $DE3/(2 \cdot DE1)$ patterns respectively allocated to 8 pairs of signals SE1 at DE1 = 2.048 Mbit/s, i.e. eight synchronous signals SY1; or 6 patterns with 6 pairs of signals SE1 and 2 patterns with one signal SE2, or 4 patterns with 4 pairs of signals SE1, and two pairs of patterns with two signals SE2; or 2 patterns with 2 pairs of signals SE1 and three pairs of patterns with three signals SE2; or 4 pairs of patterns with 4 signals SE2; or 8 patterns with signal SE3 at DE3 = 34.368 Mbit/s.

30 The multiplex signals SM0 to SM3 have bit rates DM0 = 5.216 Mbit/s, DM1 = 10.433 Mbit/s, DM2 = 20.866 Mbit/s and DM3 = 41.732 Mbit/s increased by a constant ratio RC = $1632/1360 = 1.2$ relative to the corresponding bit rates of the synchronous signals SY1, SY2, 2 SY2 and SY3. The
35 highest bit rate DM3 of the bit rates of the multiplex

signals SM0 to SM3 is equal to the constant bit rate DC = 41.732 Mbit/s in the transmission cable CA.

Regardless of the multiplex signal SMk produced by the frame forming circuit FTH, the respective multiplex signal frame has the common radio frame structure shown in FIG. 7. The width of a bit in the radio frame is a function of the bit rate of the multiplex signal SMk. The bit width differences between signals SMk are compensated in the oversampling circuit SUR which oversamples the signal SRk with a sampling ratio $2^{3-k} = DC/DM0 = 8$ for mode M0, $DC/DM1 = 4$ for mode M1, $DC/DM2 = 2$ for mode M2, or $DC/DM3 = 1$ so that the bit rate of the signal at the output of the transceiver ETR is always equal to the constant bit rate DC = 41.732 Mbit/s. As shown in FIG. 1, the output of the transceiver ETR is that of the cable interface IC1 which codes the oversampled resultant signal SSURk, for example using the bipolar HDB3 code, and matches it to the characteristics of the cable CA. Thus, a bit of the signal SR0, SR1 or SR2 is repeated 8 times, 4 times or twice in succession in the signal SSUR0, SSUR1 or SSUR2 at the bit rate DC.

272 additional bits BS in each frame pattern are divided between a frame alignment word on 8 bits, a variable allocation field AV on 120 bits, a constant allocation field AC on 16 bits and an error correcting code field CCE on 128 bits. The fields AV and AC guarantee a minimum transmission capacity that varies as a function of the bit rate of the multiplex signal SMk for additional transmission channels and identical operation, regardless of the mode selected and consequently the number 2^k of frame patterns. Depending on the nature of an additional channel, the number of bits reserved for it is therefore variable or constant.

The constant allocation field AC shown in FIG. 7 includes a telephone service channel call request bit AVdS, four error information bits E1 to E4, three free bits CL1 to CL3, four frame synchronization bits SYT1 to SYT4 and four quality bits Q.

The AVdS bit at a predetermined state indicates the use of a telephone service channel VdS, i.e. a call being set up or already set up on the telephone service channel VdS whose payload field is included in the variable allocation field AV and has a length inversely proportional to the bit rate of the multiplex signal SMk. The channel VdS transfers call requests between the transceivers ETR of two radio stations communicating in accordance with the invention, and preferably transfers call requests between the transceiver ETR concerned, which is inside the building, and the radio transceiver ERA, which is several hundred meters away. A telephone call is set up on the telephone service channel by maintenance personnel, for example, without using any other intermediate transmission system.

The bits E1 to E4 are reserved for collecting error information supplied by an error correction circuit included in the circuit CRE of the transceiver ERA. These bits are local information, indicative of a pattern including errors which may or may not have been corrected, and are inserted into the next pattern. The bits E1 to E4 are processed when they are received by the transceiver ETR of the radio station to estimate the error rate according to the corresponding transmission direction of the radio link. For example, the bits E1 to E4 indicate that an erroneous byte has been detected and corrected and that a pattern includes a number of erroneous bytes greater than the correction capacity of the Reed-Solomon code, i.e. at least 9 bytes, and that

these bytes cannot therefore be corrected. If the radio link includes two transmission channels which back each other up, pairs of bits E1-E2 and E3-E4 are assigned to each transmission channel.

5 The three bits CL1 to CL3 remain free so that they can be allocated to new services.

 The four bits SYT1 to SYT4 in each pattern are reserved for synchronization of the radio modular frame. These bits complete the alignment word MVT of each
10 pattern and contribute to the synchronization of a "multiframe" of patterns which is in fact coincident with the modular frame.

 The four bits Q of the constant allocation field AC are allocated to the collection of information needed to
15 produce quality criteria for the link between the transceivers of the radio station. These bits carry the following information :

 - a fault bit DEF to signal a loss of alignment in the preceding frame ;

20 - two anomaly bits AN1 and AN2 for respectively signaling code violation on the cable CA and a minimum number of erroneous bytes in the preceding pattern ;

 - an erroneous block return bit RBE corresponding either to the receive direction opposite the emit
25 direction of the local station and indicating reception of a frame carrying an uncorrected pattern indication or an indication of a frame including at least one code violation, or reception of a frame carrying remote frame alignment loss indication, or to the local detection of a
30 frame alignment loss.

 All this data is inserted into the pattern or frame following that in which the corresponding event occurs.

 FIGS. 8, 9 and 10 respectively show the allocation
35 of the bits of the 120-bit variable allocation field AV

into a pattern as a function of mode M0, mode M1 and mode M2 or M3.

At the beginning of field AV 24 bits in mode M0 or 72 bits in mode M2 or 96 bits in mode M2 or M3 are respectively reserved for an auxiliary channel VAux which is processed in an auxiliary channel forming circuit MFVA (FIG. 2) connected to the circuit FTH as a function of the operating mode selected under the control of the unit UC. The data relating to the auxiliary channel is transmitted in the form of serial signals accompanied by a corresponding clock signal and frame synchronization information. Table 5 below gives one example of the distribution of bits and the transmission bit rates for the auxiliary channel. Depending on its use, the auxiliary channel signal can be formatted as an auxiliary frame whose structure is not predetermined by the modular frame itself but depends only on the intended application, within the limits of the characteristics set out in table 5.

TABLE 5

	Mode (Mbit/s)	Pattern frequency (kHz)	No. of bits	Bit rate (kbit/s)
M0	2 x 2	3.196	24	76.7
M1	4 x 2	6.392	72	460.2
M2	8 x 2	12.785	96	1227.4
M3	16 x 2	25.571	96	2454.8

According to table 5, the maximum bit rate offered to an auxiliary channel is increased to the bit rate of the respective resulting signal in the circuit MFVA and is equal to the radio frame frequency of the respective resulting signal multiplied by the number of bits available for the auxiliary channel.

The applications described above are based entirely on the transmission capacity of each auxiliary channel and are given by way of non-limiting example only.

5 In mode M0, the auxiliary channel VAux transmits one asynchronous signal at 9 600 bit/s or one signal at 64 kbit/s.

In mode M1, the channel VAux routes one signal at 256 kbit/s or at least four signals at 64 kbit/s.

10 In mode M2, the bit rate offered to the auxiliary channel VAux is significantly higher than in the preceding modes and enables up to four signals at 256 kbit/s to be transmitted.

15 In mode M3, the bit rate offered to the auxiliary channel VAux is still higher. It can be used to transmit one signal at 2.048 Mbit/s and one signal at 256 kbit/s or four signals at 64 kbit/s. FIG. 11 shows a frame structure divided into three sectors each of 32 bits. In this example, the first four bits of each sector are respectively allocated to the four signals at 64 kbit/s or allocated to the signal at 256 kbit/s.

20 Whichever mode applies, the digital signals are processed in the circuit MFVA by increasing their bit rates as a function of the characteristics of the auxiliary channel. The asynchronous signals, typically at 4 800 bit/s to 19 200 bit/s, are transmitted oversampled at 5 times their nominal bit rate at least. The channels at 64 kbit/s or 256 kbit/s are transmitted in packets. The channel at 2 048 kbit/s, which can be transmitted only in mode M3 (16 x 2 Mbit/s), is processed like an incoming plesiochronous signal. It is inserted into the auxiliary frame after synchronization to its rhythm by positive stuffing.

35 Still referring to FIGS. 8 to 10, the variable allocation field AV in each pattern includes 32, 16 or 8

bits in mode M0, M1 or M2, M3 reserved for a 64 kbit/s network telephone service channel VdSR. Then 4 bits, 2 bits or 1 bit are allocated to a channel DIA for the dialog between the control unit UC in the transceiver ETR and the microcontroller MC in the transceiver ERA. The dialog includes, in the ETR to ERA transmit direction, the "uplinking" of remote control commands such as changing groups of plesiochronous signals and characteristics relative to the group selected, power adjustment, and in the ERA to ETR receive direction, the "downlinking" of status or fault indications such as change of group, alarms, switching status, received radio field level.

12, 6 or 3 bits are then allocated to the telephone service channel VdS for setting up an audio call between the two stations of the radio link or between the transceivers ETR and ERA in the radio station. The associated calls are signaled by the bits AVdS.

12, 6 or 3 bits maximum are then offered to each of two digital data channels DN1 and DN2 in the field AV. Each channel DN1, DN2 transmits through oversampling an asynchronous signal at 9 600 bit/s, for example.

Finally, 8, 4 or 2 and 16, 8 or 4 bits are respectively reserved for two longitudinal telemonitoring channels TSL1 and TSL2 which carry dialog between transceivers on the same link. The channel TSL1 is used to manage the point-to-point radio link and the channel TSL2 is used for network management.

Referring again to FIG. 1, the encoded oversampled signal SSURk at 41.732 Mbit/s transmitted via the cable interface IC1 in the coaxial cable CA is decoded in the cable interface IC2 of the radio transceiver ERA. The undersampling circuit SOE detects each group of 2^{3-k} consecutive bits in the decoded oversampled signal, i.e.

each group of 1, 2, 4 or 8 bits for the operating mode M3, M2, M1 or M0, thereby signalling the oversampling ratio 2^{3-k} to the microcontroller MC and thereby undersampling the signal transmitted via the cable CA with a ratio $1/2^{3-k}$ to return the multiplex signal SMk to the radio frequency emission circuit CEM via the digital filter FIE.

Depending on the oversampling ratio 2^{3-k} , and therefore on the operating mode Mk, the microcontroller MC programs the emit digital filter FIE in the baseband. The bandwidths of the programmed filter are compatible with the bit rate DMk of the returned resulting signal SMk corresponding to the selected mode Mk. In the circuit CEM the filtered signal modulates an intermediate frequency carrier which is then transposed to the radio frequency.

At the receiving end, a radio digital frame signal at the bit rate DMk in accordance with the invention is processed by operations which are substantially the reverse of those described in detail above for the emission of a signal of this kind.

In the radio transceiver ERA the received radio frame signal is amplified, transposed and demodulated to yield a baseband signal in the radio frequency reception circuit CRE. In particular, the received signal is filtered by frequency filters selected by the microcontroller MC from a battery of switched filters in the circuit CRE as a function of the operating mode Mk. The received baseband signal is then filtered according to the operating mode Mk by a programmable filter included in the demodulation and digital filtering circuit FIR. The received baseband signal is then oversampled in the oversampling circuit SUE as a function of the ratio 2^{3-k} to transmit a digital signal at the bit

rate DC = 41.732 Mbit/s in the coaxial cable CA, encoded via the cable interface IC2.

After it is decoded in the cable interface IC1 in the transceiver ETR, the demultiplexing device DMUX
 5 undersamples the signal received via the cable CA to yield a multiplex digital signal at the bit rate DMk as a function of the sampling ratio 2^{3-k} relating to the operating mode Mk signaled by the control unit UC. The received multiplex signal is then deformatted and
 10 demultiplexed into the synchronous signals corresponding to the selected group under the control of the unit UC. The bits of the fields AV, AC and CCE in each pattern (FIG. 7) of the received multiplex signal in part are processed by the control unit UC, in particular to detect
 15 errors and generate alarm signals, and in part directed to the various channels VAux, VdSR, VdS, DN1 and DN2. The synchronous signals resulting from the demultiplexing of the received multiplex signal are desynchronized by unstuffing and then coded in HDB3 transcoding circuits
 20 into corresponding plesiochronous signals which correspond to the selected group.

Alternatively, access to a received component signal at the bit rate DE1, DE2 or DE3 in the form of the corresponding synchronous signal SY1, SY2 or SY3 can be
 25 sufficient. Demultiplexing the received multiplex signal in fact consists in extracting from it the patterns corresponding to the required synchronous signal. Extraction of this kind is beneficial in an intermediate radio station of the relay station type for most signals
 30 transmitted and of the router type for signals whose patterns are to be extracted.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE
PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS :

5 1 - A digital frame having a predetermined duration
resulting from the multiplexing of plesiochronous digital
signals, said frame comprising patterns having a common
structure and a predetermined length which are
independent of the bit rates of said plesiochronous
digital signals to be multiplexed of a group selected
from a plurality of groups of plesiochronous digital
10 signals having bit rates which are substantially
multiples of each other, said patterns including a
predetermined number of additional bits and a
predetermined number of bits of respective synchronous
signals having bit rates which are multiples of each
15 other and result from synchronization of plesiochronous
digital signals of said selected group, each
plesiochronous digital signal of said selected group
being allocated a number of patterns in the frame equal
to the integer part of the quotient on dividing the bit
20 rate of said each plesiochronous digital signal of said
selected group by the lowest bit rate of said
plesiochronous digital signals.

25 2 - A frame according to claim 1, wherein said
quotient is replaced by the quotient obtained on dividing
the bit rate of said each plesiochronous digital signal
of said selected group by the product of the lowest bit
rate of said plesiochronous digital signals and a
predetermined integer which is equal to a submultiple of
30 the integer part of the quotient on dividing the bit rate
of plesiochronous signals just higher than said smallest
bit rate by said smallest bit rate, a synchronous signal
corresponding to said selected group having the lowest
bit rate resulting from synchronization and multiplexing
35 of a number of plesiochronous digital signals at said

lowest bit rate equal to said predetermined integer, and a single pattern being allocated in said frame to said synchronous signal having said lowest bit rate.

5 3 - The frame according to claim 1, wherein the additional bits are divided between an alignment word, a constant allocation field, a variable allocation field varying as a function of the bit rate of a multiplex signal including the frame corresponding to said selected
10 group, and an error correcting code field, said fields having respective predetermined lengths.

 4 - The frame according to claim 3, wherein said constant allocation field includes frame synchronization
15 bits and bits for collecting error information and quality bits.

 5 - The frame according to claim 3, wherein said variable allocation field includes bits of an auxiliary
20 channel whose offered bit rate increases as the bit rate of said multiplex signal increases.

 6 - The frame according to claim 3, wherein said variable allocation field includes bits which are
25 reserved for a predetermined number of telephone and data transmission channels and whose number decreases as the bit rate of the selected multiplex signal increases.

 7 - The frame according to claim 3, wherein said variable allocation field includes bits allocated to a
30 telephone service channel whose number decreases as the bit rate of the selected multiplex signal increases, and said constant allocation field includes a bit indicating a call request on said telephone service channel.

35

8 - A method of forming a digital frame, comprising the following steps:

- 5 - constituting groups of plesiochronous digital signals from a plurality of given plesiochronous digital signals having bit rates which are substantially multiples of each other, the sums of the bit rates of said plesiochronous digital signals in the group being substantially multiples of each other,
- 10 - selecting one of said plesiochronous digital signal groups,
- synchronizing the plesiochronous digital signals in said selected group to yield synchronous signals having bit rates which are multiples of each other,
- 15 - allocating each synchronous signal a number of patterns of predetermined structure in the frame equal to the integer part of the quotient on dividing the bit rate said each synchronous signal by the lowest bit of said plesiochronous digital signals, and
- 20 - forming a multiplex signal including said frame by inserting in each pattern a predetermined number of bits of the respective synchronized signal and a predetermined number of additional bits.

25 9 - The method according to claim 8, wherein at least one synchronous signal includes a frame including a synchronization word, a plurality of stuffing indication bits and bits of a single corresponding plesiochronous digital signal.

30 10 - The method according to claim 8, wherein said quotient is replaced by the quotient obtained on dividing the bit rate said each synchronous signal by the product of the lowest bit rate of said plesiochronous digital signals and a predetermined integer which is equal to a
35 submultiple of the integer part of the quotient on

dividing the bit rate of the plesiochronous signals just higher than said lowest bit rate by said lowest bit rate, and wherein the step of synchronizing plesiochronous digital signals to said lowest bit rate is replaced by a
5 step of multiplexing and synchronizing the plesiochronous digital signals at said lowest bit rate into synchronous signals in numbers equal to said quotient on dividing the bit rate of said each synchronous signal by said product when said selected group includes plesiochronous digital
10 signals at said lowest bit rate in a number at least equal to said quotient.

11 - The method according to claim 8, including the steps of:

15 - providing a plurality of modular synchronizing means for synchronizing the plesiochronous digital signals, and

- operating a number of synchronization means equal to the number of plesiochronous digital signals of the
20 selected group and programmed in accordance with the bit rates thereof.

12 - The method according to 8, wherein the bit rate of the multiplex signal is at most equal to the
25 constant bit rate on a transmission medium, and including a step of oversampling the multiplex signal with an oversampling ratio between the bit rate of the transmission medium and the bit rate of the multiplex signal to transmit an oversampled resultant signal at
30 said constant bit rate.

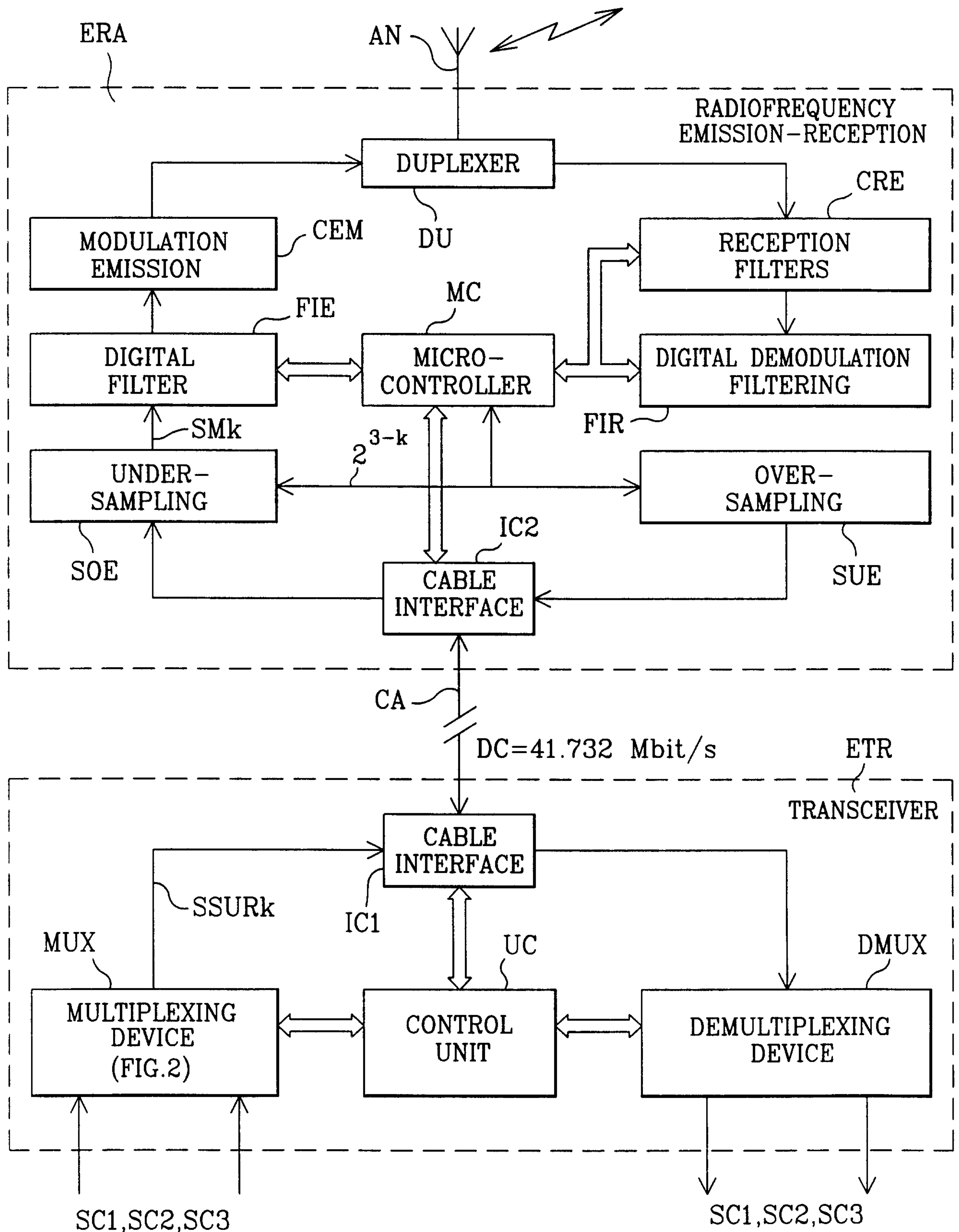
13 - The method according to claim 12, wherein the transmission medium connects a transceiver at the base of a radio station and a radio transceiver of said radio
35 station, and the method comprises in said radio

transceiver a step of undersampling said oversampled resultant signal with the reciprocal of said oversampling ratio and a step of selecting filters as a function of said oversampling ratio.

5

14 - The method according to claim 8, wherein inserting said additional bits into said frame includes the inserting a frame alignment word, a constant allocation field, a variable allocation field which
10 varies as a function of the bit rate of the multiplex signal and an error correcting code field, said fields having respective predetermined lengths.

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FIG.1

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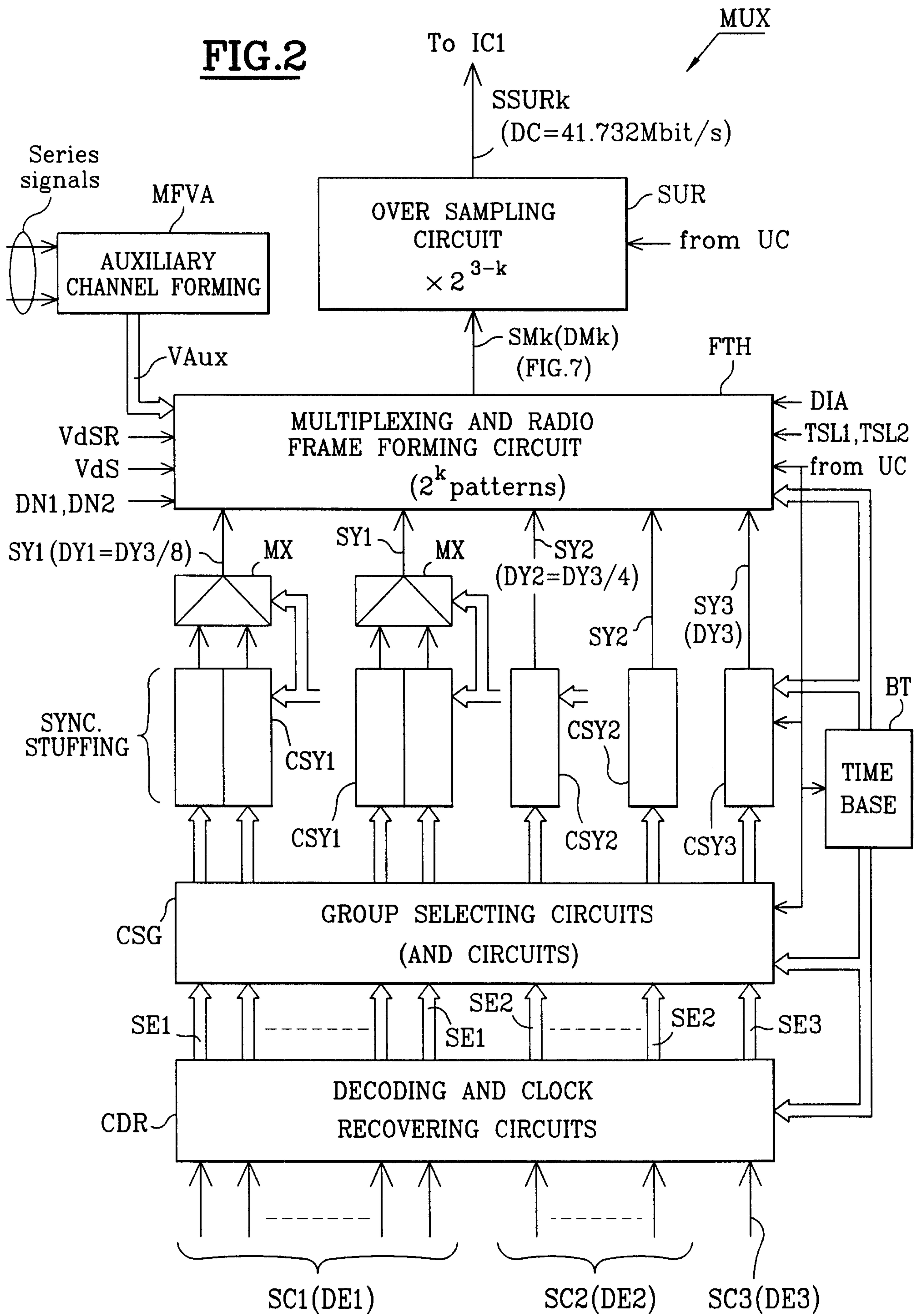
FIG.2

FIG.3

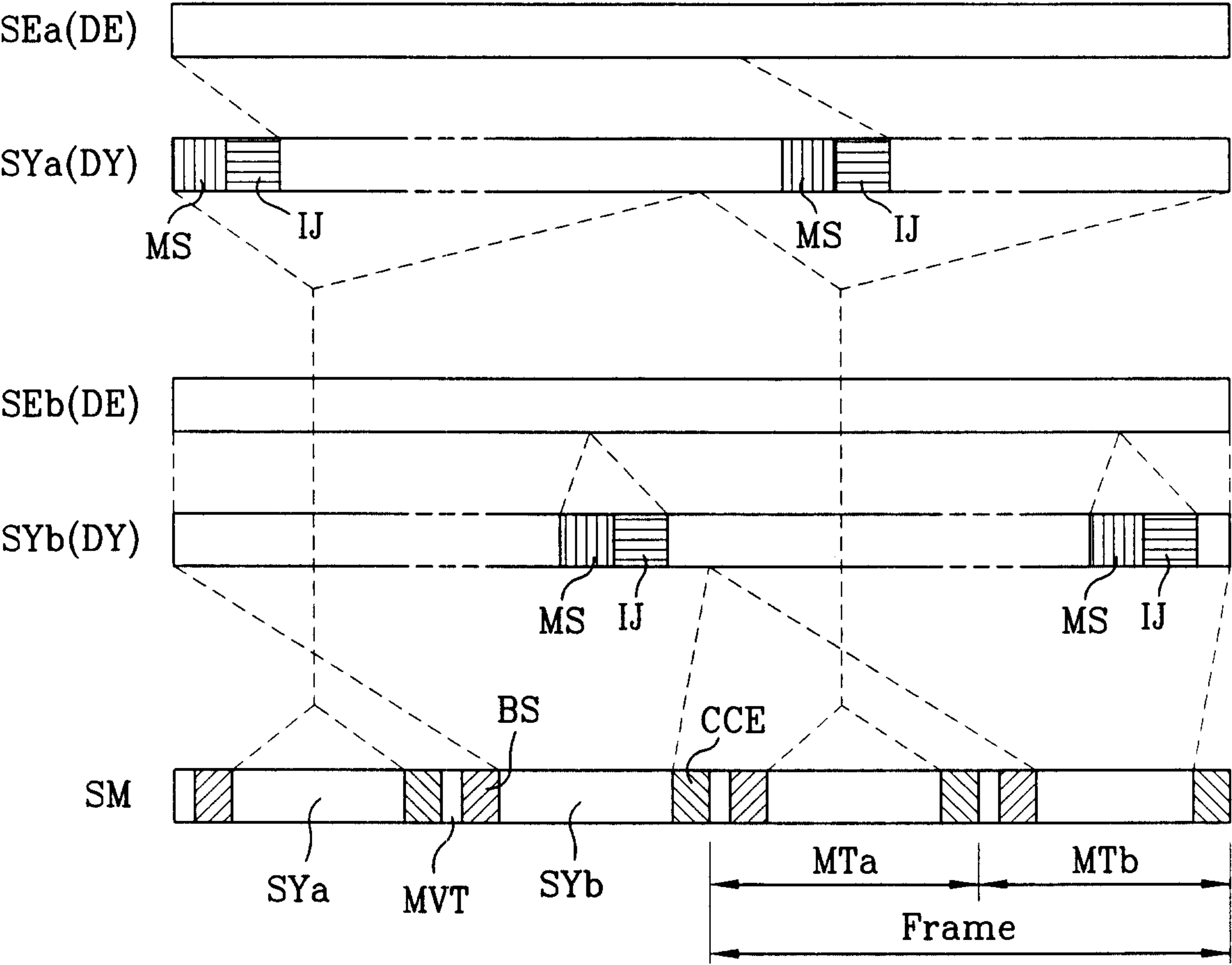


FIG.4

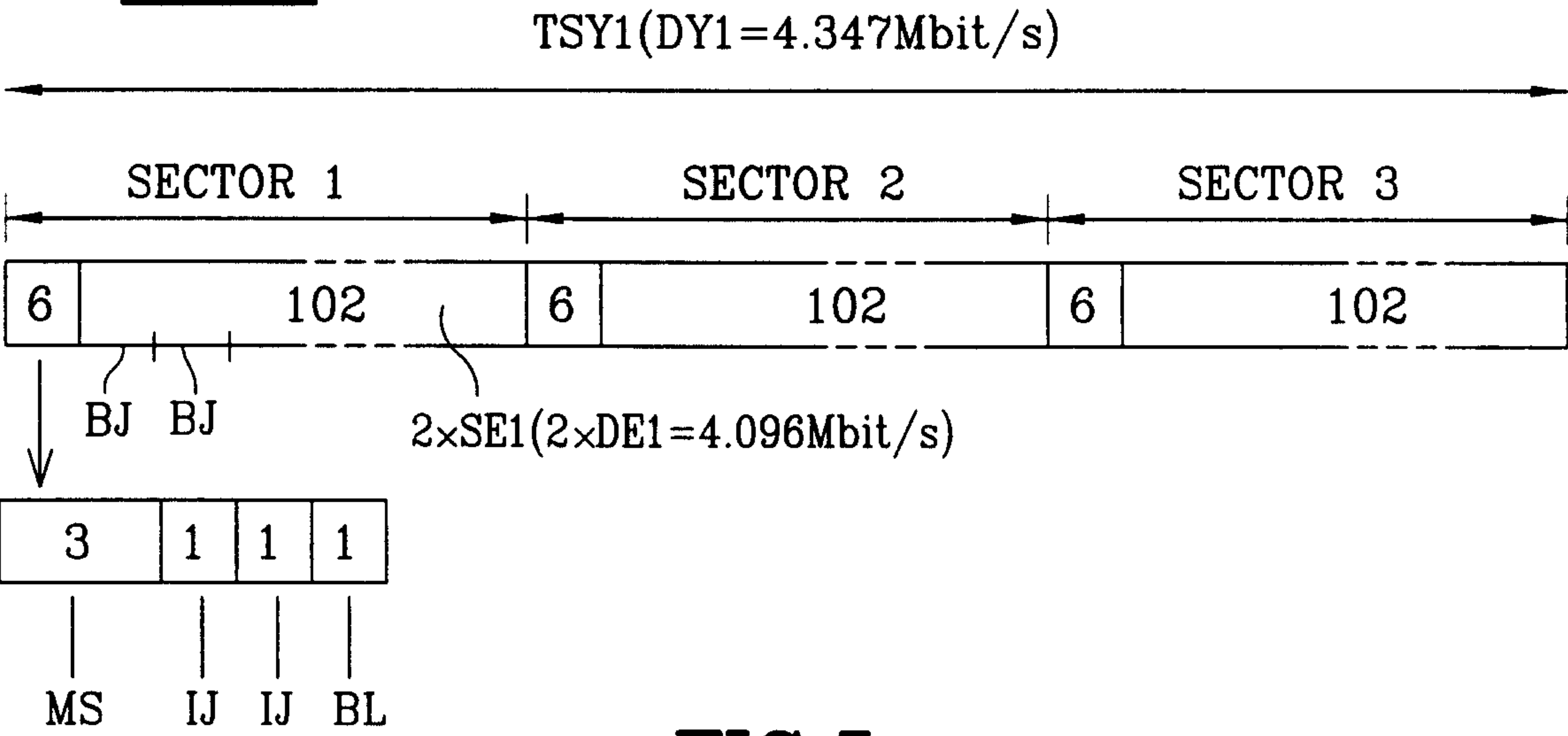


FIG.5

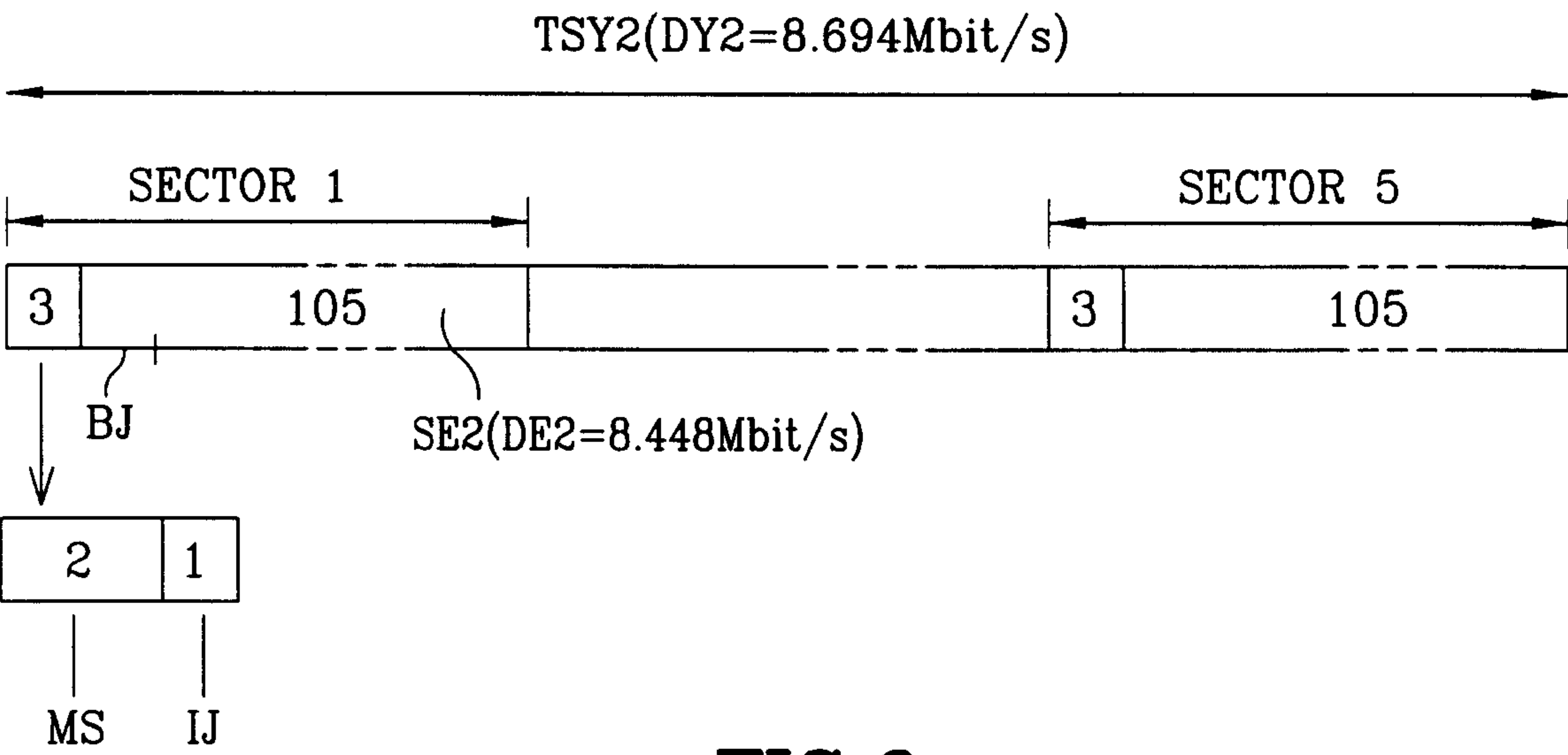
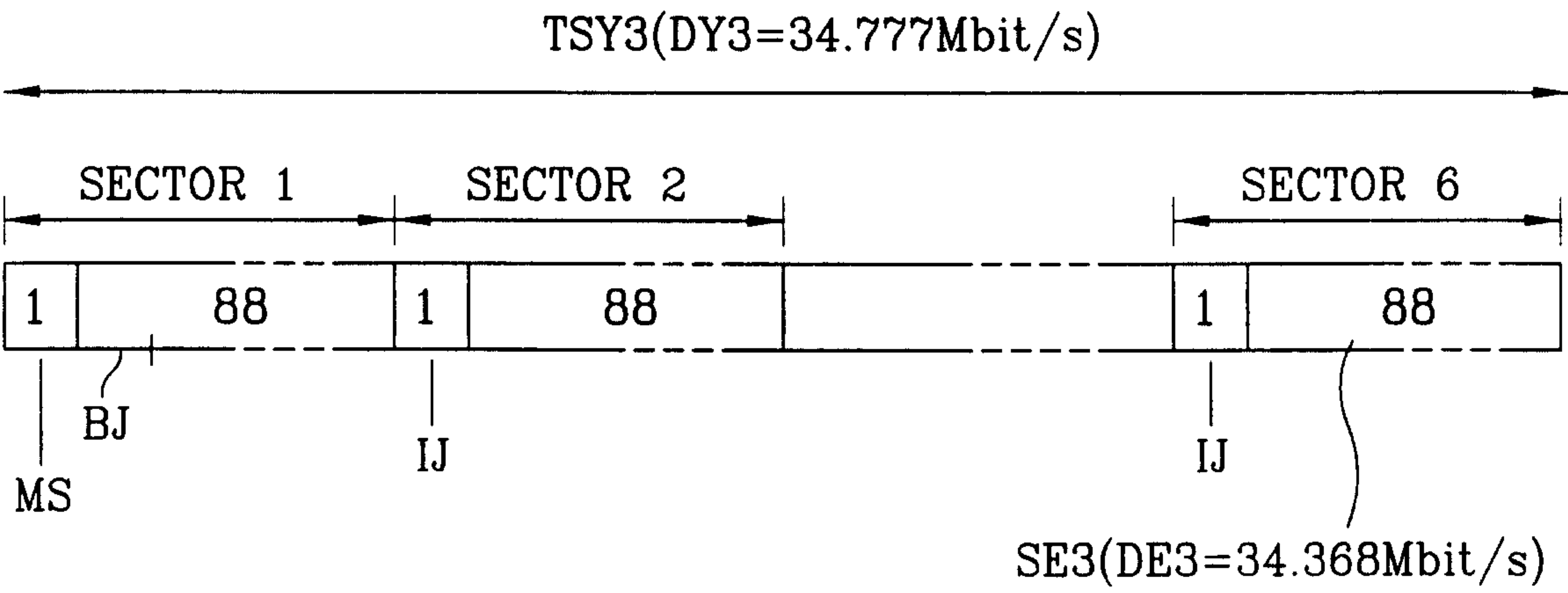


FIG.6



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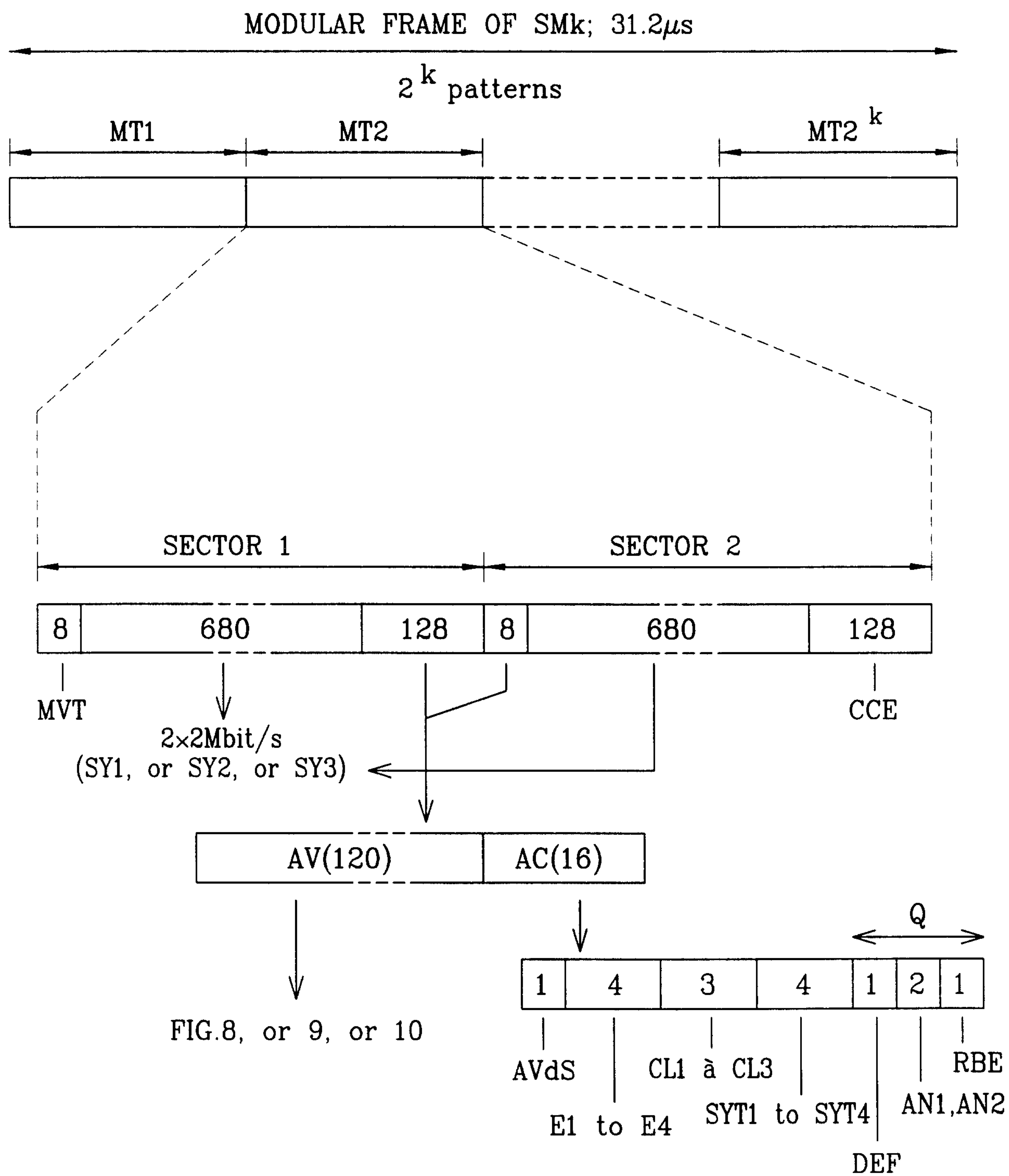
FIG.7

FIG.8

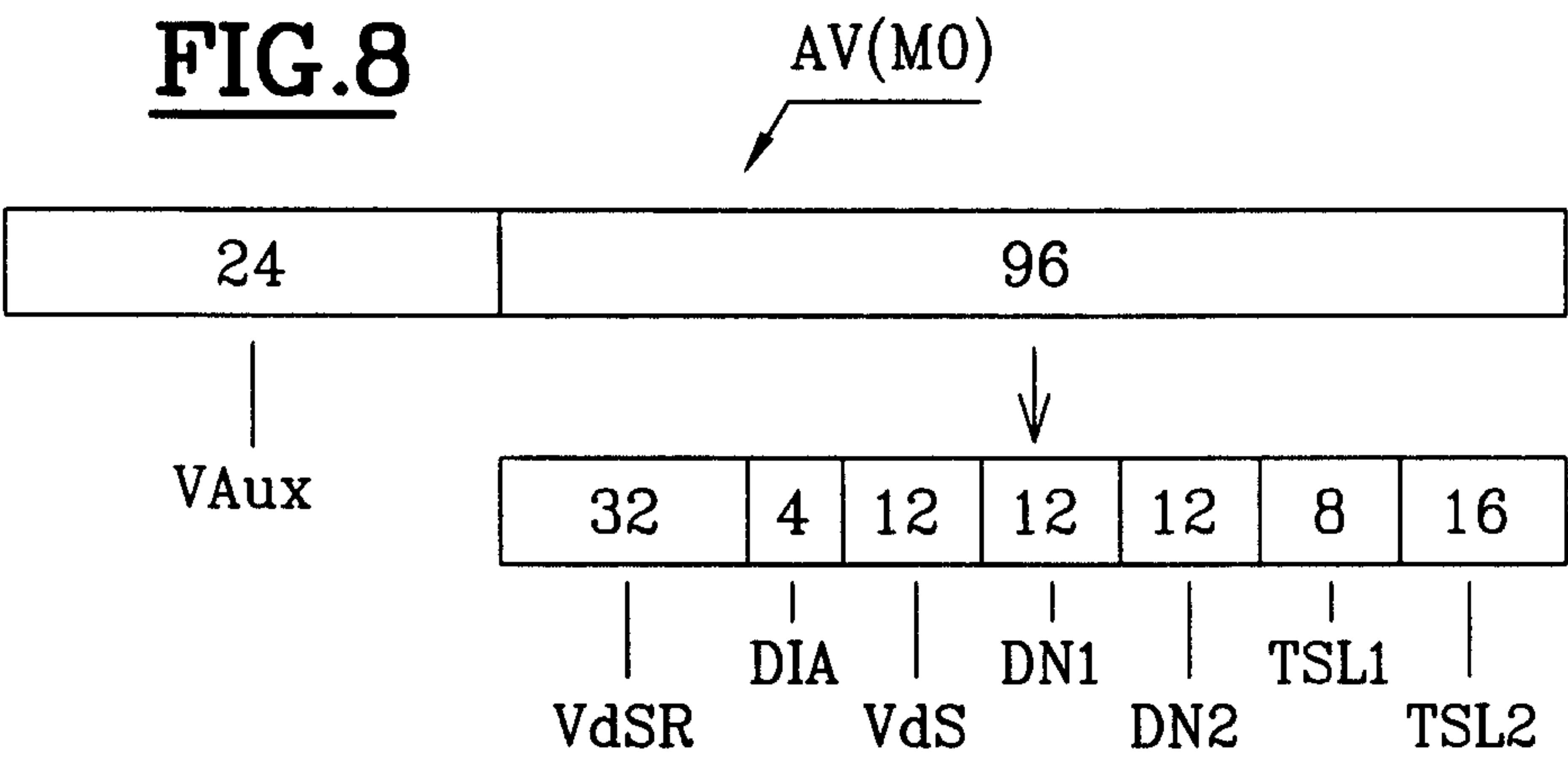


FIG.9

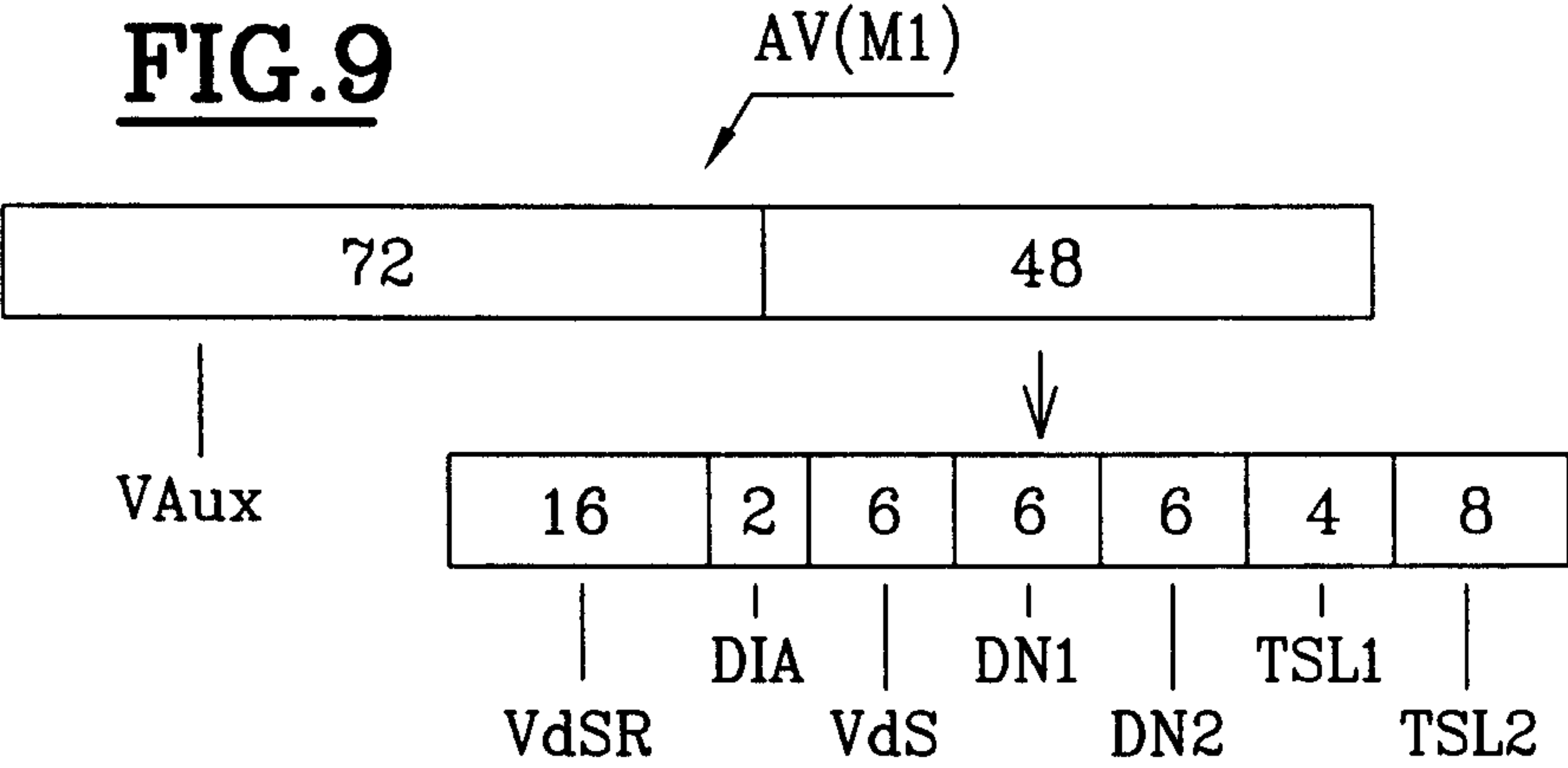


FIG.10

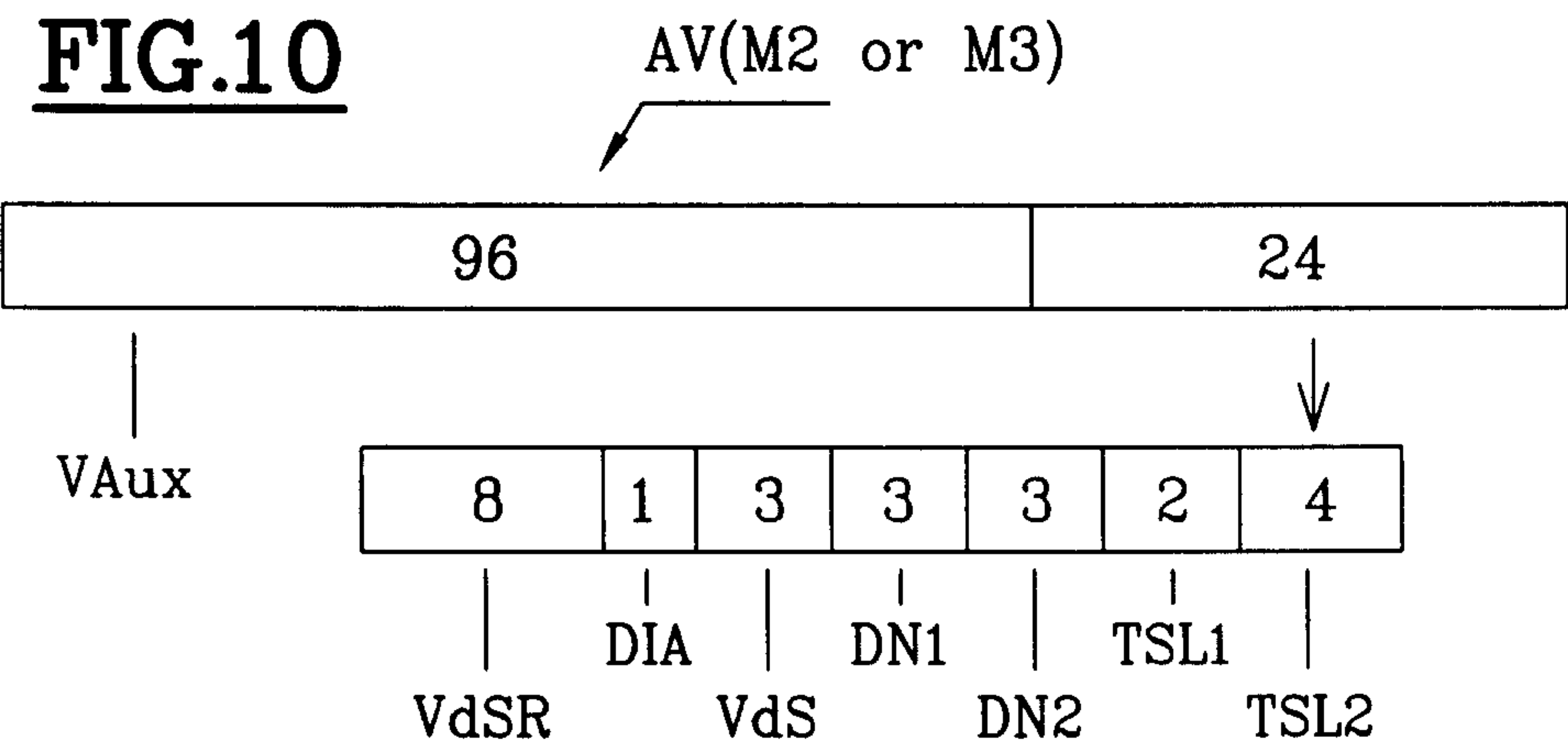


FIG.11

