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(71) Applicant: M-PULSE MICROWAVE [US/US]; 576 Charcot Avenue, San Jose, CA 95131 (US).

(72) Inventor: RICHARDS, John, Gareth ; 4847 Tonino Drive, San Jose, CA 95131 (US).

(74) Agents: VINCENT, Lester, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, CA 90025 (US).

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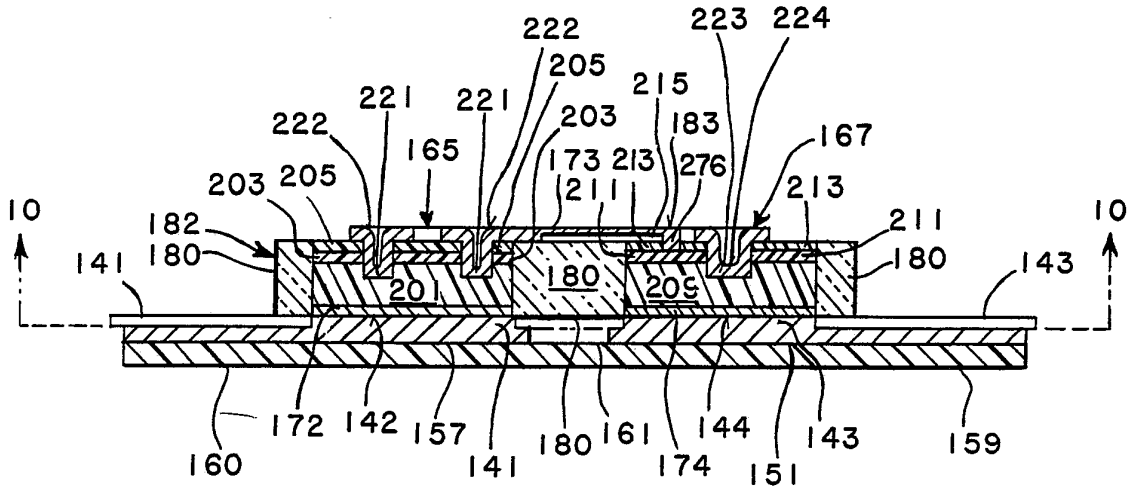

(57) Abstract

A ring quad (140) comprised of four diodes (142, 144, 146, 148). Bridges (173, 175, 177, 179) couple the anodes (183, 185, 187, 181) and cathodes (282, 284, 286, 288) of the diodes. Beam leads that are part of a lower lead (141, 143, 145, 147) package are coupled to the bottoms of the cathodes of the diodes. A method of forming a ring quad, including the steps of forming an oxide layer on top of silicon (301), forming a plurality of wells, cutting the oxide and silicon into a plurality of mesas (442, 44, 446, 448) filling channels (305, 306, 307) bordering each mesa with glass (180), forming a plurality of openings (481, 483, 485, 487), such that the metal contacts the N- layer (203, 211, 259, 253), forming a plurality of cathodes by placing metal into each of the plurality of wells such that the metal contacts the N+ layer (201, 209, 257, 251), coupling the cathodes and anodes, cutting central channels (161, 163) through a portion of glass, removing the bottom silicon, and coupling beam leads (141, 143, 145, 147) that are part of a lower lead package to the metalized bottoms (172, 174, 176, 178) of the N+ layers.

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"AN IMPROVED BEAM LEADS FOR SCHOTTKY-BARRIER DIODES IN A RING QUAD"

FIELD OF THE INVENTION

The present invention pertains to the field of balanced mixers comprised of diodes. More particularly, this invention relates to a ring quad comprised of four diodes.

BACKGROUND OF THE INVENTION

A ring quad can be used in a double-balanced mixer. Balance is an important characteristic for a ring quad, because better balance means more efficiency. Good balance means that the capacitance associated with each diode of the ring quad is approximately equal and that the inductance associated with each diode of the ring quad is also approximately equal.

In early prior art ring quads, four diodes were interconnected with wires in a ring arrangement. The outside electrical connection comprised four wires. Disadvantages of this prior art configuration included high capacitance, high inductance, and poor balance.

Other prior art ring quads have used beam leads instead of wires to provide interconnection. The beam leads have resided on the top of the ring quad and have provided interconnections between the anodes and cathodes of the respective diodes of the ring quad. Beam leads have also been used on the top of the prior art ring quads as flying leads to provide connection to external circuitry. The flying beam leads have been structurally supported by the diode blocks. A glass layer has been used in the prior art ring quad to hold the four diode blocks together.

A prior art ring quad with flying beam leads on the top of the ring quad has several disadvantages. Capacitance, inductance, and balance

problems can arise from improper bonding of the beam leads. The beams for the ring quad diodes do not always seat properly during packaging. The relatively large beam leads are prone to bending, resulting in capacitance, inductance, and balance problems. Dynamic resistance problems can also arise.

Moreover, the prior art ring quads can be fragile given that (1) a relatively thin layer of glass is used to hold the four diodes together and (2) the flying beam leads present a relatively large lever arm to the top of the ring quad.

A further disadvantage of the prior art configuration is that power dissipation is constrained by the fact that having only connections to the tops of the diodes and not to both the tops and bottoms of the diodes means that power is not dissipated throughout the full three-dimensional volume of each diode. In other words, power is dissipated across a portion of each diode of the prior art ring quad rather than fully through each diode.

Another disadvantage of the prior art ring quad is that, even under normal conditions, pulse transients can sometimes result in carbon trails reaching or jumping across the prior art topography from cathode to anode, given that connections are made only to the tops of the diodes and that the cathodes and anodes reside relatively close to each other. Such carbon trails can destroy the cathode/anode topography of the prior art ring quad. Given that ring quads are often used in mixers, and that mixers are used for sidebands and for modulation, such pulse transients are not infrequent.

An additional disadvantage of the prior art ring quad is that forming an efficient doubly double-balanced mixer (comprised of eight diodes) in three-space is difficult given that (1) the leads interconnecting the anodes and cathodes of each ring quad and (2) the flying beam leads of each ring quad all reside on the top of each ring quad.

SUMMARY AND OBJECTS OF THE INVENTION

In view of the limitations of known ring quads, one of the objectives of the present invention is to provide a ring quad with low capacitance, low inductance, and good balance.

Another objective of the present invention is to provide a ring quad that is less fragile and less prone to beam bending.

Another objective of the present invention is to provide a ring quad that has good power dissipation.

A further objective of the present invention is to provide a ring quad with small geometries and high wafer packing density.

These and other objects of the invention are provided for by a ring quad comprised of a first diode, a second diode, a third diode, and a fourth diode. The first diode has an anode at the top and a cathode. The second diode has an anode at the top and a cathode. The third diode has an anode at the top and a cathode. The fourth diode has an anode at the top and a cathode. A first bridge couples the top of the cathode of the first diode to the anode of the second diode. The first bridge runs from the top of the first diode to the top of the second diode. A second bridge couples the top of the cathode of the second diode to the anode of the third diode. The second bridge runs from the top of the second diode to the top of the third diode. The third bridge couples the top of the cathode of the third diode to the anode of the fourth diode. The third bridge runs from the top of the third diode to the top of the fourth diode. A fourth bridge couples the top of the cathode of the fourth diode to the anode of the first diode. The fourth bridge runs from the top of the fourth diode to the top of the first diode. First connection means is coupled to

the metalized bottom of the cathode of the first diode. Second connection means is coupled to the metalized bottom of the cathode of the second diode. Third connection means is coupled to the metalized bottom of the cathode of the third diode. Fourth connection means is coupled to the metalized bottom of the cathode of the fourth diode.

The above-mentioned objects and other objects of the invention are also provided for by a method of forming a ring quad that includes four diodes. An oxide layer is formed on top of silicon. The silicon has an N^- layer below the oxide and an N^+ layer below the N^- layer. A plurality of wells are formed by etching through the oxide and the N^- layer to the N^+ layer for each well. The oxide and silicon is cut into a first mesa, a second mesa, a third mesa, and a fourth mesa, with a plurality of empty channels bordering each mesa and silicon under each channel. Each mesa has an upper oxide layer, a middle N^- layer, a lower N^+ layer, and at least one well. The channels are filled with glass. A plurality of openings are formed through the oxide to the N^- layer, wherein each mesa has at least one opening. A plurality of anodes are formed by placing metal into each of the plurality of openings such that the metal contacts the N-layer. A plurality of cathodes are formed by placing metal into each of the plurality of wells such that the metal contacts the N^+ layer. The cathode of the first mesa is coupled to the anode of the second mesa. The cathode of the second mesa is coupled to the anode of the third mesa. The cathode of the third mesa is coupled to the anode of the fourth mesa. The cathode of the fourth mesa is coupled to the anode of the first mesa.

Central channels are cut through a portion of the glass down to the silicon to form a module comprising first, second, third, and fourth mesas of silicon, wherein each of the first through fourth mesas is surrounded on its sides by glass. The silicon is removed up to the bottom of the glass, wherein the silicon beneath the module is removed and the first mesa becomes a first diode, the second mesa becomes a second diode, the third mesa becomes a third diode, and the fourth mesa becomes a fourth diode. The bottom of the N^+ layer of each diode is metalized. First connection means are coupled to the bottom of the N^+ layer of the first diode. Second connection means are coupled to the bottom of the N^+ layer of the second diode. Third connection means are coupled to the bottom of the N^+ layer of the third diode. Fourth connection means are coupled to the bottom of the N^+ layer of the fourth diode.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

Fig. 1 is an electrical circuit diagram of a ring quad comprised of four diodes.

Fig. 2 is a top view of a prior art ring quad.

Fig. 3 is a side cross-sectional view of the prior art ring quad of Fig. 2.

Fig. 4 is a bottom view of the prior art ring quad of Fig. 2.

Fig. 5 is an pictorial view of the prior art ring quad of Fig. 2.

Fig. 6 is a top view of a ring quad with lower leads.

Fig. 7 is a side cross-sectional view of the ring quad of Fig. 6.

Fig. 8 is a bottom view of a module of four diodes of a ring quad.

Fig. 9 is a top view of the lower lead package of a ring quad.

Fig. 10 is a bottom cross-sectional view of a ring quad.

Fig. 11 is an pictorial view of a ring quad, which does not show the lower lead package.

Fig. 12 is a cross-sectional side view of a ring quad during fabrication.

Fig. 13 is a top view of a ring quad during fabrication.

DETAILED DESCRIPTION

With reference to the drawings, Fig. 1 illustrates an electrical circuit schematic of a prior art ring quad 10 The cathode of diode 12 is electrically connected to the anode of diode 14 via lines 24 and 26. The cathode of diode 14 is electrically connected to the anode of diode 16 via lines 28 and 30. The cathode of diode 16 is electrically connected to the anode of diode 18 via lines 32 and 34. The cathode of diode 18 is electrically connected to the anode of diode 12 via lines 36 and 22.

The ring quad 10 shown in Fig. 1 can be used in a double-balanced mixer. Flying leads 21, 23, 25, and 27 connect to circuitry 10 at points 11, 13, 15, and 17, respectively. Flying leads 21, 23, 25, and 27 connect to other circuitry (not shown) that uses ring quad 10 in a well-known manner. Such other circuitry could include coupling transistors (not shown), for example.

Good balance is a desirable characteristic of a mixer. To get good balance, the capacitance of each diode in the mixer should be approximately equal. In addition, the inductance of each diode in the mixer should be approximately equal. In other words, the capacitances of diodes 12, 14, 16, and 18 should approximately be equal. In addition, the inductances of diodes 12, 14, 16, and 18 should be approximately equal.

In an early prior art ring quads, wires were used as lines 24, 26, 28, 30, 32, 34, 36, 22, 21, 23, 25, and 27 to provide respective connections to diodes 12, 14, 16, and 18. Such prior art ring quads with wires often exhibited high capacitance, high inductance, and poor balance.

Fig. 2 is the top view of prior art ring quad 50 with beam leads 51, 53, 55 and 57. Beam leads 51, 53, 55, and 57 act as the flying leads for ring quad 50. In packaging prior art ring quad 50, ring quad 50 is turned upside down and beam leads 51, 53, 55, and 57 are welded to respective leads of a lead package (not shown). Ring quad 50 and the lead package (not shown) can be epoxy encapsulated or placed in a ceramic package.

Blocks 52, 54, 56, and 58 are the four diodes of ring quad 50. Diodes 52, 54, 56, and 58 are each Schottky-barrier diodes. For diode 52, a metal-semiconductor junction lies under anode 79. Metal bridge 71 connects anode 79 to cathode 63. Cathode 63 is a well or depression in which metal reaches down to contact a layer of N^+ type silicon. Similarly, metal bridge 73 connects anode 81 with cathode 65 of diode 56. Metal bridge 75 connects anode 83 of diode 56 to cathode 67 of diode 58. Likewise, metal bridge 77 connects anode 85 of diode 58 to cathode 61 of diode 52.

A thin layer of glass 59 structurally holds ring quad 50 together. That is, glass 59 holds diodes 52, 54, 56, and 58 together. Leads 51, 53, 55, and 57 reside above glass 59. In other prior art ring quads (not shown), the glass holding the diodes together (i.e., the glass corresponding to glass 59) extends beyond the outer perimeter of the diodes (i.e., extends beyond the outer perimeter or edges of the diodes corresponding to diodes 52, 54, 56, and 58).

In prior art ring quad 50, diode block 52 has to be large enough to support flying beam lead 51. Likewise, diode blocks 54, 56, and 58 must

be large enough to structurally support respective beam leads 53, 55, and 57.

Fig. 3 is a cross-sectional side view of ring quad 50 of Fig. 2 taken along line 3-3 of Fig. 2. In Fig. 3, it can be seen that beam lead 57, cathode 67, and bridge 75 are one piece of metal. At anode 83, a metal-semiconductor junction is formed between Schottky-barrier metal layer 103 and N^- type silicon layer 99. The metal can be titanium, for example. Bridge 75 connects anode 83 with cathode 67. Cathode 67 is comprised of an ohmic contact metal layer with a layer 68 of gold on the top. The metal can be titanium, for example. The metal of cathode 67 contacts from the top surface to layer 91 of N^+ type silicon by contacting down into a well or depression, as shown in Fig. 3. The metal outside of the well or depression of cathode 67 becomes lead 57 or bridge 75. Layer 93 is a layer of N^- type silicon above layer 91. Layer 95 is a oxide layer above layer 95.

Likewise, for diode block 56, cathode 65 is comprised of an ohmic contact metal layer with a layer 66 of gold on top. The metal can be titanium, for example. The metal of cathode 65 contacts from the top surface to layer 97 of N^+ type silicon by contacting down into a well or depression, as shown in Fig. 3. The metal outside of the well or depression of cathode 65 becomes lead 55. Layer 99 is a layer of N^- type silicon above layer 97. Layer 101 is a layer of oxide above layer 99.

Layer 59 is a thin layer of glass holding diode blocks 52, 54, 56, and 58 together. Glass layer 59 is typically 18-20 microns thick or approximately two-thirds of a mil thick. The metal leads, including lead 57, are typically about one-half of mil thick. The spacing between the

diode blocks, including diode blocks 56 and 58, is typically about 3.5 mils. The combined depth of layers 99 and 97 is typically 2.5 mils.

Fig. 4 is the bottom view of prior art ring quad 50 shown in Fig. 2. Again, diode blocks 54, 52, 58, and 56 are held together by glass 59. Leads 51, 57, 55, and 53 can be seen in part in Fig. 4. Bridges 71, 77, 75, and 73 reside on the other side of glass 59.

Fig. 5 is an pictorial view of prior art ring quad 50 of Fig. 2. As shown in Fig. 5, the flying beam leads 51, 53, 55, and 57 as well as the metal bridges 71, 73, 75, and 77 all reside on the top of ring quad 50. Thus flying leads 51, 53, 55, and 57, together with interconnections 71, 73, 75, and 77, substantially reside in a two dimensional plane, or, in other words, in two-space. Moreover, the connection of the flying leads 51, 53, 55, and 57 to diodes 52, 54, 56, and 58 of prior art ring quad 50 is quite similar to the way flying leads 21, 23, 25, and 27 are connected to diodes 12, 14, 16, and 18 of prior art ring quad 10 of Fig. 1.

Because flying leads 51, 53, 55, and 57, together with interconnections 71, 73, 75, and 77, approximately reside in a two-dimensional plane, power is not dissipated throughout the full three-dimensional volume of each diode. In other words, power is dissipated across a portion of each diode of prior art ring quad 50 rather than fully through each diode. This is especially the case if a signal has a fast rise time, because there is not enough time for the energy to dissipate throughout the entire volume of diodes 52, 54, 56, and 58 of prior art ring quad 50.

Moreover, given that connections 51, 53, 55, and 57 are made only to the tops of the diodes and that cathode/anode pairs 61/79, 63/81,

65/83, and 67/85 reside relatively close together, pulse transients can sometimes result in carbon trails reaching or jumping from the cathodes to the anodes. Such carbon trails can destroy the cathode/anode topography of prior art ring quad 50.

As seen in Fig. 5, each of the diode blocks 52, 54, 56, and 58 has an upper oxide layer, a middle N^- type silicon layer, and a lower N^+ type silicon layer. Diode block 52 has an upper oxide layer 125, a middle N^- type silicon layer 123, and a lower N^+ type silicon layer 121. Diode block 54 has an upper oxide layer 131, a middle N^- type silicon layer 129, and lower N^+ type silicon layer 127. Diode block 56 has an upper oxide layer 101, a middle N^- type silicon layer 99, and a lower N^+ type silicon layer 97. Diode block 58 has a upper oxide layer 95, a middle N^- type 93, and a lower N^+ silicon layer 91.

Cathode wells 61, 63, 65, and 67 are shown in Fig. 5 extending down to respective N^+ layers 121, 127, 97, and 91. Leads 51, 53, 55, and 57 each have a semicircular indentation around anodes 59, 81, 83, and 85. This semicircular indentation or curvature allows the cathode to be close to the anode and at the same time helps to reduce the Faraday effects that result from sharp edges.

Glass 59 resides in a well, or etched pit, in diode blocks 52, 54, 56, and 58.

In fabricating prior art ring quad 50, an oxide layer is first formed on top of a thick wafer of silicon. The silicon has an N^- type layer below the oxide and a N^+ type layer below the N^- layer. A mask, or pattern, is then applied to the front oxide layer. The oxide is then etched away according to the pattern. A relatively large area is etched to provide a

location for glass. Oxide islands or mesas are left after the etching process. Glass fill is applied. The glass is heated and flows across the top of the ring quad and resides in the etched areas for the glass.

Deep etches are made into the silicon to form cathode wells. Smaller openings are etched through the oxide to form anodes.

A first layer of metal is deposited by metal deposition in a high-vacuum system to the top of the wafer. A second layer of metal is then deposited by metal deposition in a high-vacuum system over the first layer of metal. The first layer of metal can be titanium, for example, and the second upper layer of metal can be gold.

The first layer of metal enters the cathode wells or depressions during deposition such that the first layer of metal contacts the N^+ layer of silicon to form cathodes. The first layer of metal also enters the anode openings during deposition such that the first layer of metal contacts the N^- layer of silicon to form anodes. The first layer of metal in the anode openings acts as the metal-semiconductor injunction for each of the anodes.

A plate, lead, and bridge structure is defined on the top of the silicon wafer by using common masking and metal etching techniques. The plates, leads, and bridges are defined such that metal runs out of cathodes 61, 63, 65, and 67 to form respective leads 51, 53, 55, and 57 and bridges 71, 73, 75, and 77.

The silicon wafer is then etched from behind in order to form diode blocks 52, 54, 56, and 58. In order to package the prior art ring quad, the prior art ring quad is turned upside down and beam leads 51, 53, 55, and 57 are welded to respective leads of a lead package (not shown). Ring

quad 50 and the lead package (not shown) can be epoxy encapsulated or placed in a ceramic package.

Beam leads 51, 53, 55, and 57 of prior art ring quad 50 do not always seat properly during packaging. The relatively large beam leads 51, 53, 55, and 57 are also prone to bending, resulting in capacitance, inductance, and balance problems. Resistance problems can also arise from the welding operation.

Prior art ring quad 50 can be fragile given (1) that a relatively thin layer of glass 59 is used to hold the four diodes 52, 54, 56, and 58 together and (2) that the flying beam leads 51, 53, 55, and 57 present a relatively large lever arm to the top of ring quad 50.

Figure 6 illustrates a top view of ring quad 140, ring quad 140 being a preferred embodiment of the present invention. Ring quad 140 is comprised of diode blocks 142, 144, 146, and 148 surrounded on the sides by glass 180. Metal bridge lead 173 connects lead 165 and cathode 282 of diode 142 to anode 183 of diode 144. Metal bridge lead 175 connects lead 167 and cathode 284 of diode 144 to anode 185 of diode 146. Metal bridge lead 177 connects lead 169 and cathode 286 of diode 146 to anode 187 of diode 148. Metal bridge lead 179 connects lead 171 and cathode 288 of diode 148 to anode 181 of diode 142.

Diode blocks 142, 144, 146, and 148, glass 180, and interconnection leads 165, 173, 167, 175, 169, 177, 171, and 179 comprise module 182, also referred to as ring quad module 182.

Ring quad 140 can be used in a double-balanced mixer.

In contrast to prior art ring quad 50, solid package leads 141, 143, 145, and 147 of ring quad 140 are located underneath respective diode

blocks 142, 144, 146, and 148 after leads 141, 143, 145, and 147 are attached (i.e., welded) to diode blocks 142, 144, 146, and 148.

Metal leads 141, 143, 145, and 147 are part of bottom lead package 159. Lead 141 rises above sector 157 of metal. Lead 143 rises above sector 151 of metal. Lead 145 rises above sector 153 of metal. Lead 147 rises above sector 155 of metal. Said sectors of metal are separated by two channels: channels 161 and 163. Beneath channels 161 and 163 lies epoxy or ceramic, which also underlies sectors 150, 151, 153, 155, and 157.

As illustrated in Fig. 6, lead 141 is soldered or epoxied to the bottom metalized portion of diode block 142. Lead 143 is soldered or epoxied to the bottom metalized portion of diode block 144. Lead 145 is soldered or epoxied to the bottom metalized portion of diode block 146. Lead 147 is soldered or epoxied to the bottom metalized portion of diode block 148.

In a preferred embodiment of the present invention, each of diodes 142, 144, 146 and 148 is a Schottky-barrier type diode.

Fig. 7 is a cross-sectional side view of ring quad 140 taken along line 7-7 of Fig. 6. As shown in Fig. 7, metal bridge 173 and lead 165 are part of the metal that connects cathode 221 to anode 183. Cathode 221 is comprised of an ohmic contact metal layer with a layer 222 of gold on the top. The metal can be titanium, for example. The gold layer 222 inhibits the oxidation of the contact metal of cathode 221. The metal of cathode 221 contacts from the top surface to layer 201 of the N^+ type silicon by contacting down into a well or depression, as shown in Fig. 7.

Diode block 142 also includes an upper oxide layer 205, a middle layer 203 of N^- type silicon, and a lower layer 201 of N^+ type silicon. Diode block 142 includes layer 172 of metal that provides a contact between layer 201 of N^+ type silicon and lead 141. The metal can be Nichrome-gold, for example.

Anode 183 includes layer 276 of Schottky-barrier metal that contacts layer 211 of N^- type silicon. The Schottky-barrier metal can be titanium, for example. There thus is a metal-semiconductor junction between layer 276 of Schottky-barrier metal and layer 211 of N^- type silicon.

Air bridge 215 is formed under metal bridge 173 to keep bridge 173 from contacting oxide layer 213. Air bridge 215 is also referred to as air gap 215.

As can be seen in Fig. 7, diode block 144 has an upper oxide layer 213, a middle N^- type silicon layer 211, and a lower layer 209 of N^+ type silicon. Layer 174 is a layer of contact metal. The contact metal can be Nichrome-gold, for example. The contact metal layer 174 means that silicon block 144 is metalized on the bottom. This ensures good contact with lead 143.

Cathode 223 is comprised of an ohmic contact metal layer with a layer 224 of gold on the top. The metal can be titanium, for example. The gold layer 224 inhibits the oxidation of the contact metal of cathode 223. The metal of cathode 223 contacts from the top surface to layer 209 of the N^+ type silicon by contacting down into a well or depression, as shown in Fig. 7.

As can be seen from Fig. 7, glass 180 surrounds diode blocks 142 and 144, and acts to hold together diode blocks 142 and 144. Glass 180 forms the outer perimeter of module 182. In a preferred embodiment of the present invention, module 182 is approximately 2.5 to 3 mils thick. As shown in Fig. 7, glass 180 is as thick as the combined thickness of layers 205, 203, 201, and 172. It is to be understood, however, that in alternative embodiments of the present invention, glass 180 can have a different thickness. For example, glass 180 could be one-half as thick as the combined thickness of layers 205, 203, 201, and 172.

As shown in Fig. 7, lead 141 rises above metal sector 157 of lower lead package 159. Metal section 157 lies on top of ceramic or epoxy layer 160, which forms the lower layer of lower lead package 159.

Empty channel 161 lies underneath the central portion of glass 180.

Lead 143 rises above metal sector 151. Metal sector 151, in turn, lies on top of ceramic or epoxy layer 160.

Fig. 8 is a bottom view of module 182. The bottom metalized portions of diode blocks 142, 144, 146, and 148 are visible. Glass 180 surrounds diode blocks 142, 144, 146, and 148. Metal bridges 173, 175, 177, and 179 are on the other side of glass 180.

Fig. 9 illustrates the top view of lead package 159 without module 182. Leads 141, 143, 145, and 147 lie in respectives sectors 157, 151, 153, and 155. Channels 161 and 163 criss-cross bottom lead package 159

Fig. 10 is bottom cross-sectional view of ring quad 140 taken along line 10-10 shown in Fig. 7. Fig. 10 shows leads 141, 143, 145, and

147 contacting module 182, but does not show the remainder of bottom lead package 159. Lead 141 is soldered or epoxied to the lower metalized portion of diode block 142. Lead 143 is soldered or epoxied to the lower metalized portion of diode block 144. Lead 145 is soldered or epoxied to the lower metalized portion of diode block 146. Lead 147 is soldered or epoxied to the lower metalized portion of diode block 148. Metal bridges 173, 175, 177, and 179 lie on the other side of glass 180.

Fig. 11 is a pictorial view of module 182 of ring quad 140. Bottom lead package 159 is not shown in Fig. 11.

Fig. 11 shows that each diode block 142, 144, 146, and 148 has three principal layers. Diode block 142 has an oxide layer 205, an N^- type silicon layer 203, and an N^+ type silicon layer 201. Diode block 142 also has a metalized layer 172 below layer 201. Diode block 144 has an upper oxide layer 213, a middle layer 211 comprised of N^- type silicon, and a lower layer 209 comprised of N^+ type silicon. A metalized layer 174 coats the bottom of the N^+ type silicon layer 209. Diode block 146 has an upper oxide layer 261, a middle N^- type silicon layer 259, and a lower layer 257 of N^+ type silicon. A metalized layer 274 coats the bottom portion of layer 257. Diode block 148 has an upper oxide layer 255, a middle layer 253 of N^- type silicon and a lower layer 251 of N^+ type silicon. In addition, a metalized layer 272 lies below layer 251. Metalized layers 172, 174, 274, and 272 can be comprised of Nichrome-gold, for example, and act as ohmic contacts.

As can be seen in Fig. 11, metal bridge 173 connects lead 165 and cathode 282 to anode 183. Metal bridge 175 connects lead 167 and cathode 284 to anode 185 of diode 146. Metal bridge 177 connects lead

169 and cathode 286 of diode 146 with anode 187 of diode 148. Metal bridge 179 connects lead 171 and cathode 288 of diode 148 with anode 181 of diode 142.

Layer 292 comprised of Schottky-barrier metal is shown in Fig. 11 with respect to anode 185 of diode block 146. As can be seen in Fig. 11, the interconnections between the cathodes and anodes of diodes 142, 144, 146, and 148 lie on the top of module of 182. As noted with respect to Fig. 10, however, leads 141, 143, 145, and 147 connect to the bottoms of the diodes of of module 182 of ring quad 140. This means that power dissipates from top to bottom through diode chips 142, 144, 146,and 148. In other words, for ring quad 140 there are three degrees of freedom for power dissipation because energy spreads through the chips to leads 141, 143, 145, and 147 rather than merely across the chips in a horizontal direction. Stated another way, the energy dissipates vertically through the chips rather than horizontally across the chips. This results in good power dissipation characteristics for ring quad 140.

The lower-lead configuration of ring quad 140 also helps to avoid the destruction of the small cathode/anode topography from carbon trails from pulse transients. Destructive carbon trails are less likely on ring quad 140 given that external connections are made to the bottoms of diodes and that interconnections between cathodes and anodes are made on the tops of the diodes of ring quad 140.

Leads 165, 167, 169, and 171 each have a semicircular portion next to respective anodes 181, 183, 185, and 187. This allows the anode to be close to the cathode and at the same time helps to reduce the Faraday effects that result from sharp edges.

Ring quad 140 allows for smaller geometries and high wafer packaging density given that diode blocks 142, 144, 146, and 148 do not have flying leads. Instead leads 141, 143, 145, and 147 are in a secondary package assembly 159 (shown in Fig. 9). Therefore, diode blocks 142, 144, 146, and 148 can be smaller because they do not have flying leads on their tops. Smaller diode blocks mean small geometries -- that is, more ring quads per silicon wafer.

Module 182 is not fragile given that glass 180 surrounds diode blocks 142, 144, 146, and 148 and can be as thick as said diode blocks, as shown in Fig. 11. Ring quad 140 is also less prone to beam lead bending given that leads 141, 143, 145, and 147 are an inherent part of bottom lead package 159 rather than on the top of module 182. In an alternative embodiment, glass 180 can be any thickness.

Ring quad 140 can be used as part of doubly double-balanced mixer. A doubly double-balanced mixer is comprised of eight diodes. A doubly double-balanced mixer can be formed by wiring together two ring quads. Such interconnection is known as a "double star" interconnection and is done in three-space with eight leads. Using two ring quads 140 in a doubly double balanced mixer simplifies the interconnection between the diodes because each ring quad 140 has leads on both the front and the back of diode blocks 142, 144, 146, and 148.

Figs. 12 and 13 illustrate partially formed module 182 of ring quad 140 during the fabrication process. The fabrication process starts with a wafer of silicon with an N^- type layer on the top and an N^+ type layer on the bottom. An oxide layer is first formed on top of the silicon wafer. The photolithography process is then used to form a plurality of wells by

etching through the oxide and the N^- layer of the silicon to the N^+ layer of the silicon for each well. In the photolithography process, a pattern or mask is used to decide which areas are to be etched and which areas are not to be etched. The wells that are etched are to be used for the cathodes of diode blocks 142, 144, 146, and 148. The wells are thus formed by a pit etch process. Next, the oxide and silicon layers are etched or sawed into a plurality of mesa-like structures (also referred to as mesas) that ultimately become the diode blocks.

Referring to Fig. 12, the silicon wafer used in the fabrication process is shown as wafer 301. Wafer 301 is approximately 10 to 12 mils thick, which the combined distance 325 and 321.

When the oxide and silicon is etched or sawed to form diode blocks 142, 144, 146, and 148, it reaches to a depth 325 as shown in Fig. 12. Depth 325 is approximately 2.5 to 3 mils. The saw or etchant penetrates to line 309 in Fig. 12. Channels 305, 306, and 307 are formed by an etch or sawing process. At this stage in the fabrication process, however, glass 180 has not yet been applied. After the sawing or etching occurs, each mesa or nascent diode block has a plurality of empty channels bordering that mesa, with silicon in the bottom of each channel. For example, mesa 331 in Fig. 12 is bordered by channels 305 and 306. Mesa 333 is bordered by channels 306 and 307. Given the channels 305, 306, and 307 only have a depth 325, it follows that the silicon of silicon wafer 301 underlies channels 305, 306, and 307.

Each mesa or nascent diode block is approximately 2.5 to 3 mils thick, which means that depth 325 is approximately 2.5 to 3 mils.

Each mesa has an upper oxide layer, a middle N^- type silicon layer, a lower N^+ type silicon layer, and a well. For example, mesa 331 (i.e., nascent diode block 331) has an upper oxide layer 310, a middle N^- type silicon layer 312 and a lower N^+ type silicon layer 314. Mesa 333 has an upper oxide layer 310, a middle N^- type silicon layer 312, and a lower N^+ type silicon layer 314. Diode blocks 331 and 333 also each have a well formed by the photolithography process referred to above (the wells are not shown in Fig. 12). In Fig. 13, well 491 is formed in mesa 442, well 493 is formed in mesa 444, well 495 is formed in mesa 446, and well 497 is formed in mesa 448.

The channels formed by etching or sawing are then filled with glass. Thus, channels 305, 306, and 307 shown in Fig. 12 are filled with glass 180.

A plurality of openings are then formed through the oxide layer to the N^- layer. The openings are for the anode contacts. Each mesa or nascent diode block gets one opening for the anode. The anode openings are formed by etching as part of the photolithography process. Each opening is a hole approximately 4 to 12 microns in diameter. In Fig. 13, anode opening 481 is formed in mesa 442, anode opening 483 is formed in mesa 444, anode opening 485 is formed in mesa 446, and anode opening 487 is formed in mesa 448.

Areas 421, 423, 425, and 427 of photoresist are applied to the top of the mesas and glass, as shown in Fig. 13. The areas of photoresist are used to form the air bridges described above, including air bridge 215 described with respect to Fig. 7.

A first layer of metal is deposited by metal deposition in a high-vacuum system to top 300 of wafer 301 of Fig. 12. A second layer of metal is then deposited by metal deposition in a high-vacuum system over the first layer of metal on top 300 of wafer 301 of Fig. 12. In a preferred embodiment of the present invention, the first layer of metal is titanium. The first layer of metal is also referred to as the contact metal. In a preferred embodiment of the present invention, the second layer of metal is gold. The layer of gold helps to inhibit or prevent the oxidation of the titanium.

The first layer of metal enters the cathode wells or depressions during deposition such that the first layer of metal contacts the N^+ layer of silicon to form cathodes. The first layer of metal also enters the anode openings during deposition such that the first layer of metal contacts the N^- layer of silicon to form anodes. The first layer of metal in the anode openings acts as the metal for the metal-semiconductor junction for each of the anodes of mesas 442, 444, 446, and 448 of Fig. 13.

A plate or lead structure is then defined on top 300 of silicon wafer 301 of Fig. 12 by using masking and metal etching techniques common to the semiconductor industry. Metal plates or leads are so defined that metal plates or leads connect (1) anode 481 of mesa 442 shown in Fig. 13 to cathode 497 of mesa 448, (2) anode 483 of mesa 444 to cathode 491 of mesa 442, (3) anode 485 of mesa 446 to cathode 493 of mesa 444, and (4) anode 487 of mesa 448 to cathode 495 of mesa 446. It follows from the discussion above that said plates or leads are comprised of a lower first layer of metal and an upper second layer of metal. Again,

in a preferred embodiment of the present invention, the first layer of metal is titanium, and the second layer of metal is gold.

The photoresist in areas 421, 423, 425, and 427 shown in Fig. 13 is then removed to form air bridges in areas 421, 423, 425, and 427 under the leads or plates connecting said anodes and cathodes. In an alternative embodiment of the invention, the photoresist is not removed. Rather, the photoresist is left in place to act as a photoresist bridge.

Central channels are then cut through selected ones of the glass-filled channels in order to form a module that includes four mesas or diode blocks forming a substantially square pattern. In Fig. 12, the central channel is cut through channels 305 and 307, but not through channel 306. Thus glass 180 remains to the left and right sides of channel 305 and to the left and right sides of 307. The result is that mesas 331 and 333 are surrounded by glass 180. As shown in Fig. 13, mesas 442, 444, 446 and 448 are surrounded by glass 480.

Referring to Fig. 12, silicon wafer 300 with mesas 331 and 333 is then sandblasted and etched from the back to remove the back silicon up to line 309. In other words, the depth of silicon indicated by length 321 in Fig. 12 is removed by sandblasting and etching. The sandblasting and etching ends once glass 180 is reached. In an alternative embodiment of the present invention, silicon wafer 300 can be back lapped.

Once the back silicon has been removed, then the bottom of module 329 is metalized. In other words, the area indicated by line 309 under module 329 is metalized.

In the preferred metalization process, Nichrome-gold is evaporated to the bottom of module 329, creating an ohmic contact. In

other words, the Nichrome-gold is evaporated onto the area indicated on line 309 under module 329. The Nichrome-gold is then etched away from the glass 180 areas, but not away from the silicon areas 314. In other words, through photomasking and etching, metal land areas are created under area 314 for mesa 331 and area 314 for mesa 333 in order to isolate the silicon regions. Thus the bottom of the N^+ silicon layer of each mesa is metalized. Module 329 is then demounted and tested. Module 329 can be tested from the bottom, or, in other words, from the area indicated by line 309. Given that one can test from the bottom, testing from the top -- using fragile top flying lead beams -- is avoided.

In an alternative embodiments of the present invention Nichrome, nickel, and other metals could be used instead of titanium in the cathodes and anodes of the diode blocks.

In alternative embodiments of the present invention, the N^- region of the diode blocks is referred to as the I region.

After module 329 has been formed and tested, it is then placed on top of bottom lead package 159 shown in Fig. 9 and is aligned as shown in Figs. 10 and 6. In other words, leads 141, 143, 145, and 147 contact respective diode blocks 142, 144, 146, and 148. Module 329 (also referred to as module 182) and bottom lead package 159 are both embedded in black epoxy or attached to metalized ceramic to form a ring quad package. Said package is generally not fragile.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be

made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A ring quad comprising:

a first diode with an anode at a top of the first diode and a cathode;

a second diode with an anode at a top of the second diode and a cathode;

a third diode with an anode at a top of the third diode and a cathode;

a fourth diode with an anode at a top of the fourth diode and a cathode;

a first bridge for coupling a top of the cathode of the first diode to the anode of the second diode, wherein the first bridge runs from the top of the first diode to the top of the second diode;

a second bridge for coupling a top of the cathode of the second diode to the anode of the third diode, wherein the second bridge runs from the top of the second diode to the top of the third diode;

a third bridge for coupling a top of the cathode of the third diode to the anode of the fourth diode, wherein the third bridge runs from the top of the third diode to the top of the fourth diode;

a fourth bridge for coupling a top of the cathode of the fourth diode to the anode of the first diode, wherein the fourth bridge runs from the top of the fourth diode to the top of the first diode;

first connection means coupled to a metalized bottom of the cathode of the first diode;

second connection means coupled to a metalized bottom of the cathode of the second diode;

third connection means coupled to a metalized bottom of the cathode of the third diode; and

fourth connection means coupled to a metalized bottom of the cathode of the fourth diode.

2. The ring quad of claim 1, wherein each of the first, second, third, and fourth diodes is a Schottky-barrier diode.

3. The ring quad of claim 1, wherein the first, second, third, and fourth diodes are surrounded on their sides by glass to form a module.

4. The ring quad of claim 3, wherein each of the first, second, third, and fourth connection means is a beam lead that is part of a lower lead package that is coupled to the module.

5. A method of forming a ring quad that includes four diodes, comprising the steps of:

forming an oxide layer on top of silicon, wherein the silicon has an N^- layer below the oxide and an N^+ layer below the N^- layer;

forming a plurality of wells by etching through the oxide and the N^- layer to the N^+ layer for each well;

cutting the oxide and silicon into a first mesa, a second mesa, a third mesa, and a fourth mesa, with a plurality of empty channels bordering each mesa and silicon under each channel, wherein each mesa has an upper oxide layer, a middle N^- layer, a lower N^+ layer, and at least one of the plurality of wells;

filling the channels with glass;

forming a plurality of openings through the oxide to the N^- layer, wherein each mesa has at least one of the plurality of openings;

forming a plurality of anodes by placing metal into each of the plurality of openings such that the metal contacts the N^- layer;

forming a plurality of cathodes by placing metal into each of the plurality of wells such that the metal contacts the N^+ layer;

coupling the cathode of the first mesa to the anode of the second mesa;

coupling the cathode of the second mesa to the anode of the third mesa;

coupling the cathode of the third mesa to the anode of the fourth mesa;

coupling the cathode of the fourth mesa to the anode of the first mesa;

cutting central channels through a portion of the glass down to the silicon to form a module comprising first, second, third, and fourth mesas of silicon, wherein each of the first through fourth mesas is surrounded on its sides by glass;

removing the silicon up to the bottom of the glass, wherein silicon beneath the module is removed and the first mesa becomes a first diode, the second mesa becomes a second diode, the third mesa becomes a third diode, and the fourth mesa becomes a fourth diode;

metalizing a bottom of the N^+ layer of each diode;

coupling first connection means to the metalized bottom of the N^+ layer of the first diode;

coupling second connection means to the metalized bottom of the N^+ layer of the second diode;

coupling third connection means to the metalized bottom of the N^+ layer of the third diode;

coupling fourth connection means to the metalized bottom of the N^+ layer of the fourth diode.

6. The method of claim 5 for forming a ring quad, wherein the metal used to form the plurality of anodes and cathodes is titanium.

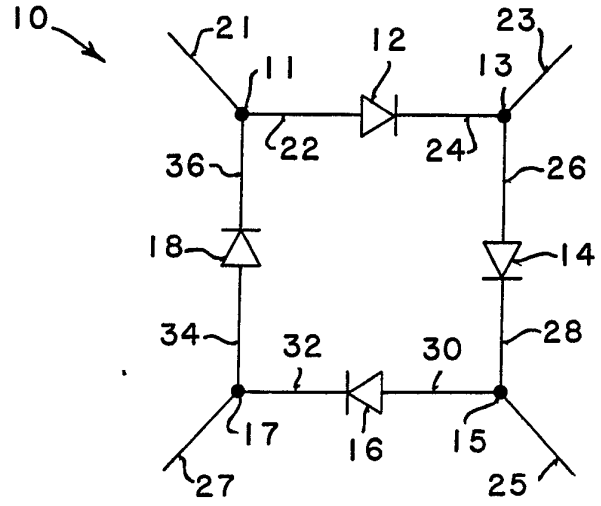
7. The method of claim 5 for forming a ring quad, wherein the metal used to form the plurality of anodes and cathodes is nickel.

8. The method of claim 5 for forming a ring quad, wherein the metal used to form the plurality of anodes and cathodes is Nichrome.

9. The method of claim 5 for forming a ring quad, further comprising the step of coating the metal used to form the plurality of the anodes and cathodes with gold.

10. The method of claim 5 for forming a ring quad, wherein each of the first, second, third, and fourth connection means is a beam lead that is part of a lower lead package.

FIG. 1
(PRIOR ART)



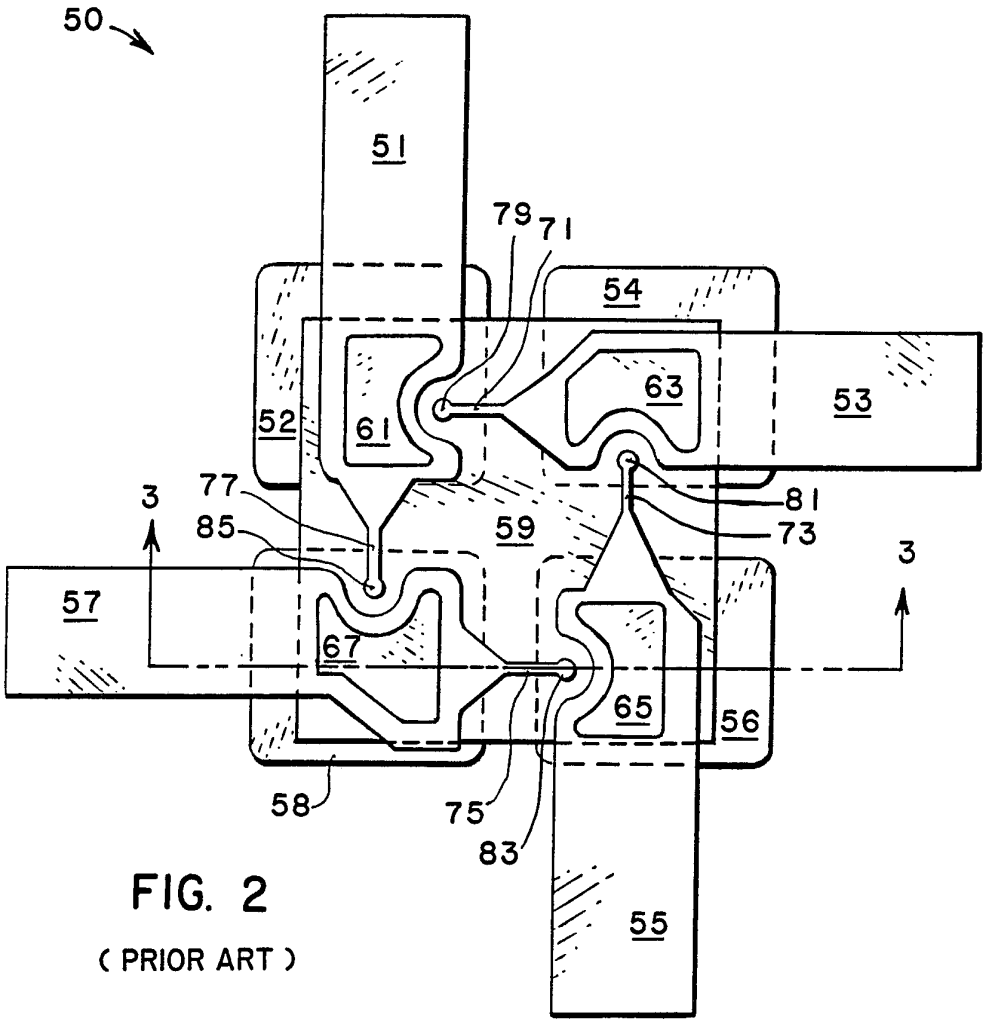


FIG. 2
(PRIOR ART)

FIG. 3
(PRIOR ART)

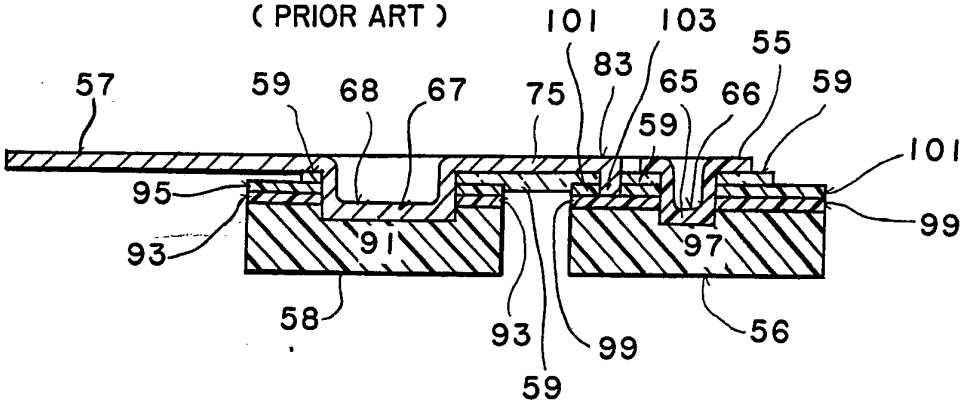
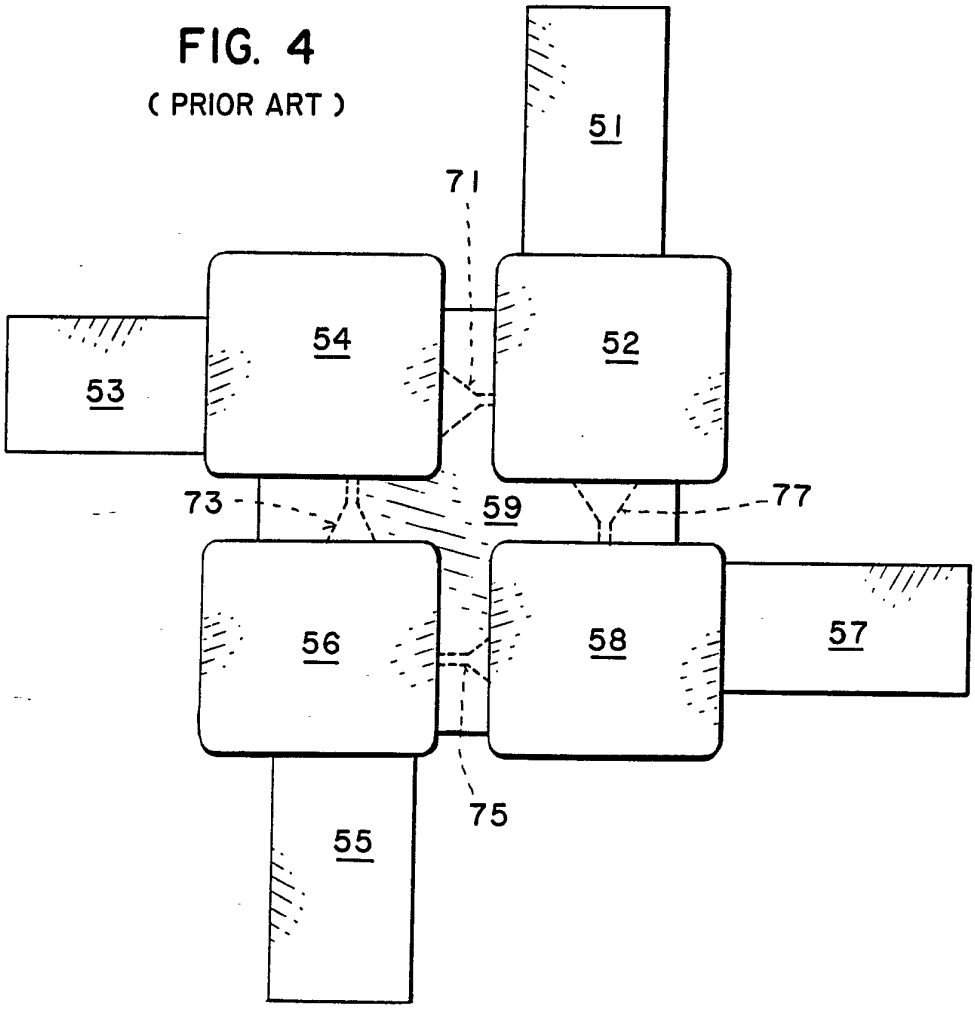


FIG. 4
(PRIOR ART)



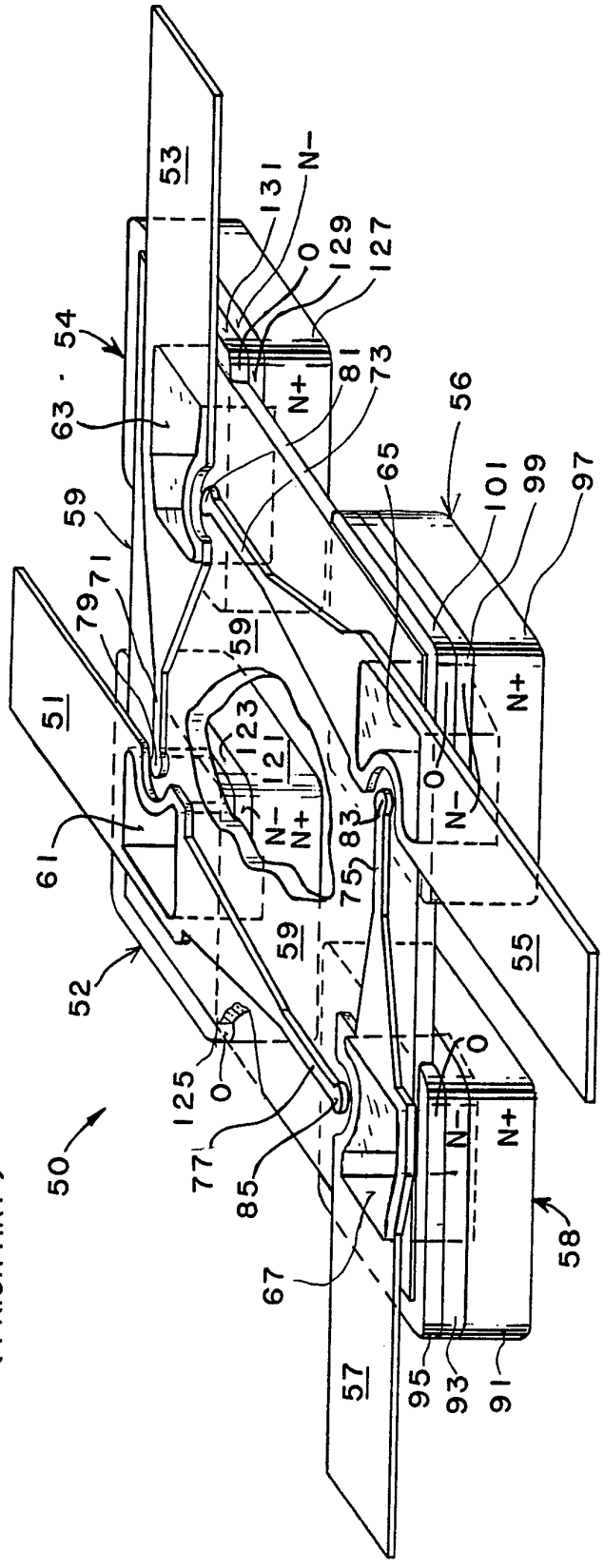


FIG. 5
(PRIOR ART)

FIG. 6

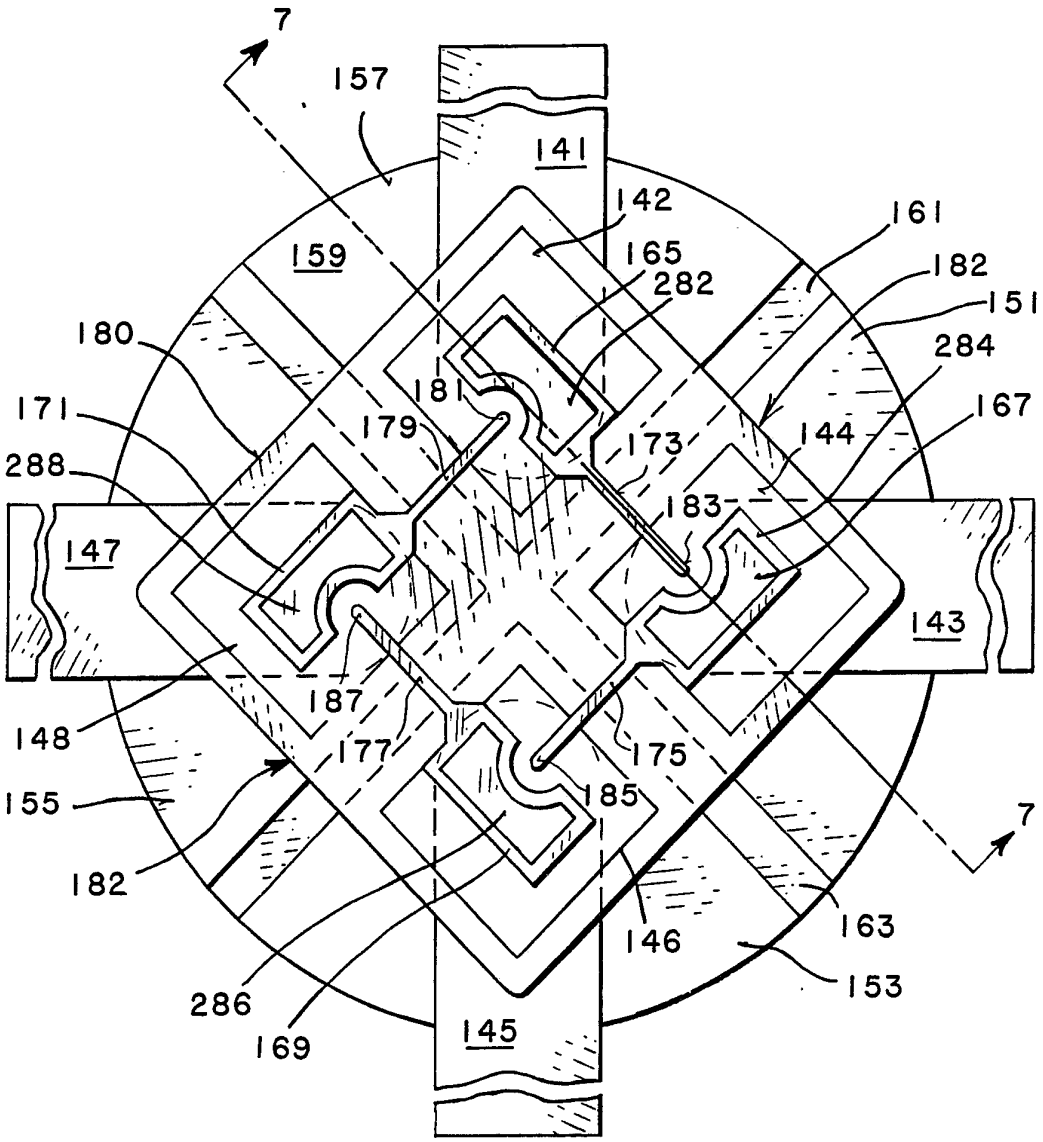

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FIG. 7

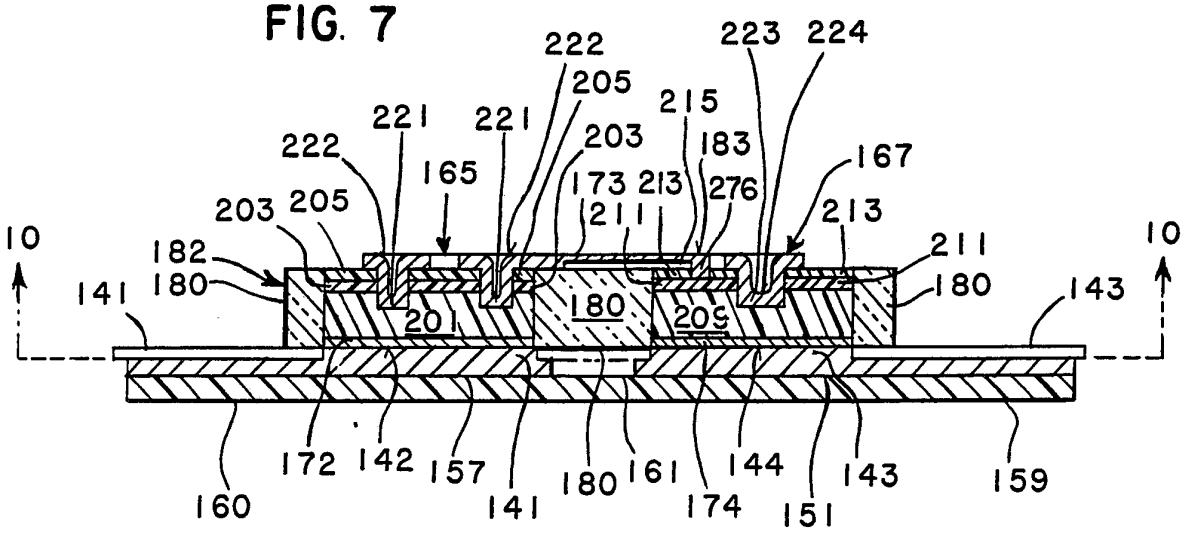
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FIG. 8

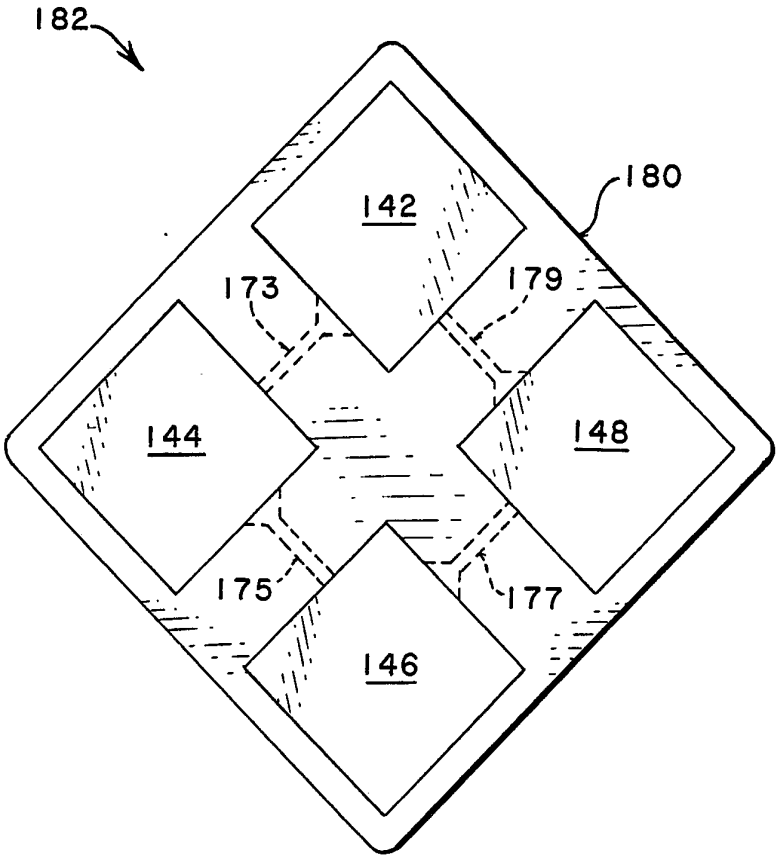
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FIG. 9

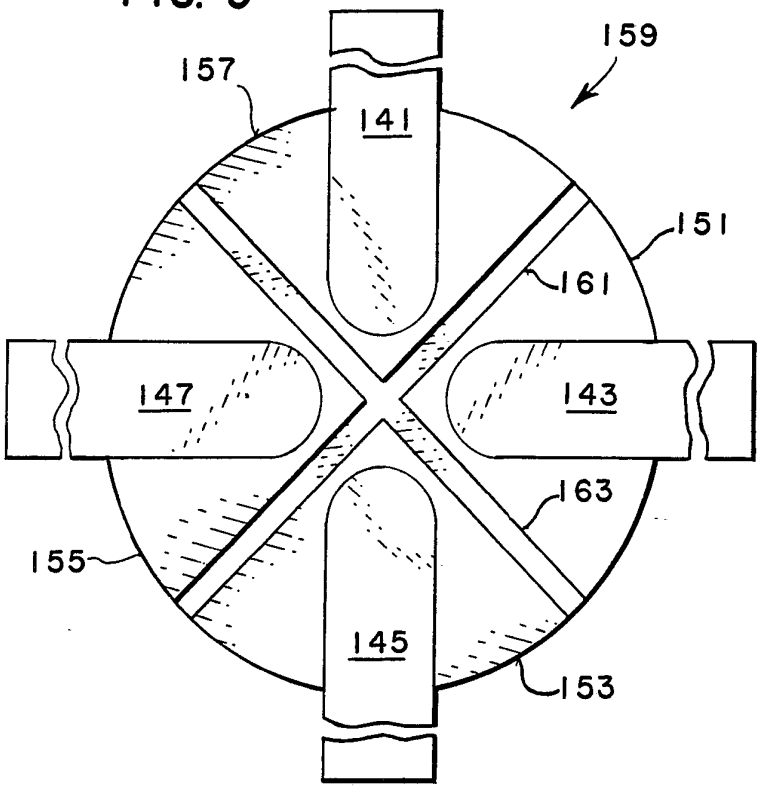
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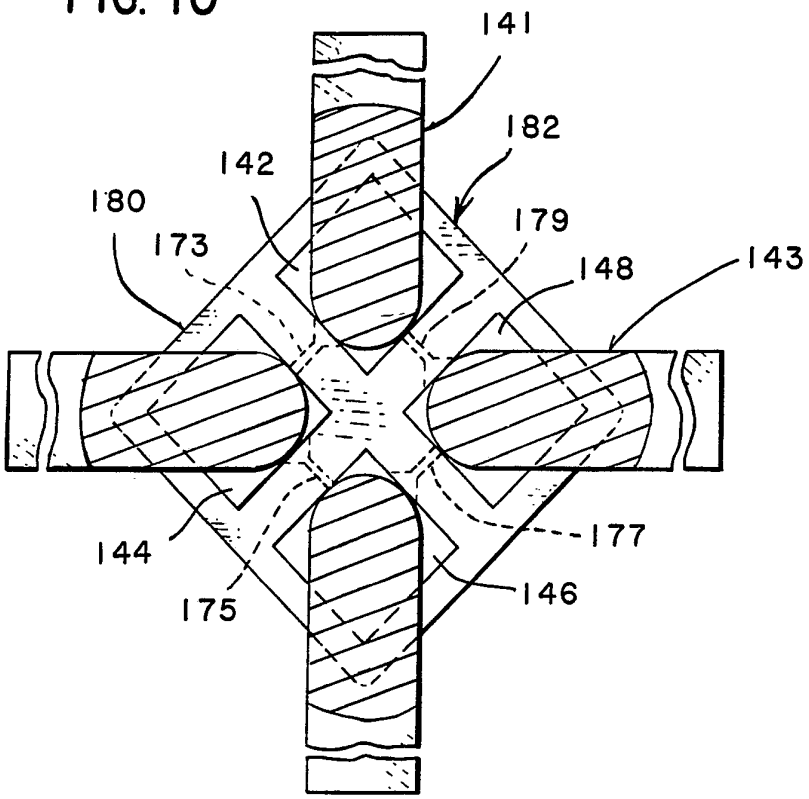
FIG. 10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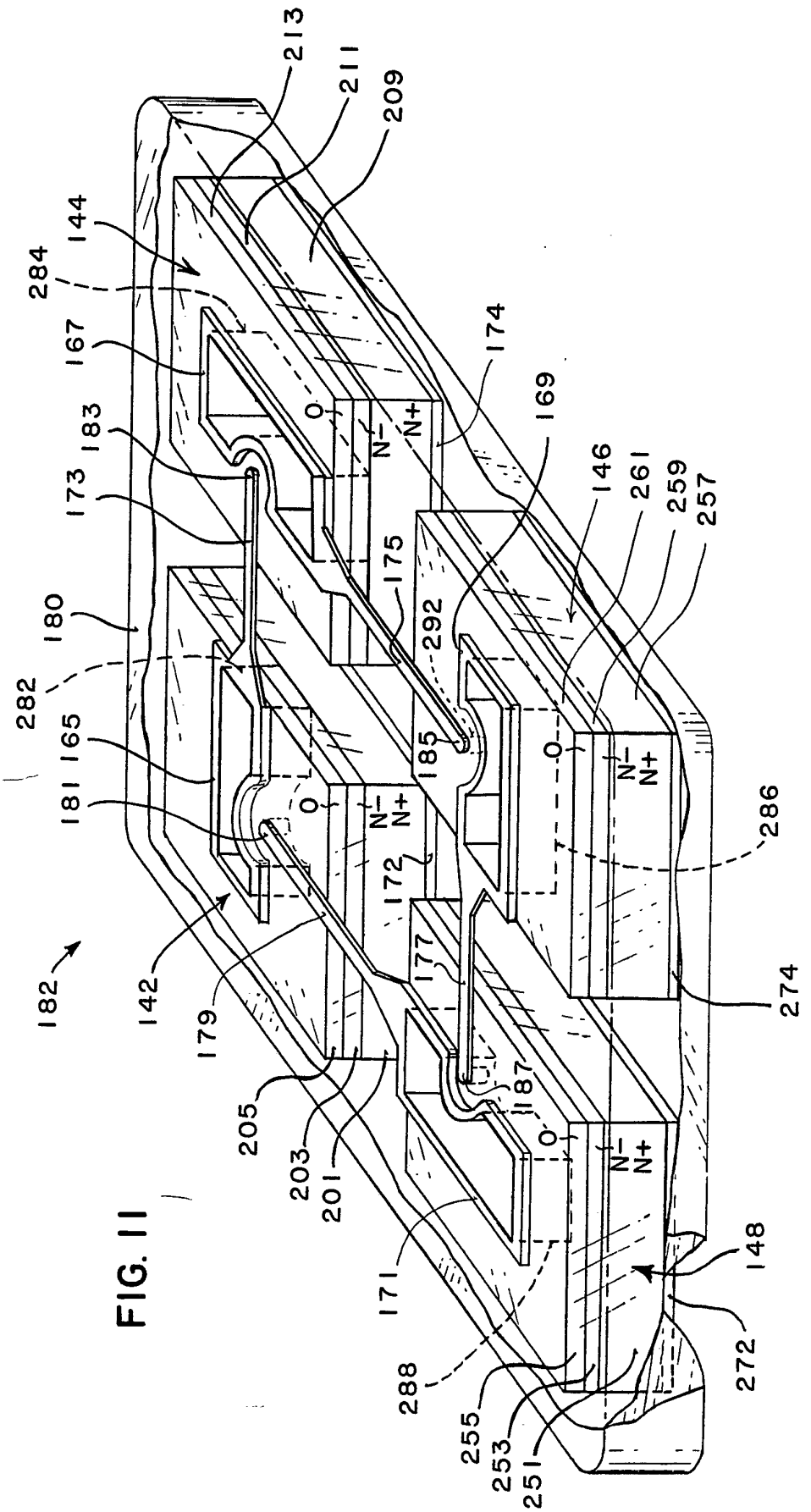
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FIG. 11

FIG. 12

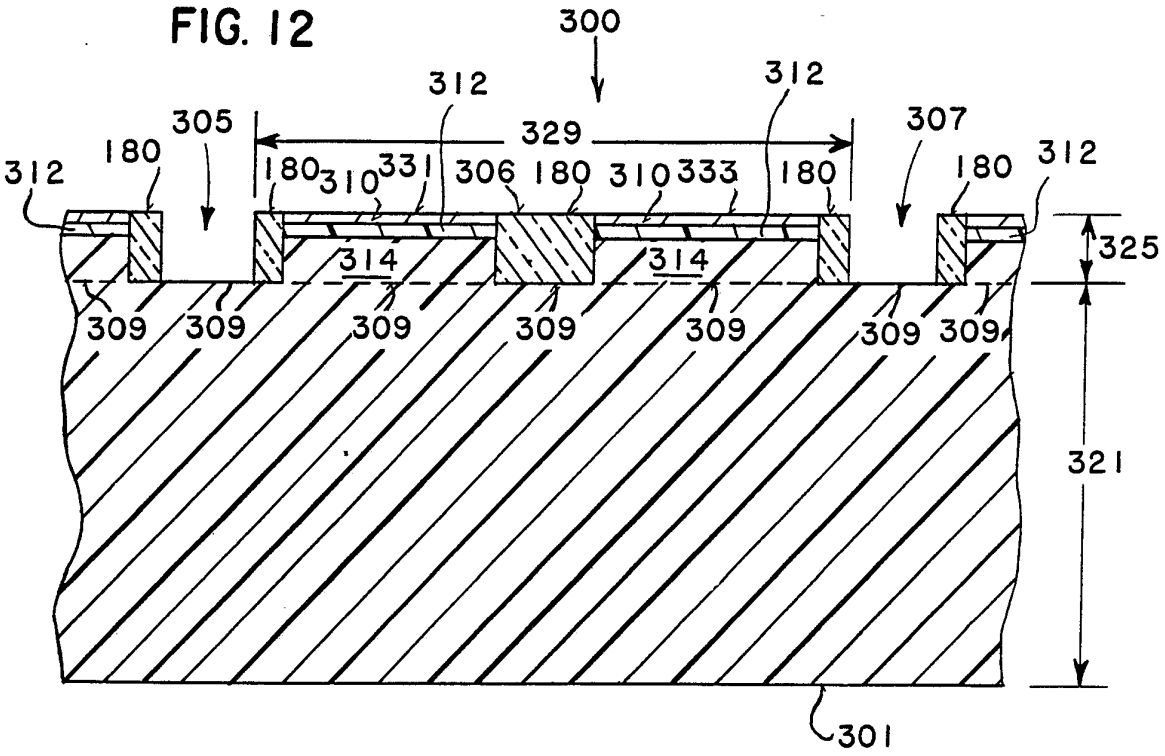
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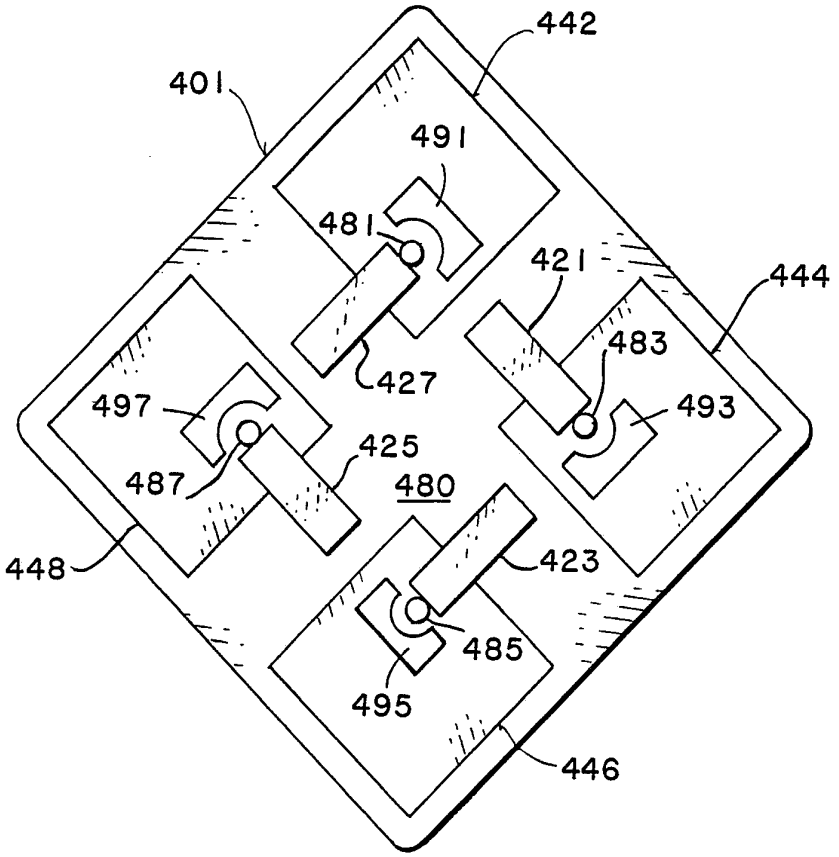
FIG. 13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INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/05243

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): H01L 29/46 29/56, 29/64, 23/48, 29/44, 29/52, 29/60
23/32 US. Cl: 357/15, 69,76

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
US	357/15, 69, 76; 455/326, 332,333; 336/26 437/182, 187, 904

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X, P Y, P	US, A 4,063,176 (Milligan et al.), 13 Dec. 1977, See Fig. 1	1 2-4
Y	US, A 3,820,235 (Guldman), 28 June 1974 Refer to Fig. 6 or Fig. 11	2, 5-9
Y,P	US, A 4,855,796 (Wong et al.), 08 Aug. 1989 Refer to Fig. 1	3, 5-9
Y	EUROPEAN, A 0,057,135 (Vora et al.), 21 Jan 1982 Refer to the claims	5-9

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
17 January 1990	21 MAR 1990
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Andrew Jones

Form PCT/ISA/210 (second sheet) (Rev.11-87)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y	US, A 3,886,578 (Eastwood et al.), 27 May 1975 Refer to Fig. 1.	4,6,9
Y	US, A 4,250,520 (Denlinger), 10 Feb. 1981 Refer to Fig. 1	4
Y	JP, A 56-148848 (Yanase) 18 Nov 1981 Refer to Abstract and Figures' next to abstract	4 4
Y	US, "Modified Beam Lead Magnetics For Handling Semiconductors" (Garceau), July 1978 Refer to pgs 11-12	4
Y	US, A 3,944,447 (Magdo et al.), 16 March 1976 See Fig 1A-1K	3, 5-9
Y,P	US, A 4,859,629 (Reardon et al.) 22 Aug. 1989 See Fig. 16	4