(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 September 2008 (04.09.2008)

PCT

(10) International Publication Number
WO 2008/105854 A1

(51) International Patent Classification:
*G02F 1/025* (2006.01)

(21) International Application Number: PCT/US2007/022945

(22) International Filing Date: 30 October 2007 (30.10.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/681,070 1 March 2007 (01.03.2007) US

(71) Applicant (*for all designated States except US*): **LUCENT TECHNOLOGIES INC.** [US/US]; 600 Mountain Avenue, Murray Hill, NJ 07974-0636 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **GILL, Douglas, M.** [US/US]; 203 Underhill Road, South Orange, NJ 07079 (US). **JONES, Christopher, D W** [CA/US]; 52 Cooper Lane, Millington, NJ 07946 (US). **PATEL, Sanjay, Shantilal** [US/US]; 24 Holmes Oval South, New Providence, NJ 07974 (US). **RASRAS, Mahmoud** [JO/US]; 34 Angela Way, Berkeley Heights, NJ 07922 (US). **WEIMANN, Nils, Guenter** [DE/US]; 35 Gates Avenue, Gillette, NJ 07933 (US).

(74) Agent: **HITT, David, H.**; Lucent Technologies Inc., Docket Administrator-room 2f-190, 600 Mountain Avenue, Murray Hill, NJ 07974-0636 (US).

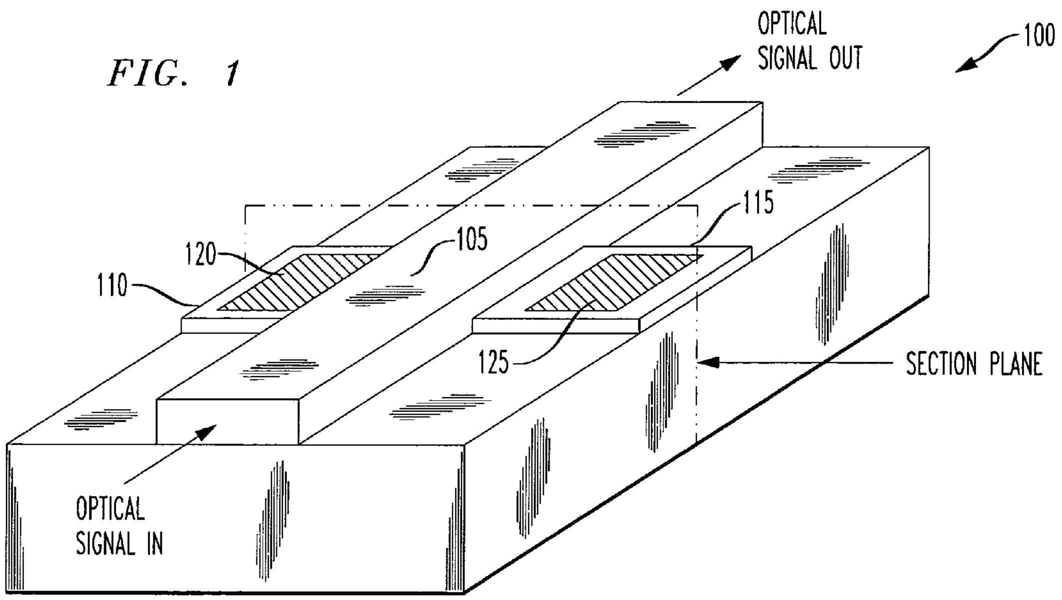
(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

(54) Title: HIGH SPEED SEMICONDUCTOR OPTICAL MODULATOR

*FIG. 1*




(57) Abstract: The present invention provides an optical waveguide modulator. In one embodiment, the optical waveguide modulator includes a semiconductor planar optical waveguide core and doped semiconductor connecting paths located adjacent opposite sides of the core and capable of applying a voltage across the core. The optical waveguide core and connecting paths form a structure having back-to- back PN semiconductor junctions. In another embodiment, the optical waveguide modulator includes a semiconductor optical waveguide core including a ridge portion wherein the ridge portion has at least one PN semiconductor junction located therein. The optical waveguide modulator also includes one or more doped semiconductor connecting paths located laterally adjacent the ridge portion and capable of applying a voltage to the ridge portion.

WO 2008/105854 A1

**Published:**
— *with international search report*

# HIGH SPEED SEMICONDUCTOR OPTICAL MODULATOR

## TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to communication systems and, more specifically, to an optical waveguide modulator and a method of operating an optical waveguide.

## BACKGROUND OF THE INVENTION

Current silicon-based (Si-based) CMOS-compatible electro-optic modulators generally have response bandwidths (*i.e.*, 3dB bandwidths) that are limited to a few gigahertz (GHz), at best. Traditional devices also have uneven responses wherein the time required to activate the device is very different from the time required to deactivate the device. These devices have traditionally relied on carrier injection into the optical waveguide to create effective optical refractive index changes. This requires a voltage bias to be applied to the device, wherein DC power consumption results.

Response speed for these devices is also limited, since carriers have to traverse the entire distance between ohmic contacts of the device in order to activate and deactivate the device. This action occurs because the response speed of the device, in the forward-biased state, is limited by the diffusion speed of the carriers across the intrinsic region of the device. Additionally, current devices have severe bandwidth limitations and incur relatively large optical losses corresponding to changes in their optical refractive index.

Accordingly, what is needed in the art is an enhanced design that overcomes some of the limitations of the current art.

**SUMMARY OF THE INVENTION**

To address the above-discussed deficiencies of the prior art, the present invention provides an optical waveguide modulator. In one embodiment, the optical waveguide modulator includes a semiconductor planar optical waveguide core and doped semiconductor connecting paths located adjacent opposite sides of the core and capable of applying a voltage across the core, wherein the optical waveguide core and connecting paths form a structure having back-to-back PN semiconductor junctions. In another embodiment, the optical waveguide modulator includes a semiconductor optical waveguide core including a ridge portion wherein the ridge portion has at least one PN semiconductor junction located therein. The optical waveguide modulator also includes one or more doped semiconductor connecting paths located laterally adjacent the ridge portion and capable of applying a voltage to the ridge portion.

In another aspect, the present invention provides a method operating a semiconductor planar optical waveguide. The method includes sending an optical signal into a semiconductor optical waveguide core of the waveguide. The method also includes modulating a voltage applied across the width or height of the core such that carrier densities adjacent back-to-back PN semiconductor junctions are modulated while the signal propagates along the core wherein a portion of each PN semiconductor junction is located in the core.

The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

**BRIEF DESCRIPTION OF THE DRAWINGS**

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a pictorial diagram of an optical waveguide modulator constructed according to the principles of the present invention;

FIGURE 2A is a cross-section view of an embodiment of an optical waveguide modulator constructed according to the principles of the present invention, wherein the view shows a simulated hole carrier distribution in the absence of an applied voltage;

FIGURE 2B is a diagram of an electrical equivalent that describes the optical waveguide modulator 200 of FIGURE 2A;

FIGURE 2C provides cross-section views showing simulated modulated hole charge concentrations in the optical waveguide core 205 of FIGURE 2A for various applied voltages;

FIGURE 3A is a diagram of a cross-section view of an alternative embodiment of a semiconductor optical waveguide modulator constructed according to the principles of the present invention.

FIGURE 3B is a diagram of a cross-section view of another embodiment of a semiconductor optical waveguide modulator constructed according to the principles of the present invention;

FIGURE 4A provides cross-section views of an alternative embodiment of an optical waveguide modulator wherein Views A and B show simulated hole and electron carrier distributions in the optical core in the absence of an applied voltage;

FIGURE 4B provides additional cross-section views of the modulator of Figure 4A that show simulations of modulated charge carrier distributions in the optical waveguide core 405 for various applied voltages;

FIGURE 5 is a diagram of a cross-section view of an embodiment of a semiconductor optical waveguide modulator constructed according to the principles of the present invention; and

FIGURE 6 is a flow diagram of a method of operating and optical waveguide carried out according to the principles of the present invention.

**DETAILED DESCRIPTION**

Herein, the various semiconductor structures may be fabricated from various semiconductors, e.g., silicon or compound semiconductors, by conventional micro-fabrication methods.

Herein, the various optical waveguide cores may be covered with one or more top optical cladding layers, e.g., silica glass layers.

Herein, electrodes may be fabricated of metal and or heavily doped semiconductor, e.g., doped polysilicon, by conventional micro-fabrication methods.

Herein, maximum cited concentrations of positive and negative charge carriers provide lower bounds on concentrations of respective p-type and n-type dopants in described semiconductor structures.

Embodiments of the present invention are particularly well suited for high speed, highly integrated, cost effective, large-scale applications of communication systems or subsystems. The CMOS compatibility of this design makes it appropriate for high-volume fabrication. The significant improvement in device response time and nonlinear response makes it suitable for applications in high bit-rate digital communication areas. The nonlinear response of the waveguide may also be used to enhance modulator linearity for analog transmission applications, as well.

Referring initially to FIGURE 1, illustrated is a pictorial diagram of an optical waveguide modulator, generally designated 100, constructed according to the principles of the present invention. The optical waveguide modulator 100 includes a semiconductor optical waveguide core 105 and first and second conductive connecting paths 110, 115, i.e., heavily doped semiconductor paths, that are in contact with first and second electrodes 120, 125, respectively. The semiconductor optical waveguide core is configured to modulate an optical signal traversing the core based on a field activated region within the core. The core provides a field activated region, wherein an applied electrical modulation signal can change the core's refractive index. The electrical modulation signal is applied between the first and second electrodes 120, 125.

The response time of embodiments of the present invention is significantly faster than current technology since charge carriers need to traverse only part way across the distance between ohmic contacts. This improvement occurs since charge transport is predominantly field assisted rather than having to rely on carrier diffusion. Additionally, no DC power consumption is required with embodiments of the new design, thereby offering an improvement in power consumption over current designs.

Embodiments of the present invention may be constructed such that the optical modulation is achieved employing only holes as carriers, rather than a combination of electrons and holes. Employing only holes may significantly reduce the optical loss associated with optical refractive index changes in the waveguide. Since embodiments may employ a physical symmetry and charges essentially do not intermingle, electrical screening issues are avoided thereby allowing charge movement to be field enhanced.

Furthermore, the electro-optic response of the semiconductor optical waveguide modulator 100 is significantly more nonlinear than traditional approaches. For digital applications, the nonlinearity of the response of the semiconductor optical waveguide modulator 100 may be used to mitigate signal degradation due to either transmitter or system bandwidth limitations. For analog applications, the nonlinearity may be used to alleviate modulator nonlinearity thereby resulting in a more linearized modulator response. This feature may be employed to counteract an inherently nonlinear modulator structure resulting from the intrinsic response of a Mach-Zehnder modulator, a ring resonator modulator or a combination of the two, for example.

The semiconductor optical waveguide core 105 may be doped with one type of species (donor or acceptor dopants). In addition, ohmic contacts are constructed proximate the ridged waveguide, which are doped, e.g., with the opposite type of species (acceptor or donor dopants, respectively). This construction provides appreciable charge carriers in the optical waveguide core 105 when there is no voltage bias applied to the device.

A voltage bias may then be applied through the first and second electrodes 120, 125 to modulate the distribution of the charge carriers within the waveguide, which in turn modulates the optical properties of the device. This is achieved with minimal AC power consumption and no DC power consumption. Modulation of the waveguide optical properties may then be used to modulate the optical intensity or phase of the light in the waveguide.

Turning now to FIGURE 2A, illustrated is a cross-section view of an embodiment of a semiconductor optical waveguide modulator, generally designated 200, constructed according to the principles of the present invention. The cross-section view represents a section as may be taken through the center of the optical waveguide modulator 100 as indicated in FIGURE 1. The optical waveguide modulator 200 includes a semiconductor optical waveguide core 205 having a ridge region and first and second heavily doped semiconductor connecting paths 210, 215 that are adjacent opposite sides of the core 205. The modulator 200 also includes first and second electrodes 220, 225 that are in contact with the respective first and second heavily doped semiconductor connecting paths 210, 215.

In the illustrated embodiment, the semiconductor optical waveguide core 205 includes back-to-back PN semiconductor junctions 206, 207 that are located proximate opposite sides of the optical waveguide core 205, as shown. Generally, the back-to-back PN semiconductor junctions may be located more centrally in the optical waveguide core 205 or even positioned asymmetrically in the optical waveguide core 205 as may be deemed advantageous to a particular polarity or charge concentration employed. The back-to-back PN semiconductor junctions 206, 207 are configured to provide a field activated region corresponding to an applied electrical modulation signal.

In the illustrated embodiment, the semiconductor optical waveguide core 205 includes a P-type dopant in a ridge shaped region and the first and second conductive connecting paths 210, 215 include an N-type dopant, located adjacent thereto. However, one skilled in the pertinent art will recognize that other embodiments of the optical waveguide core 205 and the first and second conductive connecting paths 210, 215 may reverse these polarities to include an N-type dopant and a P-type dopant, respectively.

During operation, the optical waveguide core 205 may have a range of charge concentrations in different spatial regions. Figure 2A illustrates a simulated hole charge carrier distribution for a zero voltage bias condition. The charge carrier concentrations shown in the waveguide can range from a concentration of about $3x10^{15}$ charges per cubic centimeter to a concentration of about $1x10^{18}$ charges per cubic centimeter. Substantial portions of the first and second conductive connecting paths 210, 215 are typically heavily doped semiconductor having a higher charge carrier concentration ranging from about $1x10^{19}$ to $1x10^{20}$ charges per cubic centimeter.

Turning now to FIGURE 2B, illustrated is a diagram of an electrical equivalent, generally designated 240, as may be employed for the optical waveguide modulator 200 of FIGURE 2A. The electrical equivalent 240 includes first and second back-to-back semiconductor diodes 245a, 245b connected having first and second terminals 250a, 250b. The first and second back-to-back semiconductor diodes 245a, 245b are oriented corresponding to the dopants of the optical waveguide modulator 200. An electrical signal generator 255 may be connected between the first and second terminals 250a, 250b, as shown.

The electrical signal generator 255 may provide an electrical modulation signal that corresponds to an AC signal having zero DC bias voltage. This non-DC biased AC signal will modulate an optical signal traversing the optical waveguide core 205 to contain frequencies that are two times the frequencies of the electrical modulating signal thereby providing a frequency doubling of the electrical modulation in the optical signal. If the electrical modulation signal provides a DC-biased AC signal, wherein the DC bias always back-biases a same one of the PN semiconductor junctions, there will be no frequency doubling of the optical signal.

Turning now to FIGURE 2C, illustrated are cross-section views showing simulations of modulated charge carrier distributions, generally designated 260, in the semiconductor optical waveguide core 205 of FIGURE 2A. The cross-section views of FIGURE 2C correspond to charge concentrations in the semiconductor optical waveguide core 205 for an electrical modulation signal 290. The electrical modulation signal 290 is an AC voltage waveform having no DC bias voltage, which switches between plus and minus five volts. In FIGURE 2C, the electrical modulation signal 290 is presented as waveforms that are representative of first and second electrode voltages 290a, 290b wherein their voltage difference corresponds to the potential difference between them with the polarities indicated. Of course, one of the electrodes may actually be grounded wherein the other employs the potential difference between them with a corresponding polarity indicated.

The cross-section view 265 illustrates a simulated symmetrical charge concentration that corresponds to the electrical modulation signal 290 crossing zero volts, thereby corresponding to a zero bias condition for the optical waveguide core 205. As the potential difference between the first and second electrode voltages 290a, 290b moves from zero volts and progresses toward a negative 10 volts, the positive charge distribution in the semiconductor optical waveguide core 205 begins to skew toward its more negative first electrode. A cross-section view 270 illustrates the simulated positive charge distribution in the optical waveguide core 205 having reached a highly asymmetrical distribution. This distribution corresponds to the first and second electrode voltages 290a, 290b having respectively reached negative and positive five volt levels at a time $t_1$.

Then, as the first and second electrode voltages 290a, 290b move to reverse their polarities, the simulated symmetrical charge carrier concentration of the cross-section view 265 is again reached at zero bias voltage. As the potential difference between the second and first electrode voltages 290b, 290a moves from zero volts and progresses toward a negative 10 volts (*i.e.*, in the opposite direction from before), the positive charge carrier distribution in the optical waveguide core 205 begins to skew toward its more negative second electrode. A cross-section view 280 illustrates the simulated positive charge carrier distribution in the optical waveguide core 205 having reached a highly asymmetrical charge distribution in the opposite direction at a time $t_2$.

In the illustrated embodiment, a complete cycle of the electrical modulation signal 290 is completed as the zero voltage level is again reached. The cross-section views 270, 280 each correspond to a peak modulation of an optical signal traversing the semiconductor optical waveguide core 205 thereby giving two cycles of optical signal modulation for a single cycle of the electrical modulating signal 290. This action therefore produces a frequency doubling of the electrical modulation signal in the modulated optical signal. Providing an electrical modulation signal that maintains either a positive or negative voltage bias (*i.e.*, does not cross zero volts) corresponds to a modulated optical signal having the same modulation frequency as the electrical modulation signal.

Turning now to FIGURE 3A, illustrated is a cross-section view of an alternative embodiment of a semiconductor optical waveguide modulator, generally designated 300, constructed according to the principles of the present invention. The cross-section view represents a section as may be taken through the center of the optical waveguide modulator 100 as indicated in FIGURE 1. The optical waveguide modulator 300 includes a semiconductor optical waveguide core 305 having a ridge region and containing alternately doped regions 306, 307, 308 that form back to back PN junctions 311, 312 within the semiconductor optical waveguide core 305.

In this embodiment, a heavily doped semiconductor connecting path 310 containing a plurality of first electrodes 320 is shown on both sides of the semiconductor optical waveguide core 305. An alternative embodiment may employ only one heavily doped semiconductor connecting path 310 containing one electrode 320. The illustrated embodiment includes a second electrode 325 located above the semiconductor optical waveguide core 305, as shown. The first and second electrodes 320, 325 allow a modulating voltage to be applied vertically across the semiconductor optical waveguide core 305. Of course, the doping polarities may be reversed as appropriate to a particular application.

Turning now to FIGURE 3B, illustrated is a cross-section view of another embodiment of a semiconductor optical waveguide modulator, generally designated 340, constructed according to the principles of the present invention. Again, the cross-section view represents a section as may be taken through the center of the optical waveguide modulator 100 as indicated in FIGURE 1. The optical waveguide modulator 340 includes a semiconductor optical waveguide core 345 having a ridge portion and containing a singularly doped region, as shown.

The optical waveguide modulator 340 employs back to back PN semiconductor junctions 346, 347 wherein the PN semiconductor junction 346 is contained between a first semiconductor slab A and a side of the semiconductor optical waveguide core 345, as shown. A first heavily doped semiconductor connecting path 350 containing a first electrode 360 is associated with the PN semiconductor junction 346. The PN semiconductor junction 347 is contained between a second semiconductor slab B and a top portion of the semiconductor optical waveguide core 345. A second heavily doped semiconductor connecting path 355 containing a second electrode 360 is associated with the PN semiconductor junction 347.

The optical waveguide modulator 340 employs a ridge portion of the semiconductor optical waveguide core 345 that is greater in height than the combined thickness of the first and second slabs A, B. Operation of the optical waveguide modulator 340 is analogous to the optical waveguide modulator 205 of FIGURE 2A. However, this structure advantageously applies the field effects of a modulating voltage between the first and second electrodes 360, 365 to the carrier concentrations in the semiconductor optical waveguide core 345 thereby providing enhanced waveguide performance.

Turning now to FIGURE 4A, illustrated are cross-section views of an alternative embodiment of an optical waveguide modulator, generally designated 400, constructed according to the principles of the present invention. As before, the cross-section views represent a section as may be taken through the center of the optical waveguide modulator 100 as indicated in FIGURE 1. In FIGURE 4A, the single optical waveguide modulator 400 is illustrated two views (views A and B) of the same embodiment. View A and View B show simulated exemplary distributions in the semiconductor optical waveguide core 405 of hole carriers and electrons, respectively, when a zero voltage is applied there across. The optical waveguide modulator 400 includes a semiconductor optical waveguide core 405 having a ridge region and first and second conductive connecting paths 410, 415, i.e., heavily doped semiconductor paths adjacent opposite sides of the ridge region of the optical waveguide core 405. The optical waveguide modulator 405 also includes first and second electrodes 420, 425 respectively lateral and adjacent to the ridge region of the optical waveguide core 405.

The semiconductor optical waveguide core 405 includes a PN semiconductor junction 406 that is located inside its ridge region, i.e., both P-type and N-type sides of the PN semiconductor junction are located in the ridge region of the optical waveguide core 405. The PN semiconductor junction provides a field activated region that responds to applied electrical modulation signals. In the illustrated embodiment, the PN semiconductor junction 406 is located in the center of the optical waveguide core 405 although it may be asymmetrically located in the ridge region in alternative embodiments. The semiconductor optical waveguide core 405 may have a range of charge carrier distributions therein. The charge carrier distribution shown is for a small negative bias voltage (*e.g.*, 0.2 volts). The positive and negative central charge concentrations 407, 408 may have average values of about $2x10^{17}$ charges per cubic centimeter and may diminish to a junction-area charge concentration of about $3x10^{15}$ charges per cubic centimeter, i.e., in charge depletion regions of the junction. The first and second heavily doped semiconductor connecting paths 410, 415 may have a high charge carrier concentration of about $1x10^{19}$ charges per cubic centimeter.

Turning now to FIGURE 4B, illustrated are additional cross-section views showing simulations of modulated charge carrier concentrations, generally designated 450, in the optical waveguide core 405 for various applied voltages. The cross-section views of FIGURE 4B correspond to charge concentrations in the optical waveguide core 405 for an electrical modulating signal that provides a reverse bias voltage 460. The reverse bias voltage 460 switches between about 0.2 volts and five volts in various views, and is applied to the optical waveguide modulator 400 to always reverse-bias the PN semiconductor junction 406.

Views A and B again show simulations of the respective hole and electron charge carrier distributions for a reverse biased voltage of about 0.2 volts. Views C and D show simulations of the respective hole and electron charge carrier distributions for a five volt reverse bias across the PN semiconductor junction 406. The optical modulation frequency is the same as the electrical modulation frequency.

Turning now to FIGURE 5, illustrated is a cross-section view of an embodiment of a semiconductor optical waveguide modulator, generally designated 500, constructed according to the principles of the present invention. General operation of the optical waveguide modulator 500 is analogous to the optical waveguide modulator 400 of FIGURE 4A. Structurally, however, first and second intrinsic semiconductor layers 530, 535 have been placed in series with each of the heavily doped semiconductor paths adjacent the ridge region of the optical waveguide core 405, as shown. Alternately, insulator materials can be used as layers 530, 535 and placed in series with each of the heavily doped semiconductor paths adjacent the ridge region of the optical waveguide core 405.

Turning now to FIGURE 6, illustrated is a flow diagram of a method of operating an optical waveguide, generally designated 600, carried out according to the principles of the present invention, e.g., the apparatus of Figures 2A, 3A, 3B 4A and 5. The method 600 may generally be used, for example, to modify optical signals in the semiconductor optical waveguide and starts in a step 605. Then, in a step 610, an optical signal is provided that traverses a semiconductor optical waveguide core, and the optical signal is modulated by a field activated region, i.e., an electro-optically active region, within the semiconductor optical waveguide core in a step 615.

In one embodiment, the semiconductor optical waveguide core includes back-to-back PN semiconductor junctions located proximate opposite sides of the optical waveguide core that provide the field activated region, e.g., as in Figure 2A. The back-to-back PN semiconductor junctions include a P-type dopant in the semiconductor optical waveguide core that can provide a charge carrier concentration within at least a portion of the optical waveguide core that is within a range of $1x10^{15}$ to $8x10^{17}$ carriers per cubic centimeter at a zero bias voltage condition. The concentration is dependent on the application device geometry and anticipated drive voltage. Correspondingly, an N-type dopant is employed in connecting paths to the optical core, wherein the connecting paths are able to carry an electrical modulating signal. In the connecting paths an average charge carrier concentration may be at least $1x10^{19}$ carriers per cubic centimeter at the zero bias voltage condition.

Alternatively, the back-to-back PN semiconductor junctions may include an N-type dopant in the optical waveguide core and a P-type dopant in connecting paths that carry a current for the electrical modulation signal to/from the optical core. In these embodiments, charge carrier concentrations may have similar values and distributions except that hole and electron concentrations are interchanged. Additionally, in some embodiments, at least one of the back-to-back PN semiconductor junctions may also include an intrinsic semiconducting or insulating layer, i.e., an undoped Si or silica glass layer, in the PN semiconductor junction region.

In another embodiment, the semiconductor optical waveguide core includes a PN semiconductor junction that provides the field activated region wherein the PN semiconductor junction is located in a central position of the optical waveguide core. A charge carrier concentration within at least a portion of the optical waveguide core is about $2x10^{17}$ carriers per cubic centimeter corresponding to the zero bias voltage condition. Correspondingly, a charge concentration within connecting paths to the electrical modulation signal is at least $1x10^{19}$ carriers per cubic centimeter corresponding to the zero bias voltage condition. Alternatively, the PN semiconductor junction may also include an intrinsic layer in the junction thereby forming a PIN junction.

Then, the field activated region is modulated corresponding to the electrical modulation signal in a step 620. In one embodiment, the back-to-back PN semiconductor junctions cooperate to produce a frequency doubling of the electrical modulation signal in the optical signal. This condition occurs when the electrical modulation signal alternately reverse biases each one of back-to-back PN semiconductor junctions. Frequency doubling of the electrical modulation signal in the optical signal is not provided when one of the back-to-back PN semiconductor junctions is continuously reversed biased condition during application of the AC electrical modulation signal. This is also the case in the embodiment when the single PN semiconductor junction maintains a continuous reverse-bias while modulating the field activated region. The method 600 ends in a step 625.

While the method disclosed herein has been described and shown with reference to particular steps performed in a particular order, it will be understood that these steps may be combined, subdivided, or reordered to form an equivalent method without departing from the teachings of the present invention. Accordingly, unless specifically indicated herein, the order or the grouping of the steps is not a limitation of the present invention.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

**WHAT IS CLAIMED IS:**

1. An apparatus, comprising:

a semiconductor planar optical waveguide core;

doped semiconductor connecting paths located adjacent opposite sides of the core and capable of applying a voltage across the core; wherein the optical waveguide core and connecting paths form a structure having back-to-back PN semiconductor junctions.

2. The apparatus of claim 1, further comprising an electrode located over a top of the optical waveguide core such that a refractive index therein may be adjusted via a voltage applied between the electrode and another electrode in contact with at least one of the doped semiconductor connecting paths.

3. The apparatus of claim 1, further comprising an electrode in a top doped semiconductor connecting path located over a top of a ridge portion of the optical waveguide core such that a refractive index therein may be adjusted via a voltage applied between the electrode and another electrode in contact with at least one of the doped semiconductor connecting paths.

4. The apparatus as recited in Claim 3 wherein the ridge portion of the optical waveguide core is greater than a combined thickness of top and bottom slabs providing the top doped semiconductor connecting path and the at least one of the doped semiconductor connecting paths.

5. A method of operating a semiconductor planar optical waveguide, comprising:

sending an optical signal into a semiconductor optical waveguide core of the waveguide;

modulating a voltage applied across the width or height of the core such that carrier densities adjacent back-to-back PN semiconductor junctions are modulated while the signal propagates along the core; and

wherein a portion of each PN semiconductor junction is located in the core.

6. The method as recited in Claim 5 wherein the back-to-back PN semiconductor junctions are located adjacent opposite sides of the optical waveguide core.

7. The method as recited in Claim 5 wherein at least one of the back-to-back PN semiconductor junctions further includes a layer sandwiched between doped semiconductor layers.

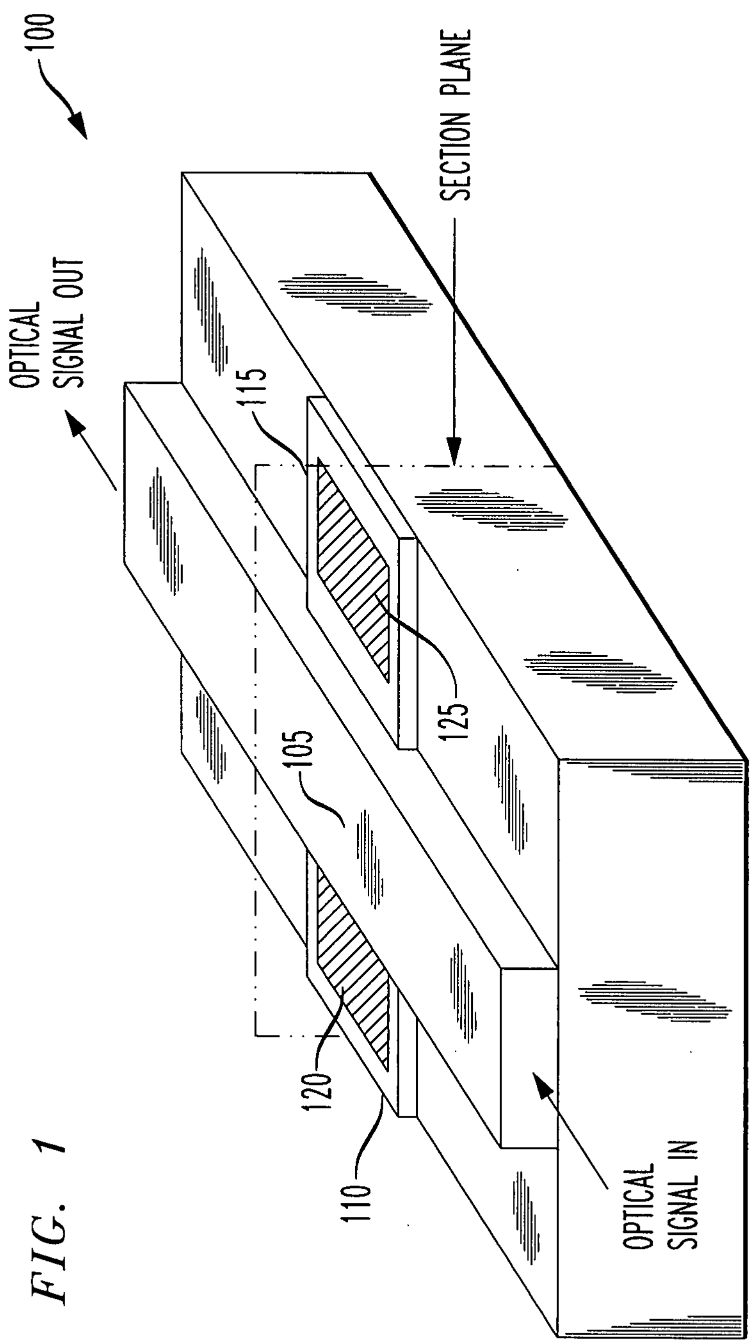
8. An apparatus, comprising:

a semiconductor optical waveguide core including a ridge portion, the ridge portion having at least one PN semiconductor junction located therein;

one or more doped semiconductor connecting paths located laterally adjacent the ridge portion and capable of applying a voltage to the ridge portion.

9. The apparatus of claim 8, further comprising an electrical contact located over a top of the ridge portion such that a refractive index therein may be adjusted via a voltage applied between the electrode and another electrode in contact with at least one of the one or more doped semiconductor connecting paths.

10. The apparatus of claim 8, wherein the electrical contact has a lateral width that is larger than a lateral width of the ridge portion.



100
SECTION PLANE
OPTICAL SIGNAL OUT
115
125
105
120
110
OPTICAL SIGNAL IN


*FIG. 1*

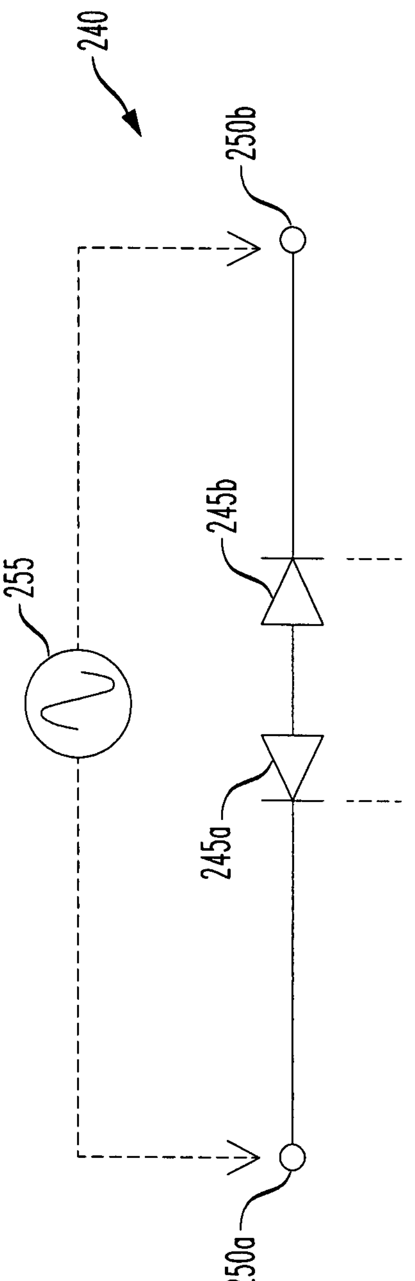

240
255
250a
250b
245a
245b

FIG. 2B

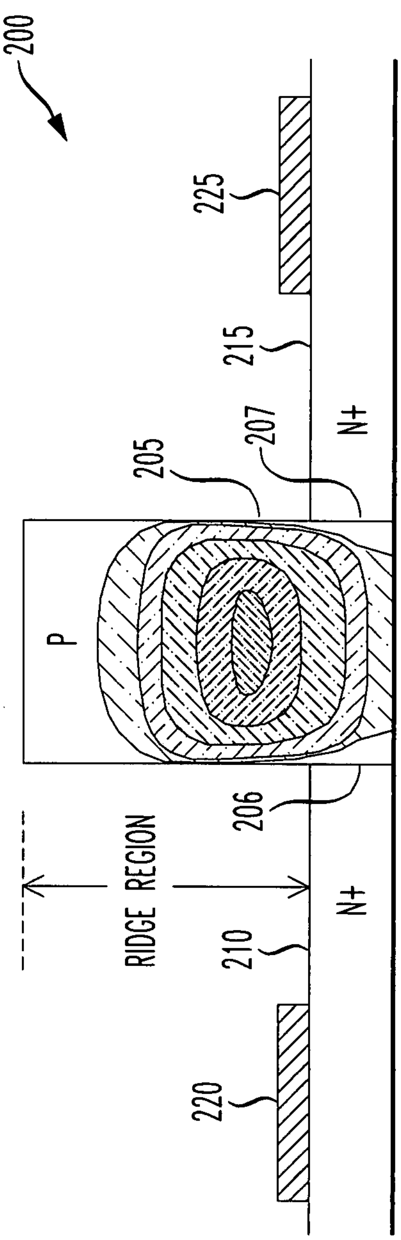

200
P
N+
N+
RIDGE REGION
205
206
207
210
215
220
225

FIG. 2A

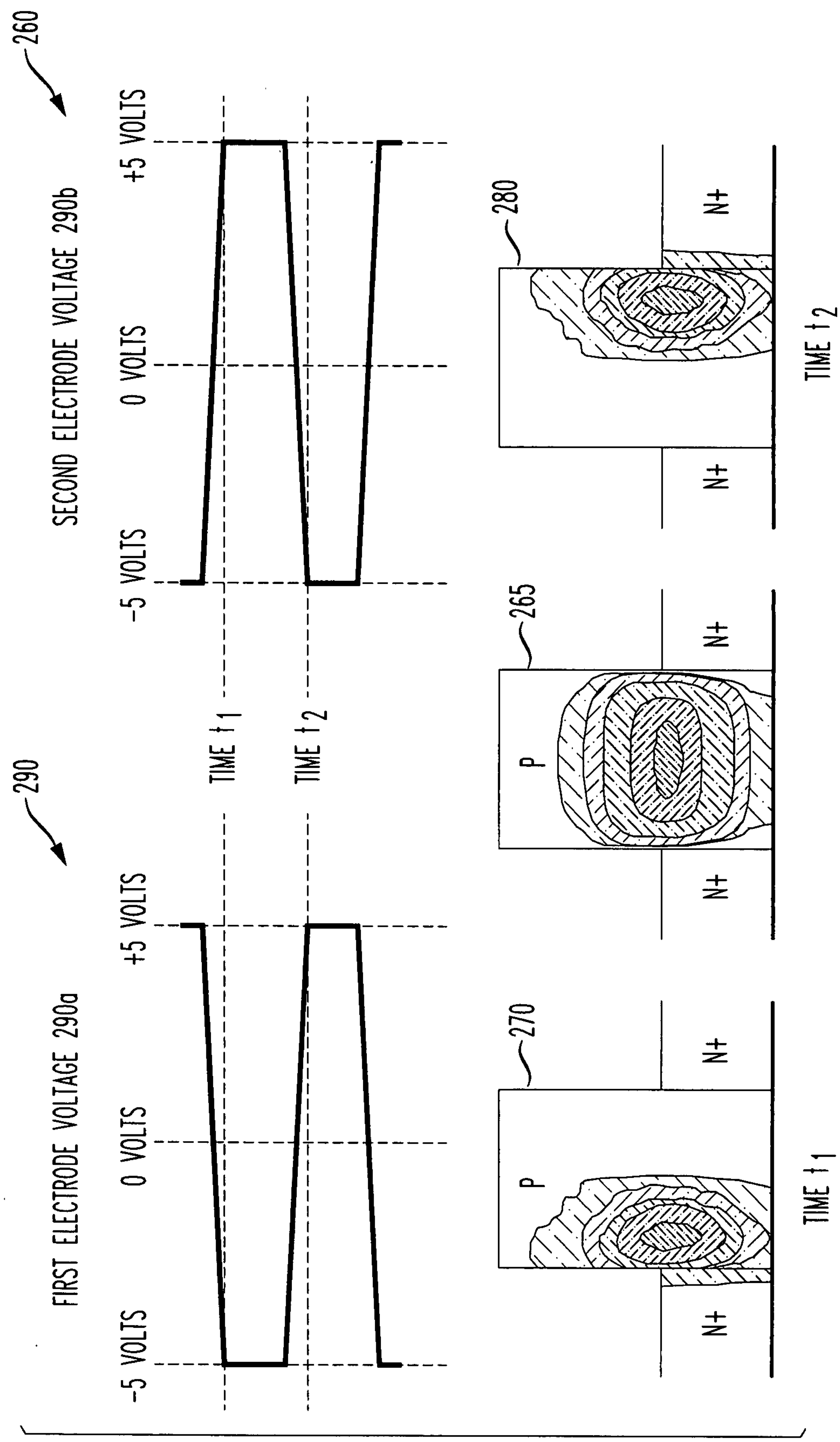

260
290
SECOND ELECTRODE VOLTAGE 290b
FIRST ELECTRODE VOLTAGE 290a
-5 VOLTS
0 VOLTS
+5 VOLTS
TIME t1
TIME t2
280
265
270
P
N+

*FIG. 2C*

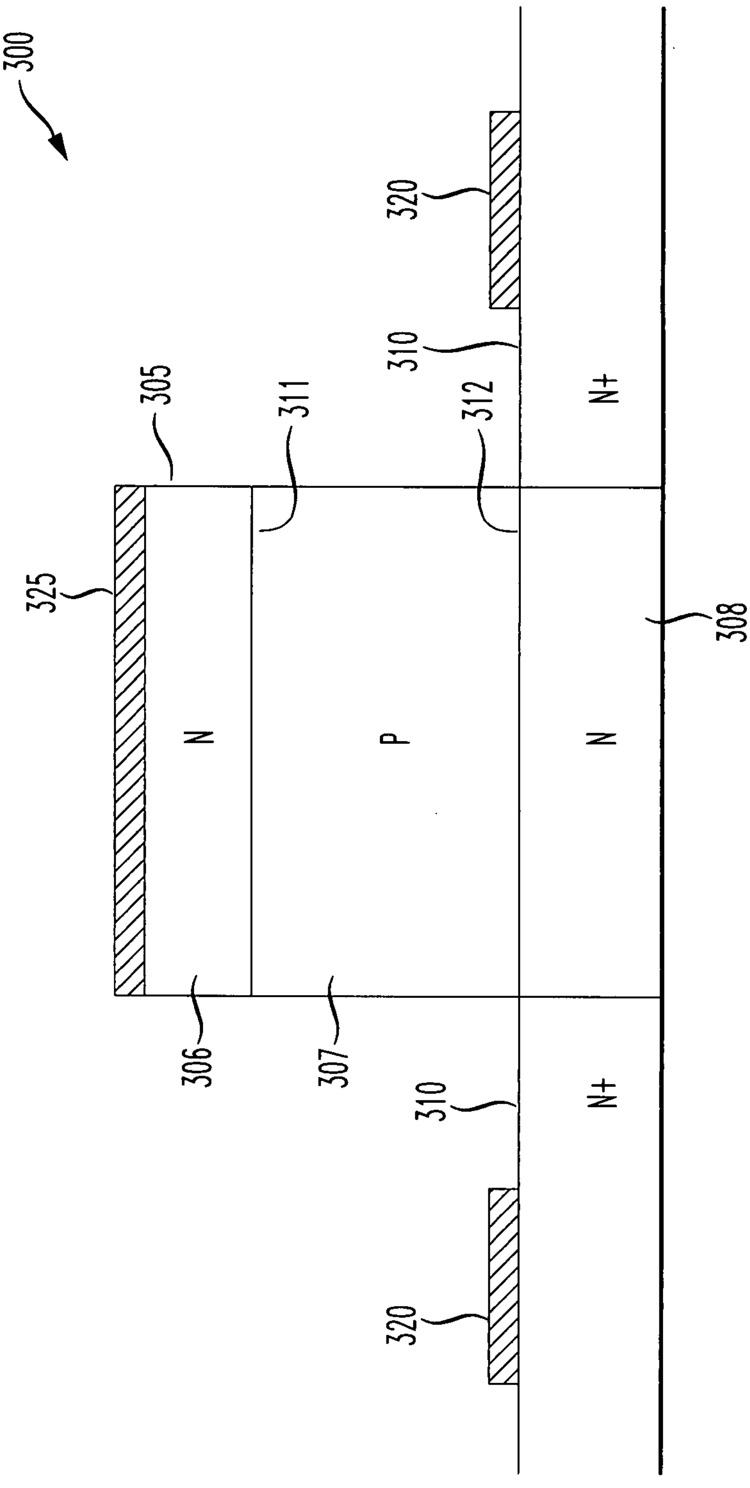



*FIG. 3A*

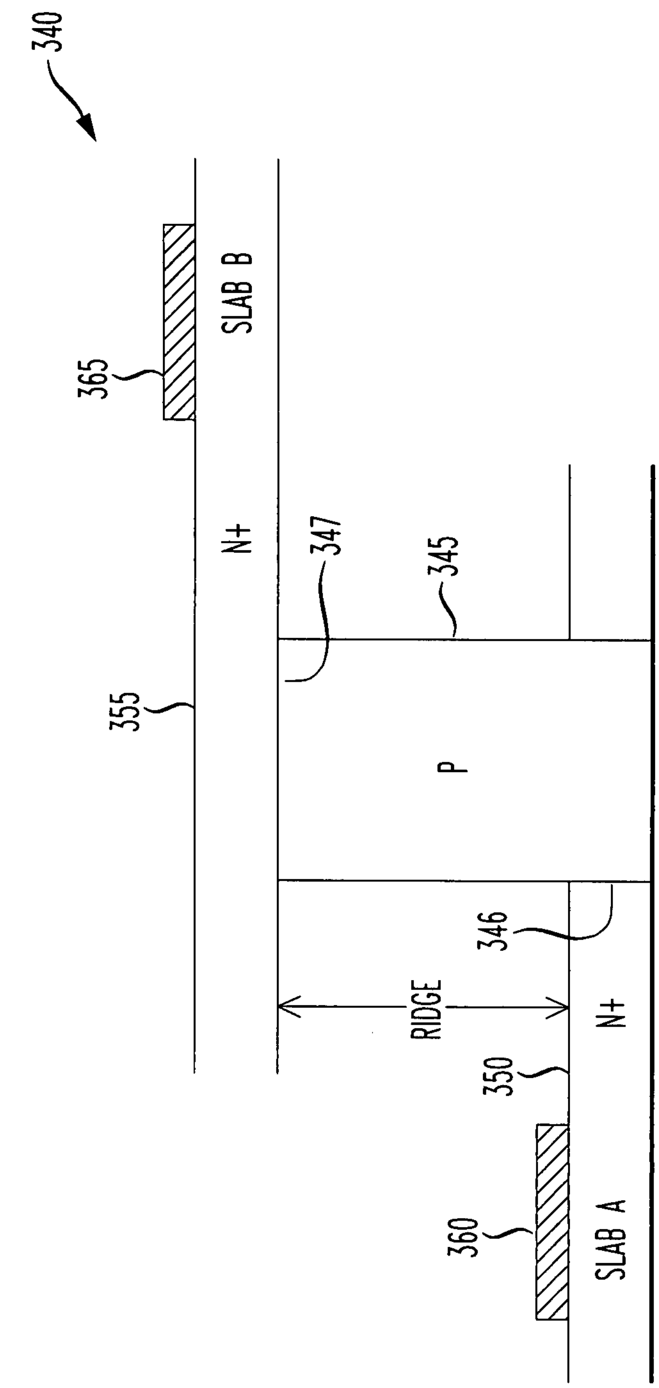



*FIG. 3B*

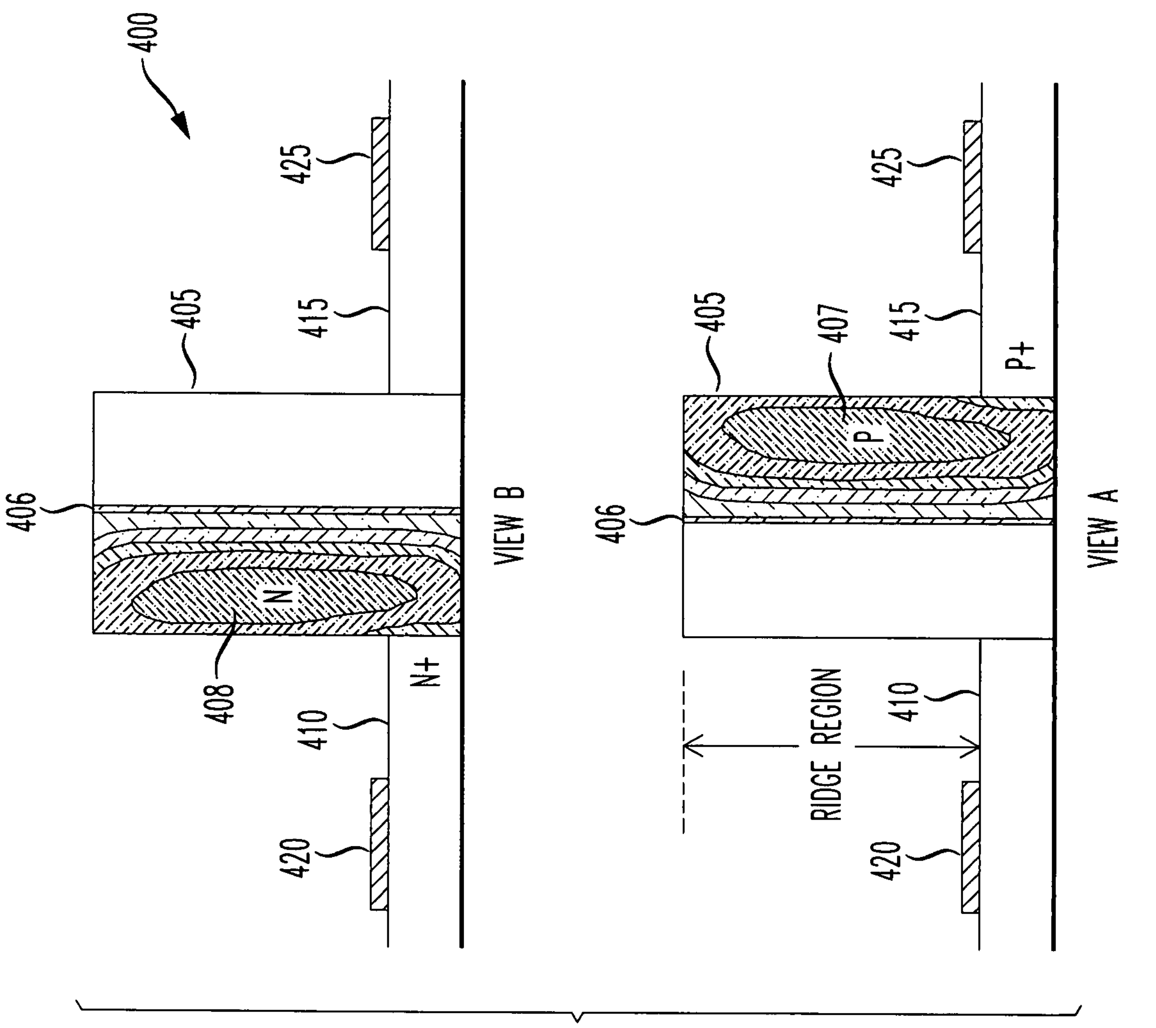

400
406
405
408
N
410
415
420
425
N+
VIEW B
406
405
407
P
P+
410
415
420
425
RIDGE REGION
VIEW A

*FIG. 4A*

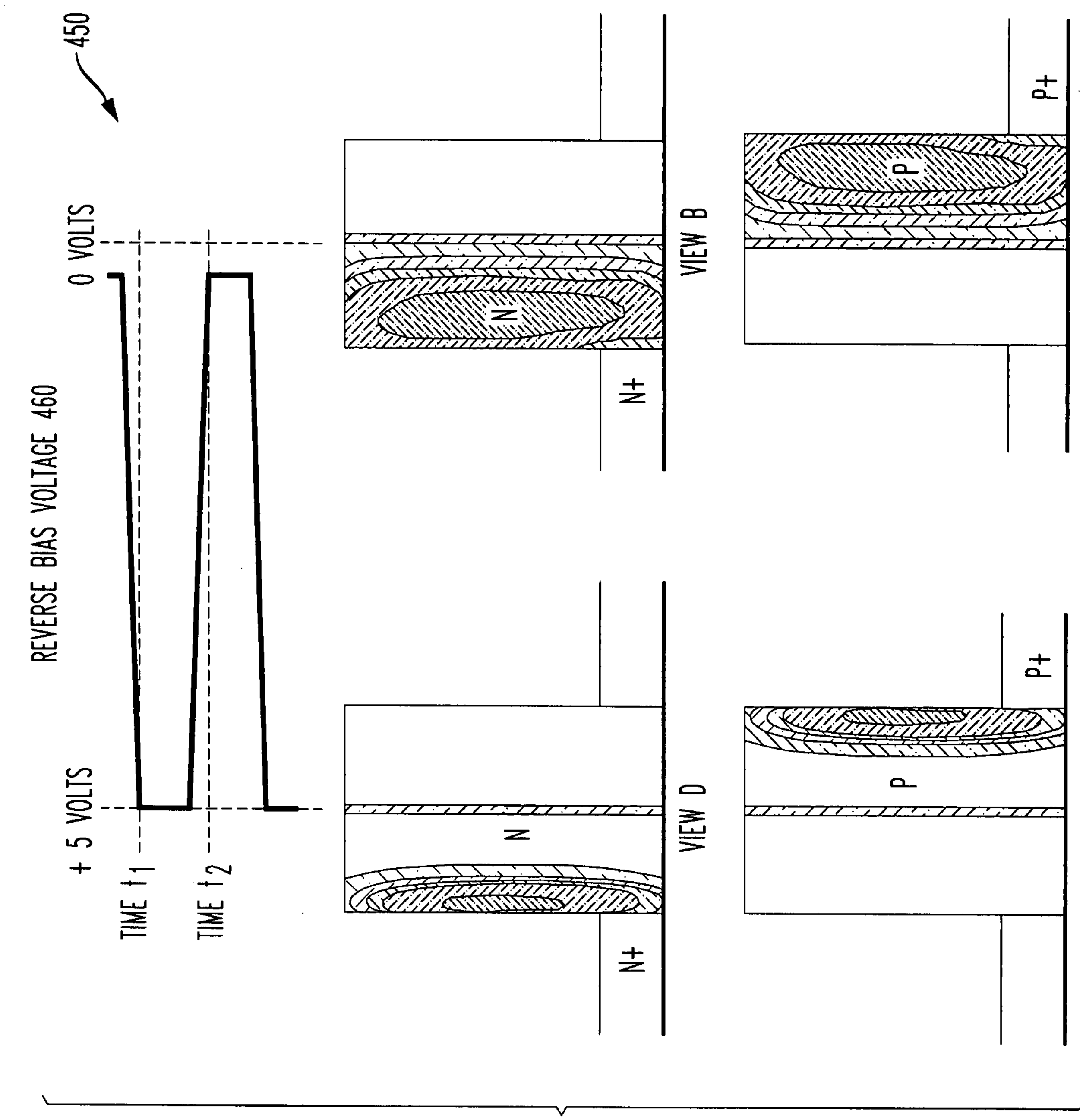

450
REVERSE BIAS VOLTAGE 460
0 VOLTS
+ 5 VOLTS
TIME t1
TIME t2
N+
N
VIEW B
N+
N
VIEW D
P+
P
P+
P

*FIG. 4B*

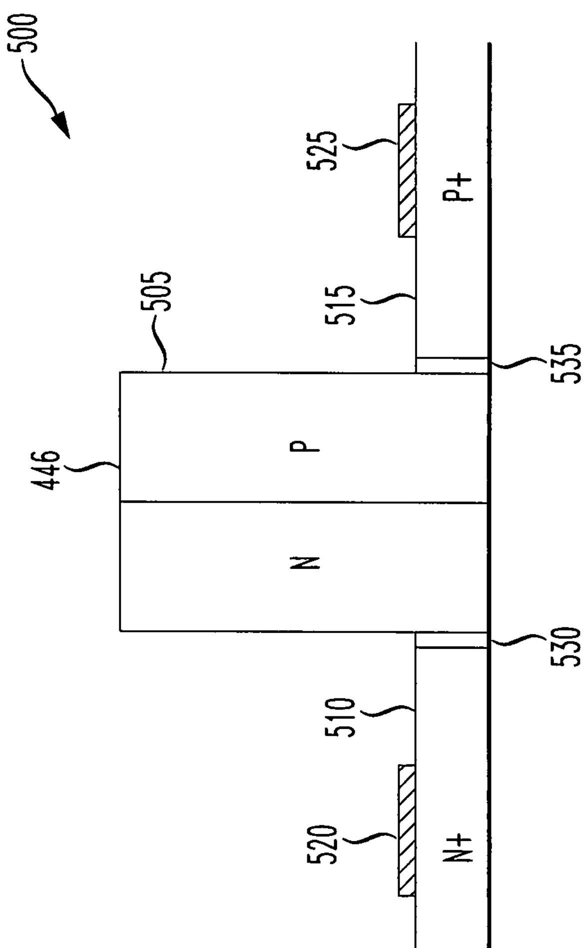



*FIG. 5*

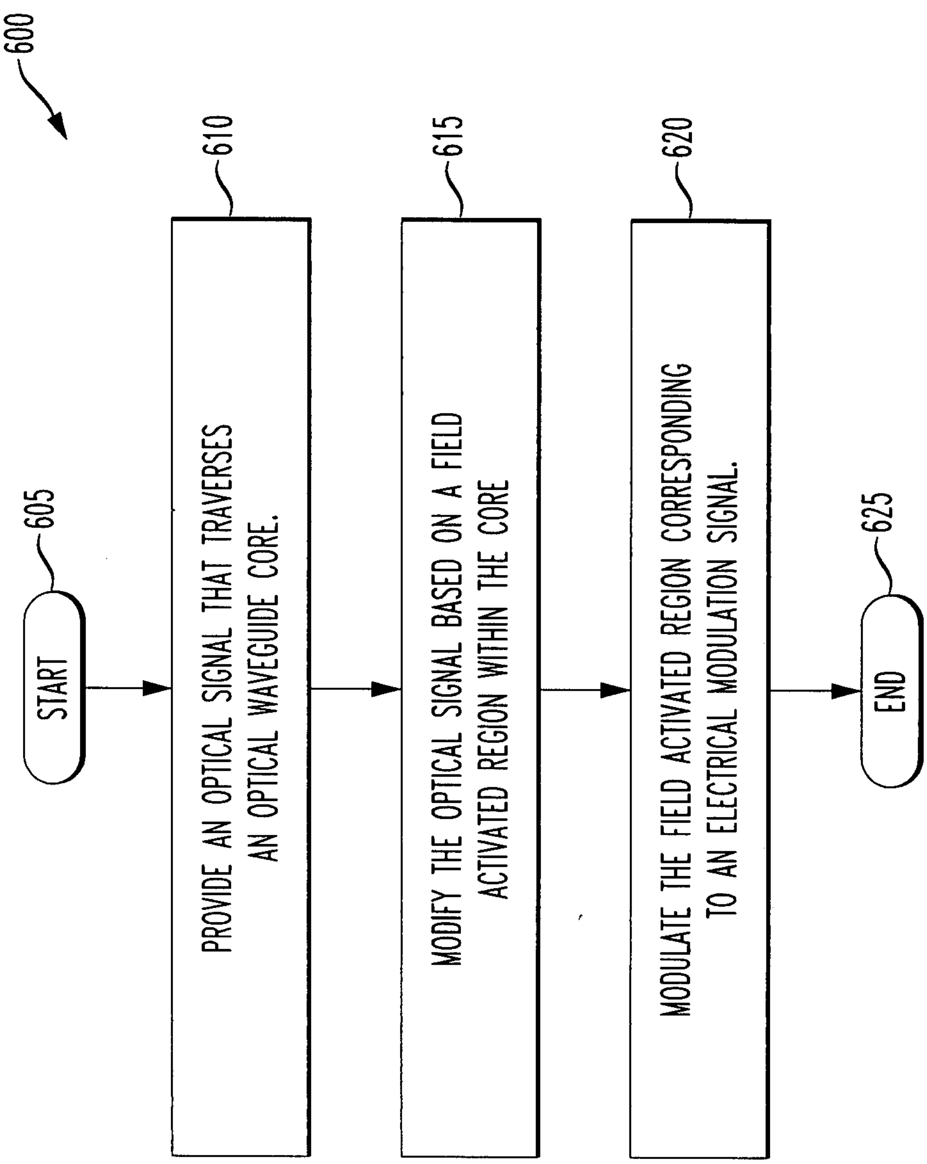

600
START
605
PROVIDE AN OPTICAL SIGNAL THAT TRAVERSES AN OPTICAL WAVEGUIDE CORE.
610
MODIFY THE OPTICAL SIGNAL BASED ON A FIELD ACTIVATED REGION WITHIN THE CORE
615
MODULATE THE FIELD ACTIVATED REGION CORRESPONDING TO AN ELECTRICAL MODULATION SIGNAL.
620
END
625

FIG. 6

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/022945

**A. CLASSIFICATION OF SUBJECT MATTER**
INV. G02F1/025

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | GB 2 348 293 A (BOOKHAM TECHNOLOGY LTD [GB]; BOOKHAM TECHNOLOGY PLC [GB]) 27 September 2000 (2000-09-27)<br>page 1, line 1 - line 5<br>page 6 - page 7<br>page 9 - page 10<br>figures 3,5<br>----- | 1-10 |
| X | US 4 997 246 A (MAY PAUL G [US] ET AL) 5 March 1991 (1991-03-05)<br>column 5, line 61 - column 6, line 17<br>figure 3<br>----- | 1,5-8 |
| X | US 2007/031080 A1 (LIU ANSHENG [US]) 8 February 2007 (2007-02-08)<br>paragraph [0002]<br>paragraph [0019] - paragraph [0024]<br>figure 1A<br>----- | 1-9 |

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 20 February 2008 | 28/02/2008 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Boubal, François |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/022945

| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT | | |
|---|---|---|
| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| X | US 7 085 443 B1 (GUNN III LAWRENCE C [US] ET AL) 1 August 2006 (2006-08-01)<br>column 1, line 18 - line 20<br>column 2, line 55 - column 3, line 46<br>column 10, line 60 - column 11, line 33<br>figures 1,11,12<br>----- | 8 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/022945

| Patent document cited in search report | | Publication date | Patent family member(s) | | | Publication date |
|---|---|---|---|---|---|---|
| GB 2348293 | A | 27-09-2000 | AU | 3441800 | A | 16-10-2000 |
| | | | EP | 1166172 | A1 | 02-01-2002 |
| | | | WO | 0058776 | A1 | 05-10-2000 |
| | | | JP | 2002540469 | T | 26-11-2002 |
| | | | US | 6298177 | B1 | 02-10-2001 |
| US 4997246 | A | 05-03-1991 | EP | 0433552 | A2 | 26-06-1991 |
| | | | JP | 2681044 | B2 | 19-11-1997 |
| | | | JP | 3196120 | A | 27-08-1991 |
| US 2007031080 | A1 | 08-02-2007 | NONE | | | |
| US 7085443 | B1 | 01-08-2006 | US | 7251408 | B1 | 31-07-2007 |