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(54) **Title:** SYSTEMS AND METHODS FOR GENERATING A DIGITAL OUTPUT SIGNAL IN A DIGITAL MICROPHONE SYSTEM

(57) **Abstract:** In accordance with embodiments of the present disclosure, a digital microphone system may include a microphone transducer and a digital processing system. The microphone transducer may be configured to generate an analog input signal indicative of audio sounds incident upon the microphone transducer. The digital processing system may be configured to convert the analog input signal into a first digital signal having three or more quantization levels, and in the digital domain, process the first digital signal to convert the first digital signal into a second digital signal having two quantization levels.



SYSTEMS AND METHODS FOR GENERATING A DIGITAL OUTPUT SIGNAL IN A DIGITAL MICROPHONE SYSTEM

RELATED APPLICATIONS

The present disclosure claims priority to United States Provisional Patent
5 Application Serial No. 61/810,075, filed April 9, 2013, which is incorporated by
reference herein in its entirety.

FIELD OF DISCLOSURE

The present disclosure relates in general to audio systems, and more particularly,
10 to compressing a digital signal in a digital microphone system.

BACKGROUND

Microphones are ubiquitous on many devices used by individuals, including
computers, tablets, smart phones, and many other consumer devices. Generally speaking,
15 a microphone is an electroacoustic transducer that produces an electrical signal in
response to deflection of a portion (e.g., a membrane or other structure) of a microphone
caused by sound incident upon the microphone.

In a digital microphone system, an analog output signal of the microphone
transducer may be processed by an analog-to-digital converter to convert the analog
20 output signal to a digital output signal, which may be communicated over a bus to a
digital audio processor for further processing. By communicating a digital signal over the
bus rather than an analog signal, the audio signal may be less susceptible to noise.

In typical digital microphone systems, a one-stage analog-to-digital delta-sigma
modulator is utilized to convert the analog output signal to a one-bit digital signal
25 compatible with the digital audio processor receiving the digital output signal. However,
one disadvantage of analog-to-digital delta-sigma modulators having a one-bit output is
that they consume significant amounts of power.

SUMMARY

In accordance with the teachings of the present disclosure, certain disadvantages and problems associated with power consumption in a digital microphone system may be reduced or eliminated.

5 In accordance with embodiments of the present disclosure, a digital microphone system may include a microphone transducer and a digital processing system. The microphone transducer may be configured to generate an analog input signal indicative of audio sounds incident upon the microphone transducer. The digital processing system may be configured to convert the analog input signal into a first digital signal having
10 three or more quantization levels, and in the digital domain, process the first digital signal to convert the first digital signal into a second digital signal having two quantization levels.

In accordance with these and other embodiments of the present disclosure, a method may include receiving an analog input signal indicative of audio sounds incident
15 upon a microphone transducer. The method may also include converting the analog input signal into a first digital signal having three or more quantization levels. The method may further include, in the digital domain, processing the first digital signal to convert the first digital signal into a second digital signal having two quantization levels.

In accordance with these and other embodiments of the present disclosure, an
20 integrated circuit may include a microphone input and a processing circuit. The microphone input may be configured to receive an analog input signal indicative of audio sounds incident upon a microphone transducer. The processing circuit may be configured to convert the analog input signal into a first digital signal having three or more quantization levels and, in the digital domain, process the first digital signal to convert the
25 first digital signal into a second digital signal having two quantization levels.

Technical advantages of the present disclosure may be readily apparent to one having ordinary skill in the art from the figures, description and claims included herein. The objects and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are explanatory examples and are not restrictive of the claims set forth in this disclosure.

5 BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

10 FIGURE 1 illustrates a block diagram of selected components of an example audio system, in accordance with embodiments of the present disclosure;

FIGURE 2 illustrates a block diagram of selected components of a digital microphone integrated circuit, in accordance with embodiments of the present disclosure;

15 FIGURE 3 illustrates a block diagram of selected components of an analog-to-digital converter, in accordance with embodiments of the present disclosure; and

FIGURE 4 illustrates a block diagram of selected components of a digital delta-sigma modulator, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

20 FIGURE 1 illustrates a block diagram of selected components of an example audio system 100, in accordance with embodiments of the present disclosure. As shown in FIGURE 1, audio system 100 may include a microphone transducer 101, a digital microphone integrated circuit (IC) 105, and a digital audio processor 109. Microphone transducer 101 may comprise any system, device, or apparatus configured to convert
25 sound incident at microphone transducer 101 to an electrical signal, for example an analog output signal ANALOG_OUT, wherein such sound is converted to an electrical signal using a diaphragm or membrane having an electrical capacitance that varies as based on sonic vibrations received at the diaphragm or membrane. Microphone transducer 101 may include an electrostatic microphone, a condenser microphone, an
30 electret microphone, a microelectromechanical systems (MEMs) microphone, or any other suitable capacitive microphone.

Digital microphone IC 105 may comprise any suitable system, device, or apparatus configured to process analog output signal ANALOG_OUT to generate a digital audio output signal DIGITAL_BUS and condition digital audio output signal DIGITAL_BUS for transmission over a bus to digital audio processor 109. Once
5 converted to digital audio output signal DIGITAL_BUS, the audio signal may be transmitted over significantly longer distances without being susceptible to noise as compared to an analog transmission over the same distance. In some embodiments, digital microphone IC 105 may be disposed in close proximity with microphone transducer 101 to ensure that the length of the analog line between microphone transducer
10 101 and digital microphone IC 105 is relatively short to minimize the amount of noise that can be picked up on an analog output line carrying analog output signal ANALOG_OUT. For example, in some embodiments, microphone transducer 101 and digital microphone IC 105 may be formed on the same substrate. In other embodiments, microphone transducer 101 and digital microphone IC 105 may be formed on different
15 substrates packaged within the same integrated circuit package.

Digital audio processor 109 may comprise any suitable system, device, or apparatus configured to process digital audio output signal for use in a digital audio system. For example, digital audio processor 109 may comprise a microprocessor, microcontroller, digital signal processor (DSP), application specific integrated circuit
20 (ASIC), or any other device configured to interpret and/or execute program instructions and/or process data, such as a digital audio output signal.

FIGURE 2 illustrates a block diagram of selected components of digital microphone IC 105, in accordance with embodiments of the present disclosure. As shown in FIGURE 2, digital microphone IC 105 may include a pre-amplifier 203, an analog-to-digital converter (ADC) 215, and a driver 219. Pre-amplifier 203 may receive
25 analog output signal ANALOG_OUT via one or more input lines which may allow for receipt of a single-ended signal, differential signal, or any other suitable analog audio signal format and may comprise any suitable system, device, or apparatus configured to condition analog output signal ANALOG_OUT for processing by ADC 215. The output
30 of pre-amplifier 203 may be communicated to ADC 215 on one or more output lines.

ADC 215 may comprise any suitable system, device, or apparatus configured to convert an analog audio signal received at its input, to a digital signal representative of analog output signal ANALOG_OUT. ADC 215 may itself include one or more components (e.g., delta-sigma modulator, decimator, etc.) for carrying out the functionality of ADC 215.

Driver 219 may receive the digital signal DIGITAL_OUT output by ADC 215 and may comprise any suitable system, device, or apparatus configured to condition such digital signal (e.g., encoding into Audio Engineering Society/European Broadcasting Union (AES/EBU), Sony/Philips Digital Interface Format (S/PDIF), in the process generating digital audio output signal DIGITAL_BUS for transmission over a bus to digital audio processor 109. In FIGURE 2, the bus receiving digital audio output signal DIGITAL_BUS is shown as single-ended. In some embodiments, driver 219 may generate a differential digital audio output signal 107.

FIGURE 3 illustrates a block diagram of selected components of a two-stage ADC 300, which may be used to implement ADC 215 depicted in FIGURE 2, in accordance with embodiments of the present disclosure. As shown in FIGURE 3, ADC 300 may include an analog delta-sigma modulator 302 and a digital delta-sigma modulator 304. Analog delta-sigma modulator 302 may comprise any suitable system, device or apparatus configured to convert an analog input signal (e.g., ANALOG_AMP) into a first digital signal having three or more quantization levels (e.g., a multi-bit signal comprised of N bits, as shown in FIGURE 3, or any other digital signal having three or more quantization levels), as may now or in the future be known in the art. Digital delta-sigma modulator 304 may comprise any suitable system, device or apparatus configured to, in the digital domain, process the first digital signal to convert the first digital signal into a second digital signal (e.g., DIGITAL_OUT) having two quantization levels (e.g., a single-bit signal or any other digital signal having two quantization levels). An example embodiment of digital delta-sigma modulator 304 is depicted in FIGURE 4.

FIGURE 4 illustrates a block diagram of selected components of digital delta-sigma modulator 304, in accordance with embodiments of the present disclosure. As shown in FIGURE 4, digital delta-sigma modulator 304 may include a loop filter 402, a quantizer 404, look-ahead circuitry 412, and excursion limiting-circuitry 414. Loop filter

402 may comprise an input summer 408 for generating a difference between the first digital signal and a digital feedback signal, and one or more integrator stages 410, such that loop filter 412 operates as a digital filter of an error signal equal to the difference between the first digital signal DIGITAL_MULTI and a digital feedback signal DIGITAL_FB, and generates a filtered digital signal to quantizer 304 based on the first digital signal and the digital feedback signal. In certain embodiments, loop filter 402 may be of at least third order (e.g., including three or more integrator stages 410). The output from loop filter 402 may be quantized by quantizer 404 which may generate the one-bit output signal DIGITAL_OUT based on its input.

Remodulation in the digital domain by digital delta-sigma modulator 304 may allow for the ability to implement significantly more accurate and complex algorithms in digital logic as compared to analog circuitry. As an example, an accurate signal limiter is an expensive analog block, but in the digital domain may be implemented with a relatively simple digital comparator. The modulation by analog delta-sigma modulator 302 to an intermediate digital signal which is remodulated to a digital signal having two quantization levels by digital delta-sigma modulator 304 may allow for much more of the complexity of the implementation to be incorporated in digital logic, which often scales well with process technology, unlike analog integrated circuitry technology. Power may also be reduced due to the partitioning between analog delta-sigma modulator 302 and digital delta-sigma modulator 304; a multi-bit analog delta-sigma modulator typically requires less power per unit of performance than a single-bit analog delta-sigma modulator.

In some embodiments, digital delta-sigma modulator 304 may comprise a look-ahead delta-sigma modulator, and thus may include look-ahead circuitry 412. A look-ahead delta-sigma modulator may be one which, with increased digital computation, may improve the quality of quantizer output values by reducing the probability of a current quantizer result causing future quantizer overload and system distortion. Look-ahead modulators may also, when compared with modulators not employing look-ahead, reduce occurrence of quantizer overload and output distortion which may occur if an input signal of a modulator is large relative to its full-scale feedback signal. Accordingly, look-ahead circuitry 412 may include circuitry to minimize quantizer overload of digital delta-sigma

modulator 304. Approaches to implementing a look-ahead delta sigma modulator, including look-ahead circuitry 412, may be described in U.S. Pat. No. 7,170,434 entitled “Look-Ahead Delta Sigma Modulator with Quantization Using Natural and Pattern Loop Filter Responses,” U.S. Pat. No. 6,879,275 entitled “Signal Processing with a Look-Ahead Modulator Having Time Weighted Error Values,” U.S. Pat. No. 7,196,647 entitled “Signal Processing with Look-Ahead Modulator Noise Quantization Minimization,” U.S. Pat. No. 7,187,312 entitled “Look-Ahead Delta Sigma Modulator Having an Infinite Impulse Response Filter with Multiple Look-Ahead Outputs,” U.S. Pat. No. 7,148,830 entitled “Look-Ahead Delta Sigma Modulator with Pruning of Output Candidate Vectors Using Quantization Error Minimization Pruning Techniques,” U.S. Pat. No. 7,138,934 entitled “Pattern Biasing for Look-Ahead Delta-Sigma Modulators,” U.S. Pat. No. 7,084,798 entitled “Look-Ahead Delta Sigma Modulators with Quantizer Input Approximations,” U.S. Pat. No. 7,190,294 entitled “Jointly Nonlinear Delta Sigma Modulators,” and U.S. Pat. No. 7,183,957 entitled “Signal Processing System with Analog-to-Digital Converter Using Delta-Sigma Modulation Having an Internal Stabilizer Loop,” all of which are incorporated herein by reference.

In these and other embodiments, digital delta-sigma modulator 414 may also comprise excursion-limiting circuitry 414. Excursion-limiting circuitry 414 may comprise any system, device, or apparatus configured to limit excursion of state variables of digital delta-sigma modulator 304 for analog input signal levels (e.g., ANALOG_OUT) having a relatively high modulation index (e.g., 0.75 or higher), wherein a modulation index is defined as a ratio of a maximum input signal to the maximum feedback signal. State variables may include those state variables of a noise-shaping filter formed by loop filter 402, wherein such state variables determine the output signal of quantizer 404. Presence of excursion-limiting circuitry 414 may provide for stability of delta-sigma modulator 304, and also reduce quantizer overload. Examples of such excursion-limiting circuitry 414 may be described in U.S. Pat. No. 6,822,594 entitled “Overload Protection and Stability for High Order 1-Bit Delta-Sigma Modulators,” U.S. Pat. No. 6,933,871 entitled “Feedback Steering Delta-Sigma Modulators and Systems using the Same,” U.S. Pat. No. 7,081,843 entitled “Overload Protection for Look-Ahead Delta Sigma Modulators,” and U.S. Pat. No. 7,358,881

entitled “Quantizer Overload Prevention for Feed-back Type Delta-Sigma Modulators,” which are all incorporated by reference herein.

This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the example embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the disclosure and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present disclosure have been described in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. A digital microphone system comprising:
a microphone transducer configured to generate an analog input signal indicative
5 of audio sounds incident upon the microphone transducer;
a digital processing system configured to:
convert the analog input signal into a first digital signal having three or
more quantization levels; and
in the digital domain, process the first digital signal to convert the first
10 digital signal into a second digital signal having two quantization levels.
2. The system of Claim 1, wherein the microphone transducer and the digital
processing system are formed on a single substrate.
- 15 3. The system of Claim 1, wherein the microphone transducer and the digital
processing system are formed on different substrates packaged within the same integrated
circuit package.
4. The system of Claim 1, wherein the microphone transducer comprises a
20 microelectromechanical systems microphone.
5. The system of Claim 1, wherein the digital processing system comprises a
feedback digital delta-sigma modulator to convert the first digital signal into the second
digital signal.
25
6. The system of Claim 5, wherein the digital delta-sigma modulator is of at
least third order.
7. The system of Claim 6, wherein the digital delta-sigma modulator
30 comprises circuitry to limit excursion of state variables of the delta-sigma modulator for
analog input signal levels having a modulation index of 0.75 or higher.

8. The system of Claim 5, wherein the digital delta-sigma modulator is a look-ahead delta-sigma modulator.

5 9. The system of Claim 5, wherein the digital delta-sigma modulator comprises circuitry to minimize quantizer overload of the digital delta-sigma modulator.

10. A method comprising:
receiving an analog input signal indicative of audio sounds incident upon a
10 microphone transducer;
converting the analog input signal into a first digital signal having three or more quantization levels; and
in the digital domain, processing the first digital signal to convert the first digital signal into a second digital signal having two quantization levels.

15 11. The method of Claim 10, wherein the microphone transducer comprises a microelectromechanical systems microphone.

12. The method of Claim 10, wherein converting the first digital signal into
20 the second digital signal comprises converting the first digital signal into the second digital signal with a digital delta-sigma modulator.

13. The method of Claim 12, wherein the digital delta-sigma modulator is of at least third order.

25 14. The method of Claim 13, wherein the digital delta-sigma modulator comprises circuitry to limit excursion of state variables of the delta-sigma modulator for analog input signal levels having a modulation index of 0.75 or higher.

30 15. The method of Claim 12, wherein the digital delta-sigma modulator is a look-ahead delta-sigma modulator.

16. The method of Claim 12, wherein the digital delta-sigma modulator comprises circuitry to minimize quantizer overload of the digital delta-sigma modulator.

5 17. An integrated circuit comprising:
a microphone input configured to receive an analog input signal indicative of audio sounds incident upon a microphone transducer; and
a processing circuit configured to:
convert the analog input signal into a first digital signal having three or
10 more quantization levels; and
in the digital domain, process the first digital signal to convert the first digital signal into a second digital signal having two quantization levels.

18. The integrated circuit of Claim 17, wherein the digital processing system
15 comprises a feedback digital delta-sigma modulator to convert the first digital signal into the second digital signal.

19. The integrated circuit of Claim 18, wherein the digital delta-sigma modulator is of at least third order.

20 20. The integrated circuit of Claim 19, wherein the digital delta-sigma modulator comprises circuitry to limit excursion of state variables of the delta-sigma modulator for analog input signal levels having a modulation index of 0.75 or higher.

25 21. The integrated circuit of Claim 18, wherein the digital delta-sigma modulator is a look-ahead delta-sigma modulator.

22. The integrated circuit of Claim 18, wherein the digital delta-sigma modulator comprises circuitry to minimize quantizer overload of the digital delta-sigma
30 modulator.

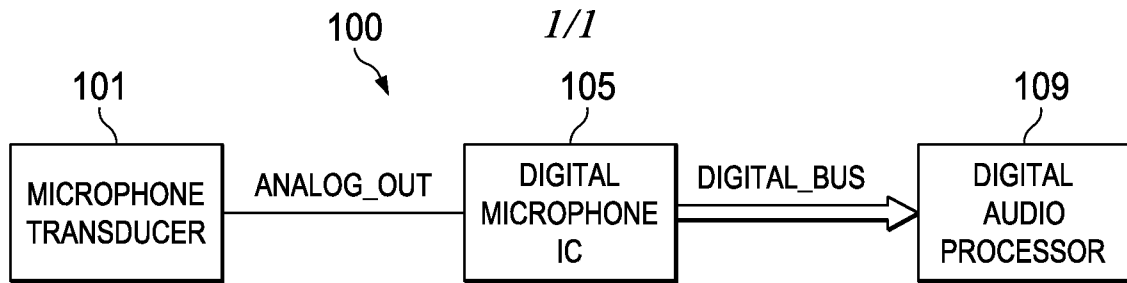


FIG. 1

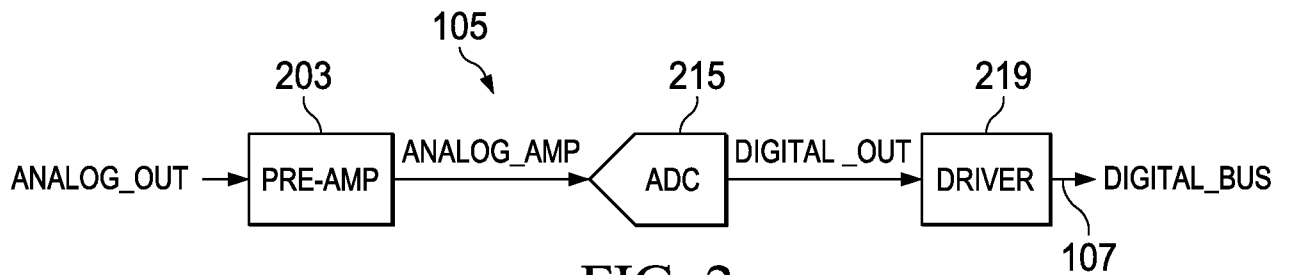


FIG. 2

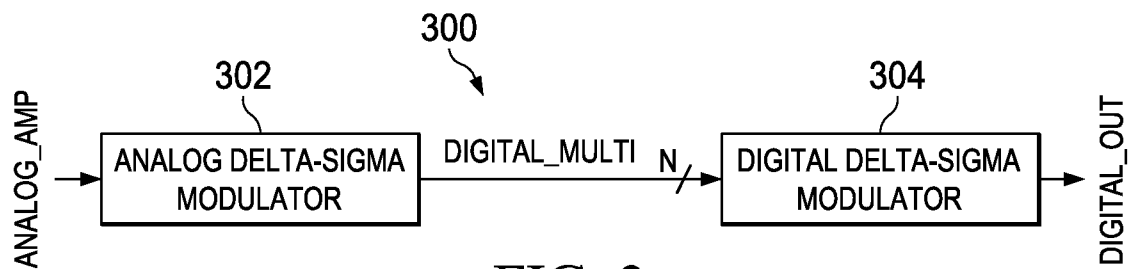


FIG. 3

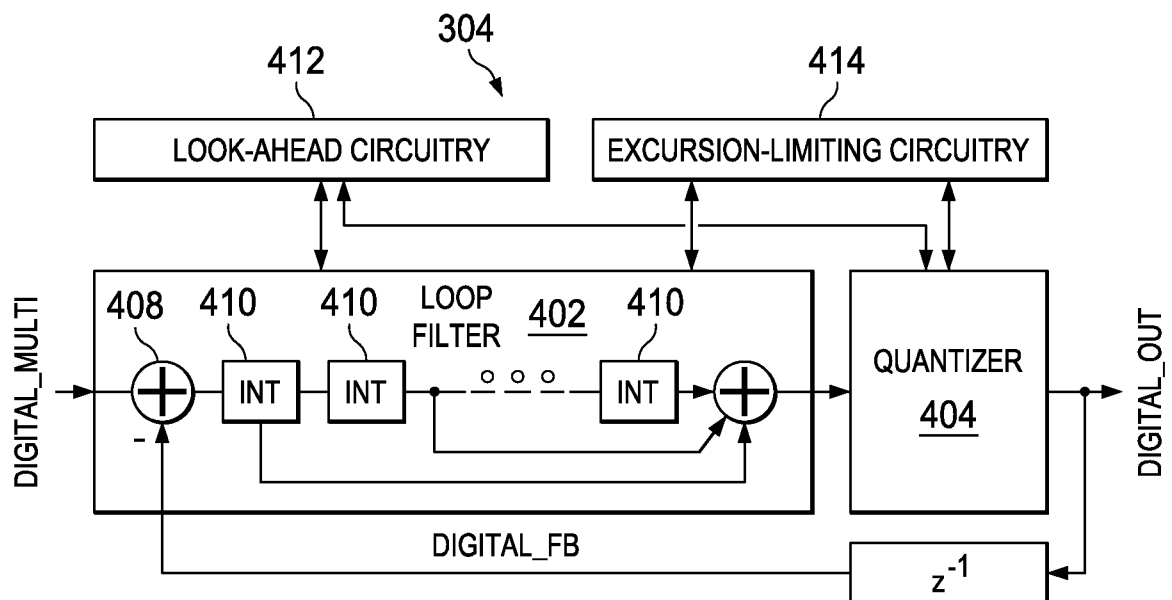


FIG. 4