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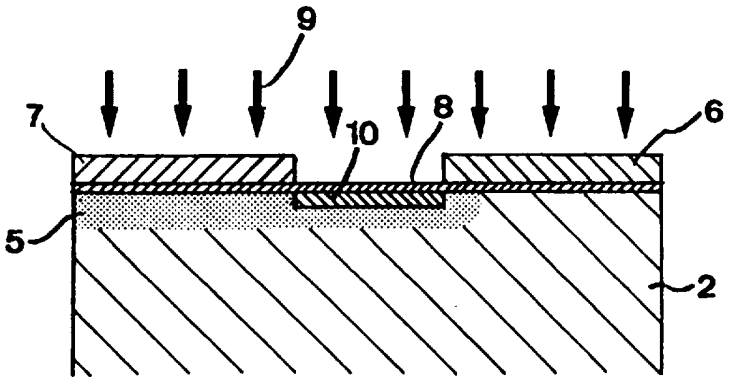
(54) Title: A METHOD FOR PRODUCING A SEMICONDUCTOR DEVICE COMPRISING AN IMPLANTATION STEP

(57) Abstract

A method for producing a semiconductor device having a semiconductor layer (2) of SiC comprises at least the steps of applying an insulating layer (1) on said semiconductor layer, implantation of an impurity dopant into said semiconductor layer and annealing this layer at such a high temperature that the implanted impurities are activated. Said insultating layer is applied before and maintained on said semiconductor layer during said annealing step. A material having AlN as major component is applied on said semiconductor layer as said insulating layer.



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A method for producing a semiconductor device comprising an implantation step

TECHNICAL FIELD OF THE INVENTION AND PRIOR ART

The present invention relates to a method for producing a semiconductor device having a semiconductor layer of SiC, said method comprising at least the steps of applying an insulating layer on said semiconductor layer, implantation of an impurity dopant into said semiconductor layer and annealing this layer at such a high temperature that the implanted impurities are activated, said insulating layer being applied before and maintained on said semiconductor layer during said annealing step.

The production of all types of semiconductor devices is comprised, such as for example different types of diodes, transistors and thyristors.

Such devices are particularly used in applications in which it is possible to benefit from the superior properties of SiC in comparison with especially Si, namely the capability of SiC to function well under extreme conditions. SiC has a high thermal stability due to a large band gap energy, such that devices fabricated from said material are able to operate at high temperatures, namely up to 1000 K. Furthermore, it has a high thermal conductivity, so that SiC-devices can dissipate a high power without overheating. SiC also has a more than five times higher

breakdown field than Si, so that it is well suited as a material in high power devices operating under conditions where high voltages may occur in the blocking state of a device.

However, this extreme chemical and physical stability of the SiC necessitates an annealing after said implantation at comparatively high temperatures, mostly above 1500°C and not seldom above 1700°C, for activating implanted impurities, which makes it impossible to leave said insulating layer on the semiconductor layer during this heat treatment would traditional insulating materials, such as SiO_2, be used.

One type of method according to the introduction is known through US patent 5 384 270, which describes a method of producing a silicon carbide MOSFET using a so called self alignment technique, i.e. the implantation of impurity dopants into said semiconductor layer of SiC is made while using layers comprising the device itself, here the gate electrode, as a mask for the ion implantation. Accordingly, the insulating layer has to be there before the ion implantation and will also be there during the following annealing step. In this case SiO_2 is accordingly used as insulating layer and the annealing temperature required for efficient activation after an implantation will damage the insulating layer, so that a semiconductor device produced in the way described in this US patent will not have an appropriate function, especially will the insulating properties be degraded and the conductivity in the inversion channel will be reduced.

The same problem exists in all types of methods in which an implantation step is carried out and it is

desired or absolutely necessary that an insulating layer remains on the SiC-layer during the annealing step, for instance for being left on the device for passivation purposes.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a method according to the introduction, which makes it possible to produce semiconductor devices having a semiconductor layer of SiC by using ion implantation while solving the problems discussed above.

This object is in accordance with the invention obtained by applying a material having AlN as major component on said semiconductor layer as said insulating layer. AlN can be made stable at least up to 2000 K and thus well capable of withstanding the high temperature activation anneal following the implantation step, so that this insulating layer will not be destroyed by said annealing. Furthermore, AlN has a very good lattice match with SiC with a misfit of only 0,7% and it has nearly the same coefficient of thermal expansion as SiC, so that it will be possible to grow an insulating layer having AlN as a major component with a high quality on the SiC semiconductor layer, and this insulating layer will not be negatively affected by the high annealing temperatures required for activating impurities implanted in SiC. The expression "as major component" means that it will be possible to add some other components to AlN for forming said insulating layer, such as smaller amounts of other Group III B-nitrides should this be desired, but such additions will decreasing the lattice match with SiC. The use of a material having AlN as major component as an insulating layer in a method for producing a semiconductor device of

this type has many advantages, which will appear from the discussion of preferred embodiments of the invention following below, wherein said insulating layer may be used for utilising the self aligned technology for isolated gate devices, as a mask for said implantation and be left on the device as a passivation layer and so on.

According to another preferred embodiment of the invention the material is $Al_xB_{(1-x)}N$. By adding B to AlN the lattice match of the insulating layer to SiC may be improved. A theoretical perfect lattice match will be obtained when x is about 0,96, i.e. the B-content is about 4%. A B-content in AlN will also increase the bandgap and the breakdown voltage thereof. Furthermore, AlBN is more resistent to oxidation than AlN.

According to a preferred embodiment of the invention said method comprises at least a step of self aligned implantation, and said insulating layer is present during this step. Thus, it will be possible to use such a layer having AlN as major component as the insulating dielectric for the production of isolated gate devices, since the insulating layer is not degraded by the activation anneal, so that this very advantageous technique for the production of semiconductor devices may be used also for the production of isolated gate devices with a semiconductor layer of SiC. This technique is very advantageous with respect to other production techniques, since you do not need any realignment between the different steps. Another advantage of this technique is that the correct alignment obtained thereby enables the reduction of parasitic losses due to limits otherwise placed in the device structure, for example capacitances resulting from overlaps.

According to another preferred embodiment of the invention a gate material, this material being a suitable refractory metal, for example Ta, layer for said semiconductor device is applied on said insulating layer before said step of self aligned implantation, said gate material layer leaving at least one opening for the penetration of the implanted impurity dopant into said semiconductor layer during said step of self aligned implantation for making the implanted region in said semiconductor layer aligned with said opening. This method has the advantages discussed above, and it may for instance be used for the production of isolated gates semiconductor devices with an insulating layer still having an excellent quality after the high temperature anneal for activating the impurity dopant implanted in the SiC-layer.

According to another preferred embodiment of the invention said method comprises a step of implantation of a P-type impurity dopant, and said insulating layer is present during the activation annealing after this implantation. It is very advantageous to be able to introduce acceptors as impurity dopants by the implantation technique, since these acceptors need a higher annealing temperature for being activated than the donors, so that this case is particularly troublesome with known insulating materials, but the thermal stability of AlN allows these high temperatures.

According to a further preferred embodiment of the invention said insulating layer is used as a mask for implantation for preventing the areas of said semiconductor layer located therebehind being reached by the impurities implanted. The use of an insulating

layer having AlN as major component as an implantation mask is very advantageous, since AlN is a radiation hard material, i.e. it is only damaged on the surface due to a high resistance to implantation and the ions so implanted in the surface layer thereof will not diffuse through said mask to the interface with the semiconductor layer during the annealing step. Thus, high implantation energies are required for implantation in SiC and the use of AlN as an implantation mask makes it possible to design such a mask with a reasonable thickness, whereas other materials, such as SiO_2, as mask material have to be much thicker. A layer having AlN as major component can therefore be used as an implantation mask enabling structures to be defined in a non-mesa planar technology, for example implanted p-n diodes, field rings etc. The mask layer will remain intact as a means of device isolation (passivation).

According to a preferred development of the embodiment of the invention described above and including the application of a gate material layer, said gate is made of a refractory metal, and this metal is TiN. This refractory metal makes it possible to use the self aligned technology for producing isolated gate devices having a semiconductor layer of SiC, since it will not be damaged by the high annealing temperatures needed for activation of the impurities implanted. Furthermore, the gate of TiN and said insulating layer, when it is made of AlN, may be grown in one single growth run facilitating the production of the semiconductor device.

According to another preferred embodiment of the invention said insulating layer is applied on said semiconductor layer at a thickness allowing implantation therethrough but adapted to prevent out-diffu-

sion of the dopants and Si-evaporation from the SiC surface during said annealing step. Selecting such a thickness of the insulating layer will make it possible to allow implantation into the SiC-layer therebehind while at the same time taking advantage of the low diffusivity in AlN for preventing out-diffusion and Si-evaporation during the high temperature annealing step.

The invention also comprises a use of a material having AlN as major component in a semiconductor device having a semiconductor layer of SiC, said device being created by a method comprising ion implantation and annealing at high temperatures for activating the implant in the presence of said material, as well as a semiconductor device produced by carrying out a method comprising the characteristics according to any of the appended method claims. The advantages of this use and such a semiconductor device has been discussed above. Such a device will of course be most suitable for high power applications thanks to the physical characteristics of SiC and AlN.

Further advantages and preferred features of the invention will appear from the following description and the other dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

With reference to the appended drawings, below follows a specific description of preferred embodiments of the invention cited as examples.

In the drawings:

Fig 1 - 4 illustrate schematically different steps of a method for producing a semiconductor power device

in the form of an isolated gate device of SiC according to a first preferred embodiment of the invention, and

Fig 5-6 illustrate schematically two of the steps of a method for producing a semiconductor power device in the form of a rectifier diode of SiC according to a second preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Fig 1 - 4 illustrate a few important steps of a large number of steps of a method according to the invention for producing an isolated gate device made of SiC for a high power application by using the implantation technique and in one step the self alignment technique. A thin insulating layer 1 of AlN has been epitaxially grown onto a low doped N-type semiconductor layer 2 of SiC, and a mask 3 is applied onto an area of said insulating layer 1 for preventing that the areas of said semiconductor layer located therebehind are reached by the impurities implanted in an ion implantation step described below. The insulating layer 1 may have a thickness of about 500 Å allowing implantation therethrough. The donor concentration in the low doped layer 2 will typically be about 10^{15} cm^{-3}. The crystal is exposed to a bombardment of ions having a kinetic energy of several hundred keV or more, for instance 300 keV, for implanting impurities of P-type into said semiconductor layer 2. These high energies are needed as a consequence of the physical properties of SiC, and a kinetic energy of 300 keV may for instance result in a penetration depth of less than 1 μm in the SiC-layer. Said impurities may for instance be B or Al. The implantation process is indicated by the arrows 4. In this way a doped P-type

layer 5 will be formed in the SiC crystal in the area not covered by said mask 3.

After that said mask 3 is removed, for instance by Reactive Ion Etching (RIE), and the crystal is heated to a temperature exceeding 1700°C for activating the acceptors implanted in said P-type layer 5. The insulating layer 1 of AlN is well capable of withstanding these high temperature activation anneal and will also prevent out-diffusion of the dopants and Si-evaporation from the SiC-surface during the annealing step. Fig 2 shows the crystal after said annealing step. After that a gate electrode material 6 is applied on a part of the insulating layer 1, and a further mask 7 is applied on another part thereof leaving an opening 8 therebetween for ion implantation. Said gate electrode 6 is made of a refractory metal, for instance TiN. After that an implantation step (see arrows 9) is carried out for implantation of a N-type impurity dopant in the SiC-layer behind said opening 8. In this way a highly doped, for instance 10^{19} cm^{-3}, N-type layer 10 is obtained. This layer 10 is aligned with the gate electrode 6, which will remain intact in the semiconductor device, so that this implantation step uses the self alignment technology. After that said mask 7 is removed and the crystal is annealed for activating the donors implanted in the highly doped N-type layer 10. The AlN-layer 1 will have the same function during this annealing step as during the annealing step described above. Following the annealing step a source area covering the implanted N^+-layer and also partly the P-layer is etched away and a metal contact layer 11 forming the source is grown.

In this way a semiconductor device having a gate 6 isolated by an isolating layer 1 having a high

quality has been produced by using the self aligned technology. The device has a source 11 and a drain not shown connected to the N^+ substrate on which the low-doped N-type layer 2 is grown. The current through this device may be controlled by controlling the gate potential.

Fig 5 and 6 illustrate some steps of another preferred method according to the invention, in which AlN is used as a material for an implantation mask and left after said implantation for passivation purposes. A layer 12 of AlN is grown onto a low-doped N-type SiC crystal 13. In a region of said insulating layer 12 insulating layer material is removed by a suitable technique, so that there will be a thin layer portion 14 having a thickness allowing the penetration of ions therethrough during an implantation step thereafter. Thus, the thickness of this layer portion 14 may be for instance 0,05 µm, whereas the thickness of the rest of the layer 12 may be for instance 1 µm, which will be enough for preventing implantation ions to reach the interface between said layer 12 and the SiC semiconductor layer 13. It may be mentioned that a layer of AlN having a thickness of 1,28 µm will be required to prevent boron having a kinetic energy of 1 MeV from penetrating to said interface, and boron is the P-type impurity that penetrates most deeply into a layer of AlN. Thus, a mask made of AlN or having AlN as major component may be made comparatively thin thanks to the radiation hardness of AlN. After that the crystal is bombarded by a P-type impurity (see arrows 15), for instance Al or B, and these impurities will penetrate through the thin layer portion 14 but not through the layer 12 forming an implantation mask. Thus, a P-type doped region 16 is formed below or behind said layer portion 14. After that the crystal is annealed at a

temperature above 1700°C for activating the acceptors in said region 16. During this anneal said thin layer portion 14 prevents out-diffusion of dopants from the region 16, and the layer 12 will not in any way be harmed by the high temperatures thanks to the physical properties of AlN. After said activation annealing said layer portion 14 is removed by for instance reactive ion etching, and an ohmic contact 17 is after that applied in the opening so formed in the insulating layer 12. The insulating layer 12 is then left as a passivation layer of the rectifier diode so created.

Accordingly, an insulating layer of AlN or of a material having AlN as major component makes it possible to use the ion implantation technique for producing semiconductor devices of SiC when it is a requirement or a desire to have said insulating layer present during the high temperature anneal for activating the impurity dopant implanted.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a man with ordinary skill in the art.

As mentioned in the introduction the invention is applicable to all types of semiconductor devices, preferably semiconductor devices adapted to operate under extreme conditions, such as high voltages and the generation of large amounts of heat, while taking advantage of the physical properties of SiC.

The invention does not only cover methods for producing SiC semiconductor devices according to the two embodiments described above, but every production method in which an implantation and after that an an-

nealing takes place in the presence of an insulating layer is within the scope of the invention.

The invention also comprises methods in which N-type impurity dopants, such as N and P, are implanted and a high temperature activating anneal is used thereafter.

All definitions concerning the materials of the different device layers do of course also include inevitable impurities as well as intentional doping when SiC is concerned.

The definition layer is to be interpreted broadly and comprise all types of volume extensions and shapes.

Claims

1. A method for producing a semiconductor device having a semiconductor layer (2) of SiC, said method comprising at least the steps of applying an insulating layer (1) on said semiconductor layer, implantation of an impurity dopant into said semiconductor layer and annealing this layer at such a high temperature that the implanted impurities are activated, said insulating layer (1) being applied before and maintained on said semiconductor layer during said annealing step,
characterized in that a material having AlN as major component is applied on said semiconductor layer (2) as said insulating layer (1).

2. A device according to claim 2, **characterized** in that the material is $Al_xB_{(1-x)}N$.

3. A device according to claim 2, **characterized** in that x is between 0.92 and 0.98, preferably around 0.96.

4. A method according to claim 1,
characterized in that said material is AlN.

5. A method according to any of claims 1-4,
characterized in that it comprises at least a step of self aligned implantation, and that said insulating layer (1) is present during this step.

6. A method according to claim 4,
characterized in that a gate material layer (6) for said semiconductor device is applied on said insulating layer (1) before said step of self aligned implantation, said gate material layer leaving at least an opening (8) for the penetration of the

implanted impurity dopant into said semiconductor layer (2) during said step of self aligned implantation for making the implanted region (10) in said semiconductor layer (2) aligned with said opening.

7. A method according to claim 6, **characterized** in that it is used for producing isolated gate semiconductor devices.

8. A method according to any of claims 1-7, **characterized** in that it is used for producing a MISFET (Metal-Insulator-Semiconductor Field Effect Transistor).

9. A method according to claim 8, **characterized** in that it comprises the following steps carried out in the order mentioned:
implanting an impurity dopant of P-type into a first region (5) of a low doped N-type SiC-layer (2) where this is not covered by a mask (3) blocking penetration of implanted ions, said SiC-layer being covered by a thin insulating layer (1) of a material having AlN as major component, annealing said SiC-layer (2) for activating said implanted impurities, applying a gate material layer (6) onto said insulating layer after removal of said mask while leaving an opening above a part of said P-type region, implanting an impurity dopant of N-type into a self aligned region (10) of said P-type region for forming a N-type region surrounded by said P-type region and annealing the SiC-layer for activating the impurities implanted in said self aligned N-type region.

10. A method according to any of claims 1-9, **characterized** in that it comprises at least a step of annealing in the presence of said insulating layer (1) at a temperature above 1500°C.

11. A method according to claim 10, **characterized** in that said temperature is above 1700°C.

12. A method according to any of claims 1-11, **characterized** in that it comprises a step of implantation of a P-type impurity dopant, and that said insulating layer (1, 12, 14) is present during the activation annealing after this implantation.

13. A method according to any of claims 1-11, **characterized** in that it comprises a step of implantation of a N-type impurity dopant, and that said insulating layer (1, 12, 14) is present during the activation annealing after this implantation.

14. A method according to claim 1, **characterized** in that said insulating layer (12) is used as a mask for implantation for preventing that the areas of said semiconductor layer located therebehind are reached by the impurities implanted.

15. A method according to claim 1, **characterized** in that said insulating layer (12) is left on said semiconductor device as a passivation layer.

16. A method according to claim 6, **characterized** in that said gate (6) is made of a refractory metal.

17. A method according to claim 16, **characterized** in that said gate (6) is made of TiN.

18. A method according to claim 17,

characterized in that said gate (6) of TiN and said insulating layer (1) being of AlN are grown in one single step.

19. A method according to any of claims 1-13 or 15-18,
characterized in that said insulating layer (1, 14) is applied on said semiconductor layer (2, 13) at a thickness allowing implantation therethrough but adapted to prevent out-diffusion of the dopants and Si-evaporation from the SiC surface during said annealing step.

20. A method according to any of the preceding claims,
characterized in that it is used for producing high power devices.

21. A method according to claim 11,
characterized in that said P-type impurity dopant is one of a) B and b) Al.

22. A use of a material having AlN as major component in a semiconductor device having a semiconductor layer of SiC, said device being created by a method comprising ion implantation and annealing at high temperatures for activating the implant in the presence of said material.

23. A semiconductor device produced by carrying out a method comprising the characteristics according to any of claims 1-19.

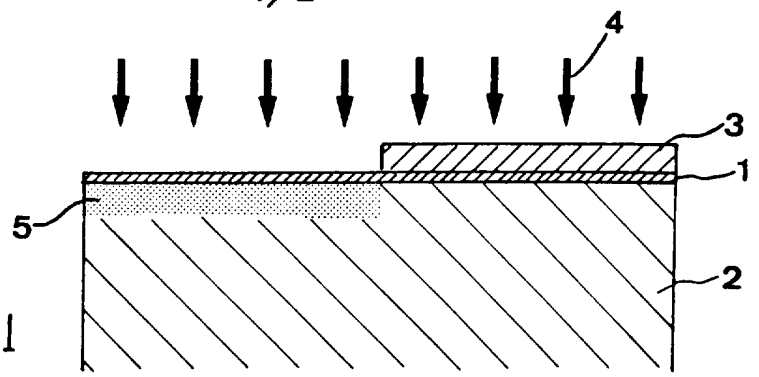

Fig 1

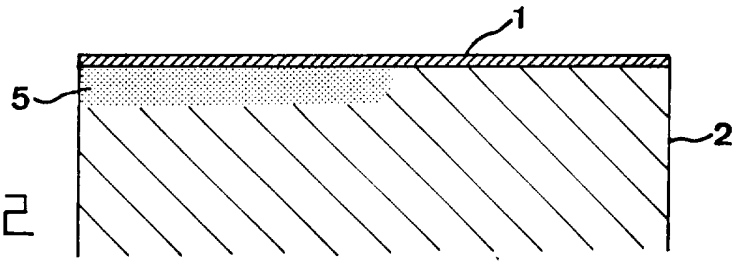

Fig 2

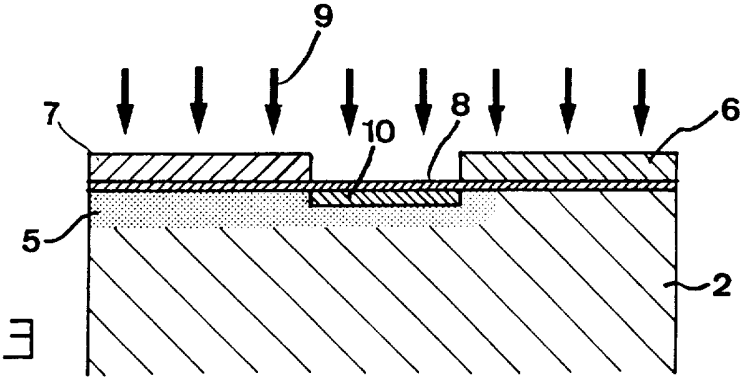

Fig 3

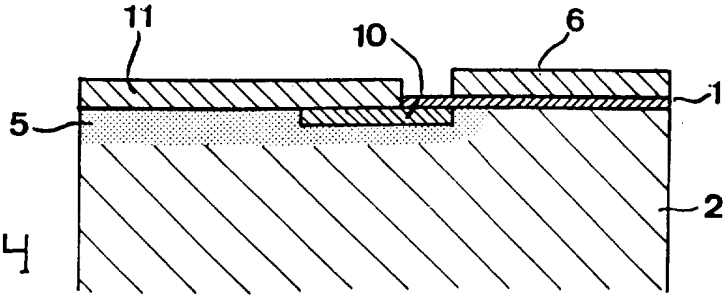

Fig 4

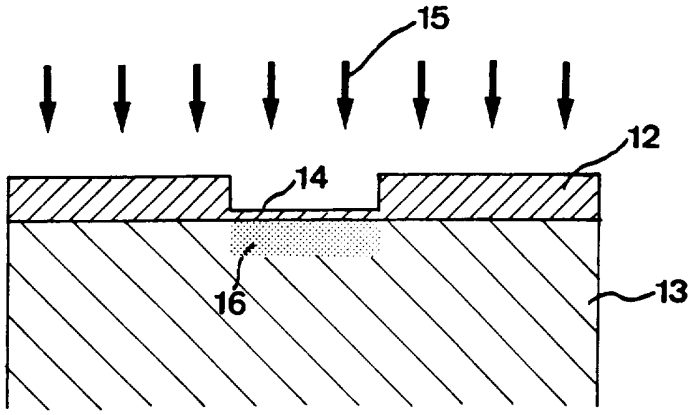

Fig 5

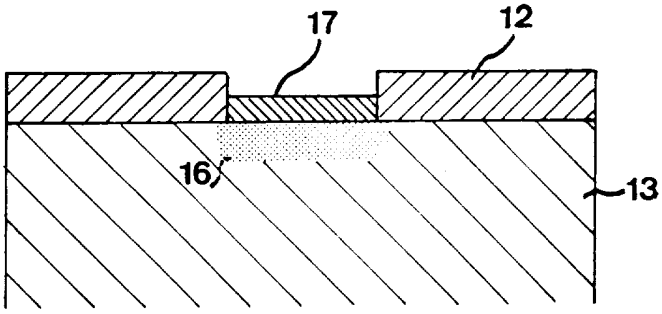

Fig 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 96/01206

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 21/265, H01L 21/318, H01L 21/324, H01L 29/24, H01L 29/201
// H01L 29/772

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 350, 351

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
E,X	WO 9632743 A1 (ABB RESEARCH LIMITED), 17 October 1996 (17.10.96), figure 4, claims 1-13, abstract	1-14,18-22
E,Y	--	15-17
P,Y	EP 0697714 A1 (SAMSUNG ELECTRONICS CO., LTD.), 21 February 1996 (21.02.96), figure 1, abstract	16-18
Y	--	5-9
A	US 5384270 A (K. UENO), 24 January 1995 (24.01.95), column 2, line 37 - column 3, line 29, figures 1,2	1-4,10-23
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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17 March 1997	19.03.97
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 96/01206

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	Patent Abstracts of Japan, Vol 7,No 222, E-201, abstract of JP,A,58-112372 (yokoyama naoki), 4 July 1983 (04.07.83)	1,4-23
A		2,3
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Y	US 4030942 A (W.A. KEENAN ET AL), 21 June 1977 (21.06.77), column 2, line 28 - column 3, line 3; column 3, line 44 - column 4, line 50, figures 1,2	9,19
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