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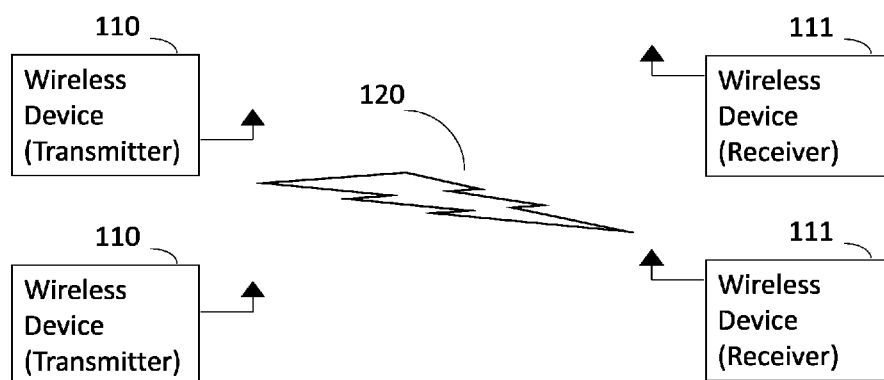
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(54) Title: SYNCHRONIZING A DIGITAL FREQUENCY SHIFT

FIG. 1



(57) Abstract: An apparatus and a method for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel are disclosed. For example, the method, by a synchronizer, transmits a DFS trigger to a Digital Front End (DFE) processor and a Local Oscillator (LO) trigger to an LO in a synchronous manner, the method, by the DFE processor, applies a DFS on received data in response to receiving the DFS trigger, the method, by the LO, applies a complementary shift on a carrier signal in response to receiving the LO trigger, the method, by the upconverter, digital-to-analog converts and radio frequency modulates the digital frequency-shifted received data and the complementary-shifted carrier signal. In another example, the method, by the synchronizer, transmits a phase error to a phase error corrector that performs a phase error correction.

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SYNCHRONIZING A DIGITAL FREQUENCY SHIFT

[0001] The present disclosure describes a method and an apparatus for synchronizing a Digital Frequency Shift (DFS). Although, the method is described for synchronizing a DFS in a device transmitting and/or receiving wireless signals over a wireless channel of a Long Term Evolution (LTE) network, the method may be implemented for signals transmitted and/or received over any type of wireless network, e.g., a 3G network, a 5G network, and the like.

BACKGROUND

[0002] A User Equipment (UE) may communicate with other network devices via a communication network. For example, a wireless UE may communicate with other wireless or wire based devices via a base station associated with a wireless communications network, e.g., an eNodeB. The UE comprises transmit and receive chains that are configured for enabling the UE to transmit and receive data wirelessly using a wireless signal via one or more antennas. As such, the UE may be referred to as a transmitter when it is transmitting data, and as a receiver when it is receiving data.

[0003] The transmit chain includes several components. When the input signal to the device traverses some nonlinear components in the transmit chain, the output includes additional unwanted signals at frequencies other than the frequency of the input signal. For example, harmonics may occur at multiples of the original frequencies and intermodulation products may occur at sums and differences of the original frequencies, and at multiples of the resulting sums and differences of those frequencies.

[0004] One approach to reduce the effect of the nonlinearity is to reduce a power level of the unwanted frequencies. For example, the power level of the unwanted intermodulation products may be reduced relative to the power level of the wanted frequencies. However, when the intermodulation products fall into sensitive regions of the frequency spectrum, e.g., within the duplex distance used for simultaneous transmission and reception, removing the unwanted frequencies may require high current consumption.

[0005] Another approach to reduce the effect of the nonlinearity is to apply a DFS in a digital baseband transmit chain and compensate for the DFS by applying a complementary shift (i.e., a complementary frequency offset) in the Local Oscillator (LO). However, the signals for applying the DFS and the complementary shift in the LO traverse different propagation paths in the device. Thus, the two shifts (i.e., the DFS and the complementary shift) may not coincide perfectly in order to reproduce an exact copy of the input signal. When the two shifts are applied at different times, a comparison of the signal before the two shifts and after the two shifts may include: an unwanted phase transient, and a static phase difference between the signal before the two shifts and the signal after the two shifts. Hence, schemes that focus on the amount of shift are sub-optimal in reproducing the input signal without phase transients and/or static phase errors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The teaching of the present disclosure can be more fully understood by reading the subsequent detailed description and examples in conjunction with references made to the accompanying drawings, in which:

[0007] FIG. 1 illustrates an exemplary wireless network for providing services to wireless devices;

[0008] FIG. 2 illustrates an exemplary apparatus for synchronizing a DFS for a signal to be transmitted over a wireless channel in accordance with the teachings of the present disclosure;

[0009] FIG. 3 illustrates an exemplary timing diagram in accordance with the present disclosure;

[0010] FIG. 4 illustrates a flowchart of an exemplary method for synchronizing a DFS in accordance with the present disclosure; and

[0011] FIG. 5 illustrates an exemplary device for performing the functions described in the present disclosure.

[0012] To facilitate reading, identical reference numbers are used to designate elements that are common to various figures, where possible.

DETAILED DESCRIPTION

[0013] The present disclosure relates to synchronizing a DFS such that the effect of nonlinearity on transmitted data is reduced. For example, in one aspect of the present disclosure, the DFS may be synchronized in a transmitter wireless device to reduce unwanted phase transients. In another aspect, a phase error may be corrected to remove static phase errors that cause phase discontinuities between consecutive data symbols. Although, the teaching of the present disclosure is described for signals of an LTE network, the apparatus and method of the present disclosure may be implemented for signals of other wireless communication networks, e.g., 3G networks, 5G networks, etc.

[0014] FIG. 1 illustrates a wireless network 100 for providing services to wireless devices. The wireless network comprises transmitter wireless devices 110 and receiver wireless devices 111 communicating over a wireless channel 120. For example, a transmitter wireless device 110 may be a user equipment. Similarly, a receiver wireless device 111 may be a user equipment. In addition, the transmitter or receiver wireless device may be a base station. It is noted that the antennas of the wireless devices 110 and 111 may be antennas of a transceiver that may be used for both transmitting and receiving of a wireless signal. As such, each transmitter or receiver wireless device may be a transmitter or a receiver, based on whether the device is receiving or transmitting the wireless signal.

[0015] As described above, the transmit chain of a device, e.g., wireless device 110, includes several components. For example, the transmit chain may include: a baseband processor, a Digital Front End (DFE) processor, a Local Oscillator (LO), an upconverter, an antenna, etc. The baseband processor may determine In-phase (I) and Quadrature (Q) components of the data (input). The I and Q components of the data may also be jointly referred to as "IQ data." The baseband processor may then provide the IQ data to the DFE processor. When the transmitter is a digital transmitter, the upconverter may comprise a Radio Frequency Digital to Analog Converter (RFDAC). When the transmitter is an analog transmitter, the upconverter may comprise: a baseband Digital to Analog Converter (DAC), an optional post-filter, and an IQ mixer.

[0016] The present disclosure describes a wireless device that provides a dedicated synchronizer. For example, in addition to the various components describes above, the wireless device of the present disclosure also provides a dedicated synchronizer. The dedicated synchronizer is for performing a DFS in the transmit device in a synchronized manner, thereby reducing unwanted phase transients and phase errors.

[0017] FIG. 2 illustrates an apparatus 200 for synchronizing a DFS for a signal to be transmitted over a wireless channel in accordance with the teachings of the present disclosure. The apparatus 200 is comprised within each transmitter wireless device 110 described above with respect to FIG. 1. The apparatus 200 comprises a synchronizer 210, a DFE processor 220, a LO 230, and an upconverter 240. In one aspect, the synchronizer 210 is a dedicated hardware.

[0018] In one aspect, the apparatus 200 also comprises a phase error corrector 250. In one aspect, the phase error corrector 250 is arranged to be part of the DFE processor 220, as shown in FIG. 2A. In another aspect, the phase error corrector 250 is arranged to be part of the LO 230, as shown in FIG. 2B.

[0019] The synchronizer 210 is operatively coupled to the DFE processor 220 and the LO 230. The DFE processor 220 and the LO 230 are operatively coupled to the upconverter 240.

[0020] In order to reduce phase transients, the synchronizer 210 is configured to transmit a DFS trigger to the DFE processor and an LO trigger to the LO in a synchronous manner. The DFS trigger is transmitted by the synchronizer 210 to trigger a DFS in the DFE processor. Similarly, the LO trigger is transmitted to the LO to trigger a complementary shift in the LO.

[0021] For clarity, the trigger transmitted by the synchronizer to the DFE processor is referred to as a “DFE trigger” and the trigger transmitted by the synchronizer to the LO is referred to as a “LO trigger.” When the type of LO is a phase-locked-loop, the trigger may also be referred to as a “PLL trigger.” In addition, it is noted that the shift in the LO is referred to as a “complementary shift” because the magnitude of the frequency offset performed by the LO is equal to the magnitude of frequency shift (i.e., the DFS) performed by the DFE processor, and the direction of frequency offset caused by the complementary shift is opposite to

the direction of frequency offset caused by the shift in the DFE processor. In other words, the DFE trigger and OL trigger are sent in a synchronized manner such that the complementary shift and the DFS cancel each other when the RF modulation is performed by the upconverter.

[0022] The DFE processor 220 is configured to apply the DFS on received data in response to receiving the DFE trigger from the synchronizer 210. For example, the DFE processor receives the data (e.g., the IQ data), applies a DFS on the received data in response to receiving a DFS trigger, processes the data, and provides the processed data to the upconverter 240. For example, the processing of the data by the DFE processor may include: converting from a first sampling rate to a second sampling rate, pulse shaping, filtering, performing gain control, etc.

[0023] The LO 230 is configured to apply a complementary shift on the carrier signal in response to receiving the LO trigger. For example, the LO 230 generates a carrier signal, applies a complementary shift on the carrier signal in response to receiving an LO trigger from the synchronizer 210, and provides the complementary-shifted carrier signal to the upconverter 240. In one aspect, the upconverter comprises an RFDAC. In another aspect, the upconverter comprises a baseband DAC, an optional post-filter, and an IQ mixer.

[0024] The upconverter 240 is configured to digital-to-analog convert and Radio Frequency (RF) modulate the digital frequency-shifted received data and the complementary-shifted carrier signal. The output of the RFDAC 240 is provided to an antenna for transmission. In other words, the data is encoded using the complementary-shifted carrier signal by performing RF modulation.

[0025] Note that the signal paths from the synchronizer 210 to the locations at which the DFS and the complementary shift (i.e., the shift in the LO) are unlikely to be the same. Similarly, the signal path between the LO and the upconverter is unlikely to be the same as the signal path between the DFE processor and the upconverter. The synchronizer 210 performs the synchronization of the DFE trigger and the LO trigger taking into account the differences in propagation delays for triggering the shifts at the two locations and for the two shifts to arrive at the

upconverter. Moreover, in one aspect, the correcting of the phase error may be to compensate for the difference in arrival times of the two shifts at the upconverter.

[0026] In one aspect, the synchronizer 210 is further configured to determine the phase error and transmit the phase error to a phase error corrector 250. The phase error corrector is configured to phase error correct the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[0027] The phase error correction provides additional advantages for some applications. For instance, suppose a device uses a transmitted signal as a reference for compensating for unwanted effects. Then, reducing static phase errors may be advantageous. For such applications, the phase error correction may be for removing static phase errors that cause phase discontinuities between consecutive data symbols.

[0028] In one aspect, the phase error correction is performed in a phase corrector arranged in the DFE processor. In one aspect, the phase error correction comprises rotating the In-phase and Quadrature components (i.e., the IQ data) to compensate for the phase error after applying the DFS. For example, the phase error correction may be to phase error correct the digital frequency-shifted received data. In one aspect, the phase error is created due to different arrival times of the DFS and complementary shifts at the upconverter 240.

[0029] In one aspect, the phase error correction is performed by a phase corrector arranged in the LO. In one aspect the phase error correction comprises adjusting a phase of the complementary-shifted carrier signal.

[0030] In one aspect, the phase error correction comprises applying DFS with a fractional delay in relation to the complementary shift in the LO. For example, a finer adjustment in the amount of DFS may be made to compensate for the additional phase error.

[0031] In one aspect, the synchronizer 210 of the present disclosure compensates for differences in sampling strobe rates used by the DFE processor 220 and the LO 230. For example, the synchronizer 210 transmits the DFS trigger and the LO trigger in a synchronous manner while compensating for differences in sampling strobe rates used by the DFE processor and the LO. In addition, the

synchronizer 210 has knowledge of a common clock rate of the device that is used for all blocks of the device. Note that the common clock rate, the sampling strobe rate of the DFE processor and the sampling strobe rate of the LO may all be different. The common clock rate and the sampling strobe rates for the DFE processor and LO are further described below, in Example–1 and FIG. 3.

[0032] The synchronizer 210 monitors sampling strobes of the DFE processor 220 and the LO 230. In addition, the synchronizer 210 is configured to have knowledge of:

- ideal application times of the DFS and complementary shift at the LO;
- a first latency, where the first latency is a latency for a signal to traverse from a first location to a second location, the first location being a location of the DFE processor at which the DFS is applied and the second location being a location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed;
- a second latency, where the second latency is a latency for a signal to traverse from a location of the LO at which the complementary shift is applied to the location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed; or
- a predetermined number of strobes to count for compensating for a difference between the first and second latencies.

[0033] In one aspect, the first latency is longer than the second latency. When the first latency is longer than the second latency, the synchronizer 210 computes the absolute time for triggering the DFS by subtracting the first latency from the ideal application time of the DFS.

[0034] In another aspect, the first latency is shorter than the second latency. When the first latency is shorter than the second latency, the synchronizer 210 computes the absolute time for triggering the complementary shift in the LO by subtracting the second latency from the ideal application time of the complementary shift in the LO.

[0035] The synchronizer 210 also monitors to determine whether a DFS event is triggered. The DFS event may be triggered by a Task List Processor (TLP) or a separate timer. When the DFS event is triggered, the synchronizer 210 may receive: a time for performing the DFS and a frequency shift (in Hertz) to be performed on received data, e.g., on IQ data. As noted above the DFE processor receives the IQ data from the baseband processor.

[0036] When the synchronizer 210 determines that a DFS event is triggered, the synchronizer transmits a DFS trigger to the DFE processor and an LO trigger to the LO in a synchronous manner for performing the DFS and the complementary shift, respectively.

[0037] The transmitting of the DFS trigger and the LO trigger in a synchronous manner may be implemented in a variety of aspects based on application. Examples 1-2 describe two aspects.

[0038]

[0039] Example -1

[0040] In one aspect, the transmitting of the DFS trigger to the DFE processor and the LO trigger to the LO in a synchronous manner comprises:

[0041] (1) Releasing a first trigger, wherein the first trigger is associated with the longer of the first latency and the second latency. The releasing of the first trigger applies either the DFS or the complementary shift, based on which shift is associated with the longer latency. For example, if the first latency (i.e., the latency of the DFE processor) is longer than the second latency, the first trigger is a DFE trigger and the DFS is applied in the DFE. In contrast, if the first latency is shorter than the second latency, the first trigger is an LO trigger and the complementary shift is applied in the LO.

[0042] (2) Starting a counter, referred to as a “delta counter”, for determining a time between when the first trigger is released, as described in (1), and detection of a first strobe associated with a second trigger that is to be released. For example, if the first trigger released in (1) is a DFE trigger, the delta counter is used to count a time until the first strobe of the LO is detected after the DFE trigger is released. Similarly, if the first

trigger released in (1) is an LO trigger, the delta counter is used to count the time until the first strobe of the DFE processor is detected after the LO trigger is released.

[0043] (3) Starting a strobes counter for counting a predetermined number of strobes for compensating for a difference between the first and second latencies. The predetermined number of strobes for compensating for the difference is known by the synchronizer.

[0044] (4) Stopping the delta counter upon detecting the first strobe associated with the second trigger that is to be released.

[0045] (5) If a phase error correction is implemented, determining a phase error. The determined phase error is computed from a frequency shift, the value of the delta counter, the values of the first and second latencies, the predetermined number of strobes for compensating for the difference between the first and second latencies, the sampling strobe rate (i.e., sampling clock rate) associated with the second trigger, and the common clock rate.

[0046] (6) When (5) is applicable, transmitting the determined phase error to the phase error corrector 250. The phase error corrector may be arranged to be either in the DFE processor 220 or LO 230.

[0047] (7) Releasing the second trigger when a value of the strobes counter reaches the predetermined number of strobes for compensating for the difference between the first and second latencies. The releasing of the second trigger applies the shift associated with the shorter latency.

[0048]

[0049] Example-2

[0050] In one aspect, the transmitting of the DFS trigger to the DFE processor and the LO trigger to the LO in a synchronous manner comprises:

[0051] (1) Releasing a first trigger, wherein the first trigger is associated with the longer of the first latency and the second latency. The releasing of the first trigger applies either the DFS or the complementary shift, based on which shift is associated with the longer latency.

[0052] (2) Starting a delta counter for determining a time between when the first trigger is released, as described in (1), and when a second trigger is to be released.

[0053] (3) Starting a strobes counter for counting a predetermined number of strobes for compensating for a difference between the first and second latencies.

[0054] (4) Detecting the first strobe associated with the second trigger that is to be released and determining a time for the second trigger. In one aspect, the time for the second trigger is determined from the predetermined number of strobes for compensating for the difference between the first and second latencies, a known strobes period, and a value of the delta counter when the second trigger is released.

[0055] (5) If a phase error correction is implemented, determining a phase error. The determined phase error is computed from a frequency shift, the value of the delta counter, the values of the first and second latencies, the sampling strobe rate (i.e., sampling clock rate) associated with the second trigger, and the common clock rate.

[0056] (6) When (5) is applicable, transmitting the determined phase error to the phase error corrector 250.

[0057] (7) Stopping the delta counter and releasing the second trigger when a value of the strobes counter reaches the predetermined number of strobes for compensating for the difference between the first and second latencies. The releasing of the second trigger applies the shift associated with the shorter latency.

[0058]

[0059] Note that, with the exception of the value of the delta counter, the synchronizer may have knowledge of values for computing the phase error prior to receiving the DFS event. Hence, in one aspect, as soon as the first strobe of the second trigger is detected, the phase error can be computed. Example-3, described below, further illustrates the computation of the phase error using aspects of Example-1, described above. It is important to note that values needed for the computation for which the synchronizer may not already have knowledge, the synchronizer may obtain the values when needed. For example, latency values may be retrieved from a database.

[0060] In one aspect, the phase error is determined without a delta counter. For example, the distances of both strobes and the strobe rates may be known. For instance, suppose both strobes are started at the same time or with a known (i.e., well-defined) distance. Then, for each strobe, a number of strobes until the DFS event is

triggered may be counted. Then, the strobe distance may be computed, without the delta counter, from the known strobe rates. This would allow to calculate the phase correction value at the first trigger (e.g. DFE trigger or LO trigger, based on which trigger is the first trigger).

Example-3: Computation of the Phase Error Correction

[0061] As described above in Example-1, the determined phase error may be computed from the frequency shift, the value of the delta counter, the values of the first and second latencies, the predetermined number of strobes for compensating for the difference between the first and second latencies, the sampling strobe rate associated with the second trigger, and the common clock rate. The determined phase error is computed below for the scenario in which the upconverter is an RFDAC. However, if the transmitter is an analog transmitter, the latencies are defined from a location of the DFE or LO at which the DFS shift or complementary shift is applied to the location of the upconverter at which the mixing occurs.

[0062] For ease of understanding, let:

- fshift: the amount of frequency shift,
- c_delta: final counter value of the delta counter,
- T_DFE: latency of DFE processor from a location of the DFE processor at which the DFS is applied to the RFDAC,
- T_PLL: latency of LO from application of the complementary frequency shift at the LO to the RFDAC,
- P: a predetermined number of LO strobes to count to compensate for a latency difference between T_DFE and T_PLL, when T_DFE is longer than T_PLL,
- D: a predetermined number of DFE processor strobes to count to compensate for a latency difference between T_PLL and T_DFE, when T_PLL is longer than T_DFE,
- fs_LO: a sampling strobe rate associated with the LO (i.e., a sampling rate of the LO),

- fs_DFE : a sampling strobe rate associated with the DFE processor (i.e., a sampling rate of the DFE processor,
- fs_clk : a clock rate common to all blocks,
- t_delta : time between the first trigger and the second trigger (i.e., time between a DFS trigger followed by an LO trigger or a time between an LO trigger followed by a DFS trigger),
- $delta\_error$: remaining time error between the arrival times of the DFS and the complementary frequency shift at the RFDAC,
- $phase\_error$: $delta\_error$ converted to phase error,
- $phase\_coeff$: a scalar value used for converting c_delta to the $phase\_error$, and
- phi_off : a scalar value used for converting the c_delta to the $phase\_error$.

[0063] Note that the values of t_delta , $delta\_error$, $phase\_error$, $phase\_coeff$, and phi_off are computed from the other parameters. The equations for determining the values of t_delta , $delta\_error$, $phase\_error$, $phase\_coeff$, and phi_off are provided below. The computation depends on whether the first trigger is for the DFE processor or for the LO.

[0064] When the first trigger is for the DFE processor:

$$t\_delta = (c\_delta / fs\_clk) + (P / fs\_LO), \quad (\text{Equation 1})$$

$$delta\_error = t\_DFE - t\_PLL - t\_delta; \quad (\text{Equation 2})$$

$$phase\_error = 2 * \pi * fshift * delta\_error \quad (\text{Equation 3})$$

$$= 2 * \pi * fshift * (t\_DFE - t\_PLL - t\_delta)$$

$$= 2 * \pi * fshift * (t\_DFE - t\_PLL - (c\_delta / fs\_clk) - (P / fs\_LO))$$

$$= 2 * \pi * fshift * (t\_DFE - t\_PLL - (P / fs\_LO))$$

$$- 2 * \pi * fshift * (c\_delta / fs\_clk),$$

$$= phi\_off - phase\_coeff * c\_delta,$$

wherein,

$$phi\_off = 2 * \pi * fshift * (t\_DFE - t\_PLL - (P / fs\_LO)), \text{ and} \quad (\text{Equation 4})$$

$$\text{phase\_coeff} = 2\pi \cdot \text{fshift} / \text{fs\_clk}. \quad (\text{Equation 5})$$

[0065] When the first trigger is for the LO:

$$t\_delta = (c\_delta / \text{fs\_clk}) + (D / \text{fs\_DFE}), \quad (\text{Equation 6})$$

$$\text{delta\_error} = t\_PLL - t\_DFE - t\_delta; \quad (\text{Equation 7})$$

$$\text{phase\_error} = 2\pi \cdot \text{fshift} \cdot \text{delta\_error} \quad (\text{Equation 8})$$

$$= 2\pi \cdot \text{fshift} \cdot (t\_PLL - t\_DFE - t\_delta)$$

$$= 2\pi \cdot \text{fshift} \cdot (t\_PLL - t\_DFE - (c\_delta / \text{fs\_clk}) - (D / \text{fs\_DFE}))$$

$$= 2\pi \cdot \text{fshift} \cdot (t\_PLL - t\_DFE - (D / \text{fs\_DFE}))$$

$$- 2\pi \cdot \text{fshift} \cdot (c\_delta / \text{fs\_clk}),$$

$$= \text{phi\_off} - \text{phase\_coeff} \cdot c\_delta,$$

wherein,

$$\text{phi\_off} = 2\pi \cdot \text{fshift} \cdot (t\_PLL - t\_DFE - (D / \text{fs\_DFE})), \text{ and} \quad (\text{Equation 9})$$

$$\text{phase\_coeff} = 2\pi \cdot \text{fshift} / \text{fs\_clk}. \quad (\text{Equation 10})$$

[0066] FIG. 3 illustrates a timing diagram 300 in accordance with the present disclosure. For the illustrative example, the sampling strobe rate 301 for the DFE processor (i.e., fs_DFE) is set to 9.6MHz. Similarly, for the LO, the sampling strobe rate 302 (i.e., fs_LO) is set to 19.2MHz. The common clock frequency 303 (i.e., fs_clk) is set to 153.6MHz. The timing diagram 300 is for a scenario in which the t_DFE 304 is longer than the t_PLL 305. The value of c_delta is known as soon as the delta counter stops, as shown in 306. The time between application of the DFS and application of the complementary shift is shown in 307. Then, equations 1-5 may be used to determine the appropriate phase correction. It is noted that the illustration of FIG. 3 and the sampling strobe rates are exemplary and not intended to limit the implementation. As such, any other sampling strobe rate may be used.

[0067] FIG. 4 illustrates a flowchart of an example method 400 for synchronizing a Digital Frequency Shift (DFS) in accordance with the present disclosure.

[0068] In one aspect of the present disclosure, the method 400 may be implemented in a wireless device that comprises one or more antennas configured to transmit a wireless signal and an apparatus, e.g., apparatus 200, for synchronizing a DFS for the

signal to be transmitted over the wireless channel. For example, the method 400 may be implemented in an apparatus 200 wherein the synchronizing is performed by synchronizer 210, applying a DFS is performed by DFE processor 220, applying a complementary shift is performed by LO 230, and the digital to analog converting and RF modulating are performed by upconverter 240, as described above. In another example, the method 400 may be implemented in an apparatus 200 wherein phase error correcting is performed by phase error corrector 250. In another example, the method 400 may be implemented in a device 500, described below.

[0069] The method 400 starts in a step 405 and proceeds to step 410.

[0070] In step 410, the method, by a synchronizer 210, transmits a DFS trigger to a DFE processor and an LO trigger to an LO in a synchronous manner.

[0071] In step 420, the method, by the DFE processor 220, in response to receiving the DFS trigger, applies a DFS on received data.

[0072] In step 430, the method, by the LO 230, in response to receiving the LO trigger, applies a complementary shift on a carrier signal.

[0073] In step 440, the method, by the upconverter 240, digital-to-analog converts and radio frequency modulates the digital frequency-shifted received data and the complementary-shifted carrier signal.

[0074] In optional step 450, the method, by the synchronizer 210, determines a phase error and provides the determined phase error to a phase error corrector 250.

[0075] In optional step 460, the method, by the phase error corrector 250, phase error corrects the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[0076] The method may then proceed to step 470 to end the synchronizing of the DFS or to step 405 to receive DFS events for triggering more synchronization of DFSs in accordance with the present disclosure.

[0077] FIG. 5 illustrates a device 500 for performing the function described in the present disclosure. The device 500 comprises a processor 501 and a memory 502 configured to store program instructions to be executed by the processor 501, where executing the program instructions causes the processor 501 to perform operations for synchronizing a DFS for a signal to be transmitted over a wireless channel, the

operations comprise, transmitting a DFS trigger to a DFE processor and an LO trigger to an LO in a synchronous manner, applying a DFS on received data in response to receiving the DFS trigger, applying a complementary shift on a carrier signal in response to receiving the LO trigger, and digital to analog converting and RF modulating the digital frequency-shifted received data and the complementary-shifted carrier signal. In addition, the operations may further comprise performing a phase error correction. The device 500 may further comprise any number and type of input/output devices 503.

[0078] It is noted that although FIG. 5 illustrates a single device, the method 400 may be implemented via any number of devices performing the operations of method 400 in a distributed manner, serial manner, or a combination thereof. In addition, the devices may be virtualized devices instantiated on servers (e.g., servers of a cloud network). As such, the representation of the hardware components of the device may be a virtualized or a physical representation, without departing from the teaching of the present disclosure. Accordingly, the method 400 may be implemented in hardware, software, or a combination thereof. It is noted that the processor 501 executing the program instructions includes the processor 501 performing the operations of the method 400 directly or indirectly. For example, the processor 501 may perform the operations in conjunction with other devices or may direct another device to perform the operations.

[0079] The following examples pertain to further embodiments.

[0080] Example 1 is an apparatus for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the apparatus comprising: a synchronizer configured to transmit a DFS trigger and a Local Oscillator (LO) trigger in a synchronous manner; a Digital Front End (DFE) processor, operatively coupled to the synchronizer, and configured to, in response to receiving the DFS trigger, apply a DFS on received data; an LO, operatively coupled to the synchronizer, and configured to, in response to receiving the LO trigger, apply a complementary shift on a carrier signal; and an upconverter operatively coupled to the DFE processor and the LO, and configured to digital-to-analog convert and radio frequency modulate the digital frequency-shifted received data and the complementary-shifted carrier signal.

[0081] In Example 2, the subject matter of Example 1, wherein the synchronizer is further configured to determine a phase error of the digital frequency-shifted received data, and wherein the apparatus further comprises: a phase error corrector configured to phase error correct the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[0082] In Example 3, the subject matter of Example 2, wherein the phase error corrector is arranged to be part of the DFE processor.

[0083] In Example 4, the subject matter of Example 3, wherein the phase error correction comprises rotating In-phase and Quadrature components of the digital frequency-shifted received data.

[0084] In Example 5, the subject matter of Example 3, wherein a phase error correction comprises applying the DFS with a fractional delay in relation to the complementary shift in the LO.

[0085] In Example 6, the subject matter of Example 2, wherein the phase error corrector is arranged to be part of the LO.

[0086] In Example 7, the subject matter of Example 6, wherein the phase error correction comprises adjusting a phase of the complementary-shifted carrier signal.

[0087] In Example 8, the subject matter of Example 2, wherein the phase error correction is based on differences in arrival times of the DFS and the complementary shift at the upconverter.

[0088] In Example 9, the subject matter of Example 1, wherein the synchronizer is a dedicated hardware.

[0089] In Example 10, the subject matter of Example 1, wherein the synchronizer is configured to transmit the DFS trigger to the DFE processor and the LO trigger to the LO upon a DFS event being triggered.

[0090] In Example 11, the subject matter of Example 10, wherein the DFS event is triggered by a task list processor or a separate timer.

[0091] In Example 12, the subject matter of Example 10, wherein the synchronizer is configured to receive, when the DFS event is triggered, a frequency shift to be performed on the received data.

[0092] In Example 13, the subject matter of Example 1, wherein the synchronizer is configured to have knowledge of: ideal application times of the DFS and complementary shift at the LO, a first latency, where the first latency is a latency for a signal to traverse from a first location to a second location, the first location being a location of the DFE processor at which the DFS is applied and the second location being a location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed, a second latency, where the second latency is a latency for a signal to traverse from a location of the LO at which the complementary shift is applied to the location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed, or a predetermined number of strobes to count for compensating for a difference between the first and second latencies.

[0093] In Example 14, the subject matter of Example 13, wherein the synchronizer configured to transmit the DFS trigger and the LO trigger in the synchronous manner comprises configuring for: releasing a first trigger, wherein the first trigger is associated with a longer of the first latency and the second latency; starting a delta counter for determining a time between when the first trigger is released and detection of a first strobe associated with a second trigger that is to be released; starting a strobe counter for counting a predetermined number of strobes for compensating for a difference between the first and second latencies; detecting the first strobe associated with the second trigger that is to be released; and releasing the second trigger when a value of the strobe counter reaches the predetermined number of strobes for compensating for the difference between the first and second latencies.

[0094] In Example 15, the subject matter of Example 14, wherein the synchronizer is configured to: determine a phase error; and transmit the determined phase error to a phase error corrector.

[0095] In Example 16, the subject matter of Example 15, wherein the determined phase error is computed from a frequency shift, the value of the delta counter, the values of the first and second latencies, the predetermined number of strobes for

compensating for the difference between the first and second latencies, a sampling strobe rate associated with the second trigger, and a common clock rate.

[0096] In Example 17, the subject matter of Example 10, wherein the first latency is longer than the second latency.

[0097] In Example 18, the subject matter of Example 10, wherein the first latency is shorter than the second latency.

[0098] In Example 19, the subject matter of Example 1, wherein the synchronizer transmits the DFS trigger to the DFE processor and the LO trigger to the LO in a synchronous manner while compensating for differences in sampling strobe rates used by the DFE processor and the LO.

[0099] Example 20 is a wireless device, comprising: one or more antennas configured to transmit a signal; and the apparatus for synchronizing a DFS for the signal to be transmitted over a wireless channel of Example 1.

[00100] In Example 21, the subject matter of Example 20, wherein the synchronizer is further configured to determine a phase error and provide the phase error to a phase error corrector configured to perform phase error correction.

[00101] Example 22 is a method for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the method comprising: transmitting, by a synchronizer, a DFS trigger to a Digital Front End (DFE) processor and a Local Oscillator (LO) trigger to an LO in a synchronous manner; applying, by the DFE processor, in response to receiving the DFS trigger a DFS on received data; applying, by the LO, in response to receiving the LO trigger a complementary shift on a carrier signal; and digital-to-analog converting and radio frequency modulating, by an upconverter, the digital frequency-shifted received data and the complementary-shifted carrier signal.

[00102] In Example 23, the subject matter of Example 22, further comprising: determining, by the synchronizer, a phase error in the digital frequency-shifted received data; and phase error correcting, by a phase error corrector, the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[00103] Example 24 is a device, comprising: a processor; and a memory configured to store a program instructions to be executed by the processor, where executing the program instructions causes the processor to perform operations for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the operations comprising: transmitting, by a synchronizer, a DFS trigger to a Digital Front End (DFE) processor and a Local Oscillator (LO) trigger to an LO in a synchronous manner; applying, by the DFE processor in response to receiving the DFS trigger, a DFS on received data; applying, by the LO in response to receiving the LO trigger, a complementary shift on a carrier signal; and digital-to-analog converting and radio frequency modulating, by an upconverter, the digital frequency-shifted received data and the complementary-shifted carrier signal.

[00104] In Example 25, the subject matter of Example 24, the operations further comprising: determining, by the synchronizer, a phase error in the digital frequency-shifted received data; and phase error correcting, by a phase error corrector, the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[00105] Example 26 is a n apparatus for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the apparatus comprising: a synchronizing means for transmitting transmit a DFS trigger and a Local Oscillator (LO) trigger in a synchronous manner; a Digital Front End (DFE) processing means, operatively coupled to the synchronizer, and for, in response to receiving the DFS trigger, applying a DFS on received data; an LO, operatively coupled to the synchronizing means, and for, in response to receiving the LO trigger, applying a complementary shift on a carrier signal; and an upconverting means operatively coupled to the DFE processor and the LO, and for digital-to-analog converting and radio frequency modulating the digital frequency-shifted received data and the complementary-shifted carrier signal.

[00106] In Example 27, the subject matter of Example 26, wherein the synchronizing means is further for determining a phase error of the digital frequency-shifted received data, and wherein the apparatus further comprises: a phase error correcting means for to phase error correcting the digital frequency-

shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

[00107] In Example 28, the subject matter of Example 27, wherein the phase error correcting means is arranged to be part of the DFE processing means.

[00108] In Example 29, the subject matter of Example 28, wherein the phase error correction comprises rotating In-phase and Quadrature components of the digital frequency-shifted received data.

[00109] In Example 30, the subject matter of Example 28, wherein a phase error correction comprises applying the DFS with a fractional delay in relation to the complementary shift in the LO.

[00110] In Example 31, the subject matter of Example 27, wherein the phase error correcting means is arranged to be part of the LO.

[00111] In Example 32, the subject matter of Example 31, wherein the phase error correction comprises adjusting a phase of the complementary-shifted carrier signal.

[00112] In Example 33, the subject matter of Example 27, wherein the phase error correction is based on differences in arrival times of the DFS and the complementary shift at the upconverter.

[00113] In Example 34, the subject matter of Example 26, wherein the synchronizing means is a dedicated hardware.

[00114] In Example 35, the subject matter of Example 26, wherein the synchronizing means is for transmitting the DFS trigger to the DFE processor and the LO trigger to the LO upon a DFS event being triggered.

[00115] In Example 36, the subject matter of Example 35, wherein the DFS event is triggered by a task list processor or a separate timer.

[00116] In Example 37, the subject matter of Example 35, wherein the synchronizing means is for receiving, when the DFS event is triggered, a frequency shift to be performed on the received data.

[00117] In Example 38, the subject matter of Example 26, wherein the synchronizing means has knowledge of: ideal application times of the DFS and complementary shift at the LO, a first latency, where the first latency is a latency for a signal to traverse from a first location to a second location, the first location being

a location of the DFE processor at which the DFS is applied and the second location being a location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed, a second latency, where the second latency is a latency for a signal to traverse from a location of the LO at which the complementary shift is applied to the location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed, or a predetermined number of strobes to count for compensating for a difference between the first and second latencies.

[00118] In Example 39, the subject matter of Example 38, wherein the synchronizing means is for transmitting the DFS trigger and the LO trigger in the synchronous manner comprises: releasing a first trigger, wherein the first trigger is associated with a longer of the first latency and the second latency; starting a delta counter for determining a time between when the first trigger is released and detection of a first strobe associated with a second trigger that is to be released; starting a strobe counter for counting a predetermined number of strobes for compensating for a difference between the first and second latencies; detecting the first strobe associated with the second trigger that is to be released; and releasing the second trigger when a value of the strobe counter reaches the predetermined number of strobes for compensating for the difference between the first and second latencies.

[00119] In Example 40, the subject matter of Example 39, wherein the synchronizing means is for: determining a phase error; and transmitting the determined phase error to a phase error corrector.

[00120] In Example 41, the subject matter of Example 40, wherein the determined phase error is computed from a frequency shift, the value of the delta counter, the values of the first and second latencies, the predetermined number of strobes for compensating for the difference between the first and second latencies, a sampling strobe rate associated with the second trigger, and a common clock rate.

[00121] In Example 42, the subject matter of Example 35, wherein the first latency is longer than the second latency.

[00122] In Example 43, the subject matter of Example 35, wherein the first latency is shorter than the second latency.

[00123] In Example 44, the subject matter of Example 26, wherein the synchronizing means is for transmitting the DFS trigger to the DFE processor and the LO trigger to the LO in a synchronous manner while compensating for differences in sampling strobe rates used by the DFE processor and the LO.

[00124] Example 45 is a wireless device, comprising: one or more antennas configured to transmit a signal; and the apparatus for synchronizing a DFS for the signal to be transmitted over a wireless channel of Example 26.

[00125] In Example 46, the subject matter of Example 45, wherein the synchronizing means is further for determining a phase error and provide the phase error to a phase error corrector configured to perform phase error correction.

[00126] It should be understood that the aspects of the present disclosure are described above by way of examples. However, the various aspects are exemplary and not limitations. Thus, the scope of the present disclosure should not be construed as being limited by any of the above aspects or examples. The breadth and the scope of the present disclosure should be defined in accordance with the scope and breadth of the following claims and/or equivalents.

What is claimed is:

1. An apparatus for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the apparatus comprising:

a synchronizing means for transmitting transmit a DFS trigger and a Local Oscillator (LO) trigger in a synchronous manner;

a Digital Front End (DFE) processing means, operatively coupled to the synchronizer, and for, in response to receiving the DFS trigger, applying a DFS on received data;

an LO, operatively coupled to the synchronizing means, and for, in response to receiving the LO trigger, applying a complementary shift on a carrier signal; and

an upconverting means operatively coupled to the DFE processor and the LO, and for digital-to-analog converting and radio frequency modulating the digital frequency-shifted received data and the complementary-shifted carrier signal.

2. The apparatus of claim 1,

wherein the synchronizing means is further for determining a phase error of the digital frequency-shifted received data, and

wherein the apparatus further comprises:

a phase error correcting means for to phase error correcting the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

3. The apparatus of claim 2, wherein the phase error correcting means is arranged to be part of the DFE processing means.

4. The apparatus of claim 3, wherein the phase error correction comprises rotating In-phase and Quadrature components of the digital frequency-shifted received data.

5. The apparatus of claim 3, wherein a phase error correction comprises applying the DFS with a fractional delay in relation to the complementary shift in the LO.
6. The apparatus of claim 2, wherein the phase error correcting means is arranged to be part of the LO.
7. The apparatus of claim 6, wherein the phase error correction comprises adjusting a phase of the complementary-shifted carrier signal.
8. The apparatus of claim 2, wherein the phase error correction is based on differences in arrival times of the DFS and the complementary shift at the upconverter.
9. The apparatus of claim 1, wherein the synchronizing means is a dedicated hardware.
10. The apparatus of claim 1, wherein the synchronizing means is for transmitting the DFS trigger to the DFE processor and the LO trigger to the LO upon a DFS event being triggered.
11. The apparatus of claim 10, wherein the DFS event is triggered by a task list processor or a separate timer.
12. The apparatus of claim 10, wherein the synchronizing means is for receiving, when the DFS event is triggered, a frequency shift to be performed on the received data.
13. The apparatus of claim 1, wherein the synchronizing means has knowledge of: ideal application times of the DFS and complementary shift at the LO,

a first latency, where the first latency is a latency for a signal to traverse from a first location to a second location, the first location being a location of the DFE processor at which the DFS is applied and the second location being a location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed,

a second latency, where the second latency is a latency for a signal to traverse from a location of the LO at which the complementary shift is applied to the location of the upconverter at which the digital frequency-shifted received data and the complementary shifted carrier signal are mixed, or

a predetermined number of strobes to count for compensating for a difference between the first and second latencies.

14. The apparatus of claim 13, wherein the synchronizing means is for transmitting the DFS trigger and the LO trigger in the synchronous manner comprises:

releasing a first trigger, wherein the first trigger is associated with a longer of the first latency and the second latency;

starting a delta counter for determining a time between when the first trigger is released and detection of a first strobe associated with a second trigger that is to be released;

starting a strobe counter for counting a predetermined number of strobes for compensating for a difference between the first and second latencies;

detecting the first strobe associated with the second trigger that is to be released;
and

releasing the second trigger when a value of the strobe counter reaches the predetermined number of strobes for compensating for the difference between the first and second latencies.

15. The apparatus of claim 14, wherein the synchronizing means is for:

determining a phase error; and

transmitting the determined phase error to a phase error corrector.

16. The apparatus of claim 15, wherein the determined phase error is computed from a frequency shift, the value of the delta counter, the values of the first and second latencies, the predetermined number of strobes for compensating for the difference between the first and second latencies, a sampling strobe rate associated with the second trigger, and a common clock rate.

17. The apparatus of claim 10, wherein the first latency is longer than the second latency.

18. The apparatus of claim 10, wherein the first latency is shorter than the second latency.

19. The apparatus of claim 1, wherein the synchronizing means is for transmitting the DFS trigger to the DFE processor and the LO trigger to the LO in a synchronous manner while compensating for differences in sampling strobe rates used by the DFE processor and the LO.

20. A wireless device, comprising:
one or more antennas configured to transmit a signal; and
the apparatus for synchronizing a DFS for the signal to be transmitted over a wireless channel of claim 1.

21. The wireless device of claim 20, wherein the synchronizing means is further for determining a phase error and provide the phase error to a phase error corrector configured to perform phase error correction.

22. A method for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the method comprising:

transmitting, by a synchronizer, a DFS trigger to a Digital Front End (DFE) processor and a Local Oscillator (LO) trigger to an LO in a synchronous manner;

applying, by the DFE processor, in response to receiving the DFS trigger a DFS on received data;

applying, by the LO, in response to receiving the LO trigger a complementary shift on a carrier signal; and

digital-to-analog converting and radio frequency modulating, by an upconverter, the digital frequency-shifted received data and the complementary-shifted carrier signal.

23. The method of claim 22, further comprising:

determining, by the synchronizer, a phase error in the digital frequency-shifted received data; and

phase error correcting, by a phase error corrector, the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

24. A device, comprising:

a processor; and

a memory configured to store a program instructions to be executed by the processor, where executing the program instructions causes the processor to perform operations for synchronizing a Digital Frequency Shift (DFS) for a signal to be transmitted over a wireless channel, the operations comprising:

transmitting, by a synchronizer, a DFS trigger to a Digital Front End (DFE) processor and a Local Oscillator (LO) trigger to an LO in a synchronous manner;

applying, by the DFE processor in response to receiving the DFS trigger, a DFS on received data;

applying, by the LO in response to receiving the LO trigger, a complementary shift on a carrier signal; and

digital-to-analog converting and radio frequency modulating, by an upconverter, the digital frequency-shifted received data and the complementary-shifted carrier signal.

25. The device of claim 24, the operations further comprising:
- determining, by the synchronizer, a phase error in the digital frequency-shifted received data; and
 - phase error correcting, by a phase error corrector, the digital frequency-shifted received data or the complementary-shifted carrier signal, based on the determined phase error.

100

FIG. 1

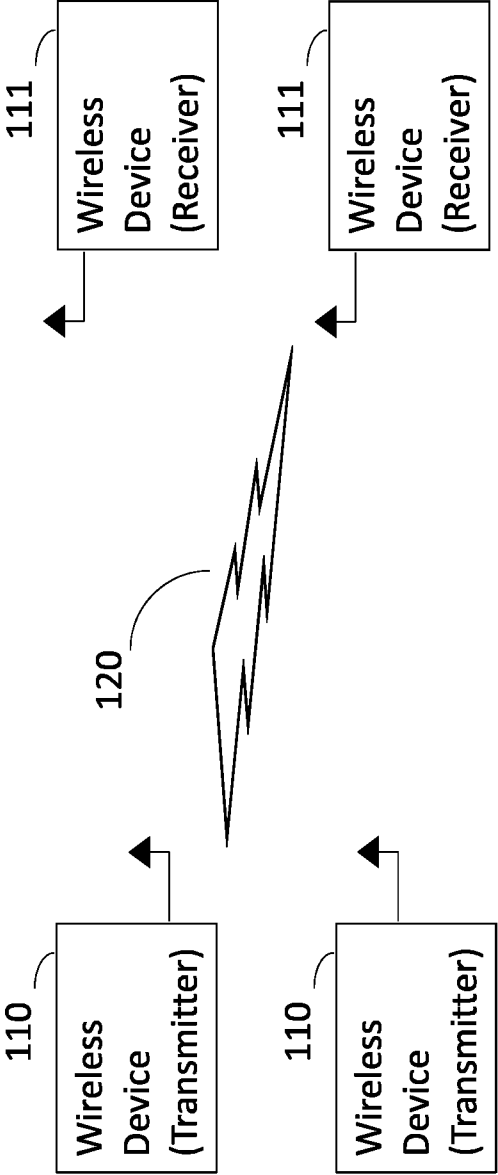
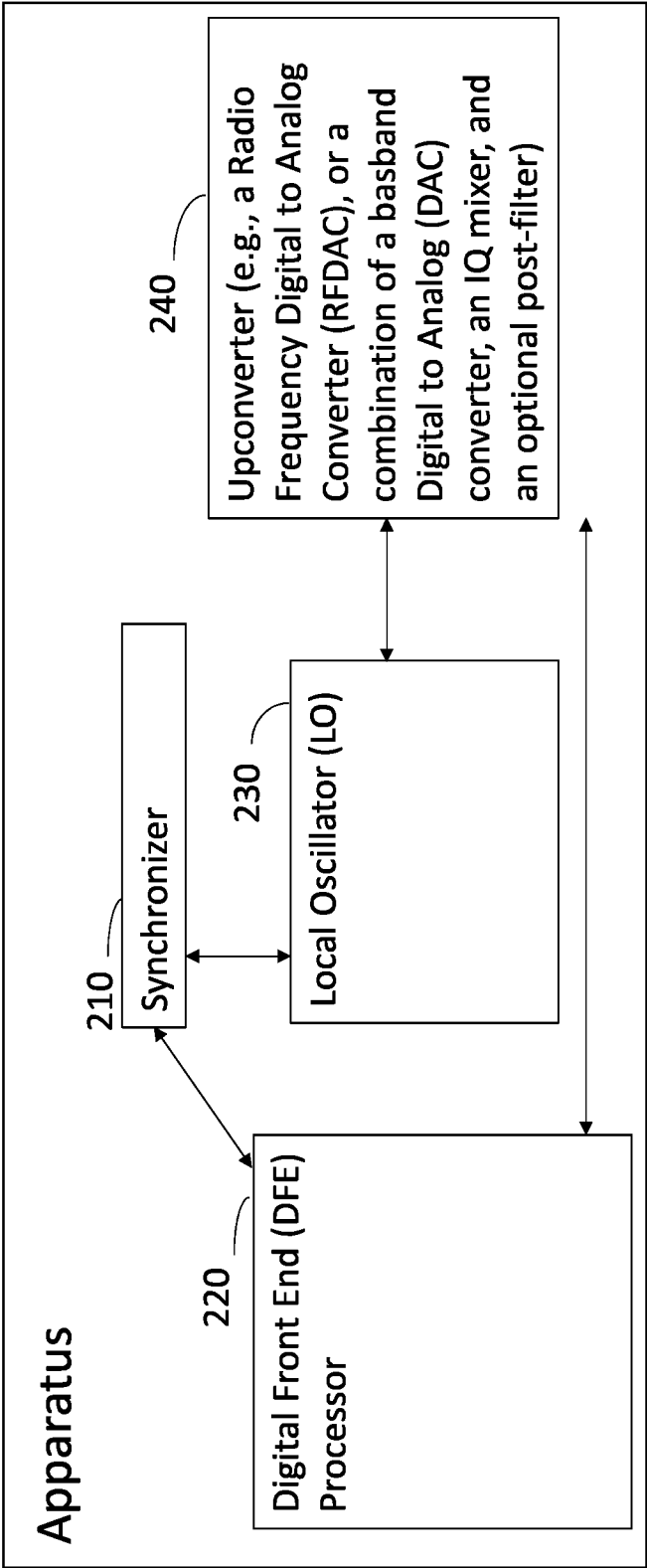


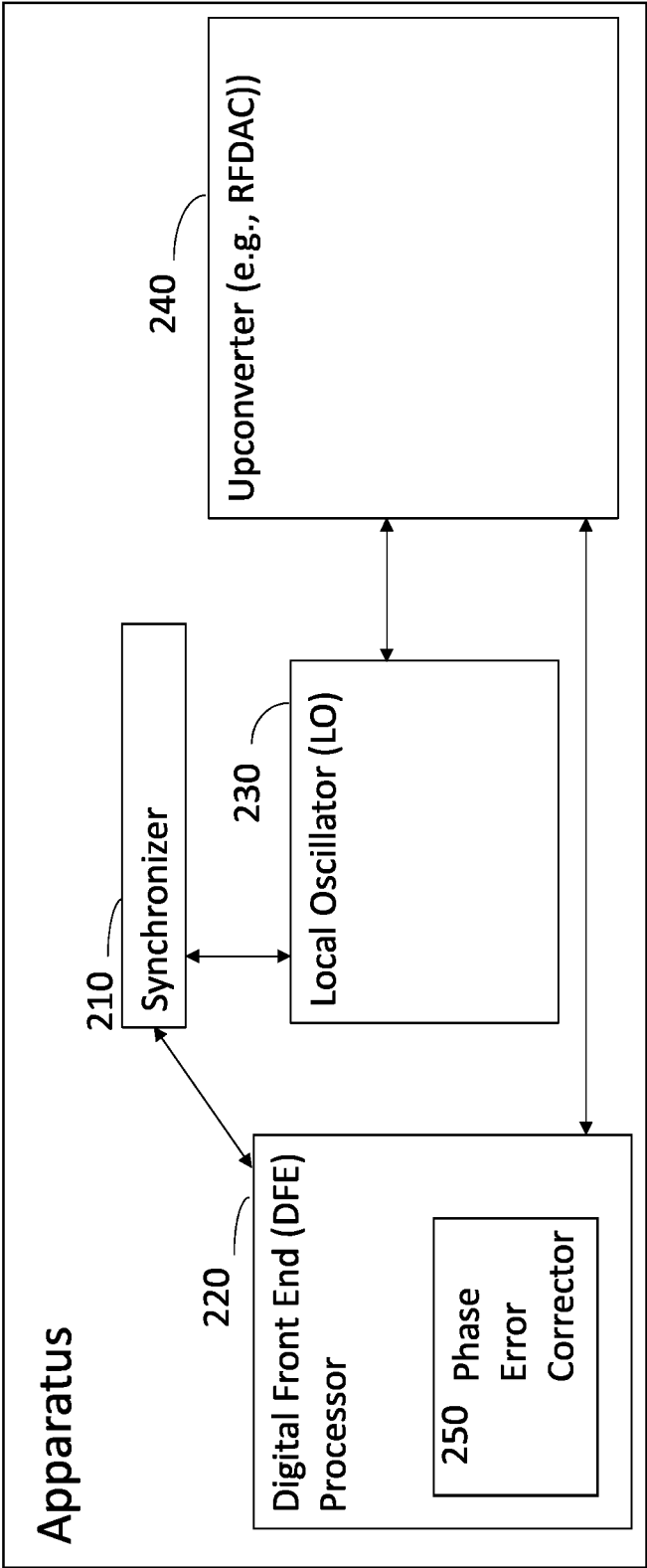
FIG. 2

200



200

FIG. 2A



200

FIG. 2B

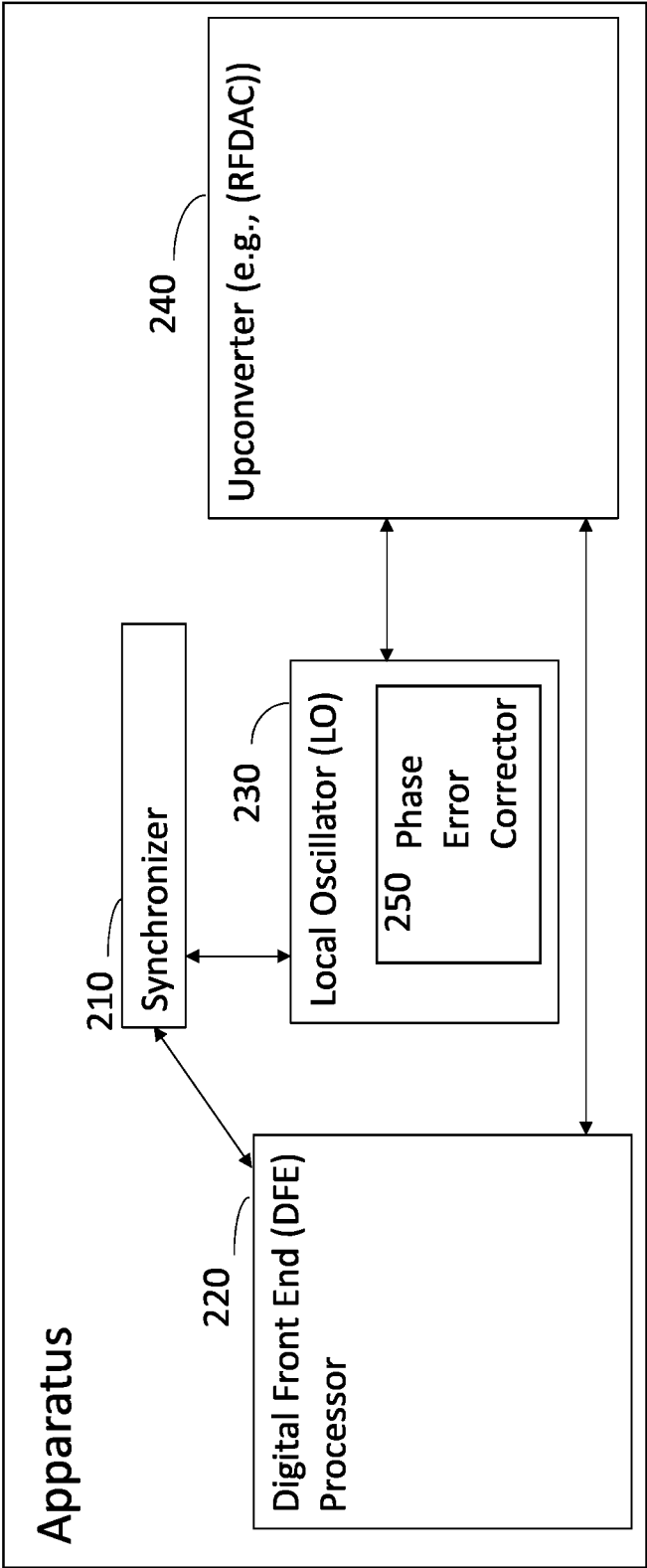


FIG. 3

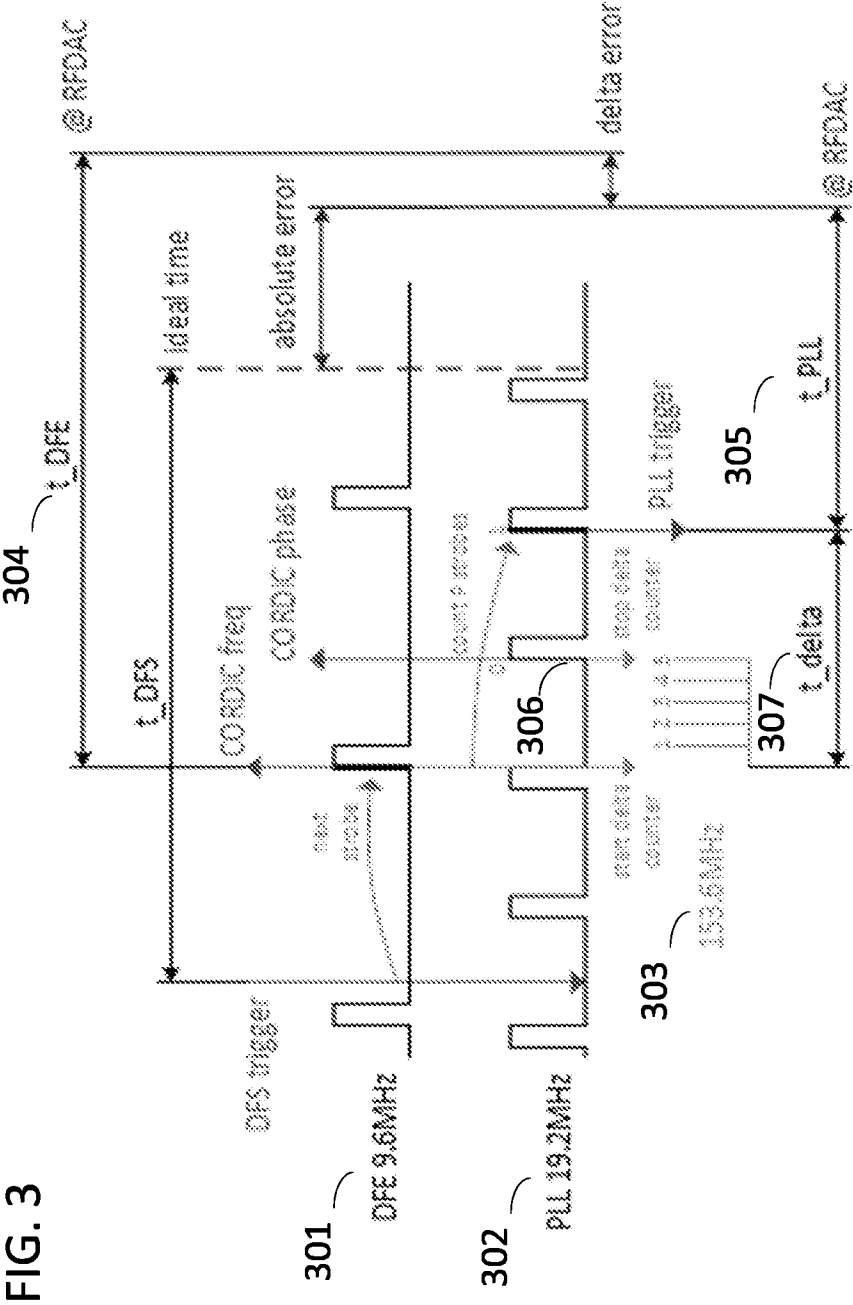
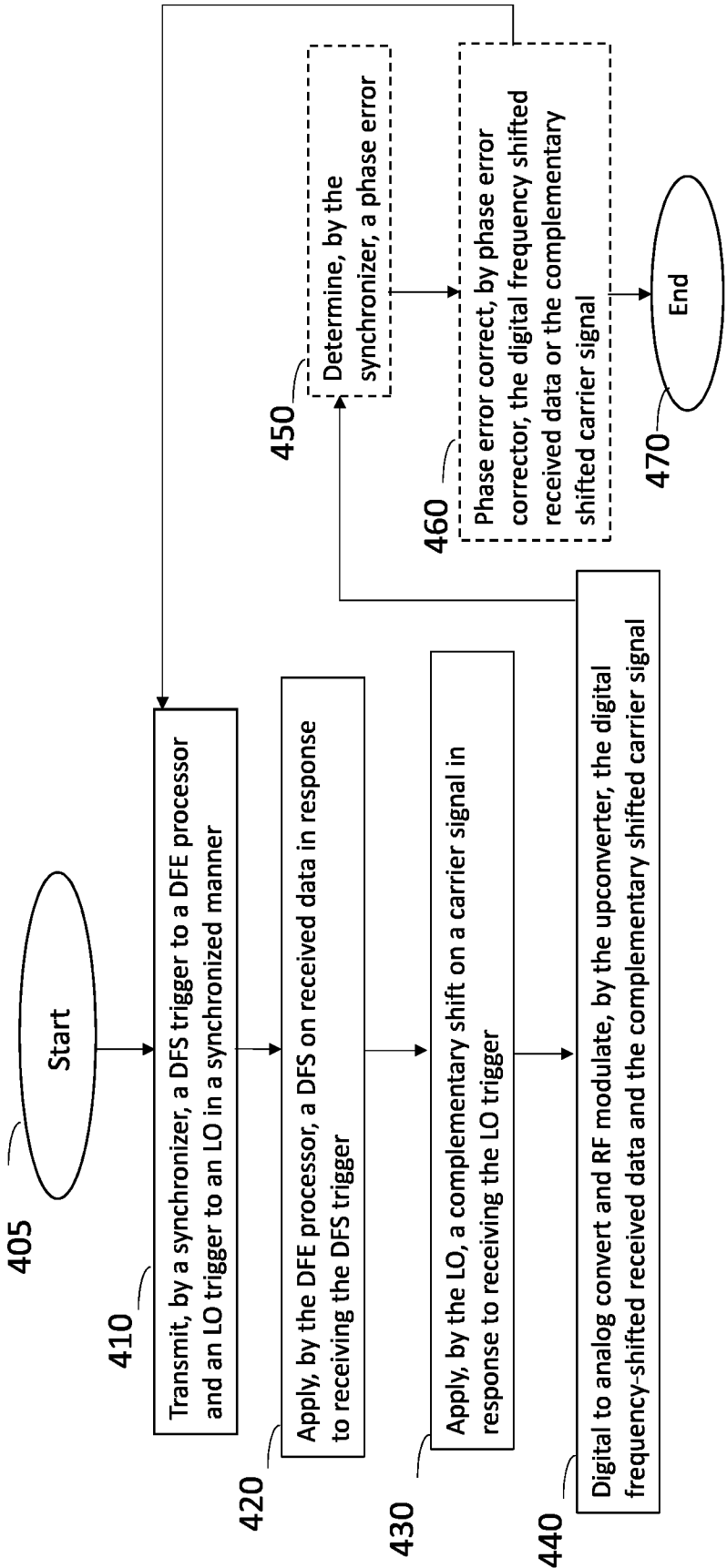


FIG. 4

400



500

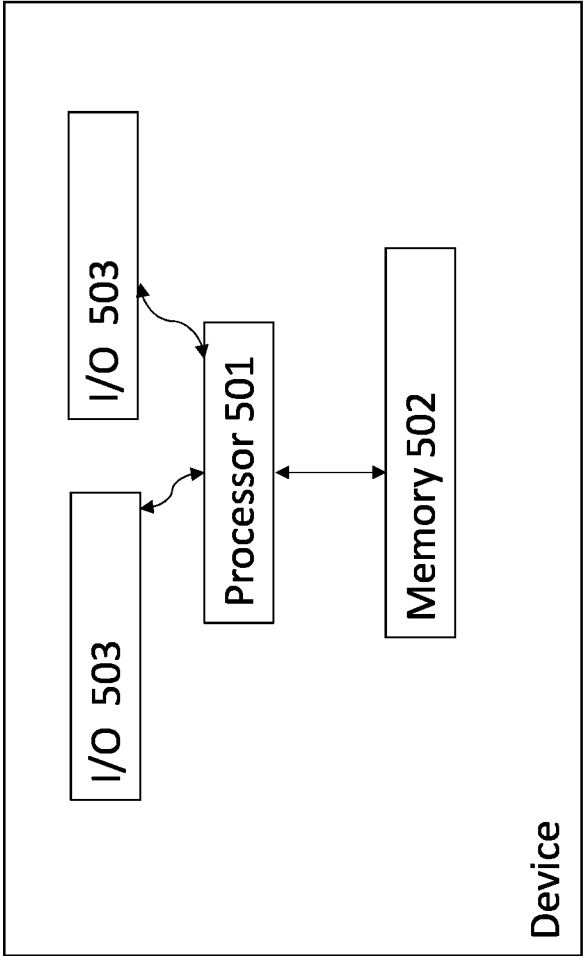


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2017/025647

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(8) - H04L 25/02; H04L 27/04; H04L 27/22 (2017.01)
 CPC - G01S 7/282; H04B 1/04; H04L 27/04 (2017.02)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 370/203; 370/350; 375/309 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2015/0282171 A1 (NOKIA SIEMENS NETWORKS OY) 01 October 2015 (01.10.2015) entire document	1-25
Y	US 9,490,826 B1 (QUALCOMM INCORPORATED) 08 November 2016 (08.11.2016) entire document	1-25
Y	US 2013/0035099 A1 (BOEJER et al) 07 February 2013 (07.02.2013) entire document	8, 14-18
A	US 2006/0067429 A1 (BEYER et al) 30 March 2006 (30.03.2006) entire document	1-25
A	US 2005/0207334 A1 (HADAD) 22 September 2005 (22.09.2005) entire document	1-25
A	US 2014/0369442 A1 (HUAWEI TECHNOLOGIES CO LTD) 18 December 2014 (18.12.2014) entire document	1-25
A	US 2004/0086070 A1 (SACHSE et al) 06 May 2004 (06.05.2004) entire document	1-25

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 May 2017

Date of mailing of the international search report

21 JUN 2017

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