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[Continued on next page]

(54) Title: DIGITAL SIGNAL ROUTING CIRCUIT

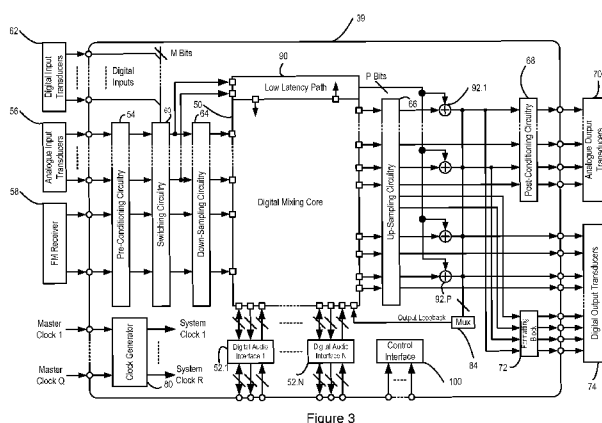


Figure 3

(57) **Abstract:** An integrated circuit is used for digital signal routing. The integrated circuit has analog and digital inputs and outputs, including digital interfaces for connection to other integrated circuits. Inputs, including the digital interfaces, act as data sources. Outputs, including the digital interfaces, act as data destinations. The integrated circuit also includes signal processing blocks, which can act as data sources and data destinations. Signal routing is achieved by means of a multiply-accumulate block, which takes data from one or more data source and, after any required scaling, generates output data for a data destination. Data from a data source is buffered for an entire period of a data sample clock so that the multiply-accumulate block can retrieve the data at any point in the period, and output data of the multiply-accumulate block is buffered for an entire period of the data sample clock so that the data destination can retrieve the data at any point in the period. Multiple signal paths can be defined by configuration data supplied to the device, either by a user, or by software. The multiply-accumulate block operates on a time division multiplexed basis, so that multiple signal paths can be processed within one period of the sample clock. Each signal path has a respective sample clock rate, and paths with different sample clock rates can be routed through the multiply-accumulate block on a time division multiplexed basis independently of each other. Thus, speech signals at 8kHz or 16kHz can be processed concurrently with audio data at 44.1kHz or 48kHz.

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- *with international search report (Art. 21(3))*
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INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2012/051193

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04M1/60
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04M H04H G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2011/010133 A1 (WOLFSON MICROELECTRONICS PLC [GB]; HATFIELD ROBERT [GB]) 27 January 2011 (2011-01-27)	98-101
Y	page 17, line 4 - page 19, line 31 page 20, line 35 - page 23, line 14 page 29, line 22 - page 30, line 8 figures 1-5	1-30, 132-166, 188-220
Y	US 2004/143715 A1 (BONACCIO ANTHONY R [US] ET AL) 22 July 2004 (2004-07-22) abstract paragraph [0021] - paragraph [0023] page 2	1-30, 132-166
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Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB2012/051193

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of Item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☒ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
1-30, 98-101, 128-220, 222-252
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2012/051193

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 976 160 A2 (YAMAHA CORP [JP]) 1 October 2008 (2008-10-01) abstract paragraph [0039] - paragraph [0042] paragraph [0075] - paragraph [0077] paragraph [0089] - paragraph [0090] figure 4 -----	1-30, 98-101, 132-166
A	EP 1 791 336 A2 (WOLFSON MICROELECTRONICS PLC [GB]) 30 May 2007 (2007-05-30) paragraph [0068] - paragraph [0069] paragraph [0077] -----	1-30, 98-101, 132-166
X	US 5 483 528 A (TELEX COMMUNICATIONS [US]) 9 January 1996 (1996-01-09)	128-131, 222
A	column 3, line 43 - line 48 column 15, line 58 - column 16, line 10 column 16, line 45 - column 17, line 59 -----	167-187
Y	US 5 729 225 A (LEDZIUS ROBERT C [US]) 17 March 1998 (1998-03-17) column 1, line 11 - line 34 column 2, line 54 - column 3, line 10 figure 1 -----	188-220
A	US 2009/196438 A1 (JEONG JONG-SIK [KR] ET AL) 6 August 2009 (2009-08-06) paragraph [0011] - paragraph [0015] paragraph [0036] paragraph [0052] - paragraph [0058] page 3; figure 3 -----	188-220
X	US 2009/204413 A1 (SINTES STEPHANE [FR] ET AL) 13 August 2009 (2009-08-13) paragraph [0015] - paragraph [0018] paragraph [0025] paragraph [0037] -----	226-252

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/GB2012/051193

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2011010133 A1	27-01-2011	CN 102474543 A GB 2469345 A KR 20120052241 A US 2011022204 A1 WO 2011010133 A1	23-05-2012 13-10-2010 23-05-2012 27-01-2011 27-01-2011
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US 2009204413 A1	13-08-2009	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-30, 98-101, 132-166

Communication devices (independent claims 98 and 99) comprising a processor and an integrated circuit comprising signal source ports and signal destination ports, a mixer or switching circuit that can be time division multiplexed between signal paths, which transfer data at a given sample rate from the source ports to the destination ports. Further independent claims 132 and 166 define integrated circuits including a mixing core and signal paths for transferring audio streams between source and destination ports according to stored configuration data sets. Finally, independent claim 1 defines an integrated circuit including a mixing core, source and destination ports and additional components like a clock generator, a multiplier-accumulator, buffers and source/destination selectors in order to transfer mixed audio stream between the source and destination ports according to stored configuration data sets.

2. claims: 31-33, 64-82, 111-118

Integrated circuits (independent claims 31, 111 and 112) including digital input and output interfaces with source and destination ports, signal processing blocks, a mixer for establishing signal paths between the source ports to the destination ports wherein one possible signal path is a direct signal path in which signals do not pass through the mixer.

3. claims: 34-57, 88-90

Integrated circuit (independent claim 34) including digital input and output interfaces with source and destination ports, signal processing blocks, a mixer for establishing signal paths between the source ports to the destination ports wherein a control block is provided for receiving user inputs and a plurality of signal paths is established on the basis of the received user input. Further independent claims 39 and 88 relate to methods of controlling integrated circuits comprising presenting to a user graphical representations of digital input and output interfaces and signal processing blocks available in the integrated circuit and further receiving user inputs identifying a set of plural signal routings that define signal paths in the integrated circuit.

4. claims: 58-63, 102, 110

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Methods (independent claims 58 and 102) of controlling an integrated circuit, the circuit comprising a plurality of sources and destinations, a mixer, the method comprising defining a plurality of paths between the source and destination port and obtaining data from the signal source port wherein data for the destination port is generated by applying scaling to the data from the source port and mixing the scaled data.

5. claims: 83-87

Integrated circuits (independent claims 83 and 84) comprising a plurality of signal sources and destinations, a mixer that can be time division multiplexed between signal paths connecting the sources and destinations, wherein data is transferred at a given sample rate, the circuits further comprising control circuitry for controlling the frequency of a data clock supplied to the mixer based on the number of signal paths and on first and second data rates.

6. claims: 91-97

Integrated circuits (independent claims 91 and 92) comprising a mixer that can be time division multiplexed between signal paths wherein each signal path transfers data at a respective sample rate from at least one signal source port to at least one destination port, wherein at successive time intervals, the signal path that is enabled by inclusion of the mixer is determined on the basis that the signal path that has the shortest time before an end of a period of a clock signal at the respective data sample rate. Further independent method claim 96 defines a corresponding method.

7. claims: 119-127

An integrated circuit (independent claim 119), comprising: clock generation circuitry for generating a plurality of clock signals at respective different frequencies, a plurality of signal processing blocks, each requiring a clock signal at a preferred frequency, a plurality of multiplexers, each associated with a respective one or more of the signal processing blocks, each receiving said plurality of clock signals, and each being controlled to pass a clock signal at the preferred frequency to the respective one or more of the signal processing blocks.

8. claims: 128-131, 167-187, 222-225

An integrated circuit (independent claim 128) or a switching circuit (independent claim 222) comprising a mixer than can be inserted into a plurality of data paths in a time

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

division multiplexed manner, such that data that is presented to the mixer by the start of one sample clock period is available for a receiving block for the whole of the next period of the sample clock.

Further independent claim 167 defines an integrated circuit for processing streams of audio samples, the circuit having a mixer comprising a multiplier accumulator, source data buffers and destination data buffers, wherein data samples of two data streams are received, stored in the buffers and multiplied according to a specific timing defined by a sample clock, wherein audio data sample is stored in a destination buffer for the remainder of a period and for the duration of a subsequent next period.

Additional independent claim 184 defines a method corresponding to claim 167.

9. claims: 188-220

An integrated circuit (independent claim 188) comprising a digital mixing core, the digital mixing core comprising: a plurality of signal source and destination ports each signal destination port having a respective data sample clock rate, a mixer, a plurality of source and destination data buffers and source and destination selector blocks, for enabling a plurality of respective signal paths between the source and destination data buffers via the mixer, the source, whereby the mixer is operable to enable a first signal path for data at a first data sample rate between first at least one source data buffers and first destination data buffer, and a second signal path for data at a second data sample rate between second at least one second source data buffer and second destination data buffer.

10. claim: 221

An integrated circuit (independent claim 221) comprising a multiply-accumulate block, wherein the multiply-accumulate block is configured to retrieve at least one input data sample from a respective input buffer, to multiply the or each input data sample by a respective scaling factor, and to generate an output data sample from the or each scaled input data sample within one cycle of a data sample clock, wherein each input buffer is configured to store a respective input data sample for a whole of said one cycle of the data sample clock, being a cycle after a cycle in which it is received, and wherein the output buffer is configured to store the output data sample for an entire cycle of the data sample clock after said cycle.

11. claims: 226-252

An integrated circuit (independent claim 247), comprising a

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

digital mixing core, the digital mixing core comprising a plurality of signal sources and signal destinations, and at least one mixer to which the signal sources and signal destinations can be connected on a time division multiplexed basis to establish signal paths, wherein each signal destination requires data at a respective predetermined sample rate, wherein the or each mixer operates at a respective mixer clock frequency, and wherein the or each mixer clock frequency is less than that necessary to be able to establish signal paths between every signal source and every signal destination during one period at the respective sample rates. A corresponding method is defined in claim 252.

Further independent claim 226 defines an integrated circuit essentially having the same features as claim 247.

Independent claim 246 defines further details concerning the frequency of the mixer clock:
