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(71) Applicant *(for all designated States except US)*: **SEAGATE TECHNOLOGY LLC** [US/US]; 7801 Computer Avenue S, Bloomington, Minnesota 55435 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **YOUNG, Kim** [KR/US]; 9151 Victoria Drive, Eden Prairie, Minnesota 55347 (US). **NURUL, Amin** [US/US]; 8797 Rainier Drive, Woodbury, Minnesota 55125 (US). **DADI, Setiadi** [ID/US]; 5841 Jeff Place, Edina, Minnesota 55436 (US). **VENUGOPALAN, Vaithyanathan** [IN/US]; 9851 Harrison Road, Apt. 308, Bloomington, Minnesota 55437 (US). **WEI, Tian** [CN/US]; 4101 West 98th Street, #202, Bloomington, Minnesota 55437 (US). **INSIK, Jin** [KR/US]; 1569 Johnny Cake Alcove, Eagan, Minnesota 55122 (US).

(74) Agent: **BUENZOW, Jennifer**; Seagate Technology LLC, 7801 Computer Avenue S, Bloomington, Minnesota 55435 (US).

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(54) **Title**: SCHOTTKY DIODE SWITCH AND MEMORY UNITS CONTAINING THE SAME

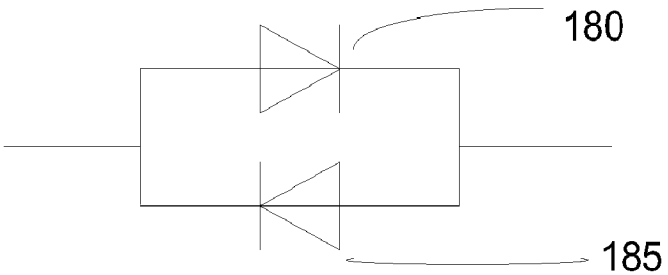

FIG. 1B

(57) **Abstract**: A switching element that includes a first semiconductor layer, the first semiconductor layer having a first portion and a second portion; a second semiconductor layer, the second semiconductor layer having a first portion and a second portion; an insulating layer disposed between the first semiconductor layer and the second semiconductor layer; a first metal contact in contact with the first portion of the first semiconductor layer forming a first junction and in contact with the first portion of the second semiconductor layer forming a second junction; a second metal contact in contact with the second portion of the first semiconductor layer forming a third junction and in contact with the second portion of the second semiconductor layer forming a fourth junction, wherein the first junction and the fourth junction are Schottky contacts, and the second junction and the third junction are ohmic contacts.

WO 2011/008650 A1

SCHOTTKY DIODE SWITCH AND MEMORY UNITS CONTAINING THE SAME

BACKGROUND

[01] New types of memory have demonstrated significant potential to compete with commonly utilized types of memory. For example, non-volatile spin-transfer torque random access memory (referred to herein as "STRAM") and resistive random access memory (referred to herein as "RRAM") are both considered good candidates for the next generation of memory. The ability of STRAM and RRAM to more effectively compete with established memory types, such as FLASH memory (NAND or NOR) can be maximized by increasing the density at which memory units (a memory cell and its associated driving device) can be formed on a chip.

BRIEF SUMMARY

[02] Disclosed herein is a switching element that includes a first semiconductor layer, the first semiconductor layer having a first portion and a second portion; a second semiconductor layer, the second semiconductor layer having a first portion and a second portion; an insulating layer disposed between the first semiconductor layer and the second semiconductor layer; a first metal contact in contact with the first portion of the first semiconductor layer forming a first junction and in contact with the first portion of the second semiconductor layer forming a second junction; a second metal contact in contact with the second portion of the first semiconductor layer forming a third junction and in contact with the second portion of the second semiconductor layer forming a fourth junction, wherein the first junction and the fourth junction are Schottky contacts, and the second junction and the third junction are ohmic contacts.

[03] Also disclosed herein is a non volatile memory element that includes a switching device having a first semiconductor layer, the first semiconductor layer having a first portion and a second portion; a second semiconductor layer, the second semiconductor layer having a first

portion and a second portion; an insulating layer disposed between the first semiconductor layer and the second semiconductor layer; a first metal contact in contact with the first portion of the first semiconductor layer forming a first junction and in contact with the first portion of the second semiconductor layer forming a second junction; a second metal contact in contact with the second portion of the first semiconductor layer forming a third junction and in contact with the second portion of the second semiconductor layer forming a fourth junction, wherein the first junction and the fourth junction are Schottky contacts, and the second junction and the third junction are ohmic contacts; and a non volatile memory cell, wherein the switching device is electrically connected in series with the non volatile memory cell

[04] Also disclosed herein is a method of forming a switching element that includes the steps of: providing a layered article, the layered article including a first semiconductor layer, an insulating layer, and a second semiconductor layer; forming a first mask region, wherein the first mask region protects only a first portion of the layered article; doping only a first portion of the second semiconductor layer using a first energy level; forming a second mask region, wherein the second mask region protects only a second portion of the layered article, wherein the first portion and the second portion of the layered article only partially overlap; doping only a second portion of the first semiconductor layer using a second energy level, wherein the first energy level and the second energy level are different, thereby forming a doped layered article; forming a contact mask on only a portion of the doped layered article; etching a portion of at least the second semiconductor layer, the insulating layer, and the first semiconductor layer; forming a first and a second metal contact in the etched regions of the second semiconductor layer, the insulating layer, and the first semiconductor layer.

[05] These and various other features and advantages will be apparent from a reading of the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[06] The disclosure may be more completely understood in consideration of the following detailed description of various embodiments of the disclosure in connection with the accompanying drawings, in which:

[07] **FIG. 1A** is a schematic diagram of an embodiment of a switching element disclosed herein;

[08] **FIG. 1B** is a circuit diagram depicting the functioning of a switching element disclosed herein;

[09] **FIG. 1C** is a current-voltage (I-V) curve of a hypothetical switching element disclosed herein;

[10] **FIGs. 2A** and **2B** are schematic diagrams of switching elements disclosed herein;

[11] **FIG. 3** is a flow chart depicting an exemplary method of forming a switching element;

[12] **FIGs. 4A** though **4G** depict a switching element at various stages of fabrication;

[13] **FIGs. 5A** through **5C** are schematic diagrams of various types of resistive sense memory (RSM) cells (**FIGs. 5A** and **5B** depict STRAM; and **FIG. 5C** depict RRAM) that can be utilized in non volatile memory elements disclosed herein;

[14] **FIG. 6A** is a schematic diagram of a non volatile memory element as disclosed herein;

[15] **FIG. 6B** is a circuit diagram of a non volatile memory element as disclosed herein;

[16] **FIGs. 7A** through **7C** are perspective views (**FIGs. 7A** and **7B**) and a diagrammatic view (**FIG. 7C**) of portions of crossbar memory arrays that can incorporate non volatile memory units as disclosed herein.

[17] The figures are not necessarily to scale. Like numbers used in the figures refer to like components. However, it will be understood that the use of a number to refer to a component in a given figure is not intended to limit the component in another figure labeled with the same number.

DETAILED DESCRIPTION

[18] In the following description, reference is made to the accompanying set of drawings that form a part hereof and in which are shown by way of illustration several specific embodiments. It is to be understood that other embodiments are contemplated and may be made without departing from the scope or spirit of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense.

[19] Unless otherwise indicated, all numbers expressing feature sizes, amounts, and physical properties used in the specification and claims are to be understood as being modified in all instances by the term "about." Accordingly, unless indicated to the contrary, the numerical parameters set forth in the foregoing specification and attached claims are approximations that can vary depending upon the desired properties sought to be obtained by those skilled in the art utilizing the teachings disclosed herein.

[20] The recitation of numerical ranges by endpoints includes all numbers subsumed within that range (e.g. 1 to 5 includes 1, 1.5, 2, 2.75, 3, 3.80, 4, and 5) and any range within that range.

[21] As used in this specification and the appended claims, the singular forms "a", "an", and "the" encompass embodiments having plural referents, unless the content clearly dictates otherwise. As used in this specification and the appended claims, the term "or" is generally employed in its sense including "and/or" unless the content clearly dictates otherwise.

[22] Spatially related terms, including but not limited to, "lower", "upper", "beneath", "below", "above", and "on top", if used herein, are utilized for ease of description to describe spatial relationships of an element(s) to another. Such spatially related terms encompass different orientations of the device in use or operation in addition to the particular orientations depicted in the figures and described herein. For example, if a cell depicted in the figures is turned over or flipped over, portions previously described as below or beneath other elements would then be above those other elements.

[23] As used herein, when an element, component or layer for example is described as being "on" "connected to", "coupled with" or "in contact with" another element, component or layer, it can be directly on, directly connected to, directly coupled with, in direct contact with, or intervening elements, components or layers may be on, connected, coupled or in contact with the particular element, component or layer, for example. When an element, component or layer for example is referred to as begin "directly on", "directly connected to", "directly coupled with", or "directly in contact with" another element, there are no intervening elements, components or layers for example.

[24] Disclosed herein are electronic devices that can be utilized as switches. The disclosed electronic devices can also be referred to as switching devices or switching elements. Generally, a switch is an electrical component that can break an electrical circuit, interrupting the current or diverting it from one conductor to another. Switches as disclosed herein can also be referred to as bi-directional switches. A bi-directional switch can break an electrical circuit and can also direct current through the switch either way. The switching devices can be utilized in applications which previously utilized or would have utilized a diode, as well as other applications. Switching devices disclosed herein can also withstand high driving currents.

[25] An embodiment of a switching device as disclosed herein can be seen in **FIG. 1A**. The exemplary switching device includes a first semiconductor layer **130**, an insulating layer **140**, a second semiconductor layer **150**, a first metal contact **160**, and a second metal contact **170**. As seen in **FIG. 1A**, the insulating layer **140** (which can also be referred to in embodiments as the first insulating layer **140**) can be positioned between the first semiconductor layer **130** and the second semiconductor layer **150**. In embodiments, the insulating layer **140** can be positioned directly between the first semiconductor layer **130** and the second semiconductor layer **150** and is in contact with both the first semiconductor layer **130** and the second semiconductor layer **150**.

[26] In embodiments, the first metal contact **160** is adjacent to the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the first

metal contact **160** is adjacent to first portions **131**, **141**, and **151** respectively of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the first metal contact **160** is in contact with the first portions **131**, **141**, and **151** of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the first metal contact **160** is in direct contact with the first portions **131**, **141**, and **151** of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**.

[27] In embodiments, the second metal contact **170** is adjacent to the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the second metal contact **170** is adjacent to second portions **133**, **143**, and **153** respectively of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the second metal contact **170** is in contact with the second portions **133**, **143**, and **153** of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**. In embodiments, the second metal contact **170** is in direct contact with the second portions **133**, **143**, and **153** of the first semiconductor layer **130**, the insulating layer **140**, and the second semiconductor layer **150**.

[28] The first portion **131** of the first semiconductor layer **130** contacts the first metal contact **160** at a first junction **162**; the first portion **151** of the second semiconductor layer **150** contacts the first metal contact **160** at a second junction **164**; the second portion **133** of the first semiconductor layer **130** contacts the second metal contact **170** at a third junction **172**; and the second portion **153** of the second semiconductor layer **150** contacts the second metal contact **170** at a fourth junction **174**. The first, second, third, and fourth junctions **162**, **164**, **172**, and **174** are either ohmic or Schottky junctions.

[29] Whenever a metal and a semiconductor are in intimate contact, there exists a potential barrier between the two materials that prevents most charge carriers (electrons or holes) from passing from one material to the other material. Only a small number of carriers have enough energy to get over the barrier and cross to the other material. When a bias is applied to the junction, it can have one of two effects: it can make the barrier appear lower from the semiconductor

side, or it can make it appear higher from the semiconductor side. The bias does not change the barrier height from the metal side. The result of this is a Schottky Barrier, which can also be referred to as a Schottky junction, or a rectifying contact, where the junction conducts for one bias polarity, but not the other. Ohmic contacts on the other hand, conduct the same for both polarities. An ohmic contact or an ohmic junction has a linear and symmetric current-voltage (I-V) curve; a Schottky contact or a Schottky junction has a non-linear and asymmetric current-voltage (I-V) curve.

[30] Whether a particular metal-semiconductor junction will be an ohmic junction or a Schottky junction can depend at least in part on the work function of the metal, the band gap of the semiconductor, the type and concentration of dopants in the semiconductor, and other factors. In general, a junction of a heavily doped semiconductor and a metal forms a thinner energy barrier (the heavier the dopant level, the thinner the barrier will be). At reverse bias conditions, charge will flow through the barrier due to quantum mechanical tunneling. In embodiments, a junction of a heavily doped semiconductor material and a metal will form an ohmic junction (the current will flow in either direction: forward biased current in one direction, tunneling in the other (reverse) direction) and a junction of an undoped or lightly doped semiconductor material and a metal will form a Schottky junction.

[31] In embodiments of switching elements disclosed herein, the first semiconductor layer **130** will have one ohmic contact and one Schottky contact and the second semiconductor layer **150** will have one ohmic contact and one Schottky contact. The orientation of the Schottky contact and the ohmic contact within the first semiconductor layer **130** will generally be opposite of the orientation of the Schottky contact and the ohmic contact within the second semiconductor layer **150**. In embodiments, the first junction **162** can be a Schottky junction, the second junction **164** can be an ohmic junction, the third junction **172** can be an ohmic junction, and the fourth junction **174** can be a Schottky junction. In embodiments, the first junction **162** can be an ohmic junction, the second junction **164** can be a Schottky junction, the third junction **172** can be a Schottky junction, and the fourth junction **174** can be an ohmic junction.

[32] The opposite orientation of the Schottky contacts and ohmic contacts within the first and second semiconductor layers **130** and **150** render switching elements having such a configuration a bidirectional switch. A bidirectional switch allows current to flow in a first direction when a current having a first polarity is applied and allows current to flow in a second direction (opposite the first direction) when a current having a second polarity (opposite the first polarity) is applied. **FIG. 1B** depicts a circuit diagram that illustrates the bidirectional nature of the switching elements disclosed herein. As seen in the circuit diagram of **FIG. 1B**, the first semiconductor layer and the second semiconductor layer provide the function of a first diode **180** and a second diode **185** respectively that are in parallel. The first diode **180** allows current to flow in an opposite direction than does the second diode **185**. **FIG. 1C** shows a current-voltage (I-V) curve for a hypothetical disclosed switching element. As seen in **FIG. 1C**, the first diode **180** has a threshold voltage V_{T1} at which a substantial current begins to flow in a first direction; and the second diode **185** has a threshold voltage V_{T2} at which a substantial current begins to flow in a second direction. As shown in **FIG. 1C**, the polarity of V_{T1} and V_{T2} are opposite, as is the current that flows from the switching element at the two voltages. This provides a switching element that essentially blocks current between the voltages V_{T1} and V_{T2} and allows current having a first polarity to flow at voltages below V_{T2} and a second polarity to flow at voltages above V_{T1}.

[33] In functioning as a switch, this means that if a voltage of less than V_{T2} is applied to the switching element, a current will flow in a first direction; whereas if a voltage of greater than V_{T1} is applied to the switching element, a current will flow in a second direction. The switching element can therefore be utilized to control the direction in which current flows through an electrically connected component, such as for example a non volatile memory cell.

[34] Switching elements as disclosed herein can advantageously provide the combination of bi-directional switching and the ability to withstand high driving current. The switching elements disclosed herein can be used where high driving current is necessary because of the relatively larger (as compared with conventional MOS transistors) cross-section of the current path of the disclosed switching element which makes it capable of flowing a relatively large amount of current. The ability to handle high driving currents can be advantageous because

the switch can then be utilized with components where a high driving current is necessary, or desired, an example of which is spin torque transfer random access memory (STRAM).

[35] **FIG. 2A** illustrates another embodiment of a switching element disclosed herein. The switching element in **FIG. 2A** includes the components discussed above and also includes other components. For example, adjacent the first semiconductor layer **230** can be another insulating layer **220**, which can also be referred to as the second insulating layer **220**. In embodiments, the second insulating layer **220** can be directly adjacent to the first semiconductor layer **230**. The second insulating layer **220** can function to electrically insulate the first semiconductor layer **230** from the substrate **210**. The substrate can be an electrically conductive, or a semiconductive material. The substrate **210** can function to provide the switching element structural stability and can aid in the formation process of the switching element.

[36] The hypothetical I-V curve that is illustrated in **FIG. 1C** is symmetrical. Generally, in order for the I-V curve of a disclosed switching element to be symmetrical, the path lengths across the first semiconductor layer and the second semiconductor layer have to be at least substantially the same and the surface area of the metal/semiconductor junctions (e.g., **162, 164, 172**, and **174**), have to be at least substantially the same. A switching element that does not have symmetrical first and second semiconductor layers and/or substantially the same surface areas can be modified to become less asymmetrical. This can be accomplished for example, by modifying the components that make up the switching element, by altering the dopants (either the identity or the amount), by altering one or both of the metal contacts, by changing other factors not discussed herein, or by altering a combination of these factors. A switching element that has a symmetrical I-V curve can be advantageous in some applications. For example, it can be advantageous for a switching element that is to be used in combination with memory elements to have a symmetrical I-V curve.

[37] The exemplary switching element illustrated in **FIG. 2A** can be relatively easily manufactured to have a symmetrical I-V curve because it is generally a relatively simple matter to make the thicknesses of the first and second semiconductor layers substantially the same. In

embodiments, a switching element that has a first semiconductor layer and a second semiconductor layer having substantially the same thickness will most likely have a symmetrical I-V curve.

[38] The exemplary switching element illustrated in **FIG. 2B** will most likely not have a symmetrical I-V curve. As seen in **FIG. 2B**, the illustrated switching element has a first semiconductor layer **230** that is significantly thicker than the second semiconductor layer **250**; and the first junction **262** and the third junction **274**, which are those of the first semiconductor layer **230** have significantly more surface area than the junctions of the second semiconductor layer **250** (namely second junction **264** and fourth junction **272** with first metal contact **260** and second metal contact **270**). This will most likely lead to the first semiconductor layer **230** having a higher threshold voltage than the second semiconductor layer **250**. Such a switching element would therefore most likely have an asymmetric I-V curve.

[39] The first semiconductor layer and the second semiconductor layer can include any semiconductive material. The first semiconductor layer and the second semiconductor layer can be, but need not be the same material. Exemplary semiconductors that can be utilized for the first semiconductor layer, the second semiconductor layer, or both include, but are not limited to, silicon, silicon containing compounds, germanium, germanium containing compounds, aluminium containing compounds, boron containing compounds, gallium containing compounds, indium containing compounds, cadmium containing compounds, zinc containing compounds, lead containing compounds, tin containing compounds. Exemplary elemental and compound semiconductors include, but are not limited to, Silicon, for example crystalline silicon, Germanium, Silicon carbide (SiC), Silicon germanium (SiGe), Aluminium antimonide (AlSb), Aluminium arsenide (AlAs), Aluminium nitride (AlN), Aluminium phosphide (AlP), Boron nitride (BN), Boron phosphide (BP), Boron arsenide (BAs), Gallium antimonide (GaSb), Gallium arsenide (GaAs), Gallium nitride (GaN), Gallium phosphide (GaP), Indium antimonide (InSb), Indium arsenide (InAs), Indium nitride (InN), Indium phosphide (InP), Aluminium gallium arsenide (AlGaAs, AlxGa1-xAs), Indium gallium arsenide (InGaAs, InxGa1-xAs), Indium gallium phosphide (InGaP), Aluminium indium

arsenide (AlInAs), Aluminium indium antimonide (AlInSb), Gallium arsenide nitride (GaAsN), Gallium arsenide phosphide (GaAsP), Aluminium gallium nitride (AlGaN), Aluminium gallium phosphide (AlGaP), Indium gallium nitride (InGaN), Indium arsenide antimonide (InAsSb), Indium gallium antimonide (InGaSb), Aluminium gallium indium phosphide (AlGaInP, also InAlGaP, InGaAlP, AlInGaP), Aluminium gallium arsenide phosphide (AlGaAsP), Indium gallium arsenide phosphide (InGaAsP), Aluminium indium arsenide phosphide (AlInAsP), Aluminium gallium arsenide nitride (AlGaAsN), Indium gallium arsenide nitride (InGaAsN), Indium aluminium arsenide nitride (InAlAsN), Gallium arsenide antimonide nitride (GaAsSbN), Gallium indium nitride arsenide antimonide (GaInNAsSb), Gallium indium arsenide antimonide phosphide (GaInAsSbP), Cadmium selenide (CdSe), Cadmium sulfide (CdS), Cadmium telluride (CdTe), Zinc oxide (ZnO), Zinc selenide (ZnSe), Zinc sulfide (ZnS), Zinc telluride (ZnTe), Cadmium zinc telluride (CdZnTe, CZT), Mercury cadmium telluride (HgCdTe), Mercury zinc telluride (HgZnTe), Mercury zinc selenide (HgZnSe), Cuprous chloride (CuCl), Lead selenide (PbSe), Lead sulfide (PbS), Lead telluride (PbTe), Tin sulfide (SnS), Tin telluride (SnTe), Lead tin telluride (PbSnTe), Thallium tin telluride (Tl_2SnTe_5), Thallium germanium telluride (Tl_2GeTe_5), Bismuth telluride (Bi_2Te_3), Cadmium phosphide (Cd_3P_2), Cadmium arsenide (Cd_3As_2), Cadmium antimonide (Cd_3Sb_2), Zinc phosphide (Zn_3P_2), Zinc arsenide (Zn_3As_2), and Zinc antimonide (Zn_3Sb_2).

[40] A portion of both the first semiconductor layer and the second semiconductor layer are doped. Doping is the process of intentionally introducing impurities into a semiconductor to change its electrical properties. The particular dopant that is chosen can depend at least in part on the particular properties that are desired in the final switching element, the identity of the semiconductor material to be doped, other factors not discussed herein, or a combination thereof. Exemplary dopants can include, but are not limited to Group III and Group V elements. In embodiments where the semiconductor materials are Group IV materials (for example, silicon, germanium, and silicon carbide), Group III or Group V elements can be utilized as dopants. Specific exemplary dopants can include, but are not limited to boron (B), arsenic (As), phosphorus (P), and gallium (Ga).

[41] The first insulating layer and the optional second insulating layer can be made of any material that is electrically insulating. The first insulating layer and the optional second insulating layer can be, but need not be the same material. Exemplary insulating materials include, but are not limited to, oxides, such as alumina (Al_2O_3), silicon oxide (SiO_2), and magnesium oxide (MgO) for example.

[42] The metal contacts can be made of any metallic material that is electrically conductive. The first metal contact and the second metal contact can be, but need not be the same material. Exemplary metal electrically conductive materials include, but are not limited to tungsten (W) or a noble metal such as gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), copper (Cu), Nickel (Ni), Silver (Ag), Cobalt (Co), Iron (Fe), or their silicides.

[43] In embodiments, the first and second semiconductor layers both are made of crystalline silicon. In embodiments, the first and second semiconductor layers are doped with boron, phosphorus, or arsenic. In embodiments, the first insulating layer and the second insulating layer if present are made of silicon oxide (SiO_2). In embodiments, the metal contacts are tungsten (W), a nickel silicide, or a cobalt silicide.

[44] An exemplary method of fabrication for a switching element, such as that depicted in **FIG. 2A** is provided in **FIG. 3** and is demonstrated stepwise in **FIGs. 4A** through **4G.** Generally, such fabrication schemes can include semiconductor fabrication methods including photolithography techniques and other removal techniques such as etching, and chemical mechanical planarization (CMP). Deposition methods, including but not limited to, plasma vapor deposition (PVD), ionized plasma based sputtering, long throw sputtering, chemical vapor deposition (CVD), atomic layer deposition (ALD), and metal organic chemical vapor deposition (MOCVD) can be utilized to deposit the various layers deposited in the exemplary method. The steps depicted in **FIG. 3** and the depiction thereof in **FIGs. 4A** to **4G** in no way limit the way in which a switching element as disclosed herein can be fabricated. It should also be noted that **FIGs. 4A** through **4G** are not necessarily to scale and do not necessarily depict the article at every state of preparation, i.e. some intermediate stages of the article may not be illustrated in the sequence of figures. The materials and processes discussed with

respect to **FIGs. 4A** to **4G** also in no way limit materials or processes that can be utilized herein.

[45] The exemplary method illustrated in **FIG. 3** and **FIGs. 4A** through **4G** depict the use of a substrate. One of skill in the art, having read this specification, will understand that use of a substrate is not necessary, switching elements as disclosed herein can be fabricated without use of a substrate, the switching element can be placed on a support after fabrication, a substrate can be utilized and then removed either during or after fabrication of the switching element, or a substrate does not need to be utilized at all. The substrate, if utilized, can include materials such as silicon, a mixture of silicon and germanium, or other similar materials.

[46] A flowchart depicting an exemplary method of fabricating a switching element disclosed herein is shown in **FIG. 3**. The first step in the exemplary method is step **310**, providing a layered article. The layered article includes at least a first semiconductor layer, an insulating layer (which can also be referred to as a first insulating layer) and a second semiconductor layer, and has the insulating layer positioned between the first semiconductor layer and the second semiconductor layer. An exemplary layered article **402** can be seen in **FIG. 4B** and includes a substrate **410**, a second insulating layer **420**, a first semiconductor layer **430**, a first insulating layer **440**, and a second semiconductor layer **450**. It should be understood, having read this specification, that a layered article could have more or less layers than that depicted in **FIG. 4B**. The layered article can be fabricated or obtained, for example through commercially available sources.

[47] Exemplary optional steps that can be utilized to fabricate the layered article are seen in steps **302**, **304**, and **306**. Step **302** includes providing a first layered structure. The first layered structure can include at least a first substrate, a second insulating layer and the first semiconductor layer, and has the second insulating layer positioned between the first substrate and the first semiconductor layer. An example of a first layered structure can include a substrate (for example a silicon wafer), having an insulating layer disposed thereon and the first semiconductor layer disposed on the insulating layer. The insulating layer of the first

layered structure (the second insulating layer) can be formed by depositing an insulating material or by oxidizing a portion of the substrate to form an insulating material from a portion of the substrate (for example SiO_2). An exemplary first layered structure **405** is shown in **FIG. 4A** and includes the substrate **410**, the second insulating layer **420** and the first semiconductor layer **430**.

[48] Step **304** includes providing a second layered structure. The second layered structure can include at least an insulating layer (which can be referred to as the first insulating layer) and a second semiconductor layer, and has the insulating layer disposed on the second semiconductor layer (or vice versa). An example of a second layered structure can include an oxidized substrate (for example a silicon wafer), where the oxidized portion becomes the insulating layer and the un-oxidized portion becomes the second semiconductor layer. Alternatively, a semiconductor material (such as a silicon wafer) can have an insulating material deposited thereon to form the insulating layer on the second semiconductor layer. In embodiments where a substrate, such as a silicon wafer, is utilized to form the second layered structure, a portion of the silicon wafer can be removed to adjust the thickness of the second semiconductor layer. This can be accomplished using techniques such as chemical mechanical planning (CMP) for example. An exemplary second layered structure **407** is shown in **FIG. 4A** and includes the insulating layer **440** and the second semiconductor layer **450**.

[49] Step **306** includes placing the first layered structure in contact with the second layered structure (or vice versa). The first and second layered structures are configured so that the insulating layer of the second layered structure is adjacent the first semiconductor layer of the first layered structure to form the layered article. In embodiments, the first semiconductor layer of the first layered structure is directly adjacent to or in direct contact with the insulating layer of the second layered structure. The first and second layered structures can then be bonded together using wafer bonding techniques. Completion of this step forms the layered article **402** that is seen in **FIG. 4B**.

[50] However the layered article is provided (whether via steps **302**, **304**, and **306** or otherwise), the next step in a method of forming a switching element is step **320**, doping the layered article. The step of doping the layered article functions to dope a portion of the first semiconductor layer and a portion of the second semiconductor layer. More specifically, the step of doping the layered article functions to dope a first portion of the second semiconductor layer and a second portion of the first semiconductor layer (or vice versa). Exemplary optional steps that can be undertaken to dope the layered article are shown in steps **322**, **324**, **326**, and **328**.

[51] Step **322** includes forming a first mask region. The mask regions (both the first mask region and the second mask region that will be discussed below) are made of materials that prevent the implantation of dopants into materials positioned below them (above and below in this context are defined by the location of the dopant source, with the dopant source being positioned above all of the layers of the layered article and the mask regions). Exemplary materials that can be utilized as mask regions include, but are not limited to, oxide materials, silicon nitrides, or photoresist. The first mask region protects only a portion of the layered article from implantation. The article depicted in **FIG. 4C** includes a first mask region **411**.

[52] The next step, step **324**, includes doping a portion of the layered article. The first mask region (formed in step **322**) allows doping of only a portion, for example a first portion, of the layered article. As seen in **FIG. 4C**, implantation (depicted by the arrows) is prevented under the first mask region and is allowed where the first mask region is not covering the layered article. Doping the first portion of the layered article is accomplished using a first energy level. In embodiments, doping the first portion results in the second semiconductor layer **450** being heavily doped and the first semiconductor layer **430** being only lightly doped or substantially not doped at all. Differential doping levels (or doping and substantially no doping) can be accomplished by using different energy levels.

[53] Step **324**, as depicted herein accomplishes preferential doping of the second semiconductor layer **450** (which is the upper layer of the layered article as depicted in this embodiment). Preferential doping of only an upper layer or layers of a layered structure can be accomplished

by doping using a lower implantation energy. Doping using lower energy can afford the dopant only enough energy to penetrate to a certain depth. **FIG. 4D** depicts the dopants **451** that are present in the second semiconductor layer **450** after completion of step **324**.

[54] Step **326**, includes forming a second mask region. The second mask region protects only a portion of the layered article from implantation. The article depicted in **FIG. 4D** includes a second mask region **413**. The location of the first mask region **411** and the second mask region **413** can at least partially overlap. In embodiments, the first mask region **411** and the second mask region **413** do not fully overlap and only partially overlap. The second mask region **413** generally protects at least the portion of the second semiconductor layer **450** that was doped in step **324**. In embodiments, the second mask region **413** generally protects the portion of the second semiconductor layer **450** that was doped in step **324** as well as a portion of the second semiconductor layer **450** that was not doped in step **324**.

[55] The next step, step **328**, includes doping a portion of the layered article. The second mask region (formed in step **326**) allows doping of only a portion, for example a second portion, of the layered article. As seen in **FIG. 4D**, implantation (depicted by the arrows) is prevented under the second mask region and is allowed where the second mask region is not covering the layered article. Doping the second portion of the layered article is accomplished using a second energy level. The second energy level is different than the first energy level (used for doping the first portion). In embodiments, doping the second portion results in the first semiconductor layer **430** being heavily doped and the second semiconductor layer **450** being only lightly doped or substantially not doped at all. Doping using a higher energy implants the dopants deeper into the layered article. Higher energy level doping also generally does not deposit dopants or at least not a substantial amount of dopants in the upper layers of the layered article. **FIG. 4E** depicts the dopants **431** that are present in the first semiconductor layer **430** after completion of step **328**.

[56] The effect of step **320**, or the optional steps **322**, **324**, **326**, and **328**, is to dope or heavily dope only a first portion of the second semiconductor layer **450** and dope or heavily dope only a second portion of the first semiconductor layer **430**. This opposite configuration of doped or

heavily doped regions in the first and second semiconductor layers **430** and **450** form the oppositely aligned ohmic and Schottky junctions (after formation of the metal contacts) in the first and second semiconductor layer **430** and **450**. The effect of step **320** is to form what is referred to herein as a doped layered article, which is seen in **FIG. 4**, and is designated as **409**.

[57] The next step in the method depicted in **FIG. 3** is step **330**, formation of the metal contacts. Generally, formation of the metal contacts can be accomplished using etching and deposition techniques. Exemplary specific optional steps that can be undertaken to form the metal contacts are shown in steps **332**, **334**, and **336**. The first step in this optional method of forming the metal contacts is step **332**, forming a contact mask. The contact mask **452**, which is depicted in **FIG. 4F** generally only masks a portion of the doped layered article. In embodiments, the contact mask **452** masks a region of the doped layered article that is not doped in either the first semiconductor layer **450** or the second semiconductor layer **430**. It can also be said that the contact mask **452** masks at least the portion of the doped layered article where the first mask region **411** and the second mask region **413** provided protection from doping. Generally, the contact mask is located in the middle of the doped layered article. In embodiments, the contact mask **452** is located such that once the doped layered article is etched, at least a portion of the doped first semiconductor layer and the doped second semiconductor layer will remain.

[58] The next step, step **334** includes etching the doped layered article using the contact mask **452**. This step functions to remove a portion or portions of the doped layered article. The portions not protected by the contact mask **452** are removed from the doped layered article. Etching can be said to form first and second metal contact regions **461** and **471**. The first and second metal contact regions **461** and **471** will eventually be filled in with metal to form the metal contacts. Etching can be carried out using known etching techniques and methods.

[59] The next step, step **336** includes depositing metal in the first and second metal contact regions **461** and **471**. In embodiments, metal can be deposited in more than just the first and second metal contact regions **461** and **471**. In embodiments, metal can be deposited on the entire doped layered article to a depth that fills the first and second metal contact regions **461** and

471 and also provides a layer on the region that was previously masked by the contact mask **452**. The extra metal can then be removed via CMP for example so that the only location that metal remains is the first and second metal contact regions **461** and **471** to form the first and second metal contacts **460** and **470**. **FIG. 4G** depicts the layered article after formation of the first and second metal contacts **460** and **470**, forming the switching element.

[60] Other optional fabrication steps not depicted or discussed herein can also be carried out before, after, during, or a combination thereof, the steps discussed and exemplified herein. The method can also be carried out to fabricate more than one switching element at one time.

[61] Switching elements as disclosed herein can be utilized along with a non volatile memory cell as a selective element for the non volatile memory cell. A non volatile memory cell utilized in a memory device as described herein can include many different types of memory. An exemplary type of non volatile memory cell that can be utilized in electronic devices disclosed herein includes, but is not limited to resistive sense memory (RSM) cells. Exemplary RSM cells include, but are not limited to, ferroelectric RAM (FeRAM or FRAM); magnetoresistive RAM (MRAM); resistive RAM (RRAM); phase change memory (PCM) which is also referred to as PRAM, PCRAM and C-RAM; programmable metallization cell (PMC) which is also referred to as conductive-bridging RAM or CBRAM; and spin torque transfer RAM, which is also referred to as STRAM.

[62] In embodiments, the RSM cell can be a STRAM cell. STRAM memory cells include a MTJ (magnetic tunnel junction), which generally includes two magnetic electrode layers separated by a thin insulating layer, which is also known as a tunnel barrier. An embodiment of a MTJ is depicted in **FIG. 5A**. The MTJ **500** in **FIG. 5A** includes a first magnetic layer **510** and a second magnetic layer **530**, which are separated by an insulating layer **520**. The first magnetic layer **510** and the second magnetic layer **530** may both independently be multilayer structures. **FIG. 5B** depicts a MTJ **500** in contact with a first electrode layer **540** and a second electrode layer **550**. The first electrode layer **540** and the second electrode layer **550** electrically connect the first magnetic layer **510** and the second magnetic layer **530** respectively to a control circuit (not shown) providing read and write currents through the

magnetic layers. The relative orientation of the magnetization vectors of the first magnetic layer **510** and the second magnetic layer **530** can be determined by the resistance across the MTJ **500**; and the resistance across the MTJ **500** can be determined by the relative orientation of the magnetization vectors of the first magnetic layer **510** and the second magnetic layer **530**.

[63] The first magnetic layer **510** and the second magnetic layer **530** are generally made of ferromagnetic alloys such as iron (Fe), cobalt (Co), and nickel (Ni) alloys. In embodiments, the first magnetic layer **510** and the second magnetic layer **530** can be made of alloys such as FeMn, NiO, IrMn, PtPdMn, NiMn and TbCo. The insulating layer **520** is generally made of an insulating material such as aluminium oxide (Al_2O_3) or magnesium oxide (MgO).

[64] The magnetization of one of the magnetic layers, for example the first magnetic layer **510** is generally pinned in a predetermined direction, while the magnetization direction of the other magnetic layer, for example the second magnetic layer **530** is free to rotate under the influence of a spin torque. Pinning of the first magnetic layer **510** may be achieved through, e.g., the use of exchange bias with an antiferromagnetically ordered material such as PtMn, IrMn and others.

[65] A particular MTJ **500** can be read from by allowing a first current to flow through the memory cell in the direction of the second magnetic layer **530** (the free layer) to the first magnetic layer **510** (the pinned layer). The resistance of the MTJ **500** can change depending on whether the free layer is aligned with or aligned opposite to the pinned layer. A voltage, dependent on the resistance can then be detected and compared to a reference voltage determine whether the MTJ is aligned or opposite, i.e., contains a "1" or a "0". A particular MTJ **500** can be written to by allowing a second current (the second current is larger than the first current) to pass through the MTJ. Passing the current through one way will write a "1" and passing the current through the other way will write a "0". The bi-directional nature of switching elements disclosed herein can provide the ability to drive current both ways through the MTJ **500**.

[66] In embodiments, the RSM cell can be a RRAM cell. **FIG. 5C** is a schematic diagram of an illustrative resistive random access memory (RRAM) cell **560**. The RRAM cell **560** includes a medium layer **512** that responds to an electrical current or voltage pulse by altering an electrical resistance of the medium layer **512**. This phenomenon can be referred to as the electrical pulse induced resistance change effect. This effect changes the resistance (i.e., data state) of the memory from one or more high resistance state(s) to a low resistance state, for example. The medium layer **512** is interposed between a first electrode **514** and the second electrode **516** and acts as a data storage material layer of the RRAM cell. The first electrode **514** and the second electrode **516** are electrically connected to a voltage source (not shown). The first electrode **514** and a second electrode **516** can be formed of any useful electrically conducting material such as, for example, a metal.

[67] The material forming the medium layer **512** can be any known useful RRAM material. In embodiments, the material forming the medium layer **512** can include an oxide material such as, a metal oxide. In some embodiments, the metal oxide is a binary oxide material or complex metal oxide material. In other embodiments, the material forming the medium layer **512** can include a chalcogenide solid electrolyte material or an organic/polymer material.

[68] The binary metal oxide material can be expressed as a chemical formula of M_xO_y. In this formula, the characters "M", "O", "x", and "y" refer to metal, oxygen, a metal composition ratio, and an oxygen composition ratio, respectively. The metal "M" may be a transition metal and/or aluminium (Al). In this case, the transition metal may be nickel (Ni), niobium (Nb), titanium (Ti), zirconium (Zr), hafnium (Hf), cobalt (Co), iron (Fe), copper (Cu) and/or chrome (Cr). Specific examples of binary metal oxides that may be used as the medium layer **512** include CuO, NiO, CoO, ZnO, CrO_2, TiO_2, HfO_2, ZrO_2, Fe_2O_3, and Nb_2O_5.

[69] In embodiments, the metal oxide can be any useful complex metal oxide such as, for example, a complex oxide material having a formula $Pr_{0.7}Ca_{0.3}MnO_3$, or $SrTiO_3$, or $SiZrO_3$, or these oxides doped with Cr or Nb. The complex can also include $LaCuO_4$, or $Bi_2Sr_2CaCu_2O_8$. One example of a solid chalcogenide material is a germanium-selenide (Ge_xSe_{100-x}) containing a

silver (Ag) component. One example of an organic material is Poly(3,4-ethylenedioxythiophene) (i.e., PEDOT).

[70] The RSM cell can also include ferroelectric capacitors having structures similar to **FIG. 5C** using materials such as lead zirconate titanate (referred to as "PZT") or $SrBi_2Ta_2O_9$ (referred to as "SBT"). In such memory cells, an electrical current can be used to switch the polarization direction and the read current can detect whether the polarization is up or down. In such embodiments, a read operation is a destructive process, where the cell will lose the data contained therein, requiring a refresh to write data back to the cell.

[71] Memory elements as disclosed include a switching element as disclosed above; and a non volatile memory cell. An exemplary embodiment of a memory element **600** as disclosed herein is depicted in **FIG. 6A**. The memory element **600** includes a switching element **615** that includes a first semiconductor layer **650**, an insulating layer **640**, a second semiconductor layer **630**, a first metal contact **660**, and a second metal contact **670** as described and exemplified above. The spatial orientation with respect to the memory cell **605** is not meant to be limited by the depiction. The orientation is generally only meant to show that the non volatile memory cell **605** is electrically connected in series to one of the metal contacts (**FIG. 6A** shows the non volatile memory cell **605** electrically connected to the second metal contact **670**, but it could of course be the first metal contact **660**).

[72] **FIG. 6B** is a circuit diagram depicting the functioning of the components of the non volatile memory element. As seen there, the switching element **615** functions as two individual diodes **611** and **612** in parallel. The switching element **615** is then connected in series to the non volatile memory cell **605** that functions as a resistor. The voltage provided by the source **680** can provide a voltage greater than V_{T1} (see **FIG. 1C**) which allows the current to go one way through the circuit or a voltage less than V_{T2} (see **FIG. 1C**) which allows the current to go the other way through the circuit. The two paths can allow various operations to be carried out on the non volatile memory cell **605**, including determining the resistance state of the non volatile memory cell **605**.

[73] Memory elements as disclosed herein can be utilized in memory arrays. In embodiments, memory elements as disclosed herein can be utilized in crossbar memory arrays. An exemplary depiction of a crossbar memory array is illustrated in **FIG. 7A**. An exemplary crossbar memory array includes a first layer of approximately parallel conductors **702** that are overlain (or underlain) by a second layer of approximately parallel conductors **704**. In embodiments, the conductors of the second layer **704** can be substantially perpendicular, in orientation, to the conductors of the first layer **702**. In embodiments, the orientation angle between the layers may be other than perpendicular. The two layers of conductors form a lattice, or crossbar, each conductor of the second layer **704** overlying all of the conductors of the first layer **702** and coming into close contact with each conductor of the first layer **702** at conductor intersections that represent the closest contact between two conductors. Although individual conductors in **FIG. 7A** are shown with rectangular cross sections, conductors can also have square, circular, elliptical, or any other regular or irregular cross sections. The conductors may also have many different widths or diameters and aspect ratios or eccentricities.

[74] Memory elements as disclosed above can be disposed at at least some of the conductor intersections of the crossbar memory arrays. In embodiments, disclosed memory elements can be disposed at substantially all of the conductor intersections. A conductor intersection connected by disclosed memory elements can be referred to as a "crossbar junction." **FIGS. 7B** and **7C** provide two different illustrations of a crossbar junction that interconnects conductors **702a** and **704a** of two contiguous layers within a crossbar memory array. The crossbar junction may or may not involve physical contact between the two conductors **702a** and **704a**. As shown in **FIG. 7B**, the two conductors are not in physical contact at their overlap point, but the gap between the conductors **702a** and **704a** is spanned by the memory element **706a** that lies between the two conductors at their closest overlap point. **FIG. 7C** illustrates a schematic representation of the memory element **706a** and overlapping conductors **702a** and **704a** shown in **FIG. 7B**.

[75] Disclosed memory elements may be advantageously utilized in crossbar memory arrays because the switching devices that are included in the memory elements can function as an

integrated selective element that can avoid or minimize disturbances on unintended cells during read, write and erase operations due to sneak currents. The switching devices disclosed herein are especially advantageous in combination with STRAM because STRAM requires writing and erasing operations to be carried out using opposite polarities.

[76] Thus, embodiments of **SCHOTTKY DIODE SWITCH AND MEMORY UNITS CONTAINING THE SAME** are disclosed. The implementations described above and other implementations are within the scope of the following claims. One skilled in the art will appreciate that the present disclosure can be practiced with embodiments other than those disclosed. The disclosed embodiments are presented for purposes of illustration and not limitation, and the present disclosure is limited only by the claims that follow.

What is claimed is:

1. A switching element comprising:

a first semiconductor layer, the first semiconductor layer having a first portion and a second portion;

a second semiconductor layer, the second semiconductor layer having a first portion and a second portion;

an insulating layer disposed between the first semiconductor layer and the second semiconductor layer;

a first metal contact in contact with the first portion of the first semiconductor layer forming a first junction and in contact with the first portion of the second semiconductor layer forming a second junction;

a second metal contact in contact with the second portion of the first semiconductor layer forming a third junction and in contact with the second portion of the second semiconductor layer forming a fourth junction,

wherein the first junction and the fourth junction are Schottky contacts, and the second junction and the third junction are ohmic contacts.

2. The switching element according to claim 1, wherein the first semiconductor layer and the second semiconductor layer are independently chosen from: silicon, silicon containing compounds, germanium, germanium containing compounds, aluminium containing compounds, boron containing compounds, gallium containing compounds, indium containing compounds, cadmium containing compounds, zinc containing compounds, lead containing compounds, and tin containing compounds.

3. The switching element according to claim 1, wherein the first semiconductor layer is crystalline silicon and the second portion is doped with phosphorus (P), boron (B), or arsenic (As).

4. The switching element according to claim 1, wherein the second semiconductor layer is crystalline silicon and the first portion is doped with phosphorus (P), boron (B), or arsenic (As).

5. The switching element according to claim 1, wherein the second portion of the first semiconductor layer and the first portion of the second semiconductor layer are heavily doped with phosphorus (P), boron (B), or arsenic (As).

6. The switching element according to claim 5, wherein the first portion of the first semiconductor layer and the second portion of the second semiconductor layer are not heavily doped.

7. The switching element according to claim 1 further comprising a second insulating layer and a substrate layer wherein the second insulating layer is located between the substrate layer and the first semiconductor layer and the second insulating layer is in contact with the first and second metal contacts.

8. A non volatile memory element comprising:

a switching device comprising:

a first semiconductor layer, the first semiconductor layer having a first portion and a second portion;

a second semiconductor layer, the second semiconductor layer having a first portion and a second portion;

an insulating layer disposed between the first semiconductor layer and the second semiconductor layer;

a first metal contact in contact with the first portion of the first semiconductor layer forming a first junction and in contact with the first portion of the second semiconductor layer forming a second junction;

a second metal contact in contact with the second portion of the first semiconductor layer forming a third junction and in contact with the second portion of the second semiconductor layer forming a fourth junction,

wherein the second junction and the third junction are ohmic contacts; and

a non volatile memory cell,

wherein the switching device is electrically connected in series with the non volatile memory cell.

9. The non volatile memory element according to claim 8, wherein the first junction and the fourth junction are Schottky contacts.

10. The non volatile memory element according to claim 8, wherein the second portion of the first semiconductor layer and the first portion of the second semiconductor layer are doped with phosphorus (P), boron (B), or arsenic (As).

11. The non volatile memory element according to claim 8, wherein the first portion of the first semiconductor layer and the second portion of the second semiconductor layer are not doped.

12. The non volatile memory element according to claim 8, wherein the first and second semiconductor layers have substantially the same thicknesses.

13. The non volatile memory element according to claim 8 wherein the non volatile memory cell is a spin torque transfer random access memory (STRAM) stack.

14. A method of forming a switching element comprising the steps of:

providing a layered article, the layered article comprising a first semiconductor layer, an insulating layer, and a second semiconductor layer;

forming a first mask region, wherein the first mask region protects only a first portion of the layered article;

doping only a first portion of the second semiconductor layer using a first energy level;

forming a second mask region, wherein the second mask region protects only a second portion of the layered article, wherein the first portion and the second portion of the layered article only partially overlap;

doping only a second portion of the first semiconductor layer using a second energy level, wherein the first energy level and the second energy level are different, thereby forming a doped layered article;

forming a contact mask on only a portion of the doped layered article;

etching a portion of at least the second semiconductor layer, the insulating layer, and the first semiconductor layer;

forming a first and a second metal contact in the etched regions of the second semiconductor layer, the insulating layer, and the first semiconductor layer.

15. The method according to claim 14, wherein the first energy is less than the second energy.

16. The method according to claim 14, wherein providing the layered article comprises:

providing a first layered structure, the first layered structure comprising a first substrate, a second insulating layer and the first semiconductor layer, wherein the second insulating layer is positioned between the first substrate and the first semiconductor layer;

providing a second layered structure, the second layered structure comprising the insulating layer and the second semiconductor layer;

placing the second layered structure in contact with the first layered structure so that the insulating layer of the second layered structure is adjacent the first semiconductor layer of the first layered structure and bonding the first layered structure to the second layered structure to form the layered article.

17. The method according to claim 16, wherein the second layered structure is formed at least in part by oxidizing a silicon wafer.

18. The method according to claim 16, wherein the second layered structure is formed at least in part by depositing an insulating material on a silicon.

19. The method according to claim 14, wherein the first and second mask regions are configured to leave a portion of the layered article undoped.

20. The method according to claim 18, wherein the undoped portion of the layered article is substantially coincident with the portion of the doped layered article that is masked by the contact mask.

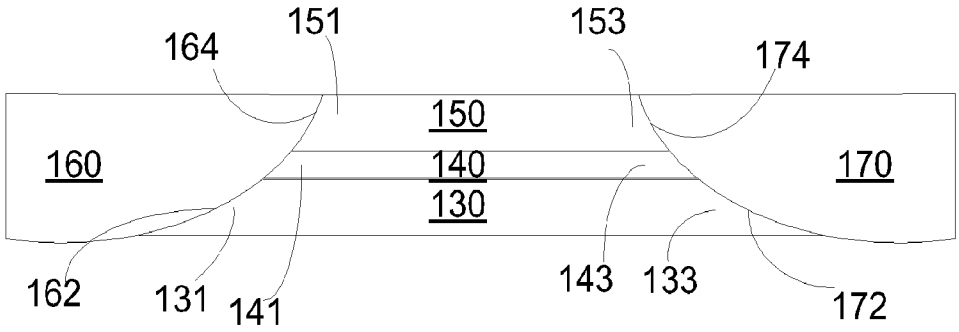

FIG. 1A

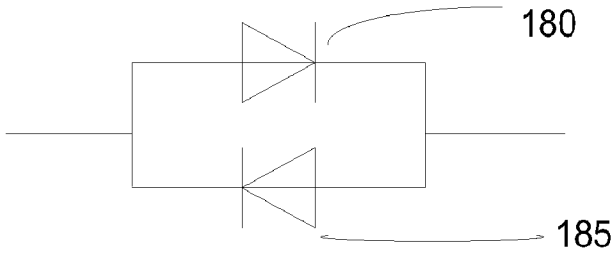

FIG. 1B

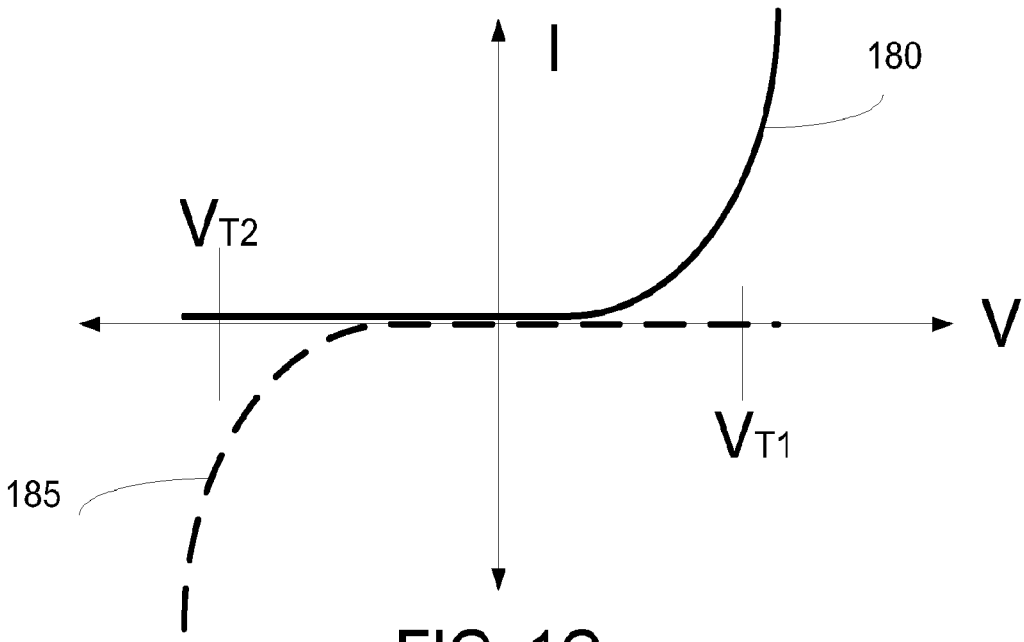

FIG. 1C

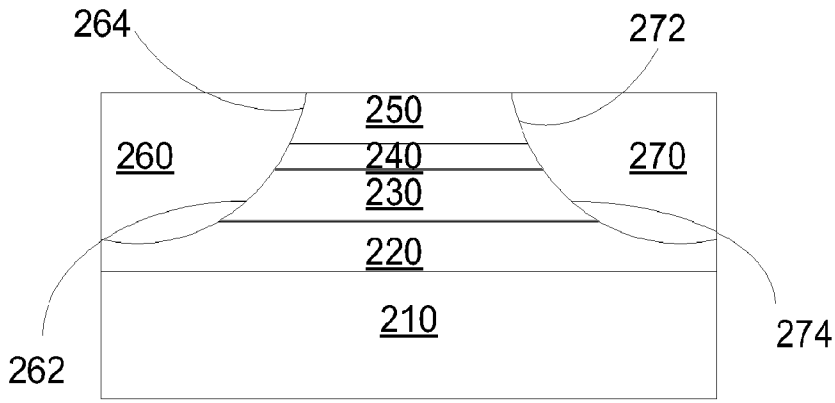
264
272
250
260
240
270
230
220
210
262
274

FIG. 2A

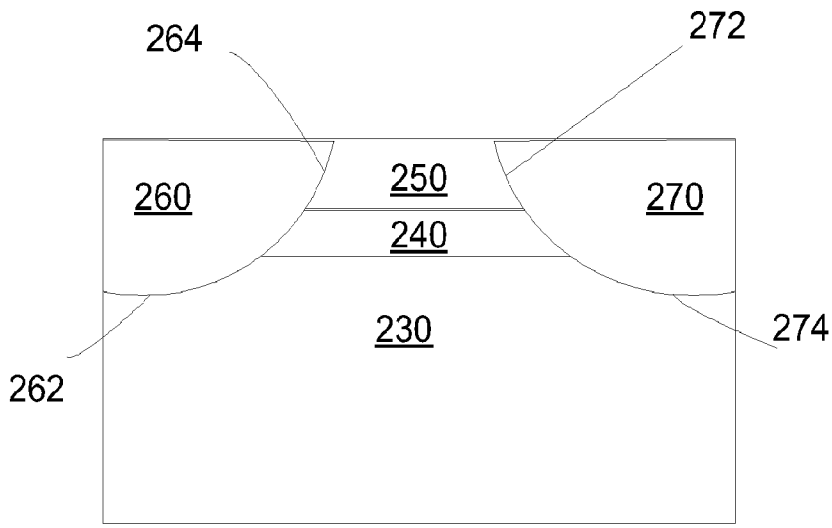
264
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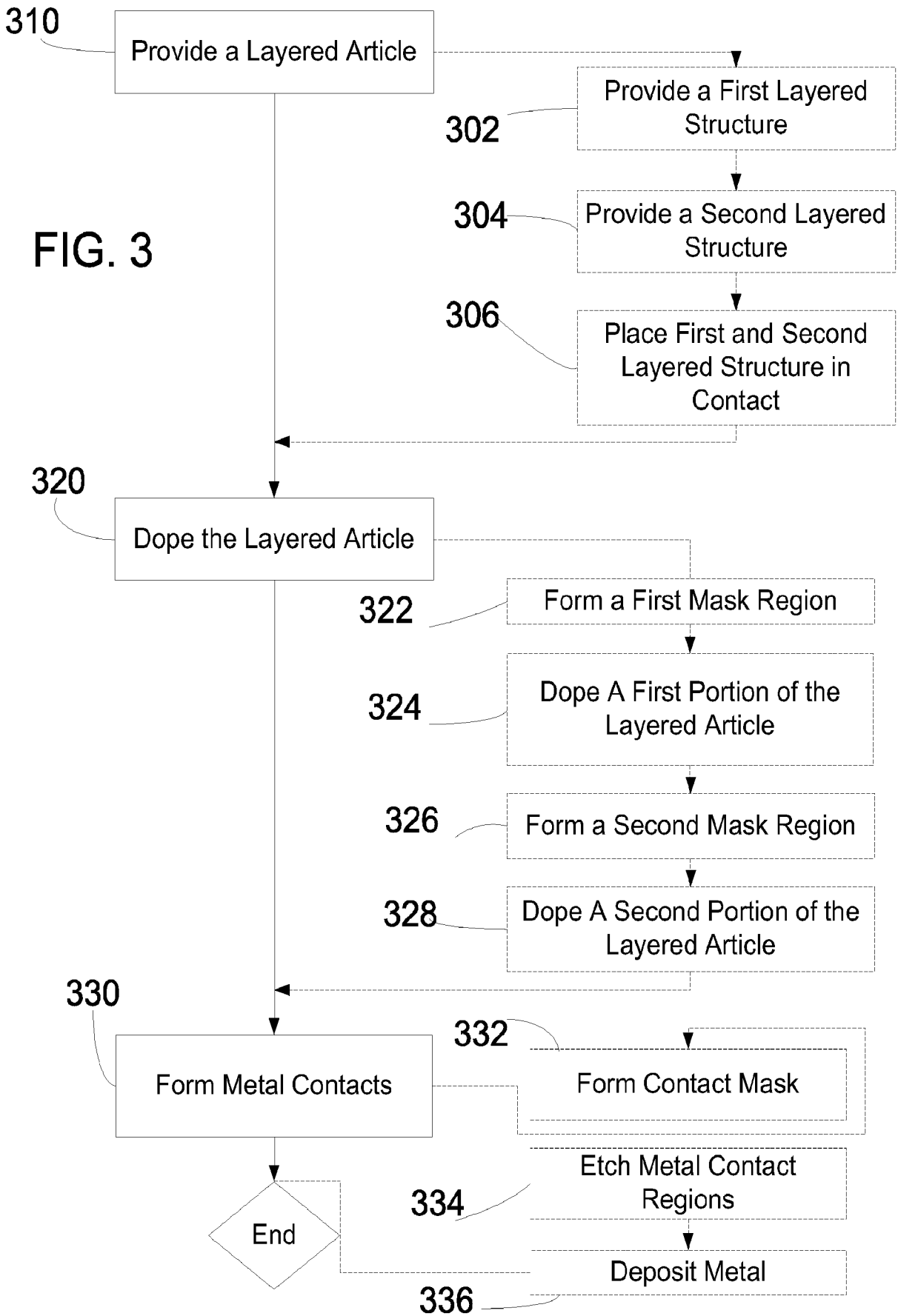
FIG. 2B

FIG. 3


310
Provide a Layered Article
302
Provide a First Layered Structure
304
Provide a Second Layered Structure
306
Place First and Second Layered Structure in Contact
320
Dope the Layered Article
322
Form a First Mask Region
324
Dope A First Portion of the Layered Article
326
Form a Second Mask Region
328
Dope A Second Portion of the Layered Article
330
Form Metal Contacts
332
Form Contact Mask
334
Etch Metal Contact Regions
End
Deposit Metal
336

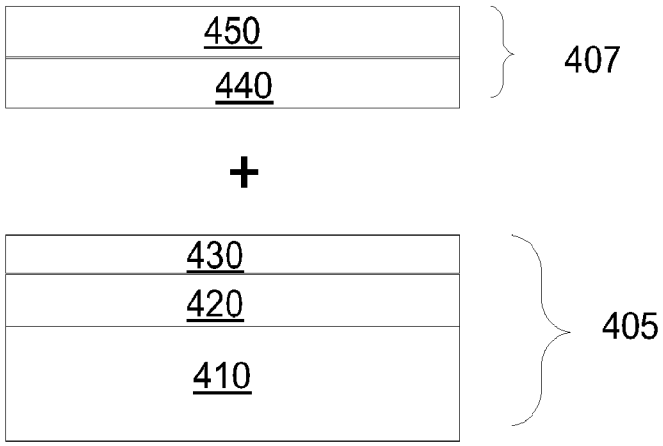


FIG. 4A

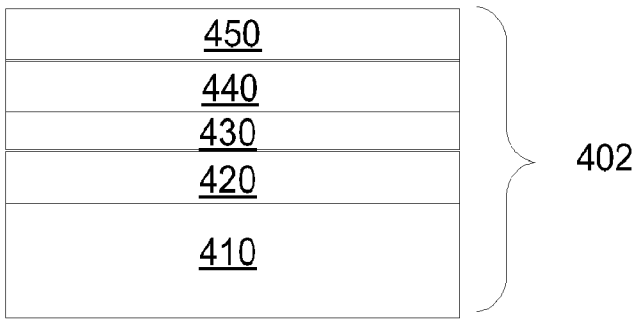


FIG. 4B

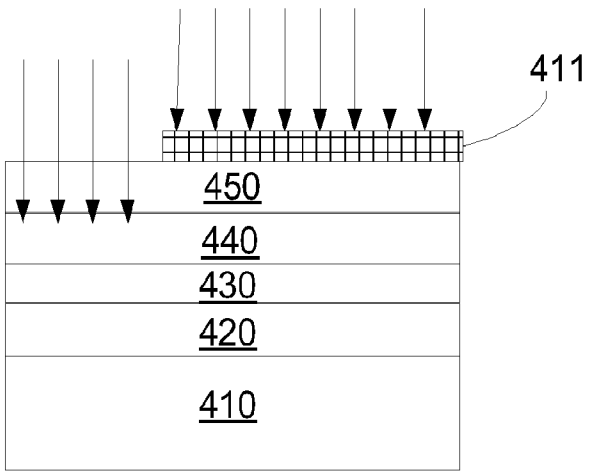


FIG. 4C

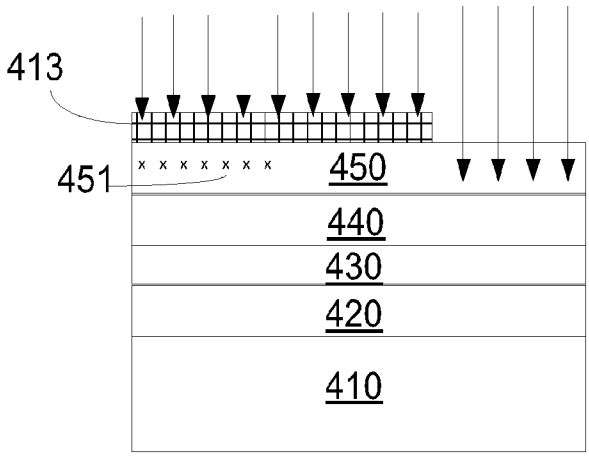


FIG. 4D

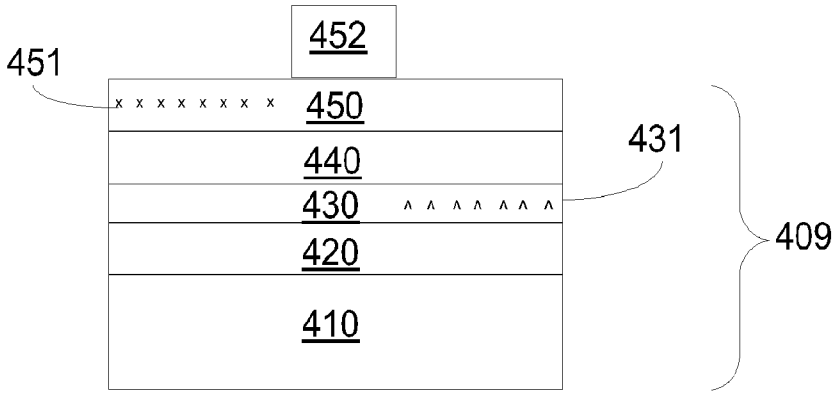


FIG. 4E

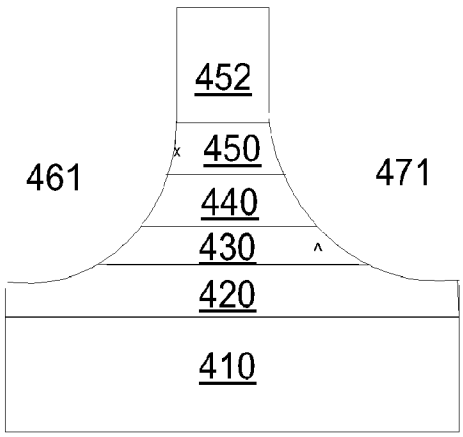


FIG. 4F

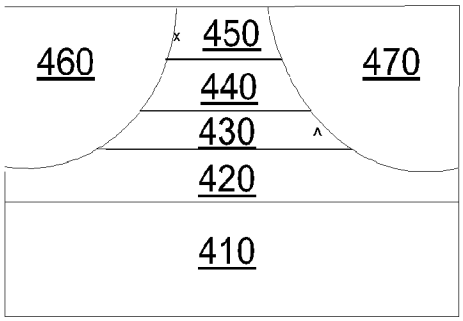


FIG. 4G

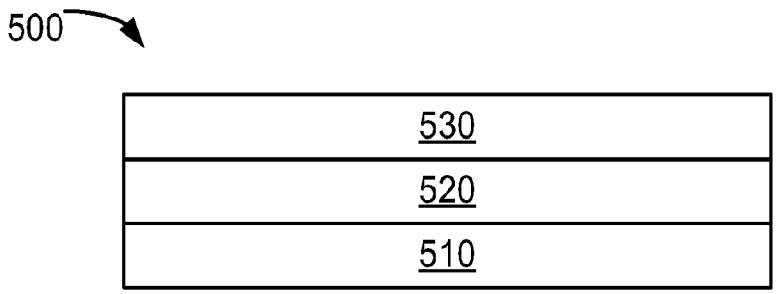


FIG. 5A

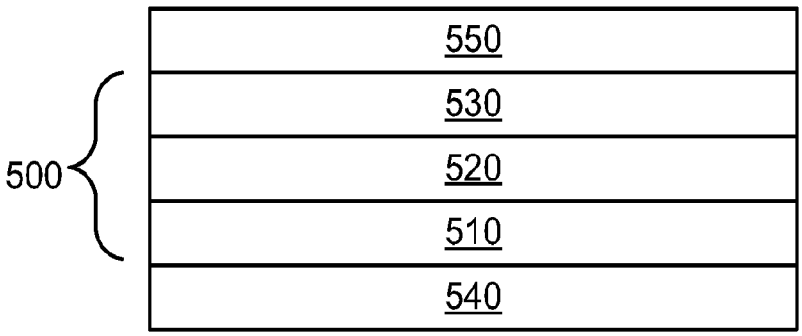


FIG. 5B

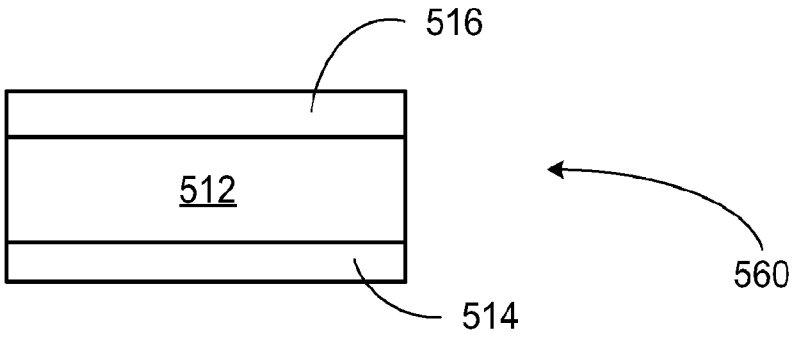


FIG. 5C

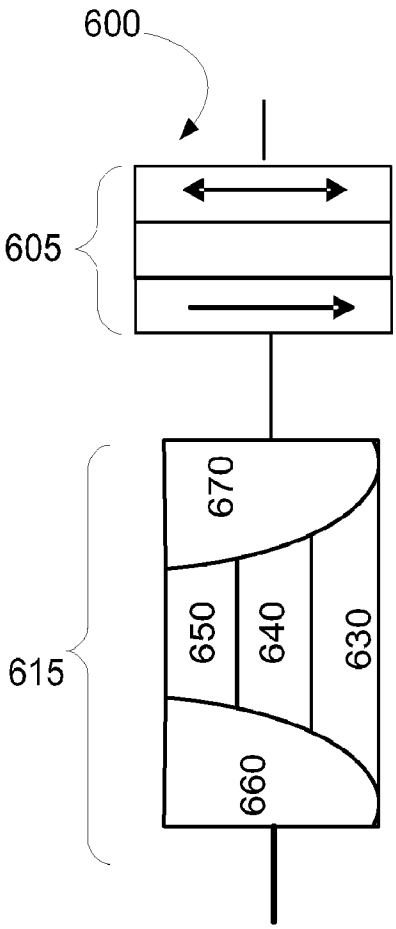


FIG. 6A

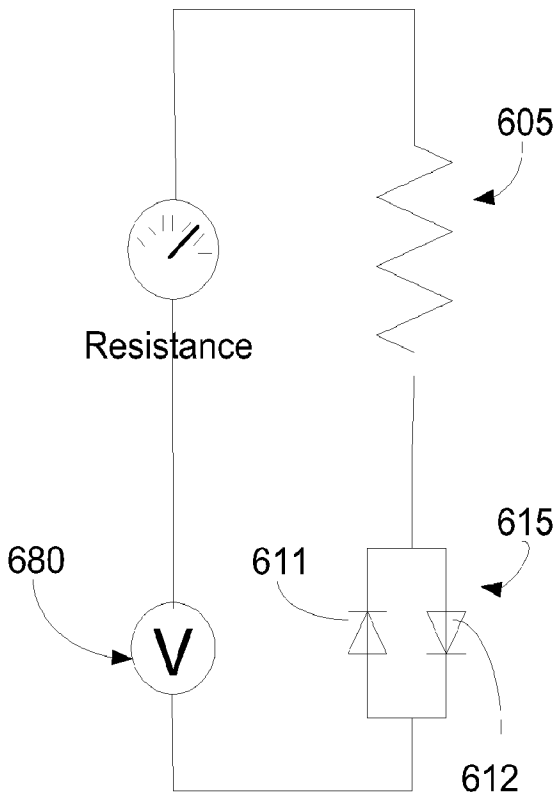


FIG. 6B

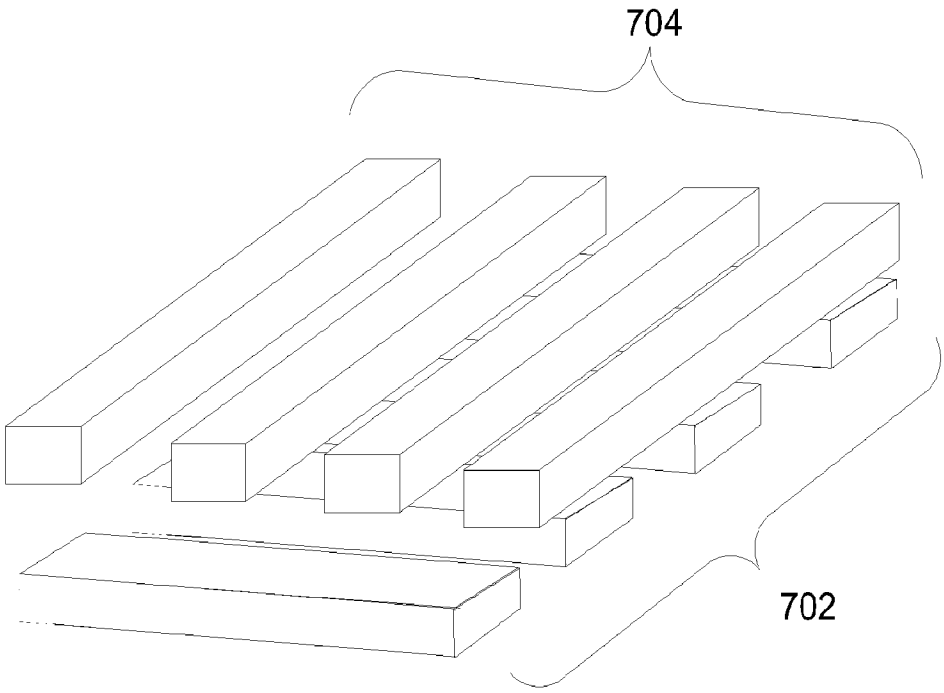


FIG. 7A

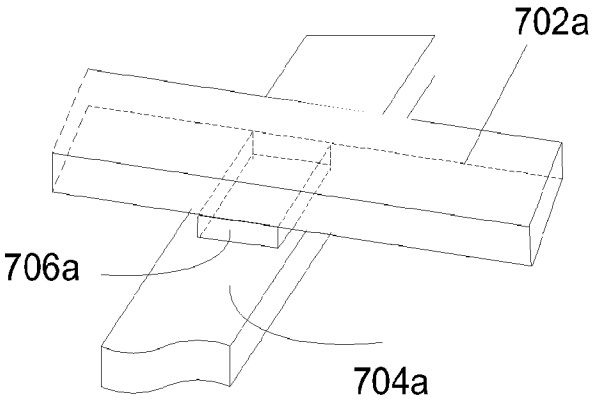


FIG. 7B

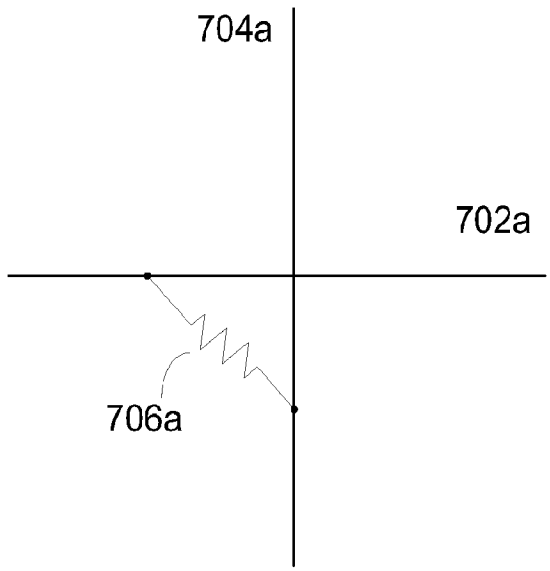


FIG. 7C

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/041539

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/06 H01L27/08 H01L27/102
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 341 114 A (CALVIELLO JOSEPH A [US] ET AL) 23 August 1994 (1994-08-23) column 7, line 67 - column 8, line 5; figures 30,32,33 column 7, line 13 - line 17 column 7, line 34 - line 37 column 6, line 55 - line 57	1,2
Y	US 4 888 304 A (NAKAGAWA KAORU [JP] ET AL) 19 December 1989 (1989-12-19) column 4, line 26 - line 34; figures 2D, 3 column 3, line 1 - line 5 column 3, line 15 - line 17	1-7
Y	US 3 746 945 A (NORMINGTON P) 17 July 1973 (1973-07-17) column 1, line 5 - line 7; figures 5,6	1-7

-/--

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 December 2010	15/12/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Seck, Martin

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/041539

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1 605 508 A2 (MA COM INC [US]) 14 December 2005 (2005-12-14) figure 1	1-6
A	US 2002/113293 A1 (ROBB FRANCINE Y [US] ET AL) 22 August 2002 (2002-08-22) paragraphs [0030], [0037]; figures 1-5	1-13
A	EP 0 281 032 A2 (TOSHIBA KK [JP]) 7 September 1988 (1988-09-07) column 2, line 49 - line 50; figures 3b,4a column 3, line 8 - line 15 column 4, line 5 - line 10 column 4, line 19 - line 25	1
X	US 2006/076548 A1 (PARK JAE-HYUN [KR] ET AL) 13 April 2006 (2006-04-13) paragraphs [0023], [0027], [0028], [0029], [0030]; figure 4	8,10,12
X Y	US 2009/168493 A1 (KIM SUNG-MIN [KR] ET AL) 2 July 2009 (2009-07-02) paragraphs [0017], [0152]; figures 3,4,17	8,10,12, 13 9,11
Y A	US 2003/169625 A1 (HUSH GLEN [US] ET AL) 11 September 2003 (2003-09-11) paragraphs [0032] - [0036]; figures 1,2,4	9,11 8,10,12
A	US 2004/256610 A1 (LUNG HSIANG-LAN [TW]) 23 December 2004 (2004-12-23) paragraph [0044]; figure 5	8-12
A	US 2008/273365 A1 (KANG SANG-BEOM [KR] ET AL) 6 November 2008 (2008-11-06) figures 1,2,5	8-12
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X	US 6 492 244 B1 (CHRISTENSEN TODD ALAN [US] ET AL) 10 December 2002 (2002-12-10) column 5, line 43 - line 50; figures 9-13 column 3, line 54 - line 61	14-20
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/041539

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-7

Switching element including Schottky and ohmic contacts to two different semiconductor layers.

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2. claims: 8-13

Non volatile memory element including switching element in two different semiconductor layers.

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3. claims: 14-20

Method of forming a switching element, the method comprising selective doping of portions of two different semiconductor layers by using different implantation energy levels.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/041539

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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