United States Patent

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[54] **PULSE POSITION MODULATED ALARM SYSTEM**

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[52] **U.S. Cl.** .....**340/164 R,** 340/224

[51] **Int. Cl.** **H04q 1/42**

[58] **Field of Search** ..340/224, 207, 183, 164 R, 150; 343/203; 325/143

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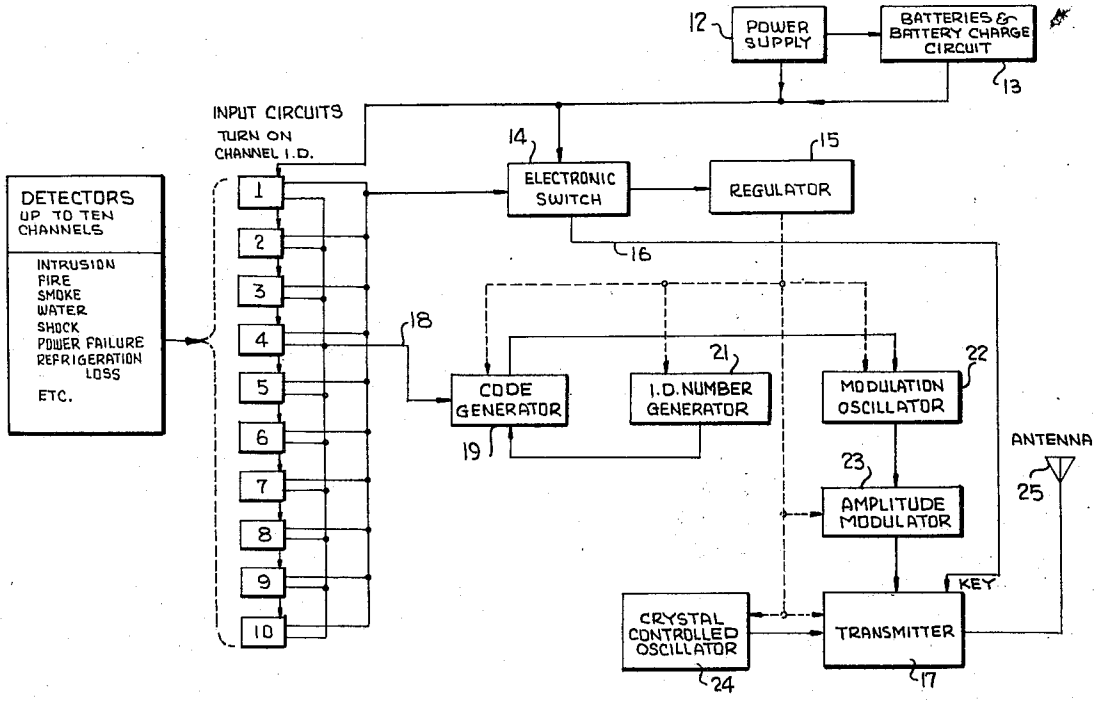
[57] **ABSTRACT**

A system for transmitting, via a radio link to a central station, alarm indications at a plurality of monitored stations. Each monitored station includes a different code identification number which controls pulse position modulation of a carrier that is transmitted to the central station only in response to an alarm condition being sensed. The type of alarm condition being sensed also pulse position modulates the carrier transmitted from the peripheral station to the central station. At the central station, the carrier is received and the pulse position modulated pulses are detected and processed to provide indications of the identity of the monitored station at which the alarm condition was sensed, as well as the cause of the sensed alarm.

13 Claims, 17 Drawing Figures



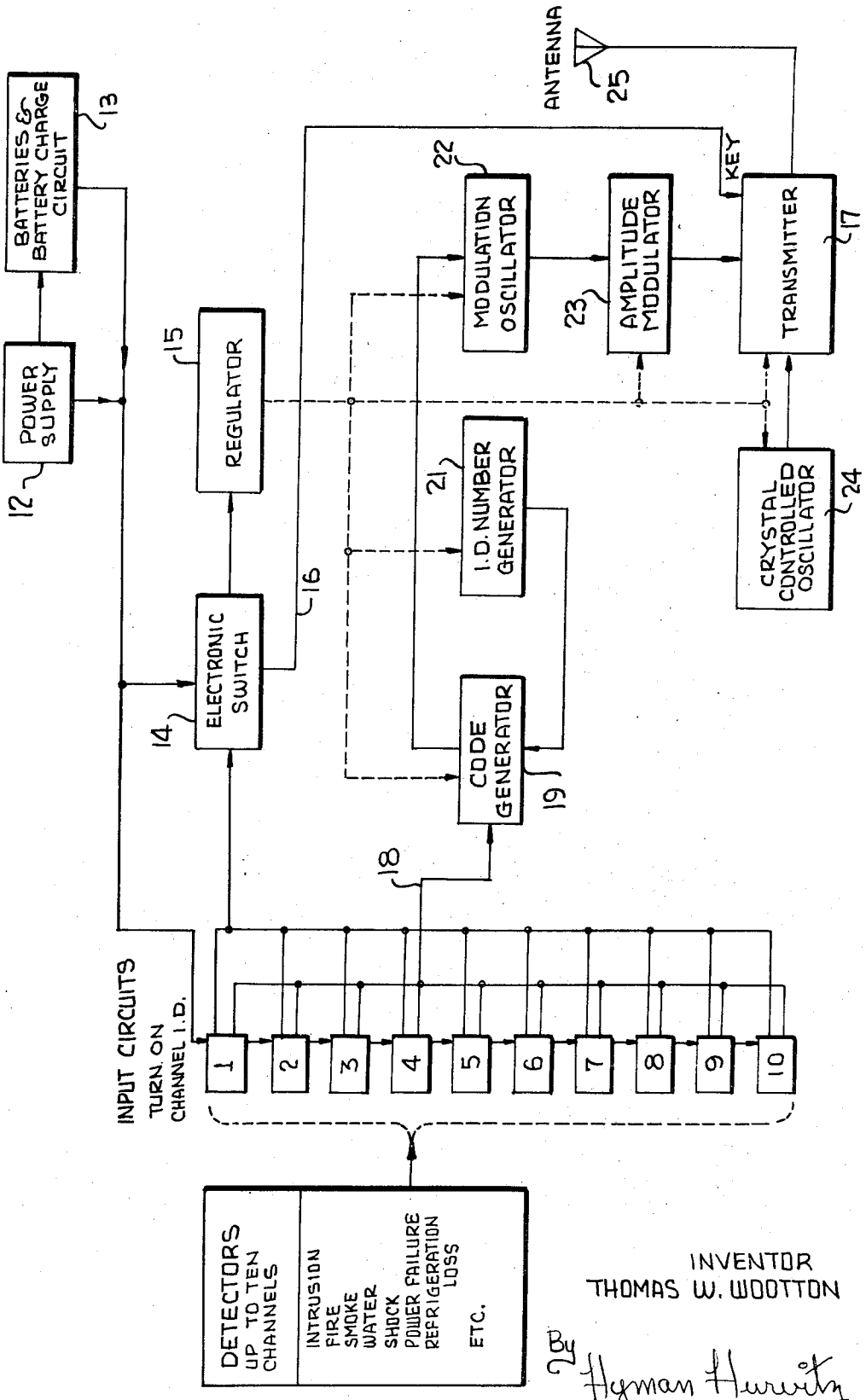


FIG. 1

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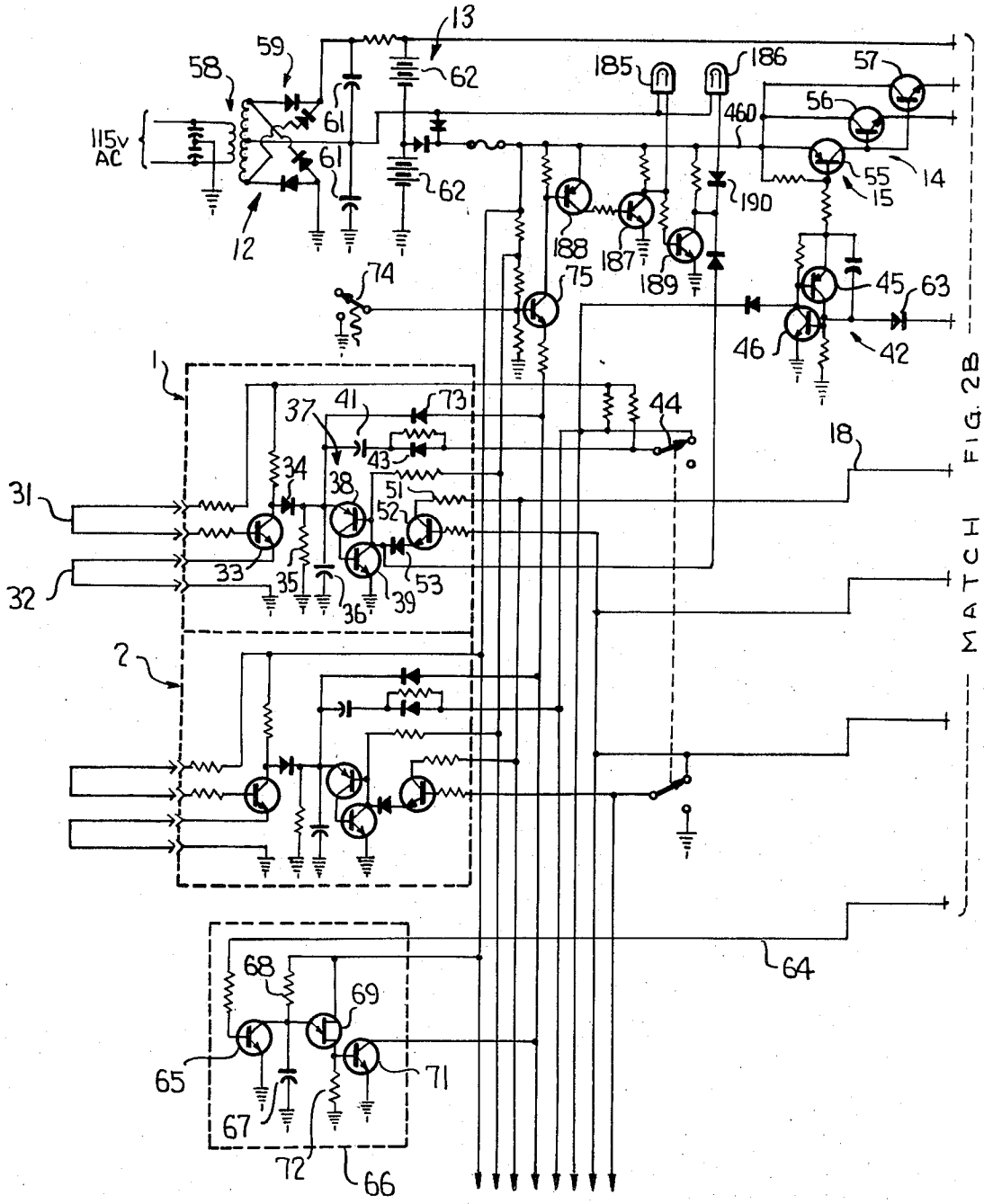

FIG.2A

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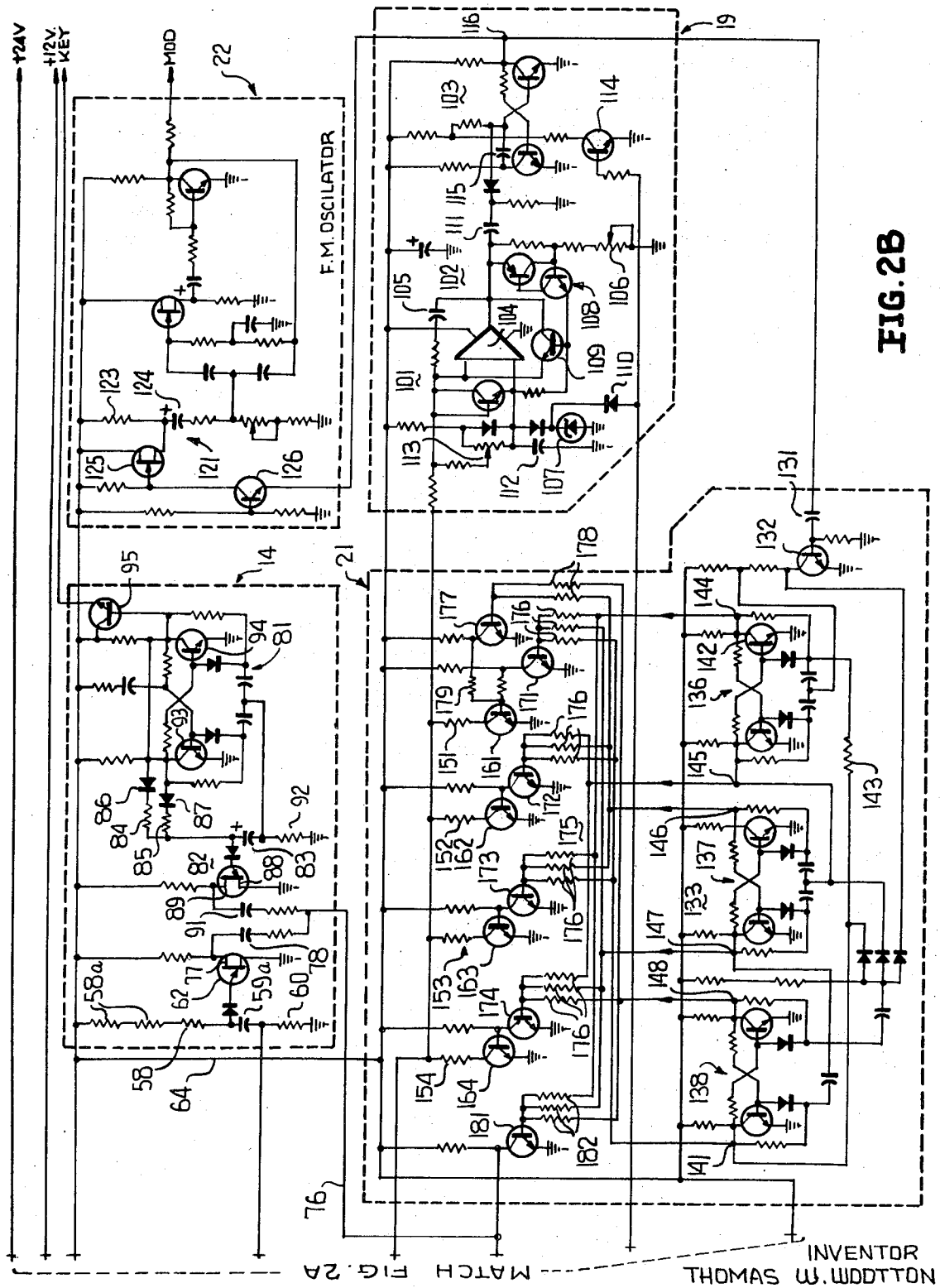

FIG. 2B

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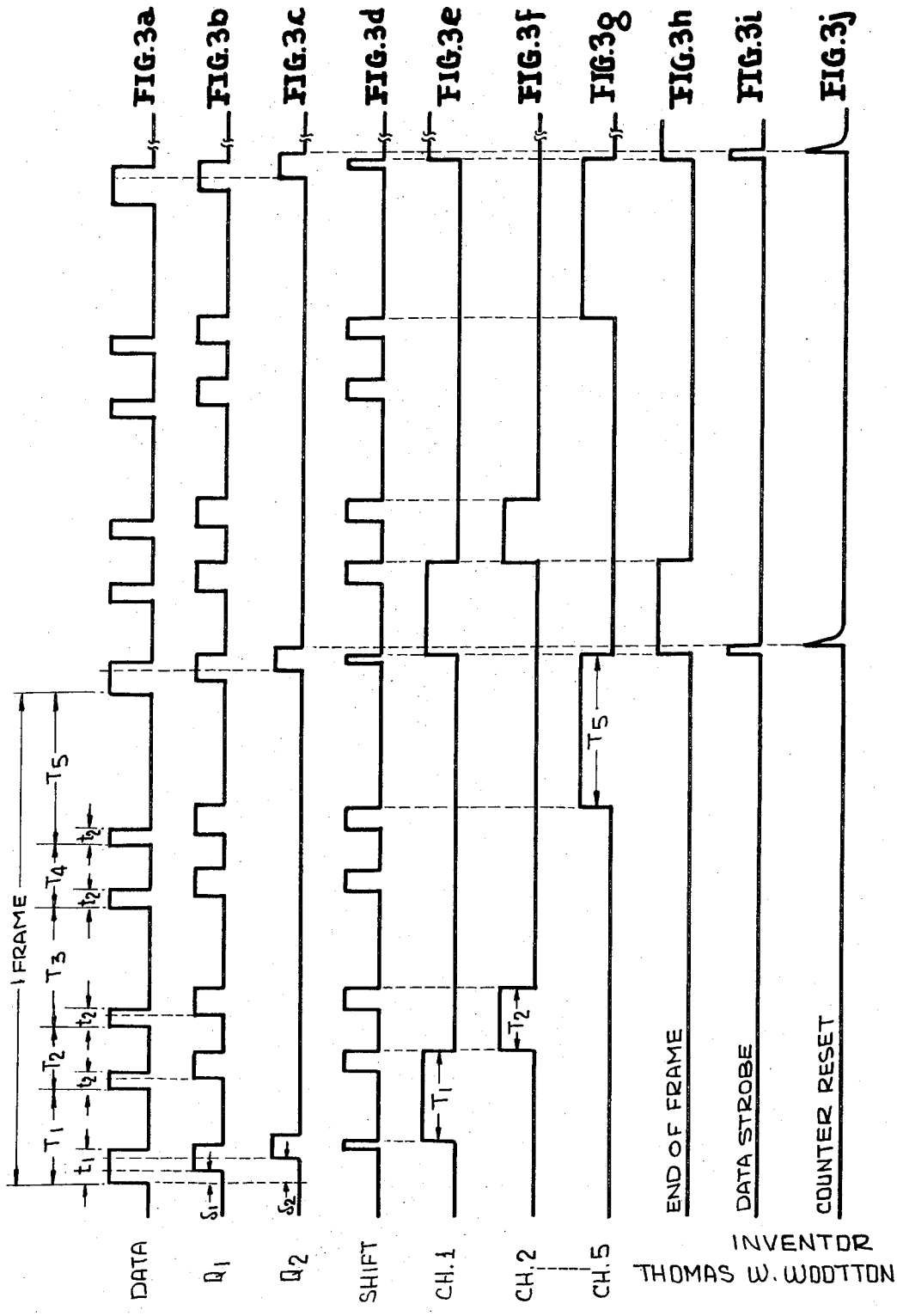

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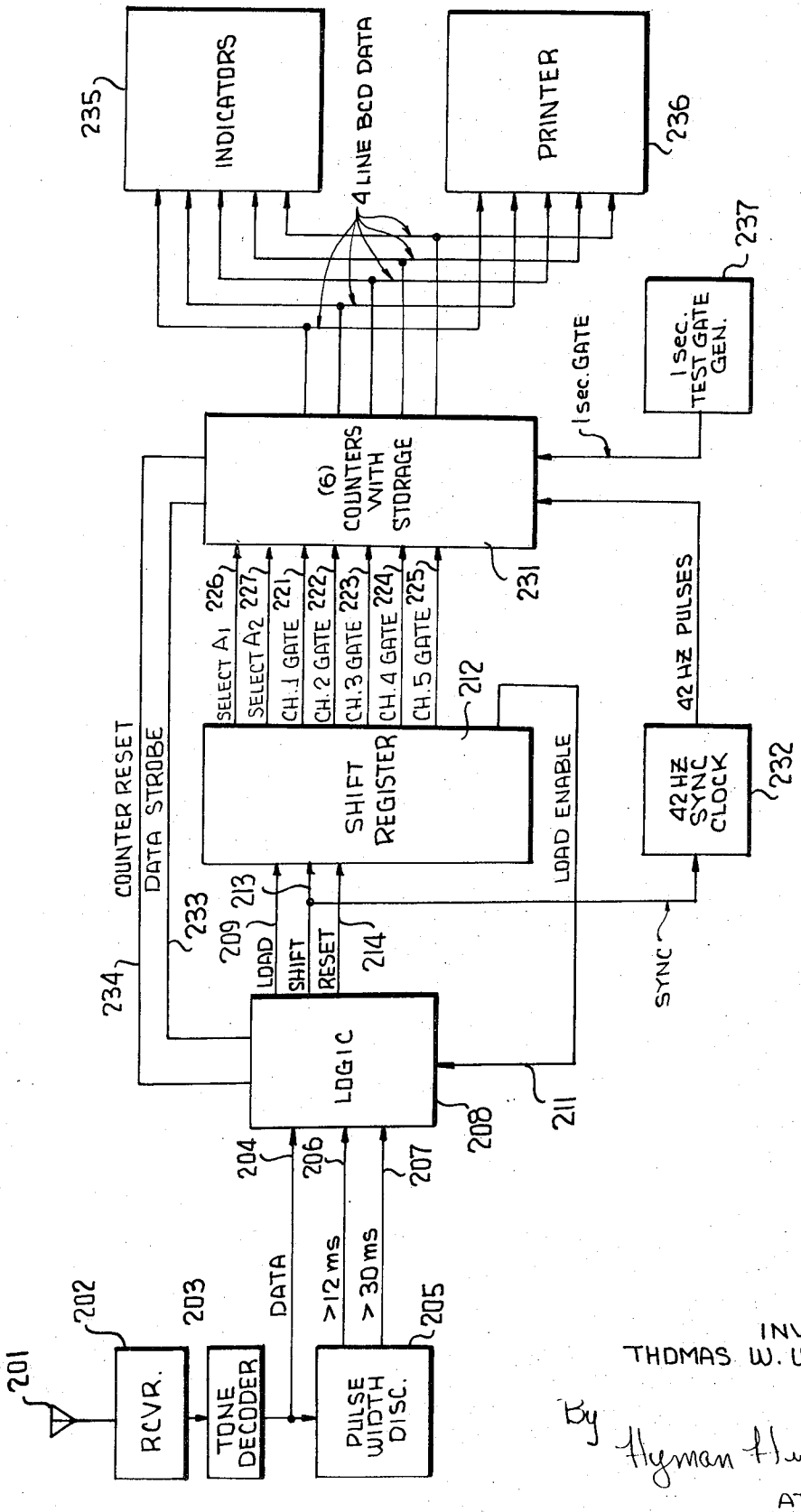

FIG. 4

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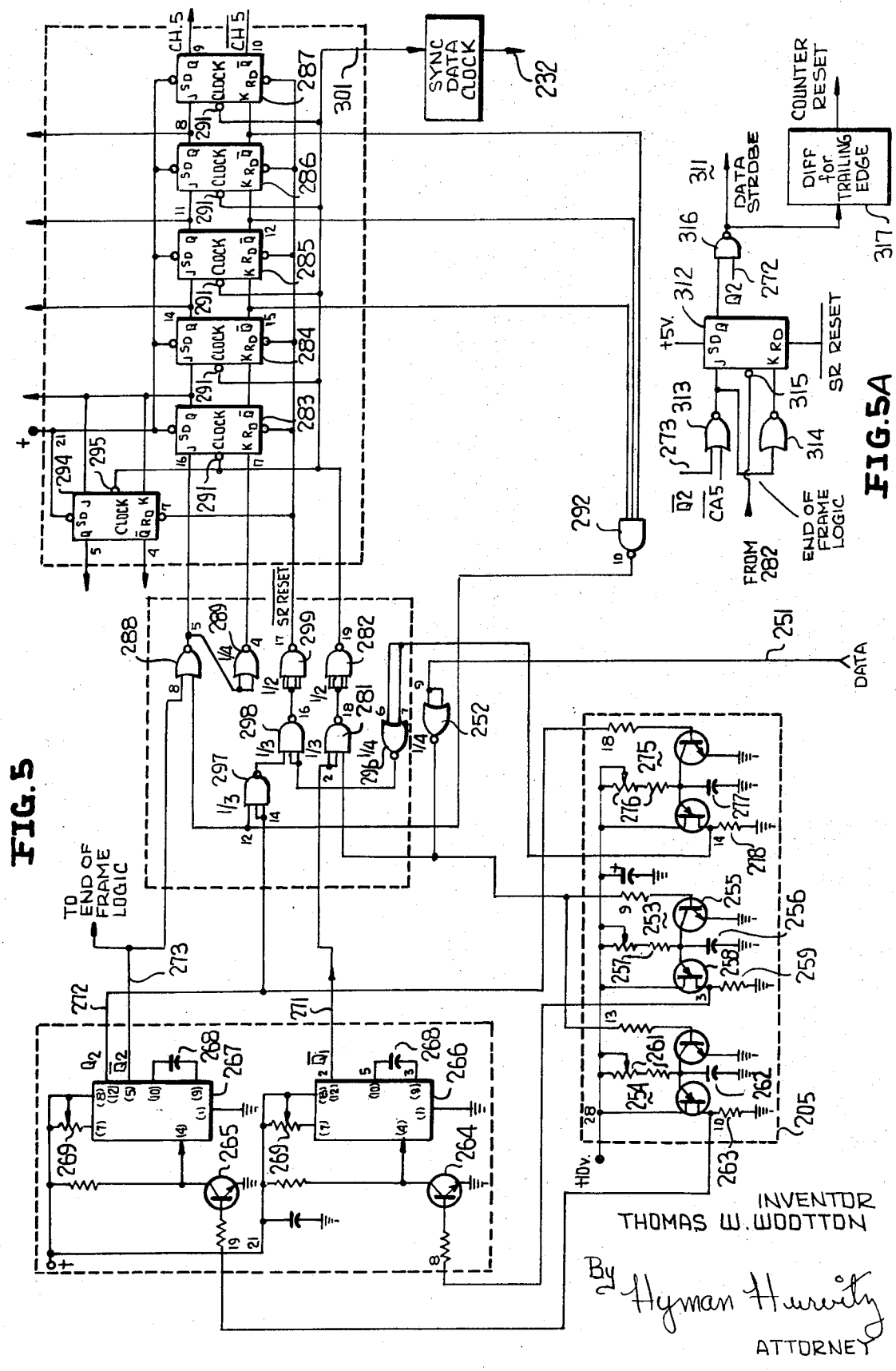

FIG.5

FIG.5A

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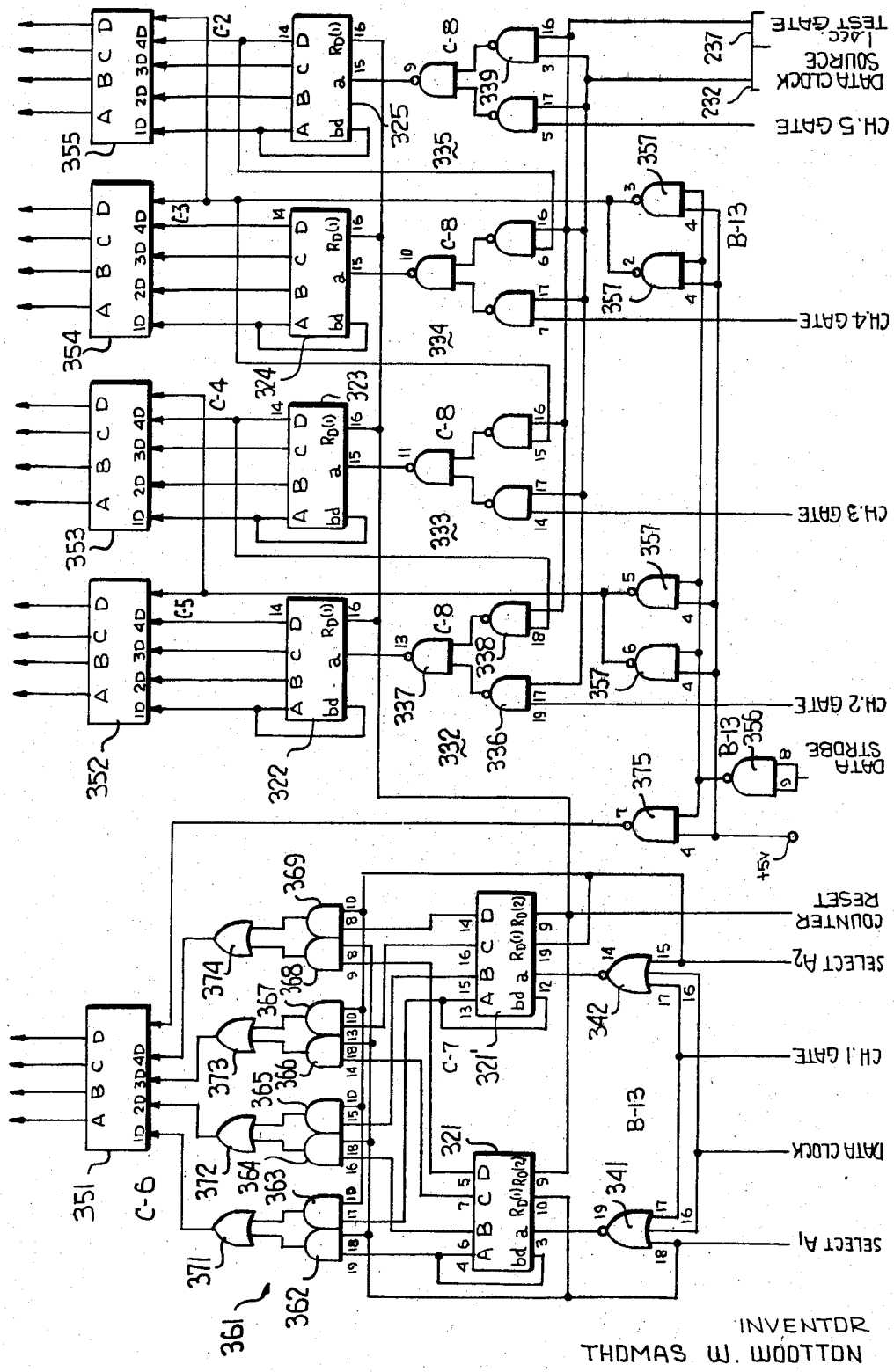

FIG.6

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PULSE POSITION MODULATED ALARM SYSTEM

The present invention relates generally to systems for monitoring alarm conditions at a plurality of peripheral stations and, more particularly, to a system for transmitting to a central station pulse position modulated signals indicative of the identity of a peripheral station sensing an alarm condition.

Briefly described, the alarm system of the present invention includes a plurality of peripheral stations which transmit via a radio link, rather than a hard wire link, signals indicative of the identity of a peripheral station where an alarm occurs, as well as the nature of the alarm. The use of a radio link, rather than a hard wire link as is generally the practice in the art, is advantageous because the need for a permanent installation is obviated and because of the ability to monitor mobile sites. A radio link is established between a particular peripheral, monitored station and the central station only in response to an alarm condition being sensed at the peripheral station. In response to an alarm condition being sensed at a particular peripheral station, a transmitter at the peripheral station is activated for a number of predetermined time periods separated from each other by a relatively long time interval. During each of the time periods a signal is repeatedly transmitted from the peripheral station to indicate the identity of the peripheral station, as well as the alarm condition being sensed. Thereby, a high integrity link between the peripheral and central stations is established. By providing relatively long time intervals between adjacent transmissions a number of peripheral stations can transmit data substantially simultaneously to the central station via a single radio band. In practice, it has been found that in excess of 80 peripheral stations can be monitored satisfactorily in this manner and studies indicate that a considerably greater number of stations can be satisfactorily handled.

Each peripheral station is identified with a different code number that is converted into a discrete valued pulse position modulated signal in response to an alarm condition being sensed. The source of the alarm condition sensed is also converted into a pulse position modulated signal that is in a wavetrain including the peripheral station identification signal. One of the pulses, a master pulse of the wavetrain which comprises a data frame, has an identifiable characteristic different from all of the other pulses of the frame enabling it to be detected at the central station and be used for enabling the master pulse to be identified with a particular bit used for signifying station identification or a sensed alarm.

At the central station frames from the peripheral stations are received, detected and processed to establish peripheral station identification and the source of the alarm at the particular peripheral station. Processing the signal at the central station involves detecting the identifiable characteristic of the frame master pulse received from the peripheral station. In response to the identifiable characteristic of the master pulse being detected, the time interval amongst the pulses is determined by gating a clock signal to a plurality of counters, at least one of which is provided for each of the pulses of the frame. The interval between adjacent pulses of succeeding frames is employed for indicating the magnitude of a data bit at the transmitting station.

Because of this factor, operations are performed during the first bit of each frame and the possibility of inaccuracies in measuring the duration of the first bit of each frame occurs. To obviate this possibility, the first bit of successive frames is fed to a pair of counters, one of which is utilized during a first frame and the second of which is employed during the succeeding frame. The two counters feed a common output display network, whereby the first data bit is presented in exactly the same form as other bits.

It is, accordingly, an object of the present invention to provide a new and improved system for monitoring at a central station alarm conditions existing at a plurality of peripheral stations.

Another object of the present invention is to provide a new and improved system for transmitting to a central station, via a radio link, indications of the identity of a peripheral station responding to an alarm condition, as well as indicative of the nature of the alarm being sensed.

Still another object of the invention is to provide a new and improved system for monitoring alarm conditions at a plurality of peripheral stations wherein indications of the station identity and nature of the cause of the alarm are transmitted to a central station by pulse position modulation on a radio link.

Still another object of the invention is to provide a new and improved alarm system employing pulse position modulation for identification of a peripheral station, wherein adjacent bits between different frames of data can be employed without affecting the accuracy of data processed at a central station responsive to the peripheral stations.

The above and still further objects, features and advantages of the present invention will become apparent upon consideration of the following detailed description of one specific embodiment thereof, especially when taken in conjunction with the accompanying drawings, wherein:

FIG. **1** is a block diagram of a preferred embodiment of a peripheral station in accordance with the present invention;

FIGS. **2***a* and **2***b*, taken together, are a circuit diagram of the station illustrated in FIG. **1**;

FIGS. **3***a*–**3***k* are waveforms useful in describing the operation of the system;

FIG. **4** is a block diagram of a preferred embodiment of a central station in accordance with a preferred embodiment of the present invention;

FIG. **5** is a circuit diagram of a portion of the central station illustrated in FIG. **4**;

FIG. **5***a* is a circuit diagram of another portion of the central station illustrated in FIG. **4**; and

FIG. **6** is a circuit diagram of another portion of the system illustrated in FIG. **4**.

The block diagram, FIG. **1**, of an exemplary peripheral station is substantially the same for all stations. The only differences between the different peripheral stations are that each is provided with a different identification code number and some may be provided with alarm sensors not included at other peripheral stations. Therefore, a description of one peripheral station suffices for all others.

The peripheral station, FIG. **1**, includes a plurality, not in excess of 10, of alarm sensor stations, each of

which may include a number of detectors. Each sensor station derives binary or on-off signals in response to occurrences, at a site where the station is located, of, for example: intrusion into the premises; fire; smoke; water; shock; power failure; and refrigeration loss. Each of sensor stations **1–10** normally derives a binary zero signal, but in response to an alarm condition being sensed derives a binary one signal. Sensor stations **1–10** are energized by d.c. power supply **12** under normal operating conditions. In the event of failure of power supply **12**, which is energized by a 115 volt, 60 Hertz source, sensor stations **1–10** are energized by a battery power supply **13** that is normally charged by power supply **12**.

Power from supply **12** or battery supply **13** is coupled to remaining circuitry in the peripheral station through electronic switch **14** and regulator **15** only in response to a binary one signal produced by one or more of sensor stations **1–10**. To the end, output signals from sensor stations **1–10** are combined and fed to electronic switch **14** to actuate the switch into a conducting state for a predetermined time interval, on the order of 3 minutes, after initial sensing of an alarm condition. During each of these 3-minute intervals, electronic switch **14** produces keyed voltages on lead **16** to enable r.f. transmitter **17** to be energized for 30-second periods with a duty cycle of approximately 33 ⅓ percent, whereby transmitter **17** is keyed on for 10-second intervals and keyed off for 20-second intervals. During a 3-minute interval, transmitter **17** is therefore keyed to an on condition for six 10-second periods. During each of the 10-second periods, transmitter **17** is supplied with at least 10 frames of data, each of which is less than one second in duration. Each data frame includes pulse position modulated bits, the positions of which indicate the code identification number of the peripheral station and a number associated with the sensor station deriving a binary one signal. By repeatedly transmitting the same data at spaced intervals over the relatively long time interval of 3 minutes, signal integrity between the peripheral station and a central station, described infra, is maintained while allowing a large number of peripheral stations to transmit on the same frequency to the central station.

Signals derived from sensor stations **1–10** are fed via bus **18** to code generator **19**, which generates a pulse position output having only one of 10 discrete values. The pulse position signal generated by code generator **19** in response to signals applied to the code generator on bus **18** indicates which one of the 10 sensor stations at the peripheral station is activated into a binary one state. The pulse position is represented by the separation between the first and second pulses of a five-bit frame. The first pulse bit in each frame, termed a master pulse, has an identifiable characteristic different from all other bits within a frame, such as a time duration greater than any of the other bits in a frame.

Code generator **19** also responds to identification number generator **21** which supplies control signals to code generator **19** in response to power being supplied to the number generator through switch **14** and regulator **15**. The identification number generator **21** included at each peripheral station is different, with each station being assigned a different number which can possibly range from 0000 to 9999. To this end, identification number generator **21** includes circuitry for deriving four channels or bits, capable of having any of the discrete levels between zero and nine. The four bits derived by number generator **21** are supplied to code generator **19** to control the relative pulse positions of the second through fifth bits or channels of each frame and the fifth bit of that frame and the first bit of the next succeeding frame. Thereby, the pulse interval between the second and third, third and fourth, fourth and fifth bits of each frame and the fifth and first bits of succeeding frames are controlled by the four bits supplied to code generator **19** by number generator **21**. During each data frame, code generator **19** therefore derives a first binary one level having a relatively long time duration followed by second, third, fourth and fifth relatively short duration binary one levels. Between each of the binary one levels derived by code generator **19** a binary zero level is derived. A binary zero level is also derived between the fifth binary one level of each frame and the first binary one level of the next succeeding frame, whereby the time period between the leading edges of the last pulse of a first frame and the first pulse of the next succeeding frame is a pulse position and indicative of one of the discrete values fed to code generator **19**. By using this pulse position technique, time spacing between adjacent frames is minimized and the need for time synchronization between adjacent frames is eliminated.

The binary one and zero levels derived by code generator **19** control the frequency of tones derived by transmitter **17**. To this end, the output of code generator **19** is supplied to modulation oscillator **22** which derives an audio frequency tone of a first frequency, 1.4 KHz, in response to a binary zero level being supplied thereto and a second audio tone, of frequency 1.5 KHz, in response to a binary one level being fed thereto. The discrete frequency tones generated by oscillator **22** are fed to amplitude modulator **23** for transmitter **17**. Transmitter **17** is also responsive to crystal controlled oscillator **24** so that it derives, while keyed on, 10 frames of r.f. signals that selectively amplitude modulate the carrier frequency of oscillator **24** by either 1.4 or 1.5 KHz. By continuously transmitting a.m. signals having only one or two modulation frequencies throughout a 10-frame interval, system noise is minimized and receiver detection problems simplified.

To enable each remote station to have substantially the same equipment, as described, the output of transmitter **17** is supplied to an omnidirectional, low-gain antenna **25**. Power supplied by transmitter **17** to antenna **25** is of a sufficiently high level to enable facile signal detection at the central station.

Reference is now made to FIGS. **2***a* and **2***b*, detailed circuit diagram of components illustrated in the block diagram of FIG. **1**, wherein sensor stations **1** and **2** are illustrated as intrusion detection devices. The remaining sensor stations **3–10** are identical to sensor stations **1** and **2**, with the only possible difference being in the type of transducers provided to establish binary one and zero levels; thereby, there is no need to illustrate details of the other sensor stations.

Sensor station **1** includes a pair of conducting tapes **31** and **32** which serve as transducers for determining if an intrusion has been made into a protected area.

Tapes 31 and 32 normally provide conducting paths to electrodes of normally conducting NPN transistor 33 and are mutually insulated from each other. When an intrusion occurs into a region being protected by tapes 31 and 32, one or both of the tapes are either open-circuited or the two tapes are short-circuited together to change the bias potential applied to electrodes of transistor 33 whereby the transistor is rendered into a cut-off condition. In response to transistor 33 being activated into a cut-off condition, the voltage of the transistor collector increases in magnitude. The increase in the collector voltage of transistor 33 is coupled through diode 34 and a filter or delay network including shunt resistor 35 and shunt capacitor 36, allowing the capacitor to charge. In response to capacitor 36 being charged for a predetermined time interval a voltage of sufficient magnitude is derived thereby to enable activation of latch circuit 37 into a conducting low impedance state. The filter circuit comprising resistor 35 and capacitor 36 thereby prevents false tripping of latch network 37 in response to noise pulses which occasionally are derived at the collector of transistor 33.

Latch network 37 is normally biased by the collector voltage of transistor 33 into a nonconducting state and is activated into a conducting state as indicated supra. The conducting state of latch 37 is maintained until the latch is reset, either manually or after a predetermined time interval, on the order of 3 minutes. Latch network 37 is a regenerative network including PNP transistor 38 and NPN transistor 39. The emitter of transistor 38 is responsive to the voltage developed across the filter network including resistor 35 and capacitor 36. The collector of transistor 38 is short-circuited to the base of transistor 39, the collector of which is connected in the regenerative network back to the base of transistor 38. With this circuit arrangement, a sufficiently high voltage applied to the emitter of transistor 38 activates both of transistors 38 and 39 into a conducting state which is maintained until the current at the emitter of transistor 38 is reduced to a predetermined level by a reset action.

Latch 37 functions in conjunction with capacitor 36 to develop a sudden decrease in the voltage across resistor 35 immediately after the latch has been triggered or activated. This is because latch 37, once fired, establishes a low impedance path across capacitor 36 to suddenly reduce the voltage across the capacitor. Since the low impedance path is maintained across capacitor 36 as long as the latch is energized no further sudden voltage changes can be developed across capacitor 36 until the latch is reset. If the alarm condition still exists when the current at the emitter of transistor 38 is reduced by the reset action, latch 37 remains in the triggered state by virtue of the current supplied thereto through diode 34. Deactivation of triggered latch 37 can therefore only occur in response to the alarm condition being remedied and reset action simultaneously occurring. Thereby, only one sudden change in the voltage across capacitor 36 can be derived in response to each alarm condition. This is desirable to preclude repeated transmission of the same information from the same peripheral station, whereby a large number of peripheral stations can be monitored, each with the same carrier transmission frequency.

Sudden changes at the input of latch 37, which therefore can occur only in response to sensor station 1 responding to an intrusion, are a.c. coupled via capacitor 41 to latching network 42 that controls activation of switch 14. To this end, the emitter of transistor 38 is connected via capacitor 41 and diode network 43 through manually activated day/night switch 44 to the input of latch 42, at the junction between the base of transistor 45 and collector of transistor 46. Day/night switch 44 is activated by a subscriber at the peripheral station to connect sensor station 1 in the circuit only while it is desired to have the premises guarded against intrusion, which generally occurs only when the subscriber is not present at the premises. Day/night switches 44 are not provided for sensor stations that must be operative while the premises are being occupied by the subscriber: examples of detectors at such sensor stations are fire detector, smoke detector, water detector and refrigeration loss detector.

Sensor station 1 is provided with a precision resistor 51 that is selectively connected in circuit with code generator 19 in response to latch 37 being activated into a conducting state by intrusion being detected by sensor 1. Resistor 51 is connected to code generator 19 during a predetermined time interval or channel within each of the data frames. To this end, resistor 51 is connected to the collector of NPN transistor 52, the emitter of which is connected via diode 53 to the collector of transistor 39, whereby in response to latch 37 being activated transistor 52 is activated into a conducting state in response to a positive bias voltage being applied to the base thereof. If latch 37 is not energized into a conducting state, transistor 52 is cut off regardless of the bias voltage applied to its base electrode. In response to transistor 52 being in a conducting state, a circuit path is established via bus 18 from ground, at the emitter of transistor 39, to resistor 51 and the input of code generator 19. A similar circuit is provided in each of the other sensors 2–10 in response to these sensors detecting alarm conditions. The valve of resistor 51 at each of the different sensors, however, is different, whereby a different value of resistance is connected by an activated sensor to number generator 21. The values of the precision resistors are selected so that 10 different discrete pulse positions, one for each of the sensors, can be derived by code generator 19.

Continuing now with the description of the circuitry for controlling power supply switch 14, latch 42 is activated into a conducting state in response to a pulse being supplied thereto through any of the capacitors 41 of the several sensors. In response to a sudden change negative going voltage change across capacitor 36, PNP transistor 55, which functions as regulator 15, is activated into a conducting state to control bias levels applied to the bases of NPN power switching transistors 56 and 57, having collectors connected to d.c. power supply line 460. Transistors 55–57 are normally in a cut-off condition, whereby the circuits energized through them are normally in an unpowered condition; these circuits are: transmitter 17, code generator 19, identification number generator 21, modulation oscillator 22, amplitude modulator 23, and crystal controlled oscillator 24. D.C. power is supplied via line 460 to transistors 55–57 by a power supply responsive to a

115 volt, 60 Hertz a.c. source that is fed to transformer 58 and converted to d.c. by rectifier 59. The d.c. output voltage across rectifier 59 and filter capacitors 61 charges batteries 62 so that these batteries are constantly maintained in a state of readiness in the event of an a.c. power failure. A tap between capacitors 61 and batteries 62 is connected in parallel to the emitter of regulating transistor 55 and switch transistors 56 and 57 to supply voltages of the appropriate level to the various circuits energized thereby.

In response to transistors 56 and 57 being activated into a conducting state, the peripheral station is allowed to remain in an energized state for only a predetermined time interval, preferably a relatively long interval, such as 3 minutes. To this end, switch 14 includes a 3-minute timer comprising series connected resistors 58, capacitor 59 and load resistor 60, all of which are connected in shunt with the emitter of transistor 56. The values of resistors 58 and capacitor 59 are selected to provide an r.c. time constant on the order of 3 minutes, whereby the voltage across capacitor 59 after 3 minutes reaches a predetermined level which can activate a trigger circuit including unijunction transistor 62. In response to the eta value (the intrinsic standoff ratio of a unijunction transistor) of unijunction 62 being reached, capacitor 59 is discharged through the unijunction transistor, whereby there is derived a relatively short duration pulse across load resistor 60. The eta value of transistor 62 can, however, be reached with the illustrated circuit approximately 3 minutes after charging of capacitor 59 commences only by lowering the high voltage base of the unijunction. The circuit is designed in this manner to synchronize cut-off of power after 3 minutes of operation in synchronism with the derivation of the first or master pulse of each data frame; the master pulse is derived on lead 76 in a manner describe infra. To establish synchronism between activation of unijunction 62 and the master pulse, the signal on lead 76 is fed to the high voltage base of the unijunction through capacitor 78, whereby the unijunction eta value is reduced, whereby capacitor 59 is discharged. The negative pulse derived across load resistor 60 is fed via diode 63 to the base of transistor 46 of latch 42 to energize the latch and remove bias current from the base of transistor 55. Thereby, transistors 56 and 57 are activated into a cut-off state and power is removed from the circuits energized through them.

In response to the cut-off of current through transistors 56 and 57 reset current is supplied to latch circuit 37 of the sensor station which had previously been activated into an alarm or tripped state. To these ends, the emitter of power switching transistor 56 is connected via lead 64 to the base of transistor 65 included in electronic reset network 66. While current is being derived from the emitter of transistor 56, transistor 65 is activated to a conducting state and capacitor 67, in the collector circuit of transistor 65, is maintained substantially at ground potential. In response to cut-off of current at the emitter of transistor 56, transistor 65 is cut off and capacitor 67 is charged through resistor 68 until the eta value of unijunction transistor 69 is reached. In response to the eta value of unijunction transistor 69 being achieved, the unijunction is rendered into a conducting state, whereby transistor 71, connected across load resistor 72 of unijunction 69, conducts for a short time interval. Conduction of transistor 71 results in a low impedance path being provided between the anode of diode 73 and ground, whereby a current path to the input of latch 37 is removed. If no other current path then exists to the input of latch 37, as occurs only if the detector tapes 31 and 32 of sensor 1 have been repaired to render transistor 33 conducting, the latch is reset. Resetting latch 37 has substantially no effect on the voltage of capacitor 36 because it is not connected to any voltage source while transistor 33 is conducting, as occurs during periods of no alarm being detected, and because of bleed resistor 35. If no alarm is detected by station 1, resetting of latch 37 can also be accomplished manually, if no automatic circuit is provided, by closing normally open-circuited, spring biased switch 74. In response to switch 74 being manually depressed, ground is momentarily established at the base electrode of normally forward biased transistor 75 to activate the transistor into a relatively high impedance state. With the emitter collector path of transistor 75 in a relatively high impedance state, the current supplied to diode 73 is reduced to extinguish latch 37.

To enable 10 data frames, each having a time duration of less than 1 second, to be transmitted with a duty cycle of approximately 33 ⅓ percent, keying levels are sequentially applied by flip-flop 81, within switch 14, to transmitter 17. Flip-flop 81 is driven by the output of timing network 82 which derives sequences of first and second short duration pulses. The first pulse derived by timing network 82 precedes the second pulse by approximately 10 seconds, and the second pulse precedes the next first pulse by approximately 20 seconds. The first and second pulses are synchronized with master pulses derived on lead 76, whereby transmitter 17 is keyed on and off at intervals in synchronism with the master pulses of spaced data frames. To assure repetitive initial turn on of the same transistor of flip-flop 81 resistor 501 and capacitor 502 are connected to the base of transistor 93, whereby transistor 93 is always initially in an on condition and transistor 94 is always initially cut off.

To these ends, timing network 82 includes capacitor 83 that is selectively connected in circuit with resistors 84 and 85 through diodes 86 and 87, respectively. Resistors 84 and 85 have differing values which, together with the value of capacitor 83, enable first and second time constants of approximately 10 and 20 seconds to be established for timing network 82. Timing network 82 also includes unijunction transistor 88, the high voltage base 89 of which is a.c. coupled via capacitor 91 to lead 76. In response to the voltage across capacitor 83 exceeding a predetermined value while base 89 of unijunction transistor 88 is at a relatively low level in response to a frame master pulse being derived on lead 76, the unijunction transistor is fired. Firing of unijunction 88 causes the charge on capacitor 83 to be dissipated through the unijunction so that a negative pulse is developed across load resistor 92, connected between capacitor 83 and ground.

The negative pulse developed across load resistor 92 is fed as a trigger to flip-flop 81 to change the conducting state of transistors 93 and 94 thereof. In response to transistor 93 being in a conducting state and transistor

94 being cut off, diode 86 is activated into a conducting state and diode 87 is cut off, whereby resistor 84 is connected in circuit with capacitor 83. In response to transistor 94 conducting and transistor 93 being cut off, the opposite conditions exist so that resistor 85 is connected in circuit with capacitor 83 to the exclusion of resistor 84. Thereby, flip-flop 81 is operated in synchronism with firing of unijunction transistor 88 and the voltage developed at the collector of transistor 94 comprises a series of rectangular waves having leading and trailing edges displaced from each other by approximately 10 and 20 seconds and in time synchronism with master pulses of spaced data frames.

The voltage at the collector of transistor 94 biases the base of transistor 95 into conducting and nonconducting states. The emitter collector path of transistor 95 is connected between the emitter of power switching transistor 56 and a keying input terminal of transmitter 17 to energize the transmitter into an active state for approximately 10 second intervals synchronized with the occurrence of the first or master pulse of the first frame in a group of 10 frames and the last pulse of the 10th frame of the group. The transmitter remains inactive for 20 seconds, until it is again energized into an active condition simultaneously with the derivation of the first master pulse of the first frame of a succeeding group of frames.

Consideration is now given to the code generator 19 for converting the value of precision resistor 51 at the sensor station which detected an alarm condition. Basically, code generator 19 includes integrator 101, a level detector 102 and a monostable or one-shot multivibrator 103. In response to the output voltage of integrator 103 reaching a predetermined level, which occurs at a time determined by the slope of the integrator output voltage, level detector 102 derives a pulse to trigger monostable 103. Code generator 19 also includes, within monostable 103, means for establishing data synchronism between the peripheral and central stations. To these ends, the first or master pulse of each frame has a longer duration than the remaining pulses of the frame, all of which have the same duration. The separation between the leading edges of adjacent pulses is a mark of pulse position. The separations are capable of having one of 10 discrete values depending upon the number of the sensor station detecting an alarm condition and the identification number of the peripheral station.

Precision resistor 51 of a sensor station detecting an alarm condition is connected in circuit with integrator 101 for a time interval equal to the first channel of each frame to determine the r.c. time constant of the integrator 101 during that channel. As seen infra, upon completion of the first channel a different resistor, indicative of a peripheral station number, is connected to the input of the integrator 101 and remains connected to the integrator only until that channel is completed. In this manner, during the different channels different resistance values are connected in circuit with integrator 101 to enable pulse position data to be derived.

Integrator 101 includes operational amplifier 104 and feedback capacitor 105. Capacitor 105 charges at a rate determined by the resistor 51 connected in circuit therewith until a predetermined voltage level, determined by the position of the slider of potentiometer 106 and the characteristics of Zener diode 107, is reached at the output terminal of amplifier 104. In response to this voltage level being reached, trigger network 108 is activated from its normally nonconducting state into a conducting state to bias the emitter collector path of transistor 109 into a low impedance state. The low impedance state of transistor 109 is connected across capacitor 105 to discharge the capacitor quickly to a reference potential, at the input of operational amplifier 104. In response to capacitor 105 being discharged to the reference potential, the output voltage of amplifier 104 suddenly decreases, whereby a negative going pulse is coupled by capacitor 111 to monostable multivibrator 103. Latch 108 is returned to a nonconducting state almost immediately after capacitor 105 has been discharged because an inadequate supply of current is fed to the latch through the capacitor. Thereby, the capacitor can again commence to be charged in response to the voltage applied to the input of integrator 101. Voltage supplied to the input of integrator 101 is filtered by shunt filter capacitor 112 to decouple sudden changes thereof at the beginning of each channel. Potentiometer 113 is provided in the input circuit of amplifier 104 to provide a bias drift adjustment; the potentiometer setting can be different for different stations, depending upon differing ambient conditions.

It is to be noted that Zener diode 107 serves a second function of controlling the voltage on lead 76 so that it can never exceed a value where false triggering of sensor stations 1–10 can occur in response to master pulses at the beginning of each frame. To this end, the cathode of Zener diode 107 is connected via hold-off diode 110 to lead 76.

To enable two different binary one pulse durations to be derived by monostable multivibrator for master pulse identification, the monostable includes a switching transistor 114 for selectively varying the potential applied to charging capacitor 115 of the monostable. The base of transistor 114 is connected via a d.c. path to lead 76 on which there is derived a level for enabling detection of which of sensor stations 1–10 is in an alarm state; this level is hereafter referred to as a sensor code gate and has a duration of one channel. In response to a sensor code gate being derived on lead 76 transistor 114 is driven from its normally cut off condition to a low impedance conducting state so that monostable multivibrator 103 derives an output pulse or binary one level for a relatively long time interval of 34 milliseconds. After the 34 millisecond time interval has been completed, monostable multivibrator changes state whereby a low level, binary zero signal is derived on lead 116. Monostable multivibrator 103 continues to derive a binary zero level until another pulse is fed thereto through capacitor 111, at the beginning of the second data channel of a frame. Thereby, the time interval between the beginning of adjacent initial activations of monostable 103 into a binary one state provide a measure of the value of the resistor connected to the input of integrator 103 during the period between the initial activations.

In response to the pulse fed through capacitor 111 at the beginning of the second channel, monostable multivibrator 103 is again activated into a binary one state, whereby a binary one level is derived on lead 116. Dur-

ing the second channel, however, monostable multivibrator **103** remains in the binary one state for a relatively short duration, such as 17 milliseconds, because forward bias is no longer applied to transistor **114** to shift the charging level of capacitor **115**. Monostable multivibrator **103** remains in the binary zero state until the third frame commences, as determined by coupling of a pulse through capacitor **111** to the monostable multivibrator. During the third channel, the monostable multivibrator **103** again derives a 17 millisecond binary one level, after which it returns to a binary zero level. Monostable multivibrator **103** continues to operate in this manner during the fourth and fifth channels of the frame while peripheral station identification bits are being applied thereto. After the fifth channel has been completed, and as the first channel of the next succeeding frame begins, monostable multivibrator **103** is activated into a condition whereby it again derives a binary one level for a 34 millisecond time interval. These 34 millisecond binary one levels derived by monostable multivibrator **103** are the master pulses having identifiable characteristics different from the other pulses of the frame and enable the central station correctly to interpret data transmitted thereto from the peripheral stations.

The binary one and zero levels derived on lead **116** at the output terminal of monostable multivibrator **103** are applied to f.m. oscillator **22** to control the frequency of the oscillator so that it derives a sinusodial output having a first frequency of 1.4 KHz in response to a binary zero level being generated on lead **116** and a second frequency of 1.5 KHz in response to a binary one being derived on lead **116**. F.M. oscillator **22** is of the conventional parallel T type and includes a frequency determining network **121** that comprises, interalia, resistor **123** and capacitor **124**. To vary the impedance of network **121** and thereby the oscillator frequency, resistor **123** is selectively short-circuited by the source drain path of field effect transistor **125** in response to the binary signal level derived on lead **116**, as coupled to the field effect transistor through the emitter collector path of switching bipolar transistor **126**. Since the remaining circuitry of oscillator **22** is conventional, no detailed description thereof is provided. The output tones of oscillator **22** are fed to amplitude modulator **23**, as described supra in conjunction with FIG. **1**.

To control the sequential readout of the first channel of each frame (the channel that indicates which of the sensor stations is detecting an alarm condition) and the second through fifth channels of each frame (the channels that designate the identification number of the peripheral station in four decimal decades), output signals of monostable multivibrator **116** are coupled via capacitor **131** and transistor **132** to divide by five counter **133**. Counter **133** includes three binary stages **134**, **135** and **136** interconnected with each other in a well known manner so that five different combinations of outputs are derived from the two output leads of each of stages **136–138**.

Because counter **133** includes three stages it can be initially activated to any one of eight different states, termed unallowable states. In the event of counter **133** being initially activated to one of the unallowable states the counter is returned to its initial state in response to the first input pulse fed thereto after application of power. To this end, the voltage at output terminal **141** of stage **138** has a binary one level only if counter **133** is in an unallowable state. This binary one level is fed back to the input of transistor **142** of stage **136** via coupling resistor **143** and causes the first pulse applied to the input of counter **133** to derive the counter to its initial condition.

Counter **133** supplies pulses in sequence to its output terminals **141** and **144–148** in response to the successive application of input pulses thereto from monostable multivibrator **103** to enable resistors indicative of the identification number of the peripheral station and the sensor station detecting an alarm condition to be connected in sequence to the input of integrator **101**. To establish identification codes for up to 9999 different peripheral stations, identification number generator **21** includes four different precision resistors **151–154**. Each of resistors **151–154** can have any one of 10 discrete values to determine the number of identification code for a particular peripheral station. Thereby, the combination of precision resistors **151–154** at each of the peripheral stations is different to establish different pulse position identification signals.

Precision resistors **151–154**, as well as the precision resistor **151** of the sensor station detecting an alarm condition, are sequentially connected in circuit with the input of integrator **101** in response to the sequential derivation of binary zero and one levels at terminals **141** and **144–148** of counter **133**. Conducting paths to the input of integrator **103** through precision resistors **151–154** are respectively provided by the emitter collector paths of normally cut off switching transistors **161–164**. The conducting states of transistors **161–164** are respectively controlled by the collector voltages of normally conducting transistors **171–174**, the bases of which are connected to be responsive to the voltages at terminals **141** and **144–148** through resistor decoding network **175**. Three decoding resistors **176** of network **175** are connected between output terminals of the three counter stages **136–138**, whereby only one of transistors **171–174** can be activated into a cut-off condition at a time. The selected one of transistors **171–174** that is driven into cut off causes the base voltage of the switching transistor **161–164** with which it is connected to be forward biased whereby a path for the corresponding one of resistors **151–154** is provided between ground and the input of integrator **101**.

In the event of counter **133** being initially in an unallowable state, identification number generator **21** is energized so that resistor **151** is initially connected in circuit with the input of integrator **101**, whereby an output signal can be derived from a monostable multivibrator **103** to enable further triggering of counter **133**. To this end, there is provided a normally conducting transistor **177**, the base of which is connected to terminals **146** and **148** of counter **133**. If counter **133** is initially in any of the unallowable states, terminals **146** and **148** feed bias voltages to the base of transistor **177** through resistors **178** to cut off transistor **177**. The collector of transistor **177** is connected via resistor **179** to the base of transistor **161**, whereby the emitter collector path of transistor **161** is activated to a closed state as long as counter **133** remains in the unallowable state.

This assures the derivation of an output pulse from monostable multivibrator 103 and drives counter 133 back to its initial condition.

To enable transistor 52 of the sensor station detecting an alarm condition in sequence with energization of transistors 161–164, transistor 181 is provided. Transistor 181 is connected via resistors 182, which can be considered as part of decoding network 175, to selected ones of terminals 141 and 144–148 in such a manner that transistor 181 is driven from its normally conducting state into a cut-off condition in response to resistor 154 being decoupled from the input of integrator 101. The collector of transistor 181 is connected to lead 76 which feeds sensor code gates to timing circuit and switch 14 and to control the conduction of transistor 114 of monostable multivibrator 103, as described supra. The collector of transistor 181 also connected to the base of transistor 52 to drive the emitter collector path of transistor 52 of the sensor station detecting an alarm condition into a conducting state, whereby precision resistor 51 at the sensor station is connected to the input of integrator 101.

A further feature of the invention concerns a network for monitoring sensor stations 1–10 and providing a visual indication to personnel at the guarded premises of one of the sensor stations being in an alarm condition or none of the sensor stations being in an alarm condition. To this end, red and green indicator lamps 185 and 186 are provided. Indicator lamp 185 is energized in response to an alarm condition being detected by any one of sensor stations 1–10, while lamp 186 is energized in response to none of the sensor stations detecting an alarm condition. Indicator lamps 185 and 186 are, in effect, responsive to the voltage at the emitter of transistor 38 of latch circuit 37.

In response to an alarm condition being detected, the emitter of transistor 38 is substantially at ground potential, which is coupled through diode 73 to the emitter of transistor 75 to activate the latter transistor into a conducting state. In response to transistor 75 being activated into a conducting state, transistor 188 is forward biased so that the collector thereof supplies positive current to the base of transistor 187. Transistor 187 is thereby activated into a conducting state and lamp 185 is energized. Simultaneously with transistor 187 being activated into a conducting state, transistor 189, the base of which is d.c. coupled to the collector of transistor 187, is rendered into a cut-off condition. With transistor 189 cut off, diode 190, connected to the collector thereof and to indicator lamp 186, is back biased. Back biasing of diode 190 prevents the flow of current to indicator lamp 186 and it is not activated as a result. In response to latch circuit 37 being in a non-conducting state, a relatively high voltage is applied to the emitter of transistor 75, whereby the conducting properties of transistors 187–189 are reversed and lamp 186 is energized to the exclusion of lamp 185.

The system of FIGS. 2*a* and 2*b* responds to the value of precision resistor 51 at a sensor station responding to an alarm condition and the values of code identification precision resistors 151–154 to derive a plurality of frames, having a wavetrain as indicated in FIG. 3*a*. From FIG. 3*a*, it is noted that the first binary one level or bit within each frame has a length, t_1, considerably in excess of the other binary bits within the frame, which bits have a duration of t_2. The time intervals T_1–T_4 between the leading edges of the adjacent pulses within the data frame respectively define the magnitude of the 10 discrete levels associated with which one of the sensor stations 1–10 detects an alarm and the three most significant decades of the station identification number. The time interval, T_5, between the leading edge of the fifth pulse in each frame and the leading edge of the first or master pulse of the next succeeding frame has one of 10 discrete levels indicative of the least significant decade of the peripheral station identification number. The time intervals T_1–T_5 define five different channels within a frame and are frequently referred to herein as such.

Data frames transmitted from different peripheral stations or from the same peripheral station in response to different sensor stations detecting an alarm condition have different frame durations whereby the frame rate can be considered essentially as random for any particular peripheral station or sensor station. The random nature of frame duration occurs because of the pulse position modulation technique whereby the spacing between adjacent pulses can be different and because the fifth channel of each frame is completely occupied by data, the magnitude of the least significant decade of the peripheral station code number. Since the last channel of each frame is followed immediately by a master pulse of the next succeeding frame, there are no unusual time segments and the highest data transmission rate possible can be employed.

The wavetrain illustrated by FIG. 3a is transmitted to the central station, the block diagram of which is disclosed in FIG. 4. The central station includes an omnidirectional antenna 201 which feeds receiver 202 that is tuned to the frequency of transmitter 17 of each peripheral station. Receiver 202 demodulates the amplitude modulated signal transduced by antenna 201 and feeds a series of tones having a frequency of 1.4 KHz or 1.5 KHz to tone detector 203. Tone detector 203 derives binary one and zero levels that are fed to data line 204 and are replicas of binary levels derived by code generator 19, FIG. 2*b*. Tone decoder 203 also drives pulse width discriminator 205 which includes a pair of output leads 206 and 207.

Discriminator 205 responds to the length of the tones derived by decoder 203 to derive, on lead 206, a binary one level in response to a binary one signal being derived by the tone decoder for a predetermined time interval slightly less than the time interval t_2 of the second through fifth pulses of each frame; in an exemplary embodiment, pulse width discriminator 205 derives a binary one level on lead 206 in response to a binary one being derived by tone decoder 203 for an interval in excess of 12 milliseconds. Discriminator 205 also includes circuitry for deriving a binary one on lead 207 in response to tone decoder 203 deriving a binary one level for a time interval slightly less than the length, t_1, of the master or first pulse of each frame; in the exemplary embodiment, discriminator 205 derives a binary one signal on lead 207 in response to decoder 203 generating a binary one level for in excess of 30 milliseconds. The wavetrains derived on leads 206 and 207 are respectively illustrated in FIGS. 3*b* and 3*c*. Discriminator 205 feeds binary one signals to leads 206 and 207 for a predetermined time interval after the

minimum elapsed detection times of 12 and 30 milliseconds. The lengths and occurrence times of the pulses derived on leads **206** and **207** are such that the trailing edges of pulses on lead **206** occur after the trailing edge of the longest data pulse transmitted from a peripheral station and the trailing edges of pulses on lead **207** occur after the trailing edge of the pulses on lead **206**.

The output signals of pulse width discriminator **205** on leads **206** and **207** are combined in logic network **208** to enable the master pulse within each frame to be detected. Logic network **208**, the details of which are described infra, derives a binary one level on load output **209** thereof in response to a master pulse being detected simultaneously with a load enable signal being supplied to logic network **208** on lead **211**. As described infra, the signal derived on lead **211** is generated by shift register **212**, which is responsive to the load indicating signal on lead **209**, as well as shift and reset signals, respectively, derived by logic network **208** on leads **213** and **214**.

Logic network **208** responds to binary one levels on data lead **204** to derive shift pulses on lead **213**, as indicated by the waveform of FIG. *3d*. The trailing edge of each shift pulse, regardless of the channel number within a particular frame, always occurs a predetermined time interval after the leading edge of the data pulses derived on lead **204**, as indicated by FIG. *3a*. The shift pulses for the second through fifth channels of each frame have leading edges displaced by the same time interval from the leading edges of the corresponding channel pulses derived on data line **204**, as indicated in FIG. *3a*. It is also to be noted that each of the shift pulses for the second through fifth channels of each frame has substantially the same duration. The time displacement and duration of the shift pulses for the second through fifth frames are identical because the apparatus in logic network **208** for deriving them is the same. The shift pulse, however, for the first channel of each frame is displaced from the leading edge of the data pulse for the first frame by a greater interval than the separation between the leading edges of the data and shift pulses for the second through fifth frames. This is to enable certain operations relating to detection of a master pulse to occur in logic network **208**, as well as to enable other operations in other circuit elements of the central station to be performed prior to the derivation of the fist shift pulse of each frame. In the event of a long, greater than 38 milliseconds; noise pulse being received, logic circuit **208** includes means for preventing derivation of a shift pulse.

The reset pulse derived on lead **214** by logic network **208** is derived in response to a master pulse not occuring within a predetermined time interval, slightly more than the maximum 1-second duration of a frame. In response to such a condition, it can be assumed that data transmission between a peripheral station and the central station has terminated, necessitating activating the decoding equipment of the central station to an initial state. A reset pulse is also derived in response to other conditions associated with a lack of synchronization between received data and the operation of the central station, as described infra.

Shift register **212** includes five cascaded binary or flip-flop elements which are activated to a binary one state in sequence and synchronously with the trailing edges of the data shift pulses on lead **204**, FIG. *3d*. The trailing edges of the shift pulses activate the cascaded five stages of shift register **212** so that only one stage is activated at a time for a duration between trailing edges of adjacent shift pulses. The separate and sequential activation of the five cascaded stages of shift register **212** for stages **1**, **2** and **5**, which correspond with channels **1**, **2** and **5**, respectively, is illustrated by the rectangular waveforms of FIGS. *3e*, *3f* and *3g*. The waveforms of FIGS. *3e*, *3f* and *3g* represent binary levels derived by the first, second and fifth stages of the five cascaded stage shift register; the output signals of the first through fifth stages of the cascaded shift register are derived on leads **221–225**, respectively.

If none of the stages of the cascaded shift register is in a binary one state or with the fifth stage of the register activated to a binary one state, as indicated by the time interval T_5 (FIG. *3g*), a load enable signal is derived on lead **211**. From an inspection of FIGS. *3d* and *3g*, the load enable signal has a binary one level in time coincidence with at least a portion of the binary one level derived on shift lead **213** in response to reception of the master pulse for the next succeeding frame. Thereby, the first stage of the five cascaded stages is loaded with a binary one signal in synchronism with a shift pulse being applied to the shift register via shift lead **213** and the first stage of the shift register is activated to a binary one state.

Shift register **212**, in addition to being provided with five cascaded stages, includes an additional stage which is partially decoupled from the five cascaded stages. The additional stage is responsive to the signals on leads **209**, **213**, and **214** in such a manner that it is activated to a first state upon the completion of the first channel of one frame and remains in that state until the first channel of the next succeeding frame has been completed. The additional stage is then activated for one frame into a second state for a corresponding time interval of the next succeeding frame. The resulting, complementary output signals of the additional stage of shift register **212** are fed to the shift register output leads **226** and **227**, respectively.

To monitor the time interval each of the stages of the five cascaded stage register in shift register **212** is activated to a binary one state, and an array of counters and storage elements is provided in network **231**. Network **231** includes six different decade counters driven at different time intervals in response to pulses derived from **42** Hertz synchronized clock **232**. Clock **232** is synchronized by the trailing edge of each shift pulse derived on lead **213** so that it derives a clock pulse in time coincidence with the trailing edge of each shift pulse. Thereby, during each channel of a frame, clock source **232** is resynchronized so that the number of pulses derived during the length of each channel is a measure of the channel duration.

The six counters within network **231** respond to the clock pulses of source **232** at different time periods controlled by the rectangular wave voltages on leads **221–227**. Two of the counters within network **231** are responsive to binary one levels on leads **221**, **226**, and **227**, while the remaining four counters are separately responsive to the binary one levels on leads **222–225**. In response to the signals on leads **222–225**, each of the

four remaining counters is activated once during each frame for time intervals coextensive with the duration of each channel. Thereby, upon completion of each data frame, each of the four remaining counters stores a decimal number signal indicative of the identification code number of the four significant decades of each peripheral station.

The first and second counters within network **231** are alternately activated during the first channel of successive frames into a state where they are responsive to clock pulses from source **232**. The alternate activation of these two counters within network **231** results from the signals applied to the counters by leads **221**, **226** and **227**. The alternately activated counters store decimal number signals indicative of which sensor station at the peripheral station detects an alarm condition. It is necessary to employ alternately activated counters for different data frames because the last channel of a first frame is followed immediately by the first channel of the next succeeding frame, necessitating alternate readout of the contents of the first and second counters into a storage register during the first channel of alternate frames. The counters employed cannot operate properly if read out while being loaded.

Network **231** is provided with five storage registers, four of which are responsive to the decade counters for channels two through five. The remaining storage register of network **231** is sequentially responsive to the two alternately activated counters. Thereby, one of the counters feeds the remaining storage stage in response to one data frame being coupled into the storage registers and the other counter feeds the register in response to the next succeeding data frame being read out.

To control readout of the counters in network **231** to the registers of the network, logic network **208** includes a data strobe output lead **233** on which is derived a relatively short duration pulse, illustrated in FIG. **3***i*. The data strobe pulse is derived immediately after termination of the trailing edge of the shift pulse for the first channel of each frame. Thereby, data are transferred from the counters to the registers of network **231** during the first channel of each data frame.

Immediately after a data strobe pulse is derived on lead **233**, logic network **208** derives a counter reset pulse on lead **234**, indicated by the waveform of FIG. **3***j*. Each counter reset pulse resets the contents of the four counters in network **231** responsive to the signals on leads **222–225** and one of the two counters responsive to the channel one signal on lead **221**. The channel one counter which is reset is the one which has just been read out and the other counter is at that time activated into a state whereby it is responsive to the clock pulses of source **232**. During the first channel of the next frame the operations of the two channel one counters are reversed.

The five registers of network **231** thereby continuously store signals indicative of the discrete values of the five different channels of each frame. The signals stored in the registers are continuously updated in response to each frame read from the counters in response to the data strobe pulse on lead **233**. Each of the signals stored in the five registers of network **231** is converted into a four-bit binary coded decimal signal that is continuously fed from the registers to a bank of indicator lamps **235** and a printer **236**. Easily read numerical indications of the identification codes of the transmitting peripheral station and the sensor station at the peripheral station detecting an alarm are provided by indicator **235**. Printer **236** responds periodically to the signals in the registers at a relatively high rate on the order of three frames a second to provide a continuous, repetitive hard copy readout of the indications of station identification and sensor station detecting an alarm condition. The repetitive readout by printer **236** provides a high degree of integrity to the system since a system operator can be assured of the identity and cause of an alarm by the repetitive printed data readout. Indicator **235** can also be provided with an audio alarm which is sounded in response to several data frames being coupled thereto.

One additional feature of the present invention concerns the ability to test the frequency of clock pulse source **232**. To this end, test gate generator **237** for deriving a binary one level for a relatively long time period, of for example 1 second, is supplied to counters of network **231** to enable the counters to be responsive to pulses from clock source **232**. While the test generator binary one signal is supplied to the counters, the counters are connected in a cascaded arrangement, whereby a carry signal is derived from a lower order counter and is supplied to a higher order counter. After the 1-second interval has been completed, the count of the several counter stages should have a predetermined value, which is read out by indicator **235**. If indicators **235** do not have an appropriate value, an indication is provided to an operator that there is either a malfunction in the counter network or clock **232** is not operating at its preassigned frequency.

Having described the block diagram of the central station and the basic operations occurring at the central station, consideration will now be given to the circuits included in pulse width discriminator **205**, logic network **208**, shift register **212**, and network **231** by referring to the circuit diagram of FIGS. **5** and **6**. The circuits of FIGS. **5** and **6** include NOR and NAND gates; in certain instances, a single input is applied to one of the NOR gates or plural inputs of one of the NOR gates are responsive to the same signal, in which cases the NOR gates function as inverters. In certain instances, all of the inputs of a NAND gate are responsive to a source source, whereby NAND gates so connected function as inverters. The circuits of FIGS. **5** and **6** also include a multiplicity of integrated circuit J-K flip-flops which include trigger or toggle input terminals, J and K input terminals that function in conjunction with the toggle input terminals, as well as set and reset input terminals that are independent of the toggle input terminal. The J-K flip-flops include binary output terminals, denominated as Q and $\overline{Q}$. The circuits of FIGS. **5** and **6** also include a number of integrated circuit one-shot multivibrators for deriving output signals of predetermined amplitude and width in response to a trigger voltage being applied thereto. Integrated circuit decade counters and registers for deriving four-bit binary coded decimal signals are also provided in the circuits of FIGS. **5** and **6**.

Considering FIG. **5** in detail, binary one and zero levels derived from tone decoder **203**, as illustrated in FIG. **3***a*, are fed by lead **251** to pulse width discrimina-

tor 205 through inverter 252. The output signal of invertor 252 is applied in parallel to timing networks 253 and 254, which are identical to each other except with regard to the value of a resistance capacitance timing circuit included in each, whereby a description of network 253 suffices for both timing networks.

Timing network 253 derives a short duration binary one pulse in response to a binary one of the data wavetrain occurring for greater than a time interval of 12 milliseconds. To this end, timing circuit 253 includes a normally conducting NPN transistor 255, having a base electrode connected to the output of inverter 252. The collector of transistor 255 is connected in shunt with timing capacitor 256 that is connected in series circuit with a d.c. voltage via resistors 257. The voltage across capacitor 256 is monitored by unijunction transistor 258, the low voltage base of which is connected to ground through load resistor 259. In the absence of a binary one in the data wavetrain on lead 251, the collector of transistor 255 substantially short circuits capacitor 256 to ground. In response to a binary one level on lead 251, the base bias of transistors 255 decreases to cut off transistor 255, thereby allowing capacitor 256 to be charged through resistors 257. With transistor 255 in a nonconducting state for a predetermined time interval, of at least 12 milliseconds and capacitor 256 is chanrged through resistors 257 until the threshold voltage of unijunction transistor 258 is reached and the unijunction is fired to discharge capacitor 256 through load resistor 259. The threshold level of unijunction transistor 258 and the magnitude of the time constant of the r.c. circuit comprising capacitor 256 and resistors 257 are such that a relatively short duration pulse is derived across load resistor 259 after a binary one level is derived on data input lead 251 for 12 milliseconds. Timing circuit 254 is similarly arranged, except that the r.c. time constant of resistors 261 and capacitor 262 is adjusted to provide a relatively short duration pulse across load resistor 263 in response to a binary one level being on data input lead 251 for a time period in excess of 30 milliseconds.

The short duration output pulses of timing circuits 253 and 254 are respectively fed to the bases of transistor inverters 264 and 265. Transistors 264 and 265 respond to the short duration pulses applied thereto by timing circuits 253 and 254 to feed triggering voltages into integrated circuit one-shot multivibrators 266 and 267. One-shot multivibrators 266 and 267 are provided with timing capacitor 268 and variable resistor 269 to determine the durations of binary one states derived thereby, as indicated by FIGS. 3*b* and 3*c*. The state of one-shot multivibrator 266 is monitored on complementary output lead 271 thereof, while the state of one-shot 267 is monitored on true and complementary leads 272 and 273.

From FIG. 3*b* it is seen that one-shot multivibrator 266 is activated into a binary one state at a predetermine time interval, 12 milliseconds, after the derivation of each binary one level in the data signal on lead 251, as represented by FIG. 3*a*. An inspection of FIG. 3*c* reveals that the output of one-shot multivibrator 267 on lead 272 is in synchronism with the master or first pulse of each frame and occurs a predetermined time interval, 30 milliseconds, after the leading edge of the master pulse of the frame. The lengths of the pulses of FIGS. 3*b* and 3*c*, which pulses are occasionally denominated as Q_1 and Q_2, respectively, are adjusted such that Q_1 slightly overlaps the widest data pulse and Q_2 slightly overlaps Q_1.

The reset pulse on lead 214, FIG. 4, is derived, inter alia, in response to no master pulse having been received for a time interval in excess of 1 second, the maximum duration of any frame. To this end, the signal on lead 272 is applied to a further timing network 275, which is substantially identical to timing networks 253 and 254, except that the r.c. time constant of resistors 276 and capacitor 277 is slightly in excess of 1 second. Thereby, a pulse is derived across load resistor 278 only in response to the output of one-shot multivibrator 267 on lead 272 having a binary zero level for a time period greater than 1 second. This signifies the failure of a master pulse to occur for slightly more than a 1-second interval and signal termination of data transmission from the peripheral station to the central station. The reset pulse generated across load resistor 278 is utilized in a manner described infra.

To derive shift pulses on lead 213 for each channel of each frame, the output of inverter 252 and the complementary output one-shot multivibrator 266 on lead 271 are combined in NAND gate 281, having an output which is phase reversed by inverter 282. The shift output signal of inverter 282, FIG. 3d, is thereby at a binary one level only in response to one-shot 266 being in a one state while the data input signal, FIG. 3*a*, has a binary zero value. Thereby, the trailing edges of the shift wavetrain, FIG. 3*d*, are in time coincidence with the trailing edges of the changes in the state of one-shot 266, as illustrated in FIG. 3*b*. Since the trailing edges of changes in the state of one shot 266 always occur a predetermined time period after the leading edges of the channel data pulses, FIG. 3*a*, the separations between trailing edges of adjacent shift pulses enable channel duration to be monitored.

One feature of the logic network for deriving the shift pulses is that a shift pulse is not derived if a noise pulse having a length considerably greater than 34 milliseconds is received at the central station. This is because of the phases of the signals applied to NAND gate 281 and the inherent gate characteristics.

Consideration is now given to shift register 212 that includes five cascaded J-K flip-flops 283–287, one being provided for each of the five different channels of each frame. Flip-flops 283–287 are designed to be activated so that flip-flop 283 is in a binary one state while the first channel of each frame is being processed; flip-flop 284 is to be activated into a binary one state while the second channel of each frame is being processed and so forth for flip-flops 285–287 vis-a-vis channels three-five.

To these ends, the shift output signal of inverter 282 is applied in parallel to the toggle input 291 of each of flip-flops 283–287. The Q and $\bar{Q}$ output terminals of the cascaded flip-flops 283–286 are respectively connected to the J and K input terminals of flip-flops 284–287 to establish the cascaded shift register configuration. Output signals are derived from flip-flops 284–287, as indicated by the waveforms of FIGS. 3*e*–3*g* at the Q output terminals of the flip-flops.

To control loading into the first shift register stage, flip-flop 283, the complementary output of one-shot

267, on lead 273, is fed in a complementary manner to the J and K input terminals of flip-flop 283 via serially connected NOR gate 288 and inverter 289, the outputs of which are respectively connected to the J and K input terminals of flip-flop 283. NOR gate 288 is also responsive to the output of NAND gate 292 which signals if none of stages 283–287 is in a one state or if only stage 287 is in a one state since it is responsive to the $\overline{Q}$ outputs of flip-flops 283–287. There is no need and it is undesirable to connect flip-flop 283 to NAND gate 292 because of the time relationship between the inputs thereof during loading. The J and K inputs of flip-flop 283 are thereby respectively provided with binary one and zero input levels in response to monostable 267 being in a one state while a binary zero is derived from gate 292 which signifies that a master pulse is being received while flip-flop 287 is in the one state (proper synchronization) or while none of flip-flops 283–287 is in the one state, as can occasionally occur due to improper synchronization. Flip-flop 283 is loaded with the signals applied to its J and K input terminals only in response to the trailing edge of a shift pulse derived by inverter 282 being fed to its toggle input terminal 291. As indicated by FIGS. 3*d*–3*e*, flip-flop 283 is therefore activated into a binary one state for the interval between the trailing edge of the relatively narrow first shift pulse of each frame and the trailing edge of the second shift pulse of each frame.

While flip-flop 283 is in a binary one state during the interval T_1, FIG. 3*e*, enable voltages are applied by the Q and $\overline{Q}$ outputs thereof to the J and K input terminals of flip-flop 284. Flip-flop 284 is not activated into a binary one state, however, until the occurrence of the trailing edge of the next or second pulse of each frame derived by inverter 282. In this manner, flip-flops 285–287 are energized in sequence for the third through fifth channels of each frame. Activation of shift register stages 283–287 into a binary one state is always a predetermined time after the leading edge of the corresponding pulse for each channel is derived on data input lead 251. Thereby, the time duration each of stages 283–287 as maintained in a binary one state serves is a measure of the five channel times of each frame. It is also to be noted that the identifiable characteristic of the master pulse, its relatively wide width of 34 milliseconds, enables proper synchronization between activation of stages 283–287 and the received data channels.

To control the two counters in network 231, FIG. 4, for the first channel of each frame, shift register 212 is provided with an additional J-K flip-flop 294 that includes a toggle input 295 driven in parallel with toggle inputs 291. Flip-flop 294 is activated so that it stays in a first state for one data frame and is switched to stay in a second state for the next succeeding data frame received at the central station. Activation of flip-flop 294 into its different states is simultaneous with activation of flip-flop 284 into its different states since the J and K input terminals of flip-flop 294 are connected to be driven in parallel by the signal derived at the Q output terminal of flip-flop 283. Thereby, flip-flop 294 functions effectively as a toggle that is activated every other time flip-flop 283 changes state, in response to the trailing edge of the Q output of flip-flop 283.

In the event of an interruption of transmission between the peripheral station and the central station, it is necessary to reset flip-flops 283–287 and 294 so that each has a zero state and flip-flop 283 can be loaded to a binary one state in response to reception of the next master pulse. To derive a reset input for flip-flops 283–287 and 294, the output signal of timing circuit 275 is reversed in phase by inverter 296, the output of which is combined with output signals of NAND gate 292 and the true output of monostable multivibrator 267 on lead 272. The signal on lead 272 and the output signal of NAND gate 292 are combined in NAND gate 297, the output terminal of which is connected to an input of NAND gate 298, having a second input responsive to the output of inverter 296. The output of NAND gate 298 is inverted in phase by inverter 299, which derives an output signal that is applied in parallel to the reset input terminal of each of flip-flops 283–287 and 294. The set input terminals of flip-flops 283–287 and 294 are connected to a d.c. power supply voltage which prevents activation of the flip-flops to the set state. The interconnections between the output signals of multivibrator 267, NAND gate 292 and timing network 275 with logic gates 296–299 are such that a reset pulse is applied by inverter 299 to flip-flops 283–287 and 294 in response to a pulse being derived from timing circuit 275 or monostable 267 being in a binary one state while any one of flip-flops 284–286 is in a binary one state. These conditions can occur in response to cessation of transmission between the peripheral and central station for a period in excess of 1 second, the maximum time duration of a data frame, or if a master pulse is being processed while the shift register has a binary one value in any of stages two, three or four, an indication of lack of synchronization between received data channels and the operation of the central station.

To control synchronization of clock source 232, the trailing edges of shift pulses derived at the output of inverter 282 are fed to the input of oscillator 232 via leads 301. As described infra, the synchronized clock pulses derived by source 232 are fed to counters in network 231.

To derive the end of frame, data strobe and counter reset signals of FIGS. 3*h*, 3*i* and 3*j*, respectively, shift register 212 includes an end of frame logic network 311. End of frame logic network 311, illustrated in FIG. 5, includes J-K flip-flop 312, having J and K input terminals driven by complementary signals. The signal supplied to the J input terminal of flip-flop 312 is derived by NOR gate 313 in response to the complementary output of monostable multivibrator 267 on lead 273 and the complementary, $\overline{Q}$, output of flip-flop 287 for the fifth channel. The output of NOR gate 313 is applied directly to the J input terminal of flip-flop 312 and is applied in inverted form via inverter 314 to the K input terminal of the flip-flop. The toggle input terminal 315 of flip-flop 312 is responsive to the trailing edge of output signals derived by inverter 282. The set and reset input terminals of flip-flop 312 are driven in parallel with the corresponding terminals of flip-flops 283–287. Thereby, the Q output terminal of flip-flop 312 is a rectangular waveform illustrated in FIG. 3*h*. The waveform of FIG. 3*h* has a binary zero level until a frame has been completed, at which time a binary one level is derived in synchronism with the trail-

ing edge of the shift pulse for the first channel of the next succeeding frame.

The Q output terminal of flip-flop **312** is combined with the true output of monostable **267** on lead **272** in NAND gate **316**. The output signal of NAND gate **316** is thereby a relatively short duration pulse having a leading edge in time coincidence with the leading edge of each end of frame pulse, illustrated by FIG. **3***h*. The trailing edge of each data strobe pulse is in time coincidence with the trailing edges of the binary one levels derived on lead **272**, FIG. **3***c*, if these binary one levels are in time coincidence with a portion of the end of frame wavetrain. The counter reset signal is derived by sensing the trailing edge of the data strobe pulse derived at the output terminal of NAND gate **316**. To this end, differentiator **317**, including circuitry for responding only to the trailing edge of the output of NAND gate **316**, is provided. The output waveform of differentiator **317** is illustrated in FIG. **3***j*.

The various output signals of FIG. **5**, derived, inter alia, from the Q output terminals of flip-flops **283–287** and **294**, the $\overline{Q}$ output of flip-flop **294**, the data strobe output of NAND gate **316**, the output signal of differentiator **317**, and the output signal of synchronized clock source **232** are combined in the counter and register circuitry specifically illustrated in FIG. **6** to enable indications of the discrete levels of the values of each channel to be measured and displayed. The network of FIG. **6** includes six integrated circuit decade counters **321**, **321'** and **322–325**. Counters **321** and **321'** are identical, each being provided with a count input, denominated as a, as well as a pair of reset to zero inputs $R_{0(1)}$ and $R_{0(2)}$. Counters **321** and **321'** are reset to zero only in response to binary one signals being simultaneously applied to the two reset inputs. Counters **321** and **321'** also include an external connection between the least significant output bit thereof, A, and an input terminal b_D to establish the binary decimal counting configuration. In addition to the A output terminal, each of the counters is provided with three other binary outputs to enable the 10 different decade states to be defined. Counters **322–325** are essentially identical to counters **321** and **321'**, except that the former counters are reset to a zero state in response to a binary one being fed only to the $R_{0(1)}$ input terminal thereof.

Counters **322–325** are employed to measure the duration of the second through fifth channels of each frame and to this end are activated to be responsive to the output of sync data clock **232** and to voltages developed at the Q output terminals of flip-flops **284–287**. Signals are coupled to the *a* or count input terminals of counters **322–325** in response to binary ones being derived at the Q output terminals of flip-flops **284–287** by combining the flip-flop output signals with the output of data clock **232** in logic networks **332–335**, one of which is provided for each of the counters **322–325**. Since each of the logic gates **332–335** is essentially the same, a description of network **332** suffices for the remaining networks, except for one aspect of network **335**.

Logic network **332** includes NAND gate **336**, having one input responsive to the signal derived at the Q output terminal of flip-flop **284** and a second input responsive to the clock signal derived by synchronized data clock source **232**. The output of NAND gate **336** is fed as one input to NAND gate **337**, the output of which drives the count input of counter **322**, at input terminal *a*. In response to each pulse derived by data clock source **232** while a binary one is being derived at the Q output terminal of flip-flop **284**, a pulse from clock source **232** is supplied to counter **322** and the state of the counter is advanced in response thereto. By selecting the clock rate of source **232** appropriately, the count stored in counter **322** after the termination of a channel corresponds with the discrete decade level of the peripheral station identification code for the most significant decade number of the code. Each of counters **323–325** is similarly activated whereby, upon completion of a data frame, these counters store decimal numbers corresponding with the three lower decades of the peripheral station code identification number.

Logic network **332** includes an additional NAND gate **338** having one input responsive to 1-second test gate generator **237** to enable the frequency of clock source **232** and the proper functioning of the counters to be ascertained. Test gate source **237** activates NAND gate **338** into an enabled condition for a period of 1 second while pulses are being derived by source **232** in a continuous manner unrelated to the occurrence of any master pulse.

While the test operation is being performed, counters **322–325** are cascaded together so that the most significant bit output terminal of one counter is fed to the count input of the next adjacent counter. To this end, a second input terminal of NAND gate **338** is responsive to the most significant bit output of counter **232**, at terminal D. The output terminal of NAND gate **338** is supplied as a second input to NAND gate **337**, whereby counter **322** can be supplied with pulses from terminal D of counter **323** while the 1-second test gate is being derived. Logic network **335** differs from logic network **332** slightly in this regard since NAND gate **339** of network **335** cannot be connected to the most significant bit output terminal of a preceding decade counter. Therefore, the input terminal of NAND gate **339** corresponding with the input terminals of NAND gate **338** is directly responsive to the output of clock source **232**. All pulses from clock source **232** propagate to the *a* input terminal of counter **325** while test gate source **237** is activated. After a count of 10 has been reached in counter **235**, the output signal derived at the D output terminal thereof is propagated to the count input terminal of counter **325**, which will not receive a further input pulse until 10 additional pulses are fed to the *a* input terminal of counter **325**. In the manner described, it is believed evident as to the manner by which counters **322–325** are responsive to the output of clock source **232** while a test gate signal is being generated.

Counters **321** and **321'** measure the duration of the first channel of alternate data frames, whereby counter **321** provides a readout of, for example, the duration of the first channels of frames **1**, **3**, **5**, etc., while counter **321'** provides a readout of the first channel of frames **2**, **4**, **6**, etc. To effect control of first channel counters **321** and **321'** in this manner, the signal at the Q output terminal of flip-flop **283** is combined in a logic network comprising NOR gates **341** and **342** with the output signals at the Q and $\overline{Q}$ output terminals of flip-flop **294**

and clock pulses derived from source 232. Each of NOR gates 341 and 342 is responsive to the voltage developed at the $\overline{Q}$ output terminal of flip-flop 283 and clock pulses derived from source 232. NOR gates 341 and 342 are respectively enabled in response to the voltages developed at the Q and Q output terminals of flip-flop 294. Thereby, in response to flip-flops 283 and 294 both being in a binary one state, clock pulses are fed through NOR gate 341 to counter 321. During the first channel of the next succeeding frame, when flip-flop 283 is in a binary one state and flip-flop 294 is in a binary zero state, pulses from source 232 are fed through NOR gate 342 to the count input terminal of counter 321'.

Upon completion of a data frame and during the first channel of the next succeeding data frame, the count stored in one of first channel counters 321 or 321' (the first channel counter which is at that time not being fed with clock pulses) is read out simultaneously with readout of the counts stored in counters 322–325. During the first channel of the next succeeding data frame, the count of the first channel counter which was not read out during the previous data frame is read out simultaneously with the counts of counters 322–325.

The counts of counters 321, 321' and 322–325 are fed to integrated circuit storage registers 351–355. Each of storage registers 351–355 is essentially the same and includes four binary stages for storing a binary coded decimal indication of the duration of a different one of the channels of the previously processed frame. Each of counters 351–355 also includes a strobe input terminal enabling it to be responsive to signals supplied to the four signal input terminals 1D-4D thereof. Binary stages within registers 351–355 are unresponsive to the signals applied to terminals 1D-4D except while a signal voltage is applied to the strobe input terminal thereof. The strobe input terminals of counters 352–355 are driven in parallel by the data strobe output of NAND gate 316, FIG. 5, having a waveform illustrated by FIG. 3*i*. The waveform of FIG. 3*i* is fed to the input terminals of register 352–355 via inverting NAND gate 356 and driver NAND gate 357, having a second input terminal maintained at a positive, enabling voltage.

Feeding of data into the input terminals 1D-4D of register 351 requires more complex circuitry than the direct connection between the A-D output terminals of counters 322–325 and the 1D-4D input terminals of registers 352–355 because register 351 is alternately responsive to the output signals of counters 321 and 321'. To effect selective and sequential coupling between the output terminals of counters 321 and 321' and the input terminals of register 351, logic network 361 is provided. Logic network 361 includes eight AND gates 362–369 and four OR gates 371–374. Corresponding output terminals of counters 321 and 321' are fed to adjacently numbered ones of AND gates 362–369, whereby gates 362 and 363 are respectively responsive to signals developed at the A output terminals of counters 321 and 321', AND gates 364 and 365 are respectively responsive to signals developed at the B output terminals of counters 321 and 325, etc., for AND gates 366–369. Even numbered ones of gates 362–369 are responsive to the voltage developed at the Q output terminal of flip-flop 294, while the odd numbered ones of gates 362–369 are responsive to the voltage developed at the $\overline{Q}$ output terminal of flip-flop 294. Thereby, in response to flip-flop 294 being in a binary one state, AND gates 362–368 are enabled to feed the output voltages at terminals A-D of counter 321 to OR gates 371–374. In a similar manner, gates 363, 365, 367 and 269 are enabled in response to flip-flop 294 being in a binary zero state to pass signals derived at output terminals A-D of counter 321' through OR gates 371–374. Output terminals of OR gates 371–374 are respectively connected to the 1D-4D input terminals of register 351. Due to the connection of NAND gate 356 through NAND gate 375 to the strobe input terminal of register 251, OR gates 371–374 feed bits into register 351 in response to the derivation of a data strobe pulse, FIG. 3*i*. After signals have been transferred from counters 322–325 to registers 352–355 and from a selected one of counters 321 or 321' to register 351, a counter reset pulse, FIG. 3*j*, is derived at the output of differentiator 317, FIG. 5. The counter reset pulse is applied in parallel to the reset input terminals, $R_{0(1)}$, of counters 322–325 to reset these four counters to a binary zero state. Simultaneously with the application of the counter reset pulse to counters 322–325, the $R_{0(2)}$ input terminals of counters 321 and 321' are supplied with the counter reset pulse. Only one of first channel counters 321 or 321' is reset at a time in response to the counter reset pulse. The first channel which is reset is the one whose count was fed into register 351 in response to the immediately preceding data strobe pulse. To this end, the $R_{0(1)}$ input terminals of counters 321 and 321' are respectively responsive to the voltages developed at the Q and $\overline{Q}$ output terminals of flip-flop 294. From the foregoing, it is evident that the contents of counters 321 and 321' are reset during the first channel of alternate frames of data received at the central station.

While there has been described and illustrated one specific embodiment of the invention, it will be clear that variations in the details of the embodiment specifically illustrated and described may be made without departing from the true spirit and scope of the invention as defined in the appended claims. For example, the code identification resistors 151, instead of being connected in parallel, can be connected in a series chain of tapped resistors which are selectively short circuited together, whereby the same basic code identification circuit can be employed at each peripheral station. Also, in some systems where it is necessary to detect only one alarm condition, or to detect the presence of a number of alarm conditions without specifying the nature of the alarm, it may be desirable to transmit a data frame containing only peripheral station identification code channels, to the exclusion of the type of alarm sensed.

I claim:

1. A system for transmitting to a central station an indication of the existence, at any one of a plurality of peripheral stations, of any one of several possible alarm conditions, comprising, in combination, means for deriving a signal in response to the occurrence of any one of said conditions, frame generating means responsive to said signal for generating a predetermined plurality of repetitive sequential substantially identical data frames, said frame generating means including

data channel producing means for producing a plurality of repetitive data channels each enduring for a discrete multiple of a predetermined unit time elapse, said data channels being respectively indicative of the identity of said peripheral station and the condition at said peripheral station; said frame generating means including means for providing a distinguishable timing signal characteristic of the first channel of each frame to distinguish same from other channels of each frame, and means for transmitting said predetermined plurality of data frames to said central station, wherein is provided means to assure that the last of said plurality of frames terminates in said distinguishable timing signal characteristic and the first of each of said channels commences with said distinguishable timing signal characteristic.

2. A system according to claim 1, wherein said each of said peripheral stations includes a normally disabled radio wave transmitter, control means responsive only to the initiation of one of said conditions for conditioning said transmitter to transmit a radio wave for only a predetermined time interval, and modulating means for modulating said radio wave according to the time durations of said channels and the identifiable timing signal characteristics of said channel of each of said repetitive data frames and means for terminating said predetermined time interval only co-incidentally with termination of one of said frames.

3. A peripheral station according to claim 2, wherein said control means includes means for periodically enabling said transmitter to an on condition for groups of said frames separated respectively by blank intervals of about twice the duration of any of said groups, and means responsive to said frame generating means to enable said transmitter at the beginning of each of said frames in response to said identifiable signal characteristic of said one channel of a first frame and to disable said transmitter after the end of one of said frames in response to the occurrence of said identifiable signal characteristic of an immediately following frame, whereby only complete frames of data are transmitted during each of said on conditions.

4. A peripheral station according to claim 1, wherein said several conditions are alarm conditions, wherein said means for deriving a signal in response to the occurrence of an alarm condition is responsive to any one of several alarm condition detectors at the peripheral station, wherein one of said channels has a time duration identifying the alarm condition occurring at the peripheral station, and wherein the time durations of the remaining channels of each frame are digitally indicative of the identification of the transmitting peripheral station.

5. A peripheral station according to claim 4, wherein said frame generating means generates a plurality of time spaced pulses during each frame, corresponding portions of adjacent ones of said pulses defining a data channel, the time duration of a first channel of each frame being indicative of the alarm condition occurring at the peripheral station, and said means for providing an identifiable signal characteristic to one of said channels provides said signal characteristic to the first channel and includes code generator means responsive to the output of an alarm condition detector sensing an alarm condition, said several alarm condition detectors each including time constant circuit means connectable to said code generating means in response to the occurrence of an alarm condition to condition said code generating means to produce pulses defining a channel of a duration indicative of the sensed alarm condition.

6. A peripheral station according to claim 5, wherein said channel generating means further includes number generator means for generating pulses defining channels of durations indicative of a plural number numerical identification of the peripheral station.

7. A radio alarm system, comprising geographically separated transmitter means for transmitting groups of information bearing frames separated by inactive periods each enduring about twice as long as one of said groups of information bearing frames, wherein said frames deriving from separate ones of said geographically separated transmitters are of random relative lengths, means for initiating transmissions of said information groups from separate ones of said transmitters at random times, and means for limiting the time of a transmission from any one of said transmitters to only but not less than several minutes, wherein is provided means for terminating said transmissions only in response to completion of one of said frames.

8. In an alarm transmitter, means for transmitting a group of successive information bearing frames, said means including means responsive to occurrence of a random event for generating a pulse of first duration for all said frames, means responsive to completion of said pulse for generating a time quantized signal representing by its duration the character of said random event, means responsive to completion of said signal for generating a sequential plurality of further time quantized signals having together a multi-digit significance, and means terminating each of said frames with one of said pulses of first duration constituting the initial pulse of a succeeding frame for all except the last frame of said group.

9. In an alarm system, a satellite radio station including a plurality of condition detector circuits, means responsive to detector circuits for initiating transmission of a pattern of information bearing pulse position modulated frames from said satellite radio station, the first pulse ofeach of said frames having a characteristic distinguishing said first pulse from all other pulses of said frames, means responsive to the one of said condition detector circuits which detects an alarm condition for generating a second pulse separated from said first pulse by a time interval equal to a multiple of a basic time interval, said multiple identifying said one of said condition detector circuits, means responsive to said second pulse for generating further pulses each separated from the pulse preceding itself by a time interval which is digitally decimally coded in terms of said basic time interval, the last of said further pulses being said first pulse of a succeeding frame and having said characteristic and the coding of said decimally coded pulses identifying said satellite radio station in terms of a multi-digit number.

10. The combination according to claim 9, wherein is provided means for transmitting said frames in a period of several minutes only, said period consisting of groups of said frames separated by silent intervals unoccupied by said frames on at least a 20 percent duty cycle basis, and means for terminating said period only in response to termination of one of said frames.

11. The combination according to claim 9, wherein is further included a central station having means responsive to said frames to record in response to each of said frames a record of the identity of said satellite station and the identity of said adverse condition, and means for disabling said means to record in response to reception of an abnormal format of one of said frames.

12. In a satellite alarm system, plural satellite stations each including an associated normally unenergized radio transmitter, an alarm condition sensing system at each station, means responsive to sensing of an alarm by said alarm condition sensing system for energizing the associated transmitter for a predetermined time interval of the order of several minutes, said transmitter including means for transmitting information bearing time position modulated plural pulse frames during said time interval, each of said frames including a master pulse of the same duration, and means for terminating said time interval only in coincidence with occurrence of one of said master pulses, said master pulses each defining concurrently the beginning of one frame and the termination of a preceding frame, said frames including plural pulses separated by information bearing digitally coded spaces which are diverse for different ones of said satellite stations and serve as identification of said satellite stations.

13. The combination according to claim 12, wherein said means for energizing includes means for alternately energizing and then de-energizing said transmitter periodically for groups of plural successive integral frames during said predetermined time interval with an on the order of a 33 percent duty cycle, and means for initiating and terminating each of said groups of plural frames during which said transmitter is energized only in coincidence with master pulses.

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