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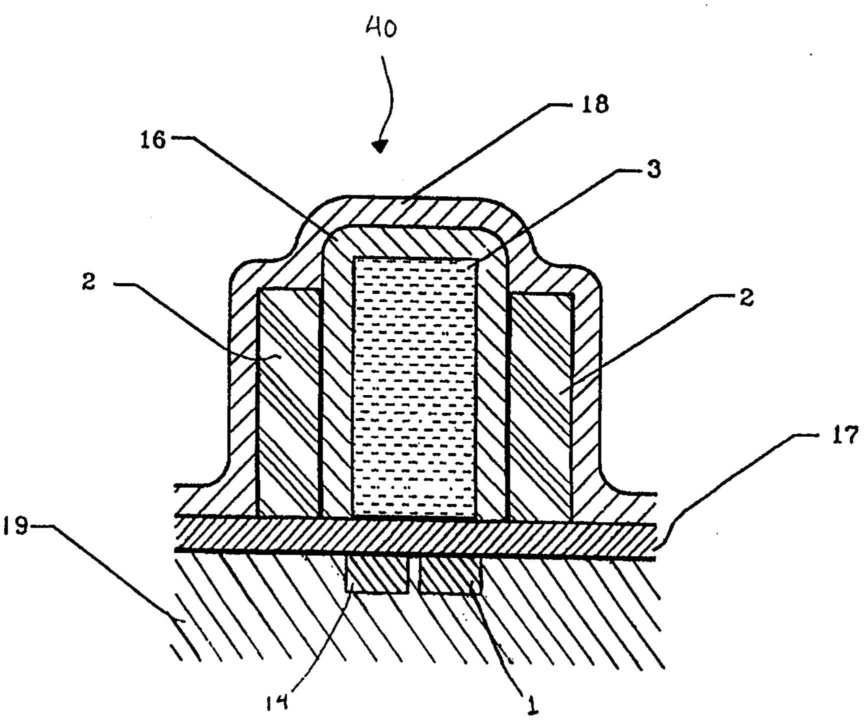
(54) Title: DUAL CONDUCTOR INDUCTIVE SENSOR FOR A NON–VOLATILE RANDOM ACCESS FERROMAGNETIC MEMORY

(57) Abstract

A non–volatile ferromagnetic RAM device which is capable of reading the data stored in each magnet quickly and efficiently utilizing a minimal number of components. Specifically there is a non–volatile ferromagnetic RAM which is capable of reading the data stored in each magnetic bit. The ferromagnetic memory cell is comprised of a base (19) that is oriented in a horizontal plane. There is also a bit (3), made of a ferromagnetic material, having: a height that is oriented perpendicular to the horizontal plane of the base, and a polarity that can be directed along the height. Additionally, there is a sense line (1), positioned proximate the bit (3) sufficient to detect the directed polarity of the bit; and a write line (2), positioned proximate the bit sufficient to direct the polarity of the bit. Additionally, there is a detector, coupled to the sense line; and a sample drive line (14), positioned proximate the bit (3) to transmit an electric pulse that will increase the directed polarity of the bit sufficient to induce a wave into the sense line that can be detected by the detector.



DUAL CONDUCTOR INDUCTIVE SENSOR FOR A NON-VOLATILE RANDOM ACCESS FERROMAGNETIC MEMORY

Related Applications

This application claims priority to U.S. Provisional Application No. 60,122,822 filed March 4, 1999.

The Field of the Invention

The present invention relates to non-volatile random access memory. More particularly, the present invention relates to a dual conductor inductive sensor for a non-volatile random access ferromagnetic memory device.

Background of the Invention

Computer memory technology has experienced profound advances in the last two decades. One of the first computer memories involved magnetic core memory technology. To form each magnetic core, a miniature toroidal-shaped ferrite core was interwoven into a fine matrix of wires. By applying a current through the wires, the core would be programmed with either a north or south directed flux path that would correspond to a logic one or zero. The advantage of magnetic core memory is that it is non-volatile, or does not need to be refreshed to remember the stored logic signal. Additionally, Core memory is also "radiation-hard" or unaffected by ionizing radiation like gamma rays. However, the assembly of the magnetic core array was very labor intensive and was quickly abandoned when semiconductor processes were developed.

Currently one of the most popular memory technologies uses either a form of MOS (metal-oxide-semiconductor) or CMOS (complementary metal-oxide-semiconductor) processes. However, it is well known that this technology requires constant refreshing of each memory cell to maintain the logic signal strength due to the inherent leakage of capacitors. This constant refreshing of the memory cells is not a problem when there is an unlimited voltage source, but in many applications, like lap top computers and cell phones, there is a finite supply. To deal with this problem, rechargeable batteries have been used in all portable electrical devices.

The problem with using devices that have capacitive memory arrays is the inconvenience in keeping the batteries properly charged every few hours. Therefore, there is a need for a non-volatile memory device that does not need to be refreshed and is inexpensive and quick to make.

Examples of patents related to non-volatile RAM, each of which are herein incorporated by reference for their supporting teachings, are as follows:

U.S. 4,360,899 to Dimyan et al. teaches a non-volatile random access memory having a plurality of magnetic cells arranged in an array on a major surface of a substrate. In operation, a single magnetic cell is selected and inductively switched between opposite remanent, (i.e. permanent) states, upon the simultaneous application of electrical pulses to a pair of conductors intersecting adjacent the selected cell. Each electrical pulse has an amplitude which is insufficient to inductively switch the remanent state of the selected cell. However, the combined amplitude of the electrical pulses is at least equal to the amplitude required for such a switch.

U.S. 5,068,826 to Mathews teaches a non-volatile, static magnetic memory device, whose operation is based on the Hall effect. The device includes a magnetic patch which stores data in the form of a magnetic field, a semiconductor Hall bar, and a pair of integrally-formed bipolar transistors which are used for amplifying and buffering the Hall voltage produced along the Hall bar. In use, current is forced to flow down the length of the Hall bar causing a Hall voltage to be developed in a direction transverse to the direction of both the magnetic field and the current. The bases of the bipolar transistors are ohmically coupled to the Hall bar to sense the Hall voltage - the polarity of which is representative of the stored information. Finally, a system of current carrying conductors is employed for writing data to individual magnetic patches.

U.S. 5,295,097 to Lienau teaches a nonvolatile random access memory having a substrate that carries separate magnetically polarizable domains. Each domain is surrounded by a full write loop member, and arranged to penetrate a Hall channel of a dual drain FET with its residual magnetic field. The domains are organized in word rows and bit columns, are each written to by a single full write current through the surrounding loop member, and each read by a comparator connected to the FET drains. The memory is capable of being fabricated in a variety of different forms.

U.S. 4,791,604 to Lienau et al. teaches a sheet random access memory (SHRAM). The SHRAM is a nonvolatile and transportable memory characterized by its cell density and relatively small size and power requirements, but having the nonvolatile character and rugged transportability of core memory, or magnetic disks or tape. The SHRAM is further characterized by a memory comprising a two dimensional magnetic substrate and a fixed driving device for writing and reading into the substrate. Further, a fixed sensing device for sensing the information is attached at each cell location. The memory media includes not only a homogeneous two dimensional substrate, but also ferrite cores formed into the substrate by photolithographic techniques, wherein the information is stored within the core and read by the sensing device from a gap defined by the core. Memory cells according to the invention can thus be arranged and organized to form destructive readout RAMs, or nondestructive readout Rams in both serial and parallel form.

U.S. 5,926,414 to McDowell et al. teaches a magnetic integrated circuit structure in combination with a carrier-deflection-type magnetic field sensor. Each of a variety of magnet structures realize a condition in which the magnetic field is substantially orthogonal to the direction of travel of carriers of a sense current, thereby achieving maximum sensitivity. By basing a magnetic memory cell on a single minium size MOS device, a small cell may be realized that compares favorably with a conventional DRAM of FLASH memory cell. The greater degree of control over the magnetic field afforded by the magnetic structures enables the cross-coupling between cells in a memory array to be minimized.

Summary of the Invention

It is therefore a feature of the present invention to provide a nonvolatile ferromagnetic RAM device which is capable of reading the data stored in each magnet quickly and efficiently utilizing a minimal number of components.

Specifically, there is a nonvolatile ferromagnetic RAM which is capable of reading the data stored in each magnetic bit.

A further aspect of the invention is to provide a ferromagnetic memory cell, comprising of a base (19) that is oriented in a horizontal plane. There is also a bit (3), made of a ferromagnetic material, having: a height that is oriented perpendicular to the horizontal plane of the base, and a polarity that can be directed along the height. Additionally, there is a sense line (1), positioned proximate the bit (3) sufficient to detect the directed polarity of the bit; and a write line (2), positioned proximate the bit sufficient to direct the polarity of the bit.

Yet, an additional feature of the invention is to provide a memory cell with a detector, coupled to the sense line; and a sample drive line (14), positioned proximate the bit (3) to transmit an electric pulse that will increase the directed polarity of the bit sufficient to induce a wave into the sense line that can be detected by the detector.

There has thus been outlined, rather broadly, the more important features of the invention so that the detailed description thereof that follows may be better understood, and so that the present contribution to the art may be better appreciated. Other features of the present invention will become clearer from the following detailed description of the invention, taken with the accompanying drawings and claims, or may be learned by the practice of the invention.

Brief Description of the Drawings

FIG. 1 is a schematic diagram of the nonvolatile random access ferromagnetic memory of the present invention.

FIG. 2 is a side sectional view of the memory cell elements presented in Fig. 1

FIG. 3 is a timing diagram of the memory cell elements of Fig. 1 for reading a single positive bit of data stored in a memory cell.

It is noted that the drawings of the invention are not so scale. The drawings are merely schematic representations, not intended to portray specific parameters of the invention. The drawings are intended to depict only selected embodiments of the invention, and therefore should not be considered to be limiting the scope of the invention. The invention will be described with additional specificity and detail through the use of the accompanying drawings. Like numbering between figures represent like elements.

Detailed Description of the Invention

The applicant has discovered that the reading of binary data stored within a ferromagnetic bit may be accomplished easily and efficiently using a dual conductor inductive sensor in intimate communication therewith. Such a device requires no moving parts or refreshing of stored logic signals, and is capable of sensing magnetically stored data at the micron and submicron levels. Referring now to Fig. 1, there is shown an electrical schematic diagram of the inventive nonvolatile random access ferromagnetic memory circuitry 100. In particular, there are ferromagnetic bits 3, each surrounded by a "set" or "write" coil 2. Isolation gates (FETs or field effect transistors) 12 are electrically coupled to bit drive lines 10 that are coupled to bit write drivers 9. Master sense driver 7 is electrically coupled through master sense drive line 6, to bit read isolation gates (or operational amplifiers) 5, that are coupled to conductor sense lines 1, which are coupled to bit sense amplifiers 11. Read drivers 13 are each coupled to read drive lines 14, which are each coupled to ground 30. Byte drivers 8 are coupled to byte drive lines 4, which are coupled to write coils 2. Cross selection between byte drive lines 4, and bit drive lines 10, are prevented by gates 12.

Referring to Fig. 2, there is illustrated a side cross sectional view of the micron, or sub-micron memory cell elements of Fig. 1. In particular, memory cell 40 has substrate 19 imbedded with sense line 1 and read bias pulse drive line, or sample drive line 14 placed side-by-side therein. In this embodiment, these lines are illustrated as being placed at the bottom of the magnet, however, they could both be placed at the top of the magnet, or with one on the top and one on the bottom and still achieve the same results. Sense line 1 and bias pulse drive line 14, may be made of any suitable conductive material known to those skilled in the art such as Al, Cu, etc. Insulation layer 17 is placed over sense line 1 and bias pulse drive line 14, which may be of any suitable insulative material known to those skilled in the art such as SiO_2, Si_3N_4. A ferromagnetic memory bit 3 is surrounded by a layer of insulation 16. Write coil 2 surrounds insulation layer 16 proximate to the memory bit. Write coil 2 may be of the same conductive materials as sense line 1 and bias pulse line drive 14. Insulation layer 16 may be of the same insulative materials as insulation layer 17. A final covering insulation layer 18 is placed over all exposed surfaces of memory cell 40 which also may be of the same insulative materials as insulation layer 16. The entire memory cell 40 is disposed upon substrate 19 which can be made of any suitable substrate material known to those skilled in the art such as silicon, glass, and GaAs. Further, substrate19 and memory cell 40 may be fabricated by any method known to those skilled in the relevant art, such as electroplating, sputtering, E-beam deposition, chemical vapor deposition, and molecular beam epitaxy.

Referring now to Fig. 3, there is illustrated a timing diagram of the memory cell elements of Fig. 1 for reading a single positive bit of data stored in an individual memory cell. Such a positive bit would represent a digital "1" with its positive "H" magnetic field. During the reading of the magnetic bit, sense sample pulse 21 is generated on bias pulse read drive line 14, and results in a field which induces a pulse into sense line 1 of Fig. 1. Additionally, pulse 21 will interact with the static, or remnant magnetic field emanating from ferromagnetic bit 3. The resultant interaction between these two fields is sense wave 23, which is produced on the sense conductor (i.e., sense line 1) depicted on lines 22 and 24, depending upon the logic signal previously stored. Specifically, as depicted on line 22, the sense wave 23 is positive as a result of the positive magnetic field. Conversely, line 24 shows the negative going sense-wave 23 that will result from a negative magnetic field.

In each case, sense strobe 26 on timing line 25 gates the frontal portion of the sense wave, which will in turn be felt at the output of bit sense amplifiers 11, as pulses 28 or 29 on timing line 27. Thus the magnetic polarity, or digital value of each ferromagnetic bit, can be determined.

Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present invention and the appended claims are intended to cover such modifications and arrangements. Thus, while the present invention has been described above with particularity and detail in connection with what is presently deemed to be the most practical and preferred embodiments of the invention, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function, manner of operation, assembly, and use may be made without departing from the principles and concepts set forth herein.

Claims

What is claimed is:

1. A ferromagnetic memory cell, comprising:

a) a base (19), oriented in a horizontal plane;

b) a bit (3), made of a ferromagnetic material, having:

1) a height that is oriented perpendicular to the horizontal plane of the base, and

2) a polarity that can be directed along the height;

c) a sense line (1), positioned proximate the bit (3) sufficient to detect the directed polarity of the bit; and

d) a write line (2), positioned proximate the bit sufficient to direct the polarity of the bit.

2. The memory cell of claim 1, further comprising:

a) a detector, coupled to the sense line; and

b) a sample drive line (14), positioned proximate the bit (3) to transmit an electric pulse that will increase the directed polarity of the bit sufficient to induce a wave into the sense line that can be detected by the detector.

3. The memory cell of Claim 2, wherein the wave induced into the sense line is a positive wave and represents a binary "1."

4. The memory cell of Claim 2, wherein the wave induced into the sense line is a negative wave and represents a binary "0."

5. The memory cell of Claim 1, wherein said write line circumscribes proximate a periphery of the bit.

6. The memory cell of Claim 2, wherein the sense line and the sample drive line are disposed in a substrate and located below the bit.

7. The memory cell of Claim 6, wherein the sense line and the sample drive line are positioned to extend approximate a central portion of the bit.

8. The memory cell of claim 2, wherein the sense line and the sample drive line are on opposite ends of the bit.

9. The memory cell of claim 8, wherein the sense line is coupled to an output sense amplifier (11).

10. The memory cell of claim 9, wherein the sample drive line is coupled to ground after passing proximate the bit.

11. A method of storing and retrieving binary data, comprising the steps of:

a) providing a memory bit, made of ferromagnetic material, having a polarity capable of being directed;

b) directing the polarity of the bit by sending a current along a write line, which is in magnetic communication with the bit, in a certain direction;

c) detecting the polarity of the bit by sending a current along a sense line, such that information about the detected polarity is transferred through the sense line to a detector coupled thereto.

12. The method of claim 11, wherein the detecting step further comprises the steps of:

a) providing a sample drive line in magnetic communication with the bit; and

b) initiating an electric pulse through said sample drive line, concurrent with the current sent along the sense line, such that the electric pulse combines with the directed polarity of the ferromagnetic bit to produce a field sufficient to cause a detectable signal in the sense line.

13. The method of claim 12, wherein the wave induced into the sense line is a positive wave and represents a binary "1."

14. The method of claim 13, wherein the wave induced into the sense line is a negative wave and represents a binary "0."

15. The method of claim 11, wherein said write line surrounds said ferromagnetic bit.

16. The method of claim 12, wherein said sense line and said sample drive line are disposed in a substrate on top of which the ferromagnetic bit rests.

17. The method of claim 16, wherein said sense line and said sample drive line are positioned centrally to the ferromagnetic bit.

AMENDED CLAIMS

[received by the International Bureau on 14 August 2000 (14.08.00) ; original claims 1-17 replaced by new claims 1-16 (3 pages)]

What is claimed is:

1. A ferromagnetic memory cell, having: a base (19), oriented in a horizontal plane; a bit (3), made of a ferromagnetic material, having: 1) a height that is oriented perpendicular to the horizontal plane, and 2) a polarity that can be directed along the height; a write line (2), positioned proximate the bit sufficient to direct the polarity of the bit; wherein the improvement comprises:

a) a sense line (1), positioned proximate the bit (3) sufficient to detect the directed polarity of the bit; and

b) a detector, coupled to the sense line; and

c) a sample drive line (14), positioned proximate the bit (3) to transmit an electric pulse that will increase the directed polarity of the bit sufficient to induce a wave into the sense line that can be detected by the detector.

2. The memory cell of claim 1, wherein the wave induced into the sense line is a positive wave and represents a binary "1."

3. The memory cell of claim 1, wherein the wave induced into the sense line is a negative wave and represents a binary "0."

4. The memory cell of claims 1 - 3, wherein said write line circumscribes proximate a periphery of the bit.

5. The memory cell of claims 1 - 4, wherein the sense line and the sample drive line are disposed in a substrate and located below the bit.

6. The memory cell of claims 1 - 5, wherein the sense line and the sample drive line are positioned to extend approximate a central portion of the bit.

7. The memory cell of claims 1 - 6, wherein the sense line and the sample drive line are on opposite ends of the bit.

8. The memory cell of claims 1 - 7, wherein the sense line is coupled to an output sense amplifier (11).

9. The memory cell of claims 1 - 8, wherein the sample drive line is coupled to ground after passing proximate the bit.

10. A method of storing and retrieving binary data, comprising the steps of:

a) providing a memory bit, made of ferromagnetic material, having a polarity capable of being directed;

b) directing the polarity of the bit by sending a current along a write line, which is in magnetic communication with the bit, in a certain direction;

c) detecting the polarity of the bit by sending a current along a sense line, such that information about the detected polarity is transferred through the sense line to a detector coupled thereto.

11. The method of claim 10, wherein the detecting step further comprises the steps of:

a) providing a sample drive line in magnetic communication with the bit; and

b) initiating an electric pulse through said sample drive line, concurrent with the current sent along the sense line, such that the electric pulse combines with the directed polarity of the ferromagnetic bit to produce a field sufficient to cause a detectable signal in the sense line.

12. The method of claims 10 - 11, wherein the wave induced into the sense line is a positive wave and represents a binary "1."

13. The method of claims 10 - 11, wherein the wave induced into the sense line is a negative wave and represents a binary "0."

14. The method of claims 10 - 13, wherein said write line surrounds said ferromagnetic bit.

15. The method of claims 10 - 14, wherein said sense line and said sample drive line are disposed in a substrate on top of which the ferromagnetic bit rests.

16. The method of claims 10 - 15, wherein said sense line and said sample drive line are positioned centrally to the ferromagnetic bit.

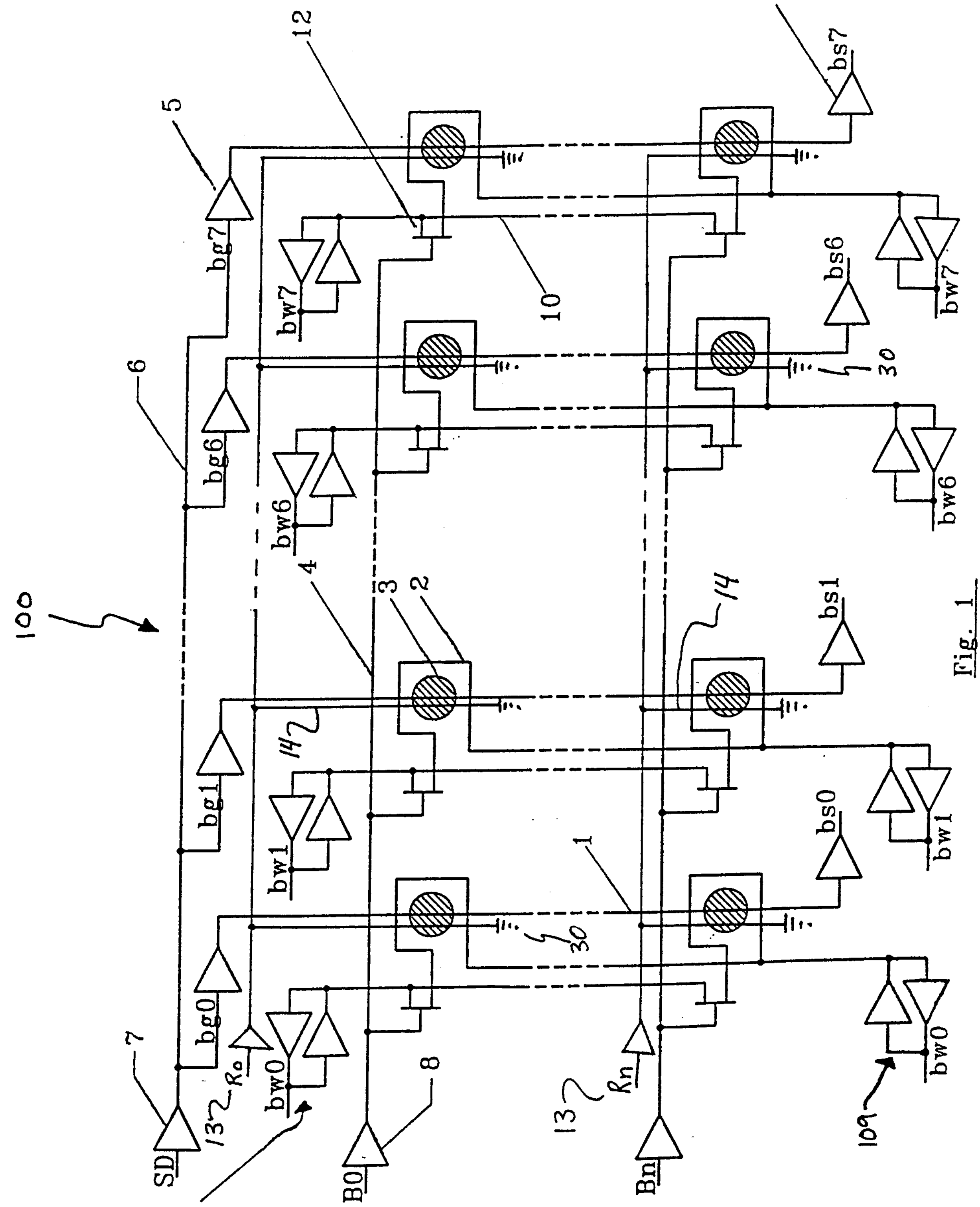

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Fig. 1

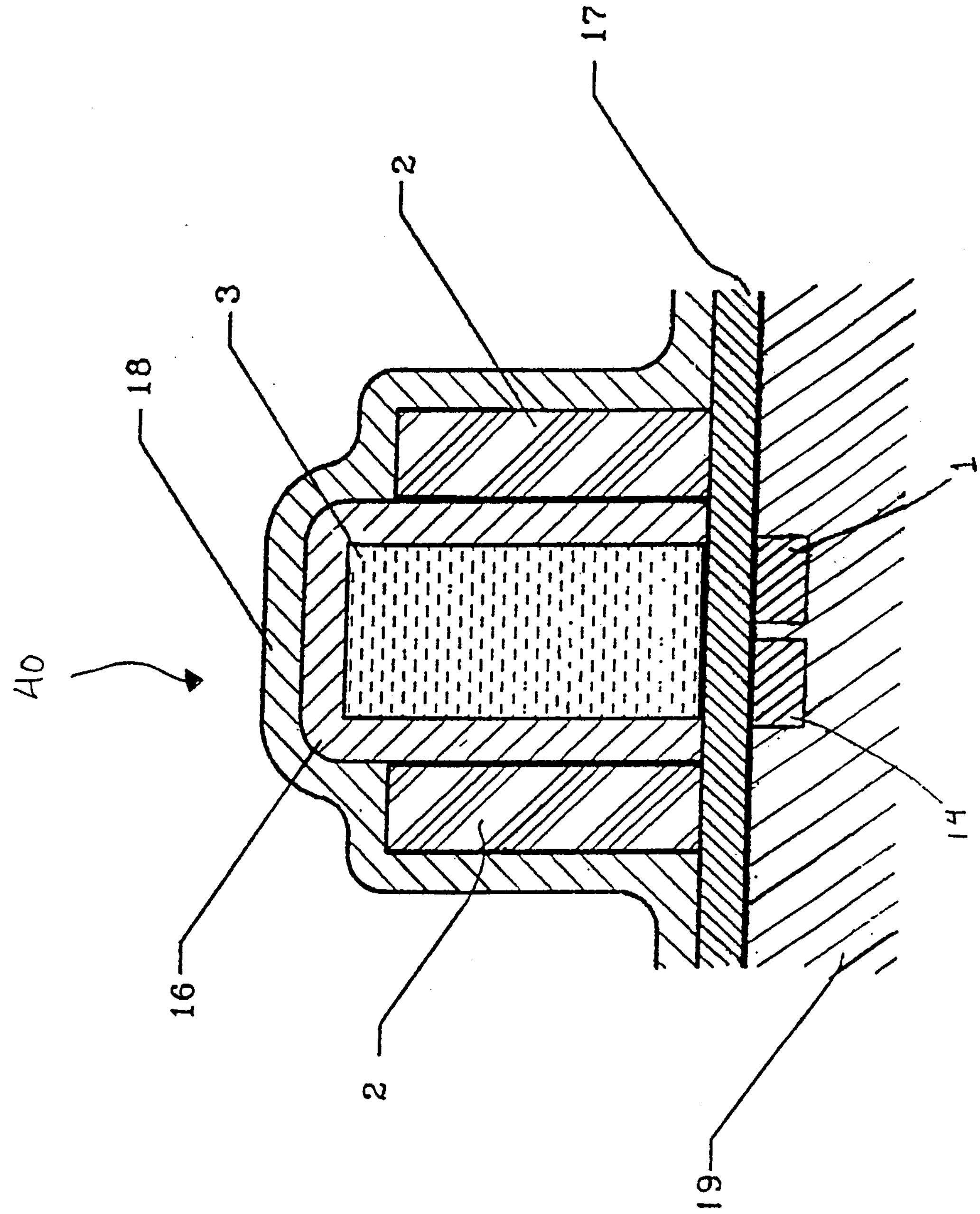

Fig. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/05698

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G11C 11/14, 11/15, 11/18; G01R 33/02
US CL :365/170, 171, 173, 8, 158,209; 324/252; 257/295
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/170, 171, 173, 8, 158,209; 324/252; 257/295

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 5,926,414 A (MCDOWELL et al.) 20 July 1999 (20-07-1999), cols. 15-17.	1-10
Y	US 5,206,590 A (DIENY et al.) 27 April 1993 (27-04-1993), col. 6, line 51 - col. 8.	11
Y	US 5,864,498 A (WOMACK) 26 January 1999 (26-01-1999), col. 6, lines 30-52 and col. 5, lines 45-60.	11
A	US 5,652,445 A (JOHNSON) 29 July 1997 (29-07-1997), col. 3, lines 17-25 and col. 10, lines 20-39.	12-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search 16 MAY 2000	Date of mailing of the international search report 12 JUN 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer A. ZARABIAN Telephone No. (703) 308-490?