(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 September 2018 (07.09.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/158190 A1

(51) International Patent Classification:
H04B 3/23 (2006.01) *H04M 11/06* (2006.01)
H04M 3/30 (2006.01)

(21) International Application Number:
PCT/EP2018/054656

(22) International Filing Date:
26 February 2018 (26.02.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17158402.2 28 February 2017 (28.02.2017) EP

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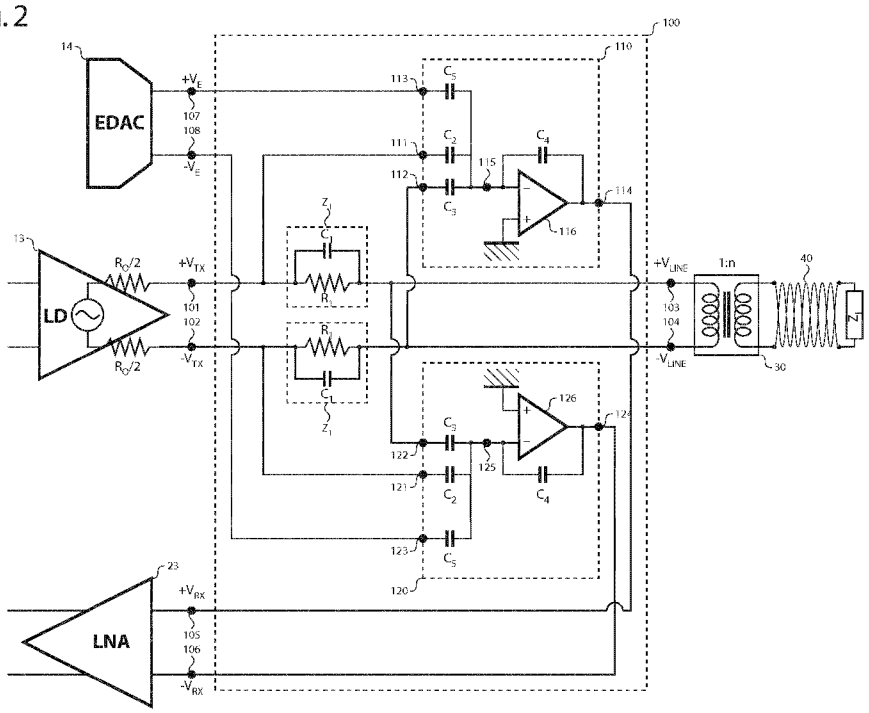
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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,

(54) **Title:** TRANSMISSION ARRANGEMENT FOR FULL-DUPLEX COMMUNICATION

Fig. 2



(57) **Abstract:** The present invention relates to a transmission arrangement (100) for coupling a pair of transmit output terminals (101, 102) to a pair of medium terminals (103, 104) coupled a transmission medium (40), and the pair of medium terminals to a pair of receive input terminals (105, 106), the pairs of transmit output terminals, receive input terminals and medium terminals carrying opposite-polarity signals ($\pm V_{TX}$; $\pm V_{RX}$;$\pm V_{LINE}$). in accordance with an embodiment of the invention, the transmission arrangement comprises a first adder (110) and a second adder (120) with respective first and second adder input terminals (111, 121; 112, 122) and respective adder output terminals (114; 124). The pair of transmit output terminals is coupled to the pair of first adder input terminals, and is further coupled through respective first impedances (Z_1) to the pair of second adder input

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SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

terminals and to the pair of medium terminals, with the first and second adder input terminals being respectively coupled to opposite-polarity transmit output terminals. The pair of receive input terminals is coupled to the pair of adder output terminals. The first impedances individually comprise a first resistor (R_1) coupled in parallel with a first capacitor (C_1). The first and second adders individually comprise second and third capacitors (C_2, C_3) between the respective first and second adder input terminals and a common terminal (115; 125), and a feedback network between the adder output terminal and the common terminal. The first capacitors have a reactance value that matches the difference between the reactance values of the second and third capacitors.

TRANSMISSION ARRANGEMENT FOR FULL-DUPLEX COMMUNICATION

Technical Field of the Invention

The present invention relates to echo suppression for full-duplex communication systems.

Technical Background of the Invention

Discrete Multi-Tone (DMT) communication paradigm combined with full-duplex transmission (all carriers are simultaneously used for both directions of communication) has proven to be particularly successful for achieving record-breaking transmission rates over copper medium, such as Unshielded Twisted Pairs (UTP) or TV broadcast coaxial cables.

Still, full-duplex is particularly challenging as new impairments arise, such as the undesired transmit echo signal that leaks into the useful receive signal.

With Time Division Duplexing (TDD, such as in use in G.fast), the transmitter is not active when the receiver is listening, so echo is definitively not an issue. Yet, with Frequency Division Duplexing (FDD, such as in use in xDSL or DOCSIS), and even more with full-duplex transmission, the transmitter and the receiver are active at the same time, and one has to come up with a solution to efficiently suppress the undesired echo signal from the receive signal.

As a first solution, the transmitter differential output and the receiver differential input are connected to the transmission line through a so-called hybrid network. The hybrid network is designed to subtract the current transmit voltage from the current line voltage at the receiver input, typically by means of hybrid coils or some resistive network.

This solution, combined with analog filtering in the receiver front-end to separate the receive signal from the echo signal, was adequate for legacy ADSL or DOCSIS communication systems where downstream and upstream communications were assigned the upper and lower parts of the spectrum with clear separation band in-between.

With the introduction of VDSL2 and its numerous transmission profiles and intertwined downstream and upstream frequency bands, analog filtering was no longer a viable option. The introduction of the cyclic suffix in addition to the cyclic prefix allows to properly align the downstream and upstream DMT symbols at both sides of the transmission line, and thus to preserve the mutual orthogonality between the downstream and

upstream carriers, meaning the transmit echo signal no longer interferes with the receive signal. Although there is still some degradation of the quantification noise when an echo signal is present at the ADC input, the dynamic range and quantification depth of the ADCs was constantly improving, and with as much as 25dB as isolation, the current hybrid designs were good enough to guarantee acceptable data rates.

That is another story with full-duplex: as the same carriers are simultaneously used in both directions of communication, the echo signal directly affects the reception and is thus perceived as additional background noise.

Furthermore, the hybrid is only designed to suppress the immediate transmit voltage, and the various delayed reflections of the transmit signal arising from impedance mismatches along the loop or cable plant (bridged tap, passive couplers, etc) and echoing back into the receiver through the receive path cannot be distinguished from the useful receive signal and therefore cannot be suppressed by the hybrid network.

Therefore the hybrid network is to be complemented with further echo suppression techniques in order to reduce that extra background noise and to achieve higher data throughputs.

For instance, one could further process the receive samples in the digital domain through an echo cancellation filter in order to cancel the residual echo signal.

Still for instance, one could combine the digital and analog approaches. The residual echo channel through the hybrid is estimated by means of some probing signals, and the residual echo signal is re-generated in the digital domain from the transmit samples, converted in the analog domain by means of an additional Digital to Analog Converter (DAC), and subtracted from the receive signal in the analog domain so as to get an almost echo-free signal at the input of the ADC. So the analog hybrid removes most of the direct echo signal, and the additional DAC kicks in to remove the residual echo due to imperfect echo cancellation in the hybrid and the various delayed echoes that cannot be suppressed by the hybrid.

Yet, there is still some residual echo left on account of the non-linear nature of the line driver. These non-linearities or distortions can hardly be predicted in the digital domain but with complex channel models and tracking

algorithms. There is thus a need for improving the hybrid design so as to get the best echo suppression in the analog domain.

Summary of the Invention

It is an object of the present invention to propose a new hybrid design that is able to operate across a wider frequency range with low insertion loss for the transmit and receive signals and high isolation between the transmit and receive ports, proper line matching, low added noise, and at lowest possible cost, power consumption and size.

In accordance with a particular aspect of the invention, a new transmission arrangement is proposed for coupling a pair of transmit output terminals to a pair of medium terminals coupled a transmission medium, and the pair of medium terminals to a pair of receive input terminals, the pairs of transmit output terminals, receive input terminals and medium terminals carrying opposite-polarity signals. The transmission arrangement comprises a first adder and a second adder with respective first and second adder input terminals and respective adder output terminals. The pair of transmit output terminals is coupled to the pair of first adder input terminals, and is further coupled through respective first impedances to the pair of second adder input terminals and to the pair of medium terminals, with the first and second adder input terminals being respectively coupled to opposite-polarity transmit output terminals. The pair of receive input terminals is coupled to the pair of adder output terminals. The first impedances individually comprise a first resistor coupled in parallel with a first capacitor. The first and second adders individually comprise second and third capacitors between the respective first and second adder input terminals and a common terminal, and a feedback network between the adder output terminal and the common terminal. The first capacitors have a reactance value that matches the difference between the reactance values of the second and third capacitors.

In one embodiment of the invention, the first resistors are matching resistors whose resistance value is determined for an input impedance of the transmission arrangement to match a characteristic impedance of the transmission medium.

In one embodiment of the invention, the transmission arrangement further comprises an adjustment circuit for

dynamically adjusting the resistance value of the first resistors.

In one embodiment of the invention, the first and second adders individually comprise, as feedback network, a fourth capacitor coupled between the adder output terminal and the common terminal.

In one embodiment of the invention, the first and second adders further individually comprise a third adder input terminal, and a fifth capacitor between the third adder input terminal and the common terminal. A further pair of transmit output terminals configured to output a differential echo cancellation signal is coupled to the pair of third adder input terminals.

In one embodiment of the invention, the first and second adders further individually comprise a high-gain differential amplifier with a pair of amplifier input terminals, the inverting terminal of which being coupled to the common terminal, and an amplifier output terminal coupled to the adder output terminal.

In one embodiment of the invention, the first and second adders form part of a receiver differential amplifier with a pair of amplifier input terminals coupled to the pair of common terminals, and a pair of amplifier output terminals coupled to the pair of adder output terminals.

Such a transmission arrangement is typically embedded within an Integrated Circuit (IC), and further forms part of an access node (or access concentrator), such as a Cable Modem Termination System (CMTS), a Distribution Point Unit (DPU), a Digital Subscriber Line Access Multiplexer (DSLAM), or a wireless base station (eNodeB, Wifi access point, etc), or forms part of a subscriber device, such as a modem, a switch, a router, or a user terminal (laptop, smart phone, etc).

So far, transformer-based or resistor-based circuits have been proposed for the design of hybrid networks. Transformer-based hybrids make use of transformers wired in such a way to achieve high isolation between certain ports and low insertion loss between other ports. To operate over large communication bandwidths, line transformers are often used. These circuits currently only exist as discrete components and are rather bulky (> 1 mm^3). Trying to integrate these components on an IC would drastically reduce performance (loss, bandwidth,

etc). Resistor-based hybrids, which have been demonstrated as discrete or on-chip solutions, can provide similar isolation and loss as transformer-based hybrids. However, resistors generate thermal noise, and their various contributions to the total receive noise power may not be negligible when the hybrid is operated over a wide frequency range (e.g., 1.2 GHz). This directly translates into a lower Signal to Noise Ratio (SNR) at the receiver, and hence a lower achievable data rate.

A new hybrid design is proposed (capacitive hybrid hereinafter). The new design includes two adders. Each adder is equipped with two signal input terminals for picking up respective shares of two opposite-polarity transmit voltages across a matching resistor, and another (as-high-as-possible) share of a receive voltage. Capacitors with low capacitance values are provisioned in series along the two input branches of the adder to sink little current from the main current driving the transmission line and to guarantee low insertion loss for the transmit signal. Another capacitor is added in parallel with the matching resistor in order to compensate for the phase shift difference through the two input capacitors and thus to achieve perfect echo cancellation at the common sinking terminal of the adder. And still another capacitor is added in the feedback loop of the adder to control the receive gain and make it frequency-independent. Inherently, these capacitors do not generate thermal noise and thus greatly improve the receiver SNR.

The matching resistor, which is the only remaining resistive component in the capacitive hybrid generating noise, has a resistance value for the input impedance of the hybrid as seen through the line terminals to match a nominal characteristic impedance of the transmission medium, typically 75Ω for a coaxial cable and 100Ω for a twisted copper pair, taking duly account of the winding ratio of the line transformer.

The value of the matching resistor can be dynamically adjusted by means of an adjustment circuit to fit the real part of the actual characteristic impedance of the transmission medium and to minimize the return loss.

Brief Description of the Drawings

The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following

description of an embodiment taken in conjunction with the accompanying drawings wherein:

- fig. 1 represents an overview of a transceiver;
- fig. 2 represents a first embodiment of a transmission arrangement as per the present invention;
- fig. 3A and 3B represent portions of this transmission arrangement for circuit analysis;
- fig. 4 represents a second alternative embodiment of a transmission arrangement as per the present invention; and
- fig. 5A to 5C represent various performance plots of a transmission arrangement as per the present invention.

Detailed Description of the Invention

There is seen in fig. 1 a communication unit 1 for communication over a wired transmission medium with one or more peer communication units. The communication unit 1 typically forms part of an access node or a CPE.

The communication unit 1 uses Discrete Multi-Tone (DMT) modulation over closely-spaced orthogonal carriers (a.k.a. tones or bins), and operates in full-duplex mode, that is to say the same carriers are simultaneously used for both downstream (towards the subscriber premises) and upstream (from the subscriber premises) communications. Thus, the aggregate capacity is doubled when compared to legacy techniques, such as FDD used for DOCSIS or xDSL communications, or TDD used for G.fast communications.

The communication unit 1 comprises a transmitter 10 with two differential transmit output terminals 101 and 102 carrying opposite-polarity transmit voltages $+V_{TX}$ and $-V_{TX}$, and a receiver 20 with two differential receive input terminals 105 and 106 carrying opposite-polarity receive voltages $+V_{RX}$ and $-V_{RX}$. The communication unit 1 further comprises a hybrid 100 coupled to the two transmit output terminals 101 and 102 and to the two receive input terminals 105 and 106, and further coupled to two line terminals 103 and 104 carrying opposite-polarity line voltages $+V_{LINE}$ and $-V_{LINE}$. The line terminals 105 and 106 are further coupled to a transmission medium through a line transformer 30 for DC-isolating the communication unit 1 from the transmission medium.

Presently, the transmission medium is depicted as an Unshielded Twisted Pair (UTP) 40, although the present invention is similarly applicable to other transmission media, such as TV

broadcast coaxial cables. The transmission line 40 is terminated with a load impedance Z_L.

The line voltages $+V_{LINE}$ and $-V_{LINE}$ encompass both respective transmit line voltages $+V_{LINE_TX}$ and $-V_{LINE_TX}$ on account of the transmit voltages $+V_{TX}$ and $-V_{TX}$ being applied over the transmit output terminals 101 and 102, and respective receive line voltages $+V_{LINE_RX}$ and $-V_{LINE_RX}$ on account of a transmit voltage being remotely applied over the transmission line 40 in the reverse direction by a peer communication unit.

The hybrid 100 is configured to pass the differential transmit voltage present on the two transmit output terminals 101 and 102 towards the line terminals 103 and 104 and the differential receive voltage present on the line terminals 103 and 104 towards the receive input terminals 105 and 106 with low insertion loss, while achieving high isolation between the transmit output terminals 101 and 102 and the receive input terminals 105 and 106.

The following relations hold:

$$\pm\mathbf{V}_{LINE_TX}(j\omega)=\pm\boldsymbol{\alpha}(j\omega)\mathbf{V}_{TX}(j\omega) \quad (1),$$

$$\pm\mathbf{V}_{RX}(j\omega)=\pm\boldsymbol{\beta}(j\omega)\mathbf{V}_{LINE_RX}(j\omega)\pm\boldsymbol{\gamma}(j\omega)\mathbf{V}_{TX}(j\omega) \quad (2),$$

wherein the boldfaced voltages denote the respective frequency-dependent complex phasors of the respective voltage signals, $\boldsymbol{\alpha}(j\omega)$ and $\boldsymbol{\beta}(j\omega)$ denote the frequency-dependent complex insertion gains for the transmit and receive signals respectively, and $\boldsymbol{\gamma}(j\omega)$ denotes the frequency-dependent complex isolation gain for the echo signal.

For proper echo cancellation, the hybrid shall be designed in such a way that:

$$|\boldsymbol{\gamma}(j\omega)|\ll|\boldsymbol{\beta}(j\omega)|\frac{V_{RMS_LINE_RX}}{V_{RMS_TX}} \quad (3),$$

while keeping the insertion losses through the hybrid as low as possible. V_{RMS_TX} and $V_{RMS_LINE_RX}$ respectively denote the Root Mean Square (RMS) value of the transmit output voltage V_{TX} at the output terminals 101 and 102 of the transmitter 10 and the RMS value of the receive line voltage V_{LINE_RX} at the line terminals 103 and 104.

The transmitter 10 and the receiver 20 comprise an analog part and a digital part.

The transmit analog part comprises a Digital-to-Analog Converter 12 (or DAC), and a line driver 13 for amplifying the

transmit signal and for driving the transmission line 40. The line driver 13 has Z_O as output impedance, which output impedance being evenly balanced between the two output terminals 101 and 102.

The receive analog part comprises a Low-Noise Amplifier 23 (or LNA) for amplifying the receive signal with as little noise as possible, and an Analog-to-Digital Converter 22 (or ADC).

Some further analog components may be present along the transmit or receive analog path. For instance, the communication unit 1 may further include protection circuitry for protecting against any current or voltage surge occurring over the transmission line 40. Still for instance, the communication unit 1 may further comprise additional amplification stages along the receive path.

The digital part is configured to operate downstream and upstream communication channels for conveying user and control traffic over the transmission line 40.

The digital part comprises a transmit digital part 11 for encoding and modulating user and control data into DMT symbols, and a receive digital part 21 for demodulating and decoding user and control data from DMT symbols.

The following transmit steps are typically performed in the transmit digital part 11:

- data encoding, such as data multiplexing, framing, scrambling, error correction encoding and interleaving;
- signal modulation, comprising the steps of ordering the carriers according to a carrier ordering table, parsing the encoded bit stream according to the bit loadings of the ordered carriers, and mapping each chunk of bits onto an appropriate transmit constellation point (with respective carrier amplitude and phase), possibly with Trellis coding;
- signal scaling;
- possibly, joint signal precoding for crosstalk mitigation,
- Inverse Fast Fourier Transform (IFFT);
- Cyclic Extension (CE) insertion; and possibly
- time-windowing.

The transmit digital part 11 supplies the cyclically-extended digital time samples to the DAC 12 for further analog conversion.

The way around, the ADC 22 supplies the digital time samples of the amplified receive signal to the receive digital part 21 for the following receive steps to be performed:

- CE removal, and possibly time-windowing;
- Fast Fourier Transform (FFT);
- Frequency EQualization (FEQ);
- possibly, joint signal postcoding for crosstalk and/or echo mitigation,
- signal demodulation and detection, comprising the steps of applying to each and every equalized frequency sample an appropriate constellation grid, the pattern of which depends on the respective carrier bit loading, detecting the expected transmit constellation point and the corresponding transmit binary sequence encoded therewith, possibly with Trellis decoding, and reordering all the detected chunks of bits according to the carrier ordering table; and
- data decoding, such as data de-interleaving, error correction, de-scrambling, frame delineation and demultiplexing.

Some of these transmit or receive steps can be omitted, or some additional steps can be present, depending on the exact digital communication technology being used.

The transmit digital part 11 and the receive digital part 21 are typically implemented by means of one or more processors. A processor should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, Digital Signal Processor (DSP), Application Specific Integrated Circuit (ASIC), Field Programmable Gate Array (FPGA), etc. Other conventional and/or custom hardware, such as Random Access Memory (RAM), non volatile storage, may also be included.

There is seen in fig. 2 a first advantageous embodiment of the hybrid 100.

The hybrid 100 is a fully-balanced transmission arrangement comprising a first adder 110 and a second adder 120. The first adder comprises input terminals 111 and 112, an output terminal 114, and an op-amp 116. And the second adder 120 similarly comprises input terminals 121 and 122, an output terminal 124, and an op-amp 126.

The first transmit output terminal 101 is coupled to a first terminal of a first impedance and to the first input terminal 111 of the first adder 110. The second terminal of the

first impedance is coupled to the line terminal 103 and to the second input terminal 122 of the second adder 120. Symmetrically, the second transmit output terminal 102 is coupled to a first terminal of a second impedance and to the first input terminal 121 of the second adder 120. The second terminal of the second impedance is coupled to the line terminal 104 and to the second input terminal 112 of the first adder 110. The first and second impedances have a common value Z_1, and comprise a resistor R1 in parallel with a capacitor C1. The output terminals 114 and 124 of the first adder 110 and the second adder 120 are coupled to the respective receive input terminals 105 and 106.

The input terminals 111 and 112 of the first adder 110 are coupled to the inverting terminal of the op-amp 116 through respective capacitors C2 and C3, the inverting terminal of the op-amp 116 acting as a common terminal 115 of the first adder 110. The output terminal 114 of the first adder 110 is looped back to the common terminal 115 through a capacitor C4. The non-inverting terminal of the op-amp 116 is grounded. Symmetrically, the input terminals 121 and 122 of the second adder 120 are coupled to the inverting terminal of the op-amp 126 through respective capacitors C2 and C3, the inverting terminal of the op-amp 126 acting as a common terminal 125 of the second adder 120. The output terminal 124 of the first adder 120 is coupled to the common terminal 125 through a capacitor C4. The non-inverting terminal of the op-amp 126 is grounded.

As aforementioned, the hybrid is designed to subtract the current transmit voltage from the current line voltage, and is thus unable to cope with the delayed signal reflections arising from impedance mismatches along the loop or cable plant (bridged tap, passive couplers, etc) and echoing back into the receiver along the receive path. For adequate echo suppression, these various echo residues need to be estimated, re-generated in the digital domain, converted in the analog domain by means of an additional DAC , and subtracted from the line signal in the analog domain.

The first adder 110 and second adder 120 then accommodate respective third input terminals 113 and 123 coupled to respective differential output terminals 107 and 108 carrying opposite-polarity echo cancellation voltages $+V_E$ and $-V_E$ generated by an additional DAC 14 (or EDAC). The third input

terminals 113 and 123 are coupled to the respective common terminals 115 and 125 through a capacitor C5.

The transmission arrangement will now be analyzed with regard to fig 3A and 3B.

As any linear circuit, the transmission arrangement as per fig. 2 can be analyzed by means of the superposition principle so as to de-correlate transmission from reception. We will first assume that the transmit output terminals 101 and 102 are fed with a differential transmit voltage $\pm V_{TX}$ only and that no transmit voltage is applied at the far-end of the transmission line 40, meaning no receive voltages $\pm V_{LINE_RX}$ is present on the line terminals 103 and 104, such as depicted in fig. 3A (TX only). Next, we will assume that a transmit voltage is applied at the far-end of the transmission line 40, yielding a differential receive voltage $\pm V_{LINE_RX}$ over the line terminals 103 and 104 produced by the transformer emf, and that no transmit voltage $\pm V_{TX}$ is applied on the transmit output terminals 101 and 102, such as depicted in fig. 3B (RX only).

There is seen in fig. 3A the various impedances loading the transmitter output, assuming 1:1 as winding ratio for the line transformer.

The transmitter is modeled as two opposite-polarity ideal voltage generators $E_{TX}^{\pm}$ having a common ground terminal with $E_{TX}^{-}=-E_{TX}^{+}$, and coupled in series with two respective output resistors $R_O/2$. Let further assume that the impedance of the transmission line as seen through the line terminals 103 and 104 consists of two load resistors $R_L/2$ between the respective terminals 103 and 104 and the ground.

Assuming that the inverting terminals of the op-amp 116 and 126 are maintained to a virtual ground voltage on account of the negative feedback, the transmitter output is loaded with a total impedance $\mathbf{Z}_{TX}$ given by:

$$\frac{\mathbf{Z}_{TX}}{2}\equiv\mathbf{Z}_2\|\left[\mathbf{Z}_1+\left(\mathbf{Z}_3\|\frac{R_L}{2}\right)\right] \quad (4),$$

with:

$$\mathbf{Z}_1\equiv R_1\|C_1=\frac{R_1}{1+j\omega C_1 R_1} \quad (5),$$

$$\mathbf{Z}_2=\frac{1}{j\omega C_2} \quad (6), \text{ and}$$

$$\mathbf{Z}_3=\frac{1}{j\omega C_3} \quad (7).$$

Let $\mathbf{V}_{TX1}^{\pm}$ denote the voltages appearing at the transmit output terminals 101 and 102 when no voltage is being received from the line. We then have:

$$\mathbf{V}_{TX1}^{\pm}=\frac{\mathbf{Z}_{TX}}{\mathbf{Z}_{TX}+R_0}\mathbf{E}_{TX}^{\pm} \quad (8), \text{ and}$$

$$\mathbf{V}_{LINE_TX}^{\pm}=\frac{\mathbf{Z}_4}{\mathbf{Z}_4+\mathbf{Z}_1}\mathbf{V}_{TX1}^{\pm}=\left(\frac{\mathbf{Z}_4}{\mathbf{Z}_4+\mathbf{Z}_1}\right)\left(\frac{\mathbf{Z}_{TX}}{\mathbf{Z}_{TX}+R_0}\right)\mathbf{E}_{TX}^{\pm} \quad (9),$$

wherein:

$$\mathbf{Z}_4\equiv\frac{R_L}{2}\|C_3=\frac{\frac{R_L}{2}}{1+j\omega C_3\frac{R_L}{2}}=\frac{R_L}{2+j\omega C_3 R_L} \quad (10).$$

The hybrid insertion loss for the transmit signal is thus given by:

$$\alpha=\frac{\mathbf{Z}_4}{\mathbf{Z}_4+\mathbf{Z}_1} \quad (11).$$

In order to get a low insertion loss for the transmit signal, one has to select a relatively small value for C_3 for $|Z4| >> |Z1|$ and $|\alpha| \simeq 1$.

As depicted in fig. 3A, let i_1 and i_3 denote the currents entering the first input terminals of the adders 110 and 120 respectively, and let i_4 and i_2 denote the current entering the second input terminals of the adders 110 and 120 respectively. Let i_L denote the current through the load R_L.

As the circuit is fully balanced, we have opposite currents circulating in the symmetric counterpart branches of the circuit, and:

$i_1 = -i_3$ and $i_2 = -i_4$ (12).

In order to get adequate echo suppression, the following relation shall hold:

$i_1 = -i_4$ and $i_2 = -i_3$ (13),

so as when a given current enters the common terminal through the first input terminal of the adder, then an equivalent current leaves the common terminal through the second input terminal of the adder, and vice-versa.

With regard to eq. (12), we then have:

$i_1 = i_2 = -i_3 = -i_4$ (14).

We further have:

$$\mathbf{V}^{+}_{TX1}=\frac{\mathbf{I}_1}{j\omega C_2} \quad (15),$$

$$\mathbf{V}^{+}_{LINE_TX}=\frac{\mathbf{I}_2}{j\omega C_3}=\frac{\mathbf{I}_1}{j\omega C_3} \quad (16)$$

$$\mathbf{V}^{-}_{TX1}=\frac{\mathbf{I}_3}{j\omega C_2}=-\frac{\mathbf{I}_1}{j\omega C_2} \quad (17), \text{ and}$$

$$\mathbf{V}^{-}_{LINE_TX}=\frac{\mathbf{I}_4}{j\omega C_3}=-\frac{\mathbf{I}_1}{j\omega C_3} \quad (18).$$

Applying Kirchoff's current law to the node $\mathbf{V}^{+}_{LINE_TX}$:

$$\frac{\mathbf{V}^{+}_{TX1}-\mathbf{V}^{+}_{LINE_TX}}{\mathbf{Z}_1}=\mathbf{I}_2+\frac{\mathbf{V}^{+}_{LINE_TX}-\mathbf{V}^{-}_{LINE_TX}}{R_L} \ ,$$

or, with further regard to eq. (15) through (18):

$$\frac{\mathbf{I}_1}{\mathbf{Z}_1}\left(\frac{1}{j\omega C_2}-\frac{1}{j\omega C_3}\right)=\mathbf{I}_1+\frac{\mathbf{I}_1}{R_L}\left(\frac{1}{j\omega C_3}+\frac{1}{j\omega C_3}\right) \ ,$$

yielding:

$$\frac{1}{\mathbf{Z}_1}\left(\frac{1}{j\omega C_2}-\frac{1}{j\omega C_3}\right)=1+\frac{1}{R_L}\left(\frac{2}{j\omega C_3}\right) \ , \text{ or}$$

$$\frac{1}{\mathbf{Z}_1}=\frac{1}{R_1}+j\omega C_1=\frac{1+\frac{1}{R_L}\left(\frac{2}{j\omega C_3}\right)}{\left(\frac{1}{j\omega C_2}-\frac{1}{j\omega C_3}\right)}=\frac{2}{R_L C_3}\left(\frac{1}{\frac{1}{C_2}-\frac{1}{C_3}}\right)+j\omega\left(\frac{1}{\frac{1}{C_2}-\frac{1}{C_3}}\right) \quad (19).$$

If we equate the real and imaginary parts of eq. (19) with the real and imaginary parts of $1/\mathbf{Z}_1$, then the following two relations shall be adhered to for adequate echo suppression:

$$\frac{1}{C_1}=\frac{1}{C_2}-\frac{1}{C_3} \quad (20), \text{ and}$$

$$\frac{1}{R_1}=\frac{2}{R_L C_3}\left(\frac{1}{\frac{1}{C_2}-\frac{1}{C_3}}\right)=\frac{2C_1}{R_L C_3} \quad (21).$$

There is seen in fig. 3B the various impedances loading the transmission line when a far-end signal is being received through the line terminals 103 and 104, still assuming 1:1 as winding ratio for the line transformer.

The line is modeled as two opposite-polarity ideal voltage generators $E^{\pm}_{RX}$ having a common ground terminal with $E^{-}_{RX}=-E^{+}_{RX}$, and coupled in series with two respective output resistors $R_L/2$.

Still assuming that the inverting terminals of the op-amp 116 and 126 are maintained to a virtual ground voltage on account of the negative feedback, the transmission line 40 is loaded with a total impedance $\mathbf{Z}_{RX}$ given by:

$$\frac{\mathbf{Z}_{RX}}{2} \equiv \mathbf{Z}_3 \| \left[\mathbf{Z}_1 + \left(\mathbf{Z}_2 \| \frac{R_0}{2} \right) \right] \quad (22).$$

Let $\mathbf{V}^{\pm}_{LINE_RX}$, resp. $\mathbf{V}^{\pm}_{TX2}$, denote the voltages produced by the transformer emf at the line terminals 103 and 104, resp. the voltages appearing at the transmit output terminals 101 and 102, when a voltage is being remotely applied over the line and no transmit voltage is being inserted by the transmitter. We then have:

$$\mathbf{V}^{\pm}_{LINE_RX} = \frac{\mathbf{Z}_{RX}}{\mathbf{Z}_{RX} + R_L} \mathbf{E}^{\pm}_{RX} \quad (23), \text{ and}$$

$$\mathbf{V}^{\pm}_{TX2} = \mathbf{Z}_5 \left(\frac{2}{\mathbf{Z}_{RX}} - \frac{1}{\mathbf{Z}_3} \right) \mathbf{V}^{\pm}_{LINE_RX} = \frac{\mathbf{Z}_5}{\mathbf{Z}_1 + \mathbf{Z}_5} \mathbf{V}^{\pm}_{LINE_RX} \quad (24),$$

wherein:

$$\mathbf{Z}_5 \equiv \frac{R_0}{2} \| C_2 = \frac{\frac{R_0}{2}}{1 + j\omega C_2 \frac{R_0}{2}} = \frac{R_0}{2 + j\omega C_2 R_0} \quad (25).$$

The differential receive voltages at the receive input terminal 105 and 106 are then given by:

$$\begin{aligned} \mathbf{V}^{\pm}_{RX} &= -\frac{1}{j\omega C_4} \left(j\omega C_3 \mathbf{V}^{\mp}_{LINE_RX} + j\omega C_2 \frac{\mathbf{Z}_5}{\mathbf{Z}_1 + \mathbf{Z}_5} \mathbf{V}^{\pm}_{LINE_RX} \right) \\ &= \frac{1}{C_4} \left(C_3 - C_2 \frac{\mathbf{Z}_5}{\mathbf{Z}_1 + \mathbf{Z}_5} \right) \mathbf{V}^{\pm}_{LINE_RX} \end{aligned} \quad (26),$$

and the hybrid insertion loss for the receive signal is given by:

$$\boldsymbol{\beta} = \frac{1}{C_4} \left(C_3 - C_2 \frac{\mathbf{Z}_5}{\mathbf{Z}_1 + \mathbf{Z}_5} \right) \approx \frac{C_3}{C_4} \quad (27),$$

which in approximation is simply the gain of the adder when the hybrid losses are neglected.

For optimal power transfer from the transmission line into the receiver and minimal signal reflection at the line terminals, the resistance value of the matching resistor R_1 is determined so as the real part of the input impedance $\mathbf{Z}_{RX}$ matches the real part of the characteristic impedance $\mathbf{Z}_C$ of the transmission line. If the impedance values C_1, C_2 and C_3 are chosen sufficiently small for the input currents i_1 to i_4 to be

low enough with respect to the main load current i_L (assumption valid at low/mid-frequencies at least), then this requirement translates into:

$R_1 = R_L/2n^2 - R_O/2$ (28),

assuming 1:n as winding ratio for the line transformer.

The reactance value of the capacitor C_1 shall substantially match the difference between the reactance value of the first input branch of one adder and the reactance value of the second input branch of the other adder, namely $1/C_2 - 1/C_3$, so as there are antiphase input currents at the common terminal of the adders.

As aforementioned, the capacitance value of the capacitor C_3 shall be chosen sufficiently small in order to have the lowest insertion loss for the transmit signal. In addition, the chosen capacitance value shall substantially match eq. (21), which is possible as eq. (20) and (21) leave some degree of freedom for selecting a capacitance value for the capacitor C_2.

The capacitance value of the capacitor C_4 determines the receive gain across the opamps 116 and 126 as per eq. (27).

The capacitance value of the capacitor C_5 determines the insertion gain of the echo cancellation voltage $\mathbf{V}_E^{\pm}$.

For instance, the following values can be used with a load resistance $R_L = 75\Omega$ (coaxial cable), a generator output resistance $R_O = 22\Omega$, and 1:1 as winding ratio for the line transformer:

- $R_1 = 26{,}5\Omega$;
- $C_3 = 1pF$;
- $C_2 = 0{,}5858pF$;
- $C_1 = 1{,}414pF$.

The resistor R_1 can be replaced by a tunable resistor. This allows to calibrate R_1 by a limited amount so as to compensate for uncertainties or deviations on the line driver output impedance Z_O or on the average line characteristic impedance Z_C. Thanks to the integration with the digital backend, this calibration can be done automatically.

For instance, the variable resistor can be implemented as a MOSFET in the linear region in parallel with another resistor. The gate voltage on the MOSFET determines the resistance between its source and drain. Capacitors are added between the body and the source, and between the source and the

gate, of the MOSFET to prevent large voltages in AC across the MOSFET terminals.

There is seen in fig. 4 a second alternative embodiment of the hybrid 100.

This embodiment differs from the first embodiment in that the two adders 110 and 120 are implemented by means of the existing LNA 23 for reduced cost and size.

The common terminals of the adders are coupled to the input terminals of the LNA 23, and the output terminals of the adders are coupled to the respective opposite-polarity output terminals of the LNA 23. Presently, the common terminal 115 of the first adder 110 is coupled to the non-inverting input terminal of the LNA 23, and the output terminal 114 of the first adder 110 is coupled to the inverting output terminal of the LNA 23, and as feedback loop to the common terminal 115 of the first adder 110 through the capacitor C4. Symmetrically, the common terminal 125 of the second adder 120 is coupled to the inverting input terminal of the LNA 23, and the output terminal 124 of the second adder 120 is coupled to the non-inverting output terminal of the LNA 23, and as feedback loop to the common terminal 125 of the second adder 120 through the capacitor C4.

The remainder of the transmission arrangement 100 is left unmodified.

The proposed transmission arrangement has a smaller footprint, and can be integrated within an IC. The capacitance values needed are compatible with the newest CMOS processes. In fact, smaller capacitors are beneficial since they allow more wideband operation. Furthermore, implementing small capacitor values is more accurate on an IC than in discrete components on a board.

There is seen in fig. 5A to 5C various performance plots for a hybrid as per the present invention.

Fig. 5A represents the various insertion gains through the capacitive hybrid versus frequency. The transmit insertion gain from the DAC output ports up to the line terminals, and including the line driver gain, is depicted as a plain-line curve (TX-line). The receive insertion gain from the line terminals up to the ADC input ports, and including the LNA gain, is depicted as a dashed-line curve (line-RX). And last, the insertion gain of the additional echo cancellation signal from the output ports of the additional DAC up to the ADC input ports

is depicted as a dotted-line curve (ECDAC-RX). As one can see, the frequency response of the hybrid is relatively flat across the 1 GHz frequency range.

Fig. 5B plot represents the Trans-Hybrid Return Loss (THRL) versus frequency, that is to say the isolation gain from the DAC output ports up to the near-end ADC input ports, including both the line driver gain and the LNA gain.

Fig. 5C plot represents the Figure of Merit (FoM), which is a more representative metric for the hybrid than the THRL. The mean FoM is about 21 dB, which a very good performance figure for such a wide frequency range (up to 1,2 GHz).

The FoM is computed from the gains TX-line and line-RX and from the THRL as follows (with gains expressed in dB):

gain(TX-line) = gain(LD) + gain(HTX-line) (29),

gain(line-RX) = gain(line-HRX) + gain(LNA) (30), and

THRL = gain(TX-RX) = gain(LD) + gain(HTX-HRX) + gain(LNA) (31),

wherein HTX and HRX respectively denote the transmit output ports and the receive input ports of the hybrid.

FOM is then given by:

FOM = gain(TX-line) + gain(line-RX) - THRL = gain(HTX-line) + gain(line-HRX) - gain(HTX-HRX) (32).

For instance at low frequencies, and based upon the plots 5A and 5B, FoM $\simeq$ 11 + 8 - (-18) $\simeq$ 37dB.

Simulations of a resistive hybrid compared to a capacitive hybrid (with ideal amplifiers, meaning no noise generated inside the amplifiers) show that the resistive hybrid produces a noise PSD of -154dBm/Hz at the receiver input, while the proposed capacitive hybrid produces a noise PSD of only -167dBm/Hz. In the resistive hybrid, the resistors in the input branches and the feedback loop dominate the noise contribution. The noise contribution of the matching resistor R_1, which is also present in the capacitive hybrid, is far lower. If the ADC noise floor is about -140dBm/Hz, the addition of a noise PSD of -154dBm/Hz results in an increase of 0,17dB of the noise PSD. However, if an LNA with a gain of 10dB is used after the resistive hybrid, the increase in the noise PSD is 1,46dB, which is rather substantial. With the proposed capacitive hybrid, and still assuming an LNA gain of 10dB, the increase in the noise PSD is only 0,09dB.

Although the above embodiments mostly focus on wired transmissions, the present invention is similarly applicable to

wireless full-duplex transmission. In this case, the transmitter output and the receiver input are coupled through the proposed transmission arrangement 100 to a transmission medium, typically a coaxial cable, carrying the transmit and receive voltages to/from one or more antennas for EM propagation over the air. The transceiver typically accommodates additional circuitries such as up-down frequency mixer, further MIMO signal processing for path diversity, etc. The transmission arrangement 100 would then form part of a wireless base station or access point, or of a wireless user terminal, such as a smart phone, a laptop, and so forth.

It is to be noticed that the term 'comprising' should not be interpreted as being restricted to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the relevant components of the device are A and B.

It is to be further noticed that the term 'coupled' should not be interpreted as being restricted to direct connections only. Thus, the scope of the expression 'a device A coupled to a device B' should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B, and/or vice-versa. It means that there exists a path between an output of A and an input of B, and/or vice-versa, which may be a path including other devices or means.

The description and drawings merely illustrate the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the principles of the invention. Furthermore, all examples recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass equivalents thereof.

CLAIMS

1. **A transmission arrangement** (100) for coupling **a pair of transmit output terminals** (101, 102) to **a pair of medium terminals** (103, 104) coupled **a transmission medium** (40), and the pair of medium terminals to **a pair of receive input terminals** (105, 106), the pairs of transmit output terminals, receive input terminals and medium terminals carrying opposite-polarity signals ($\pm V_{TX}$; $\pm V_{RX}$; $\pm V_{LINE}$),

wherein the transmission arrangement comprises **a first adder** (110) and **a second adder** (120) with respective **first and second adder input terminals** (111, 121; 112, 122) and respective **adder output terminals** (114; 124),

wherein the pair of transmit output terminals is coupled to the pair of first adder input terminals, and is further coupled through respective **first impedances** (Z_1) to the pair of second adder input terminals and to the pair of medium terminals, with the first and second adder input terminals being respectively coupled to opposite-polarity transmit output terminals, and the pair of receive input terminals is coupled to the pair of adder output terminals,

wherein the first impedances individually comprise **a first resistor** (R_1) coupled in parallel with **a first capacitor** (C_1),

wherein the first and second adders individually comprise **second and third capacitors** (C_2, C_3) between the respective first and second adder input terminals and **a common terminal** (115; 125), and **a feedback network** between the adder output terminal and the common terminal,

and wherein the first capacitors have a reactance value that matches the difference between the reactance values of the second and third capacitors.

2. **A transmission arrangement** (100) according to claim 1, *wherein* the first resistors are matching resistors whose resistance value is determined for **an input impedance** of the transmission arrangement to match **a characteristic impedance** of the transmission medium.

3. **A transmission arrangement** (100) according to claim 2, *wherein* the transmission arrangement further comprises **an adjustment circuit** for dynamically adjusting the resistance value of the first resistors.

4. **A transmission arrangement** (100) according to claim 1, *wherein* the first and second adders individually comprise, as feedback network, **a fourth capacitor** (C_4) coupled between the adder output terminal and the common terminal.

5. **A transmission arrangement** (100) according to claim 1, *wherein* the first and second adders further individually comprise **a third adder input terminal** (113; 123), and **a fifth capacitor** (C_5) between the third adder input terminal and the common terminal,
and wherein **a further pair of transmit output terminals** (107, 108) configured to output **a differential echo cancellation signal** ($\pm V_E$) is coupled to the pair of third adder input terminals.

6. **A transmission arrangement** (100) according to claim 1, *wherein* the first and second adders further individually comprise **a high-gain differential amplifier** (116; 126) with a pair of amplifier input terminals, the inverting terminal of which being coupled to the common terminal, and an amplifier output terminal coupled to the adder output terminal.

7. **A transmission arrangement** (100) according to claim 1, *wherein* the first and second adders form part of **a receiver differential amplifier** (23) with a pair of amplifier input terminals coupled to the pair of common terminals, and a pair of amplifier output terminals coupled to the pair of adder output terminals.

8. **An integrated circuit** comprising **a transmission arrangement** (100) according to any of claims 1 to 7.

9. **An access node** comprising **a transmission arrangement** (100) according to any of claims 1 to 7.

10. **An access node** according to claim 9, *wherein* the access node is **a Cable Modem Termination System CMTS**, and the transmission medium is **a coaxial cable**.

11. **An access node** according to claim 9, *wherein* the access node is **a Distribution Point Unit DPU**, and the transmission medium is **a twisted copper pair**.

12. **An access node** according to claim 9, *wherein* the access node is **a Digital Subscriber Line Access Multiplexer DSLAM**, and the transmission medium is **a twisted copper pair**.

13. **An access node** according to claim 9, *wherein* the access node is **a wireless base station**, and the transmission medium is coupled to one or more antennas for signal transmission and reception over the air.

14. **A subscriber device** comprising **a transmission arrangement** (100) according to any of claims 1 to 7.

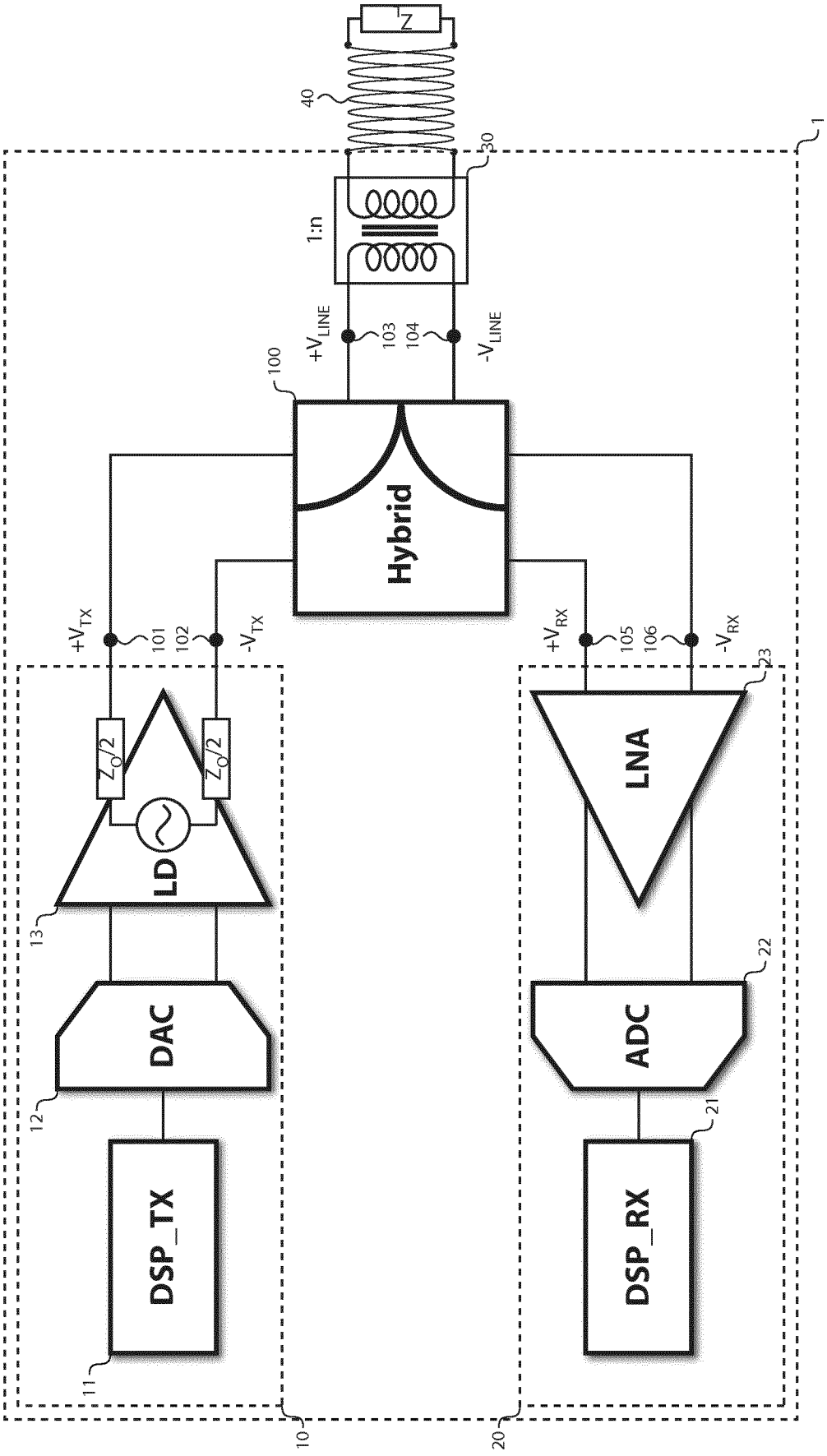

Z
40
30
1
1:n
+V_LINE
103
104
-V_LINE
100
Hybrid
+V_TX
101
102
-V_TX
+V_RX
105
106
-V_RX
23
LNA
Z_O/2
Z_O/2
LD
13
22
DAC
ADC
12
21
DSP_TX
DSP_RX
11
10
20

Fig. 1

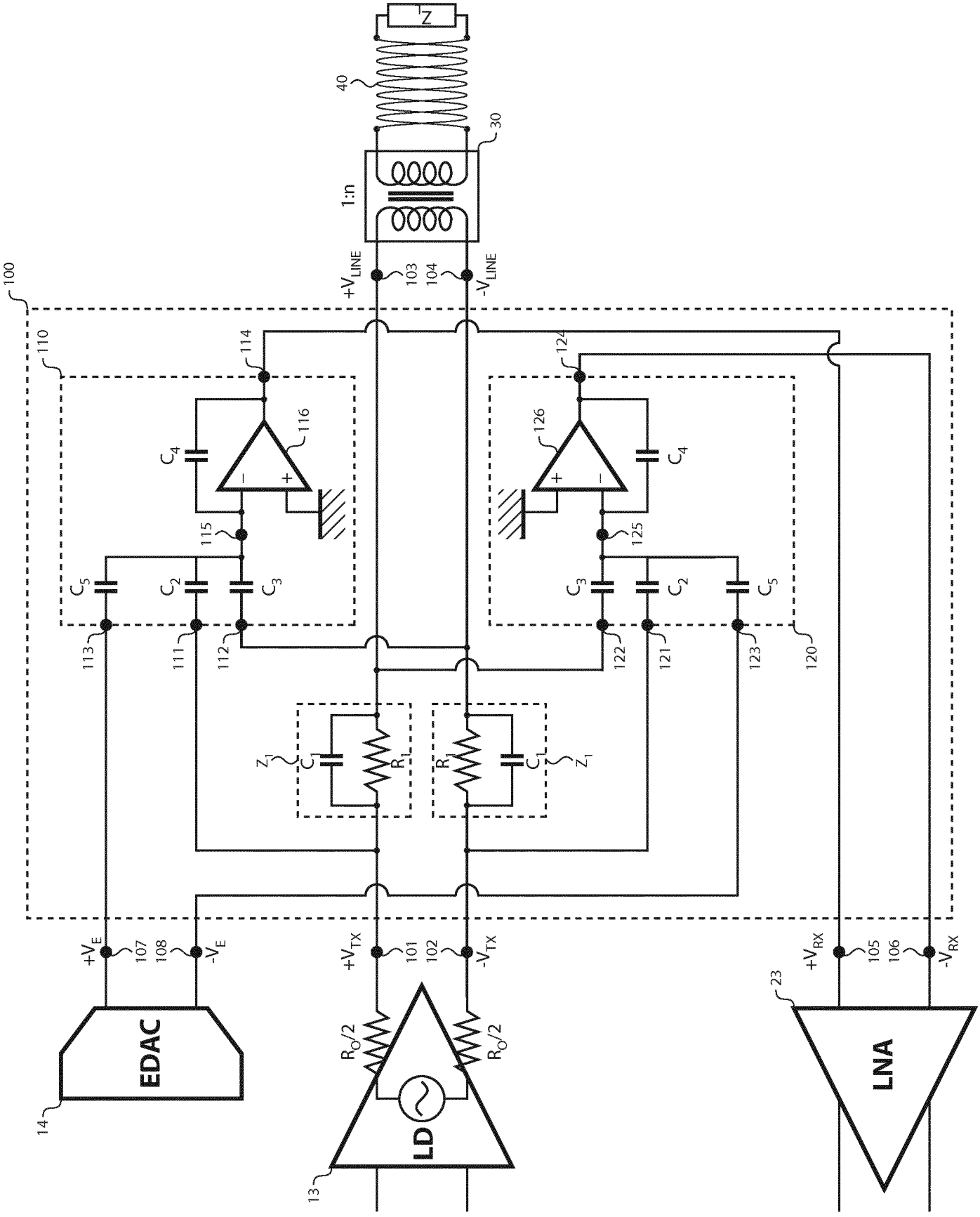

Z
40
30
1:n
+V_LINE
-V_LINE
103
104
100
110
114
124
116
126
C4
C5
C2
C3
115
125
111
112
113
120
121
122
123
Z1
C1
RL
+VE
-VE
107
108
+VTX
-VTX
101
102
+VRX
-VRX
105
106
EDAC
14
RO/2
LD
13
LNA
23

Fig. 2

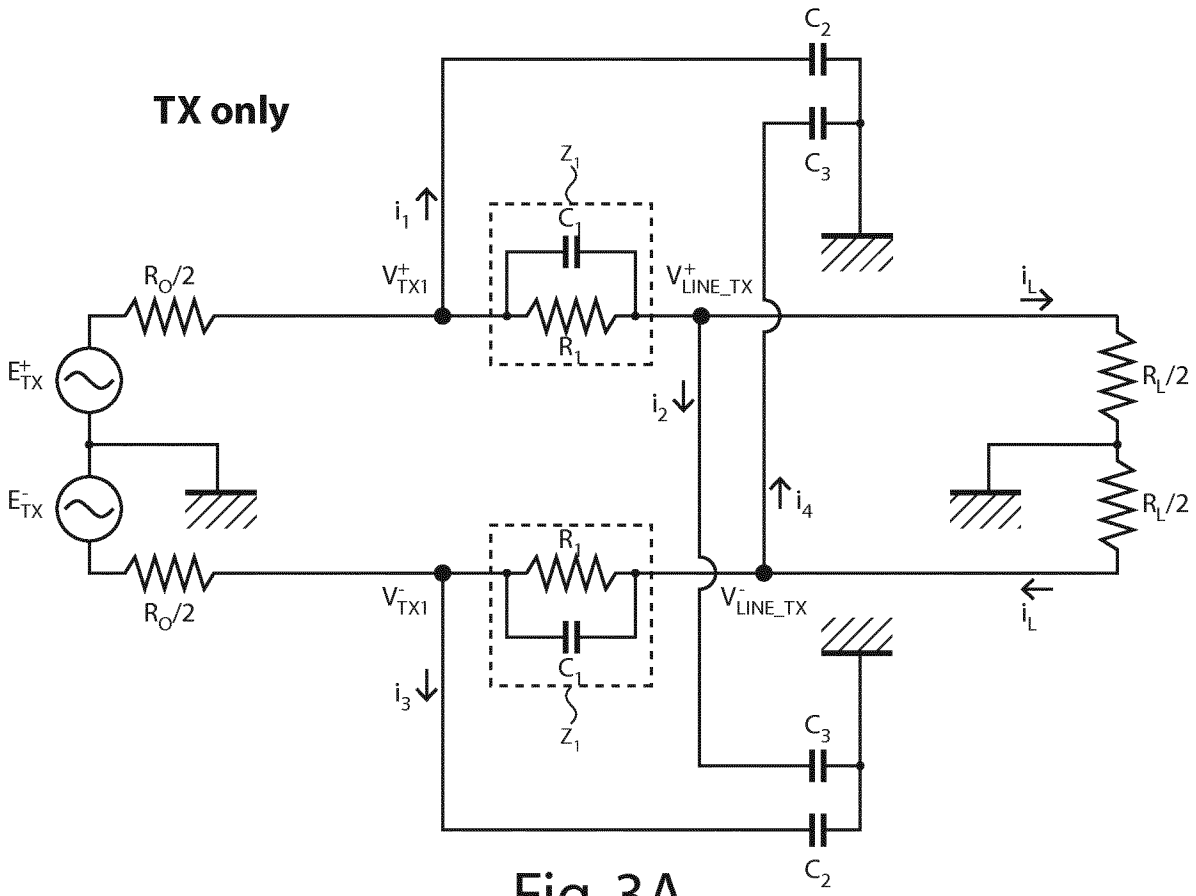

TX only
C2
C3
Z1
i1
C1
R1
R0/2
V+TX1
V+LINE_TX
iL
E+TX
i2
RL/2
E-TX
i4
RL/2
R1
R0/2
V-TX1
V-LINE_TX
iL
C1
i3
Z1
C3
C2

Fig. 3A

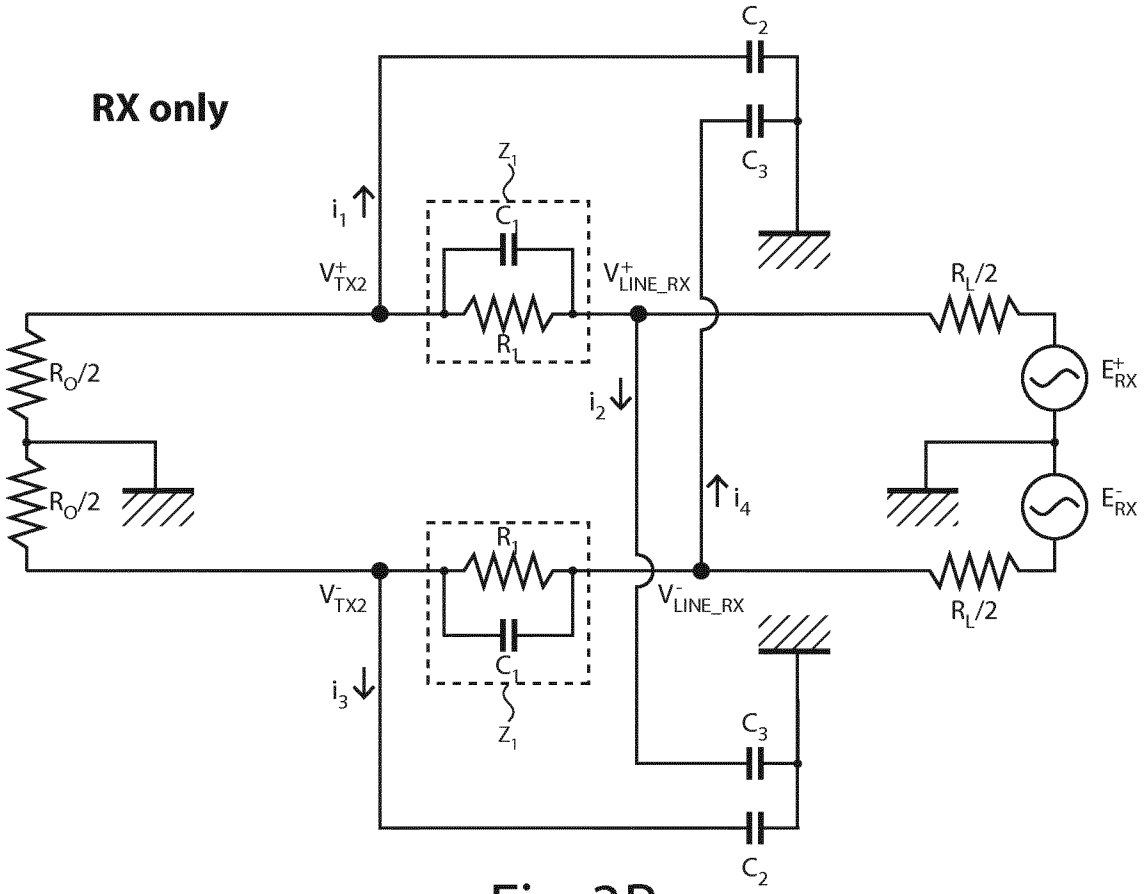

RX only
C2
C3
Z1
i1
C1
R1
V+TX2
V+LINE_RX
RL/2
R0/2
E+RX
i2
R0/2
i4
E-RX
R1
V-TX2
V-LINE_RX
RL/2
C1
i3
Z1
C3
C2

Fig. 3B

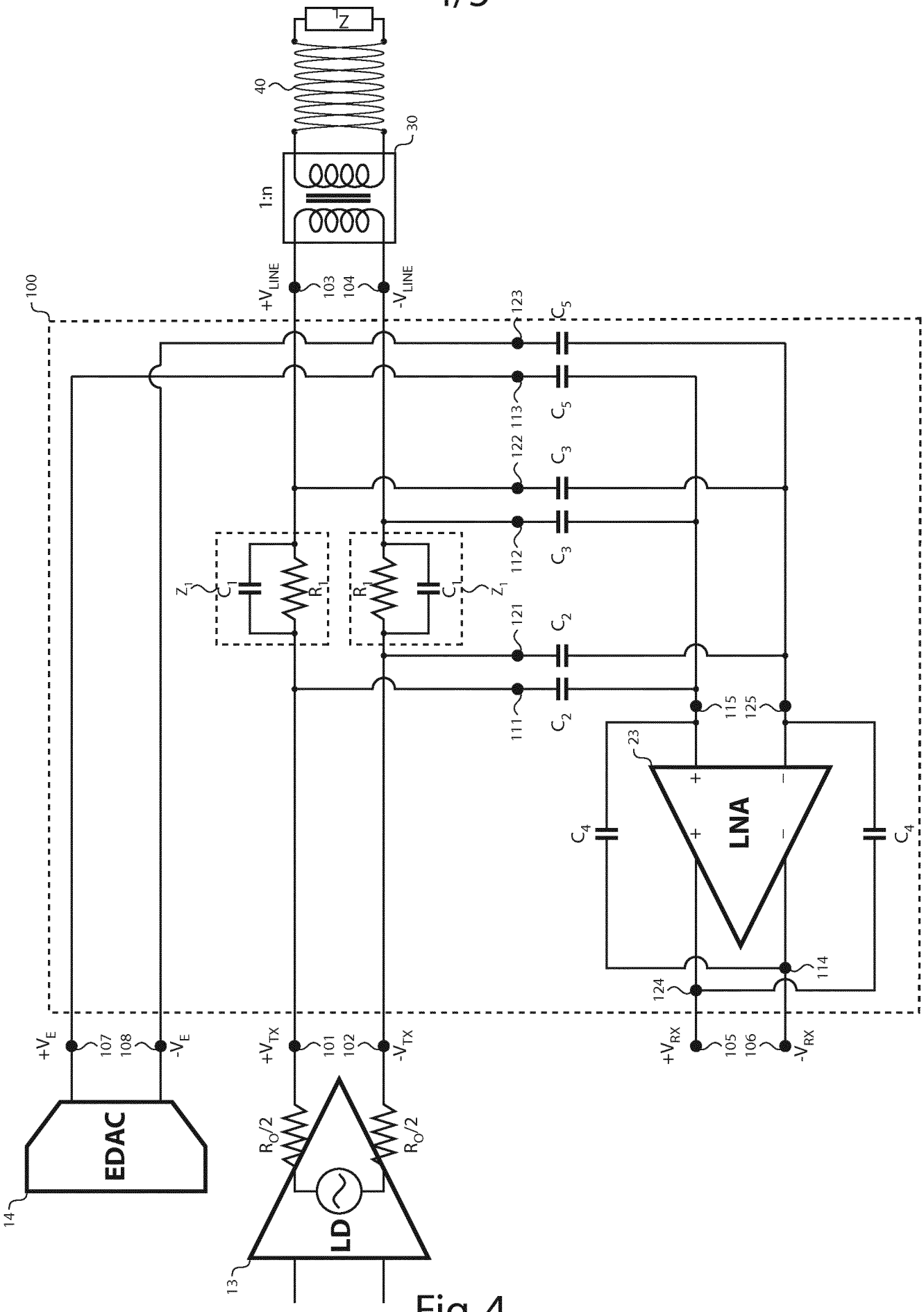

Z
40
30
1:n
100
+V_LINE
103
104
-V_LINE
123
C_5
122
113
C_3
112
C_3
Z_1
C_1
R_1
R_1
C_1
Z_1
121
C_2
111
C_2
115
125
23
LNA
C_4
C_4
114
124
+V_RX
105
106
-V_RX
+V_E
107
108
-V_E
EDAC
14
+V_TX
101
102
-V_TX
R_O/2
R_O/2
LD
13

Fig. 4

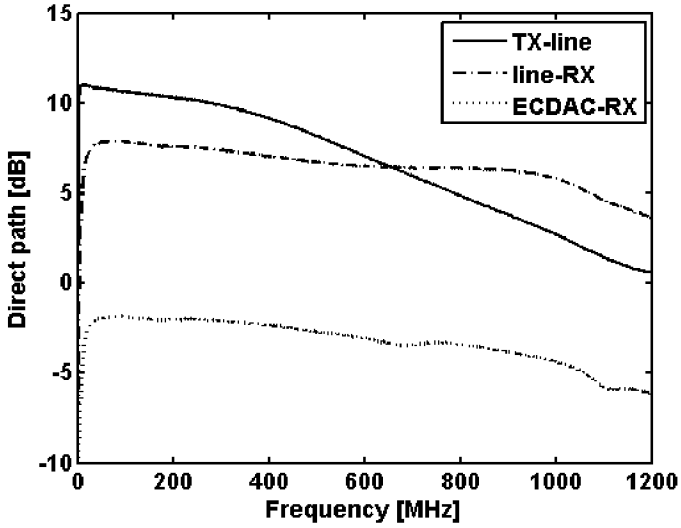


Fig. 5A

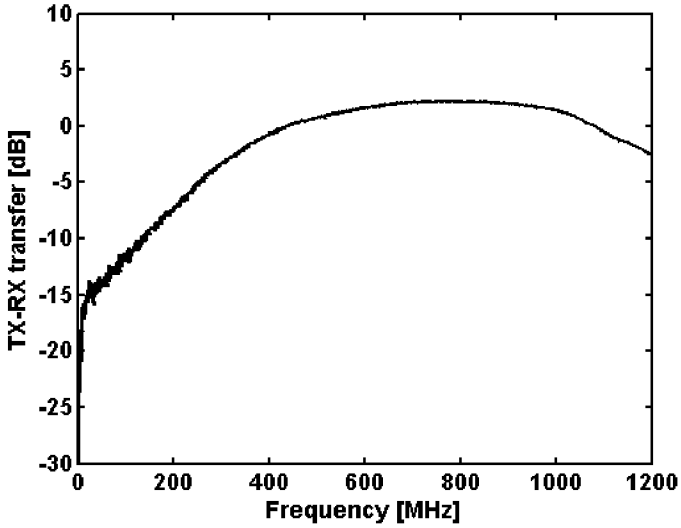


Fig. 5B

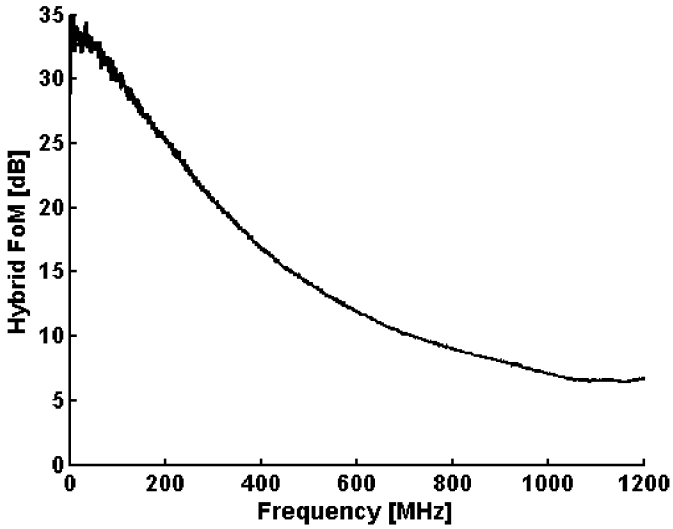


Fig. 5C

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/054656

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B3/23 H04M3/30 H04M11/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B H04M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2003/142688 A1 (CHOU GERCHIH [US] ET AL) 31 July 2003 (2003-07-31) paragraph [0029] - paragraph [0030] paragraph [0040] - paragraph [0055] figure 10	1-14
A	US 2003/169875 A1 (LEE SANG-SOO [US] ET AL) 11 September 2003 (2003-09-11) paragraph [0019] - paragraph [0022] figure 4	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 April 2018	26/04/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Amadei, Davide

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2018/054656

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003142688 A1	31-07-2003	NONE	
US 2003169875 A1	11-09-2003	NONE	